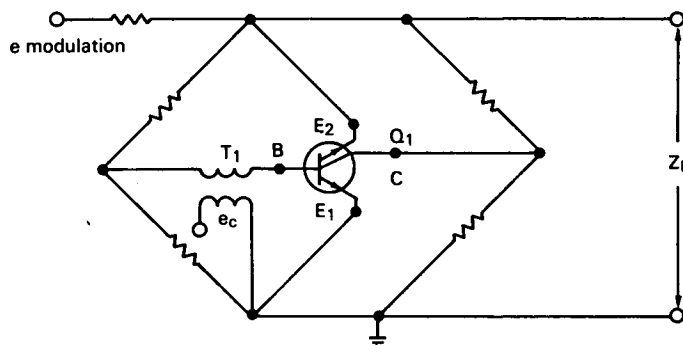


# NASA TECH BRIEF



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## Double Emitter Suppressed Carrier Modulator Uses Commercially Available Components



### The problem:

To design a suppressed carrier modulator that will develop a signal-to-carrier output ratio of 40 db or greater with a signal input of 2.5 volts peak to peak. All tuning potentiometers must be eliminated and all sideband harmonics must be less than the carrier output amplitude.

### The solution:

A double emitter suppressed carrier modulator circuit using commercially available circuit components.

### How it's done:

A commercially available double emitter chopper transistor  $Q_1$  (type 3N74) is used to achieve the required carrier suppression by means of symmetrical circuit configuration. To reduce the carrier output from a modulator, a bridge circuit is required to balance the effects of the carrier current as it switches the double emitter transistor from cutoff to saturation. By tying the collector of  $Q_1$  to a resistor bridge and the base-transformer combination to a separate resistor bridge, any voltages developed by the circuits are balanced with respect to the load impedance and

ground. The voltage developed across the emitter  $E_1$  of the transistor to the base junction B is equal and opposite to the voltage developed across emitter  $E_2$  to the base junction. Therefore, the  $E_1$  to  $E_2$  voltage sum is approximately zero with respect to the load impedance  $Z_L$ . Any stray capacitance between the collector and either emitter, or the base and either emitter is also in the balanced RC bridge network.

The values of the base bridge resistors and the collector bridge resistors are partially determined by the capacitance between: (1) both emitter junctions and the base, and (2) both emitter junctions and the collector. Because of the internal capacitance, the resistors will vary in value depending on the frequency of the carrier  $e_c$  through  $T_1$ . The circuit develops a signal-to-carrier output ratio to meet the 40 db requirement.

### Notes:

1. The circuit, as designed, is intended for use from 450 to 520 kHz carrier frequencies. This approaches the upper frequency limit of the 3N74 double emitter transistor because of internal base-emitter capacitances.

(continued overleaf)

2. Inquiries concerning this invention may be directed to:

Technology Utilization Officer  
Marshall Space Flight Center  
Huntsville, Alabama 35812  
Reference: B67-10101

**Patent status:**

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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of IBM  
under contract to  
Marshall Space Flight Center  
(M-FS-2494)