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CIRCUIT PERFORMANCE OF A PARASITIC-LOADING DIGITAL SPEED CONTROLLER FOR A 400-HERTZ TURBINE-DRIVEN ALTERNATOR

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ABSTRACT

Parasitic speed controllers are used in space power electrical generating systems to maintain the speed of the turbine-driven alternators within specified limits. Selected subcircuits for a solid-state parasitic-loading speed controller were assembled and tested. The test results as obtained to date consist of the performance evaluation of the frequency reference and the period counter subcircuits. These circuits performed as expected.

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E-6854

SUMMARY

Electrical power generating systems have been under investigation by the Lewis Research Center. The power systems have been designed for possible use in space applications and use a parasitic-loading speed controller to maintain speed (output frequency) of the turbine-driven alternator. The controller maintains this speed by applying parasitic loads to the alternator so that the total alternator load remains constant. Previous speed controllers have utilized analog control logic and phase-controlled power output stages. A solid-state digital speed controller utilizing integrated circuits was designed and the critical subcircuits were fabricated. The preliminary test results are presented herein. This investigation was initiated as part of a continuing effort to expand upon the parasitic-loading control techniques for turbine-driven alternators.

The test results as obtained to date consist of the performance evaluation of the frequency reference and the period counter subcircuits. The relative propagation delay between these two subcircuits is of prime importance. The circuit for each function performed as expected as indicated by the photographs of the subcircuit voltage waveshapes and the indicated propagation delays.

INTRODUCTION

The space power electrical generating systems which the Lewis Research Center has been investigating (refs. 1, 2, 3, 4) have utilized electronic controllers to maintain the speed of the turbine-driven alternator within desired limits.

The controller maintains this speed (system frequency) by applying (or removing) parasitic loads to the alternator so that the total alternator load, including alternator losses, balances the developed turbine power. The alternator load consists of the useful system output and the housekeeping loads required to operate the power generating system. The housekeeping loads include the parasitic-loading speed controller.

The speed controllers which have been used in previous power generation systems have utilized analog control logic and phase-controlled power output stages (refs. 5, 6, 7). Potential areas for improvement in speed controller performance are efficiency, control linearity, load balance, electromagnetic interference (EMI), and a reduction in harmonic generation. A solid-state digital speed controller was designed and analyzed as part of a continuing effort to expand upon the parasitic-loading control techniques for turbine-driven alternators. The results of this analysis were reported previously (ref. 8). The assembly and test of the critical subcircuits for this digital speed controller was subsequently initiated. The circuit hardware was assembled in breadboard form. The results of this fabrication and test program as completed to date are being reported herein. The circuit hardware has been assembled for the frequency reference, period counter, deviation error detector and low frequency detector. The circuits not fabricated are the magnitude error detector, decoder and power output stages. Test results are presented in this report for the frequency reference subcircuit and the period counter. The propagation delays in these subcircuits are of prime importance in that the differences must be minimized. The discussion of the reference frequency and period counter circuits include typical waveshapes and measured propagation delays.

THEORY OF OPERATION

A block diagram of the subcircuits which comprise the digital speed controller is illustrated in figure 1.

The mode of operation of these subcircuits was discussed in reference 8, however, to summarize here, the speed controller compares two square wave signals, one being the reference frequency and the other being proportional to alternator frequency. Following a fixed time delay, the 1mHz subcarrier is gated on for the time difference between these two signals. The number of 1mHz subcarrier pulses gated on is proportional to the alternator frequency error, specifically 1 subcarrier pulse exists for each 0.01 hertz frequency error. The gated subcarrier pulses are decoded to permit the application of parasitic load to the alternator. The power output stage applies parasitic power at zero and/or 180 electrical degrees of alternator voltage. The frequency error signal is generated for line frequencies both above and below the frequency reference (folded function). The low frequency detector therefore prevents the application of parasitic load whenever the line frequency is below the reference frequency. The speed controller being reported here utilizes five (5) three-phase parasitic loads designated to be 1.0, 1.0, 2.0, 2.0 and 2.0 per unit respectively, where the per unit base is defined as ALTERNATOR POWER RATING.

APPARATUS AND PROCEDURE

A block diagram of the test facility is shown in figure 2. The digital speed controller was fabricated entirely of transistor-

transistor logic (TTL) and diode-transistor logic (DTL) integrated circuits (IC). Two frequency sources were used for simulation of the digital clock and the alternator line frequency. The frequency sources produced positive voltage pulses of the required amplitude to drive the logic gates. The collector voltage waveforms of each counter which comprises the frequency reference were recorded. From these recordings each propagation delay, and an overall value for the propagation delay of the frequency reference subcircuit were determined. Voltage waveforms of all the timing functions generated by the period counter were recorded and from these data the correct phasing of the timing signals was verified. All test data were obtained by use of a dual-beam four-trace oscilloscope. Figure 2 further includes the significant device specifications for the test equipment. The photograph of figure 3 illustrates the test setup as used in this program. All tests were conducted at room temperature and at sea level barometric pressure.

RESULTS AND DISCUSSION

Frequency Reference

The block diagram of the frequency reference subcircuit is illustrated in figure 4a. The frequency reference consists of four divide-by-five synchronous counters, one divide-by-ten synchronous counter and two J-K (ref. 9) bistable circuits. The two bistable circuits (divide by 2) each generate symmetrical square wave signals for the 400 hertz reference and the 1mHz subcarrier. The applied frequency is 10mHz which is first divided by ten to generate the subcarrier (1mHz) and then subsequently divided by 2500 which provides a reference frequency of 400.00 hertz. Synchronous counters were used to minimize the propagation delay of the subcircuit (ref. 9). With synchronous counting, each data output (bistable collector) is only delayed by the propagation delay of one bistable circuit. This is accomplished, as is illustrated in figures 4b and 4c, by triggering all the bistable circuits simultaneously. Consequently, the switching time is limited by the speed of one bistable.

The importance of circuit delay time in this system was discussed in reference 8, however, to summarize here, the delay in the frequency reference subcircuit and the period counter should be identical, preferably zero. Any difference in delay between these two subcircuits results in a reduced gating period which, at worst case, would alter the error count. This would generate a false error signal which would apply an incorrect magnitude of parasitic load.

Figure 4b illustrates a typical divide-by-five synchronous counter using individual J-K bistable flip flops. Figure 4c illustrates a divide-by-ten synchronous counter. This counter illustrates one concept of MSI (Medium Scale Integration) packaging.

The collector voltage waveforms as generated by the divide-by-five counter, illustrated in figure 4b, are shown in figure 5. The significant feature illustrated here is that the counting sequence is coincident with the negative-going transition of the input signal.

By using a combination of TTL logic functions, the clock frequency is counted down by a factor of ten to produce the square wave subcarrier signal, as indicated in figure 4a. Figure 6a illustrates the input-output relationship for the combined circuit. The clock pulses which are coupled through to the output could be reduced by incorporating better isolation in the system. Figure 6b illustrates the phase relationship between the clock pulse and negative-going edge of the output signal. Figure 6c illustrates the relationship between the same input and the positive-going edge of the output signal. The largest delay between these two signals is the value considered representative of the circuit. It can be seen from figures 6a, 6b, and 6c that the propagation delay between this 10mHz clock and the 1mHz output signal is approximately 24 nanoseconds. An additional delay is generated by utilizing a 10mHz clock. This delay is 50 nanoseconds (one-half of the pulse period). These two delays represent the total delay incurred in gating a subcarrier from the alternator line (ref. 8). Since the speed controller error signal is comprised of subcarrier (S.C.) pulses, the total delay (50 nsec + 24 nsec = 74 nsec) will decrease the one count error (400.01 Hz) window (which is 500 nsec maximum) by 74 nsec. For the system to react to a one count error, the error pulse need only be 50 nsec wide. Therefore, the total maximum delay (74 nsec) is acceptable. A clock frequency greater than 10mHz would further reduce the delay ($1/2\ f_{clock}$). However, using a higher frequency would increase the amount of electrical interference.

A combination of IC modules as indicated in figure 4a are used to generate a 400.00 hertz reference frequency from the 1mHz subcarrier. The voltage waveshapes at the input and output of each synchronous counter are illustrated in the various photographs of figure 7. For each counter, two photographs are presented which depict the input-output signal relationship for the negative-going and the positive-going edge of the output signal. In each photograph, the top two waveshapes illustrate the basic counting function of the counter while the bottom two waveshapes indicate the relative delay within the circuit.

In photographs 7a and 7b, the synchronous TTL divide-by-ten counter waveshapes are illustrated. The significant characteristics here are that the module transfers data on the positive-going edge where the remaining counters in this digital speed controller transfer on the negative. The other characteristic is the propagation delays for the negative and positive edges are 16 nanoseconds each. The propagation delays for each synchronous counter have been itemized in Table 1. The rise time of the test equipment was relatively long compared to the measured counter propagation delays. As a result, the measured delays can only be considered as approximating the actual delays. The total delay was 116 nanoseconds.

F_{line} Period Counter

The f_{line} period counter samples the alternator frequency in a speed control system (ref. 8) and generates digital signals at several preselected intervals. These signals are used for various functions throughout the speed controller, one of which provides the fixed delay required to generate a pulse error count. The logic diagram of the f_{line} period counter is shown in figures 8a, b and c. The period counter consists of a 17-count synchronous counter, a function generator and a strobe generator. The synchronous counter has capabilities of counting to 31; however, the count is limited to 17 by use of internal reset. The total propagation delay of the f_{line} period counter should approximate the 116 nsec delay of the frequency reference. As such, a synchronous counter utilizing DTL logic modules was developed (DTL has a propagation delay of ~35 nanoseconds compared to ~13 for TTL). The function generator and the strobe generator use TTL logic. The function generator shown in figure 8b converts the outputs of the synchronous counter to signals for use throughout the speed controller as itemized below. The functions generated are $\overline{0T}$, $\overline{1T}$, $\overline{10T}$, $\overline{15T}$, $\overline{16T}$ and $\overline{17T}$. These "T" functions represent specific intervals of time during a sampling cycle (ref. 8). A given T represents the period of a specific alternator positive half cycle; for instance 10T represents the period of the positive part of the 10th alternator cycle following the start of the sampling cycle. The application of these "T" functions is itemized below:

Period Number	Function
$\overline{0T}$, $\overline{1T}$	reset various controller subcircuits
$\overline{10T}$	initiates low frequency detector
$\overline{15T}$	reset temporary storage subcircuit
$\overline{16T}$	gate error signal into temporary storage
$\overline{17T}$	gates parallel data into SCR power circuits

The strobe generator, as shown in figure 8c, consists of an eight count asynchronous counter with associated NAND circuits to generate the timing signals $\overline{17TR1}$, $\overline{17TR3}$ and $\overline{17TR5}$. These timing signals are used for data transfer and circuit reset functions.

The waveshapes of the individual output signals of the function generator are illustrated in figure 9. The significant features of these waveshapes are that the transition in the output signal coincides with the negative-going edge of the f_{line} (input) signal. The propagation delay of the circuit was estimated since efforts to measure the delay in the output signals were ineffective. This restriction

was not critical since the phase difference between the period counter signals and the signals of the frequency reference will be minimized. The waveshapes illustrated in figure 10 indicate the output signals generated by the asynchronous counter and those signals generated by the NAND Logic modules which make up the strobe generator. The output signals are one (1) microsecond wide which repeat every eight (8) microseconds. A photograph of these output signals is shown in figure 11. The strobe generator is gated on every 17T of the alternator line frequency after which the circuit is toggled (ref. 10) every one microsecond by the subcarrier. The photograph depicts the generation of the first, third and fifth subcarrier signals, which are used for circuit reset functions. The propagation delay of the strobe generator was estimated to be 52 nanoseconds while the estimated delay for the f_{line} period counter was 100 nanoseconds total.

CONCLUDING REMARKS

The frequency reference and f_{line} period counter circuits for a parasitic-loading Digital Speed Controller were designed and tested. Both circuits performed as expected.

Photographs of the significant subcircuit output signals verify the results obtained. The significant results are (1) the propagation delay of the frequency reference was measured to be 116 nanoseconds while (2) the propagation delay of the period counter was estimated to be 100 nanoseconds.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, March 1, 1972.

TABLE I

PROPAGATION DELAY OF FREQUENCY REFERENCE COUNTERS

f_{in}	f_{out}	Positive-Going Edge (nsecs)	Negative-Going Edge (nsecs)
10 mHz	1 mHz	20	24
1 mHz	100 kHz	16	16
100 kHz	20 kHz	20	8
20 kHz	4 kHz	24	8
4 kHz	800 Hz	24	12
800 Hz	400 Hz	8	8

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10. Anon.: Digital Application Notes - EECologic 2. Electronic Engineering Co. of California, Mar. 1970.

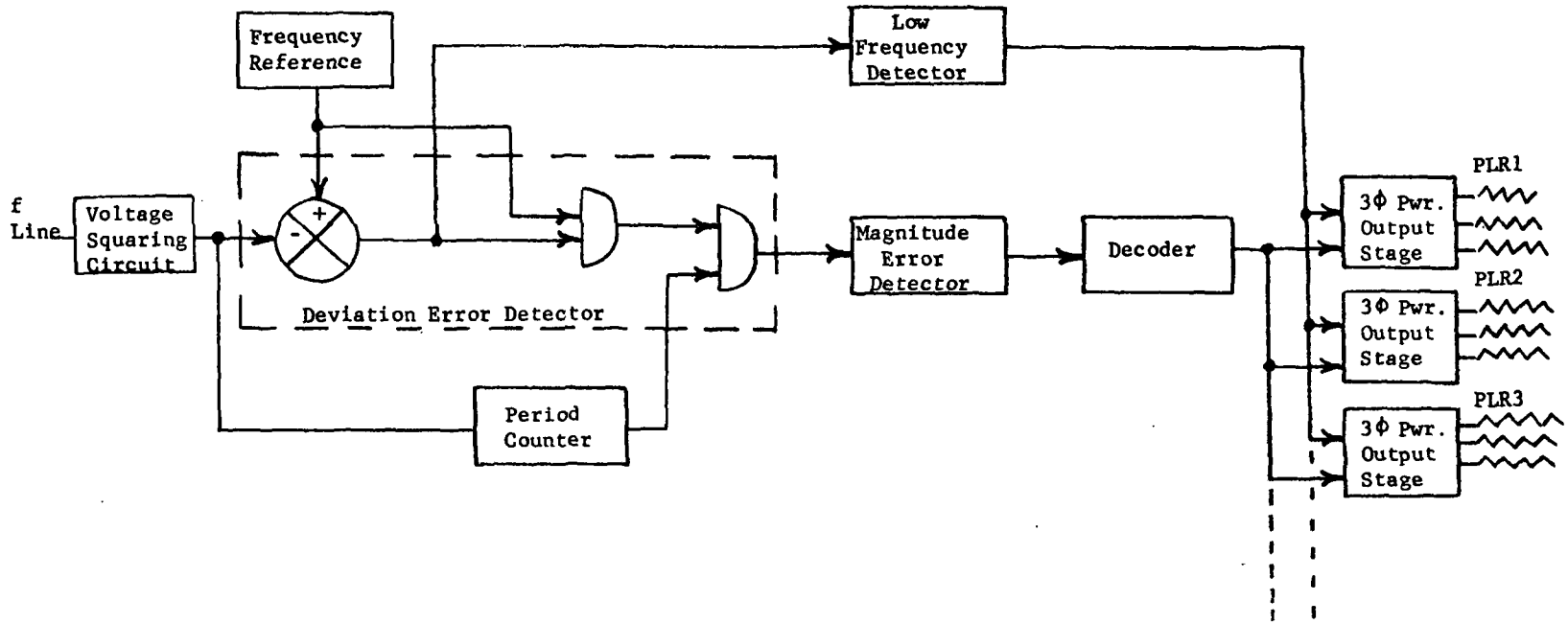


Figure 1 - Abbreviated Block Diagram Digital Speed Controller

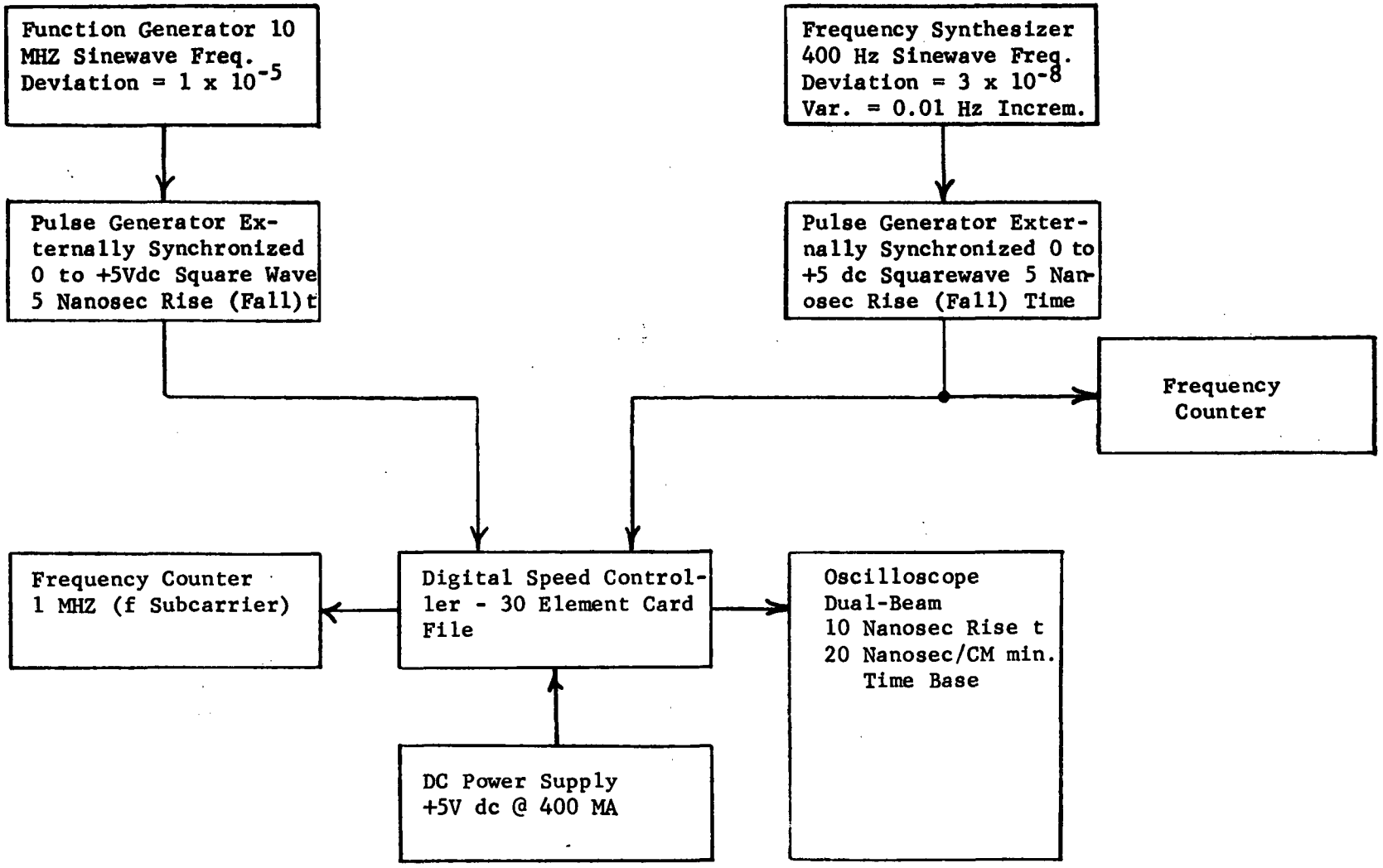


Figure 2 - Apparatus Block Diagram

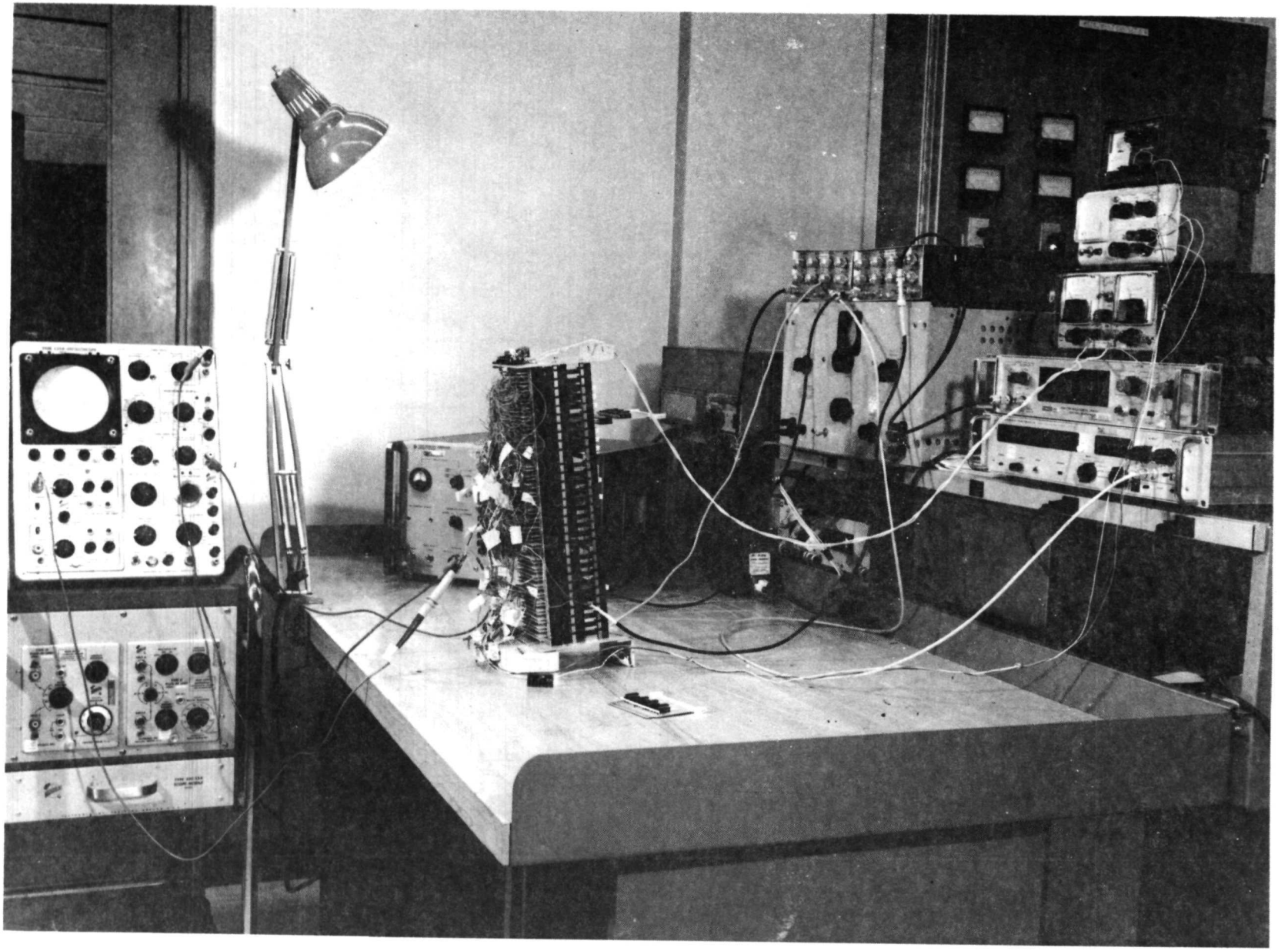
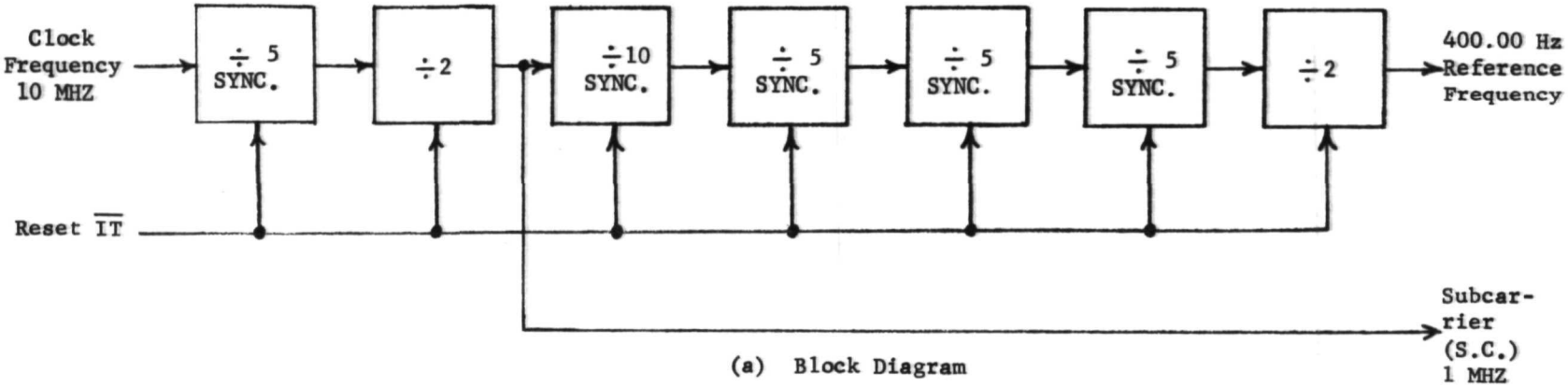
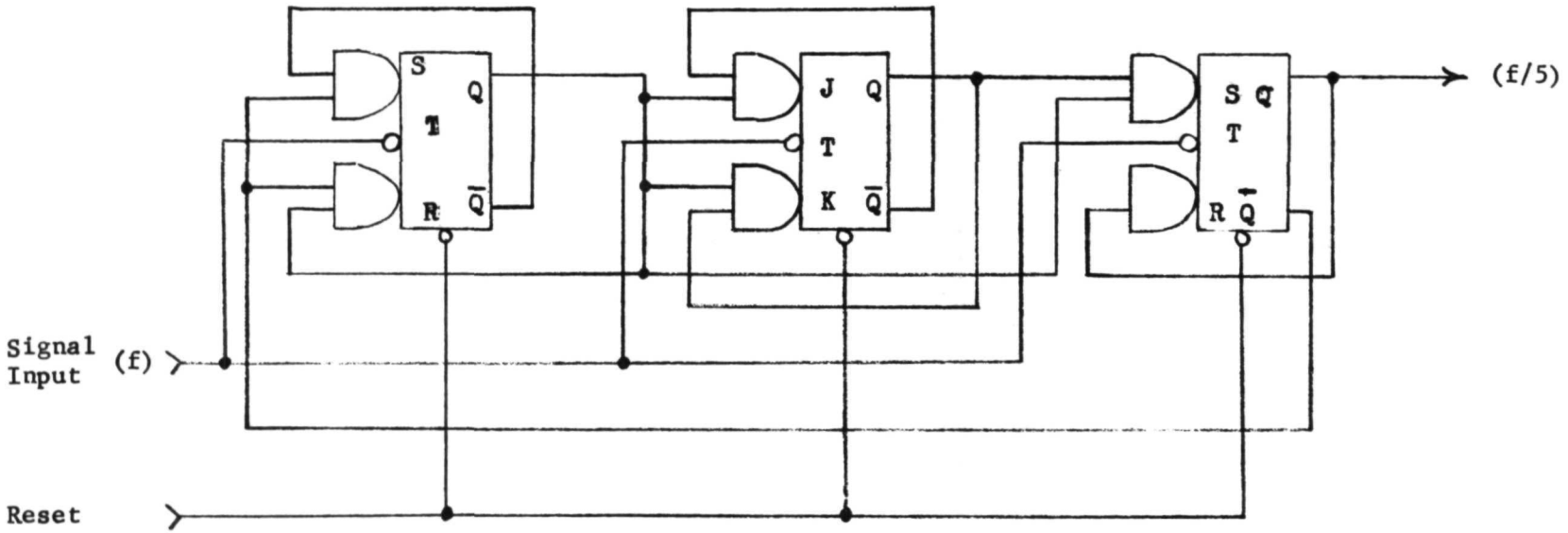


Figure 3 - Test Facility



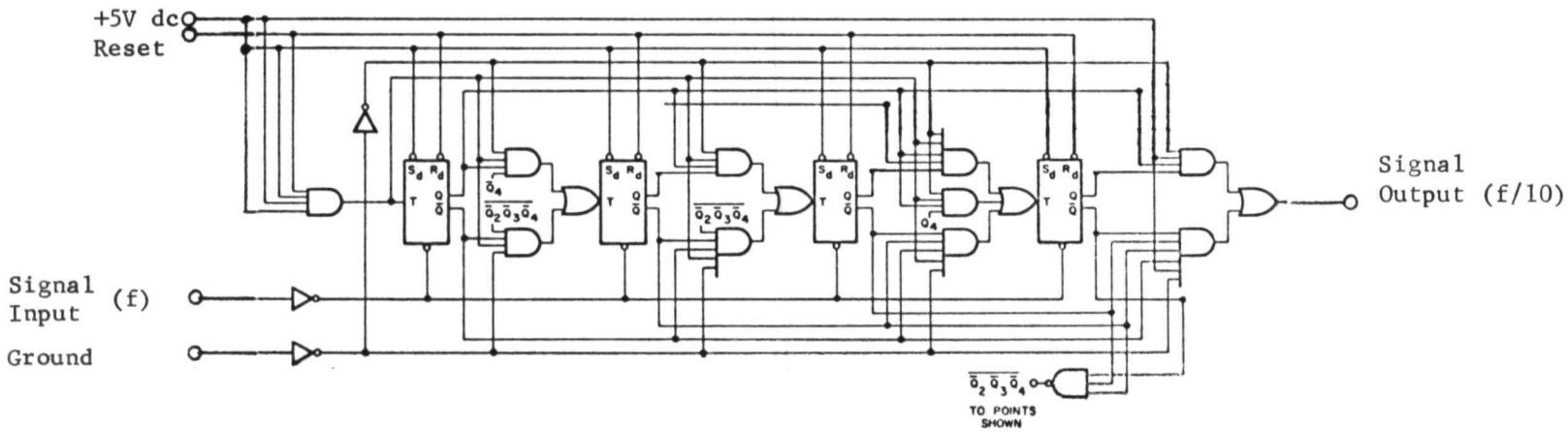
(a) Block Diagram

Figure 4 - Frequency Reference Logic Diagram



(b) Divide-By-Five (÷ 5) Synchronous Counter (Typical Circuit)

Figure 4 (Cont.)



(c) Divide-By-Ten ($\div$ 10) Synchronous Counter

Figure 4 (Cont.)

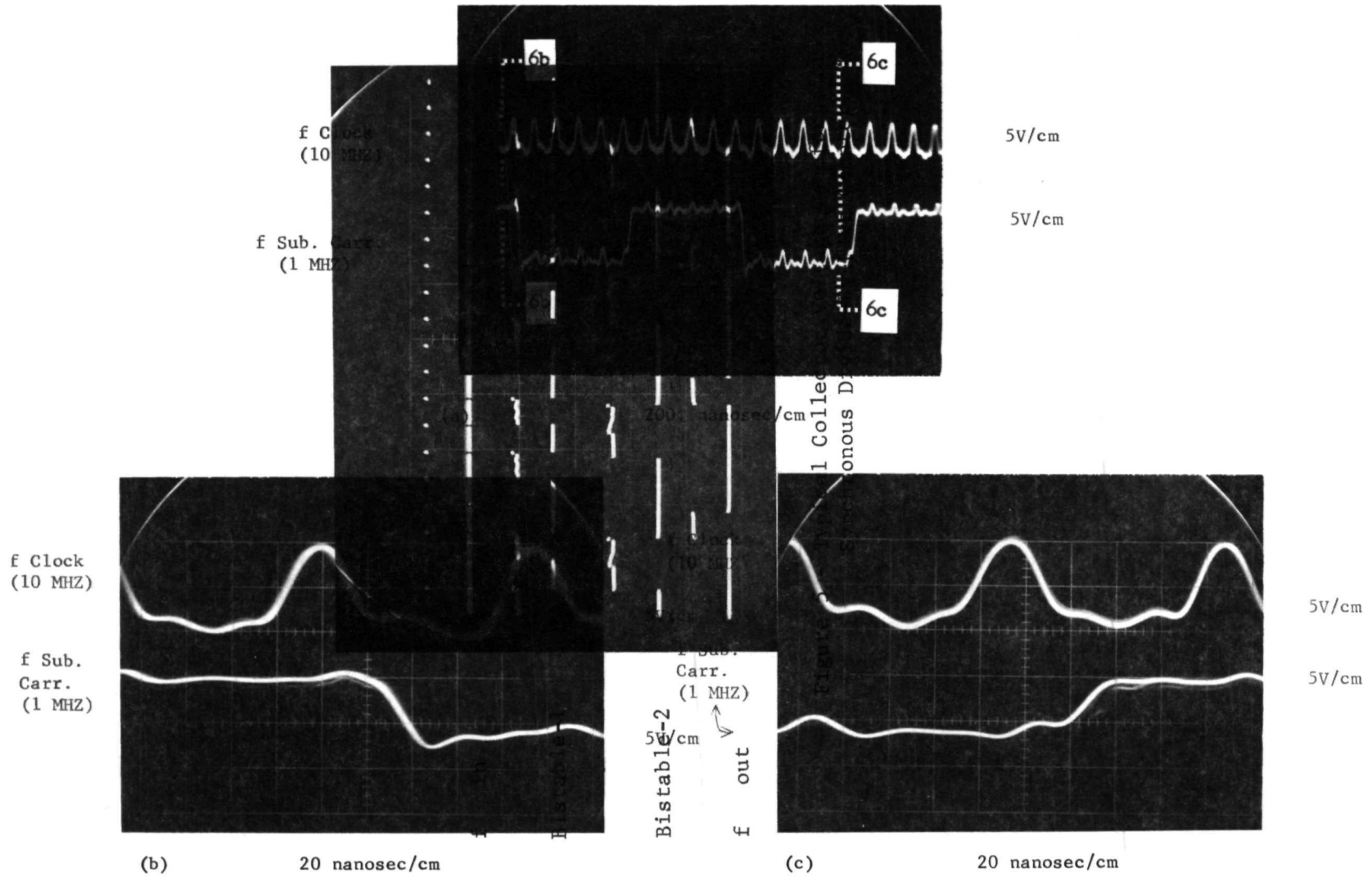


Figure 6 - Frequency Reference - Input/Output. Relationship of f Clock and f Sub. Carr. Counter

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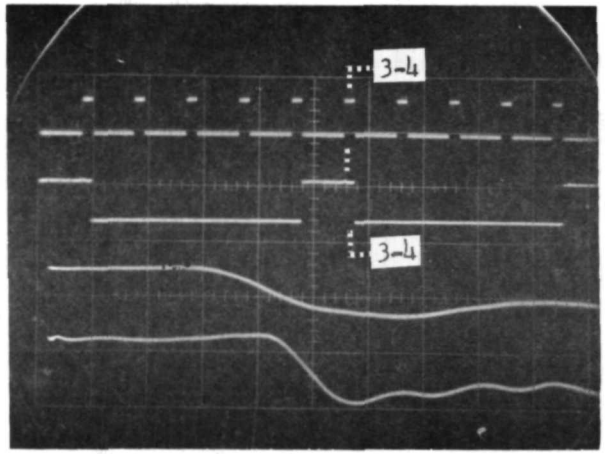
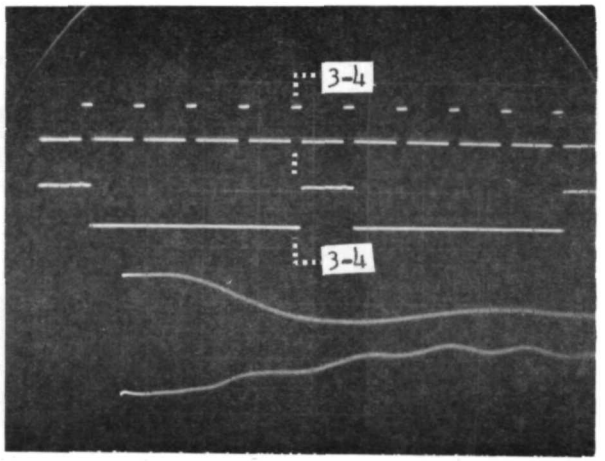
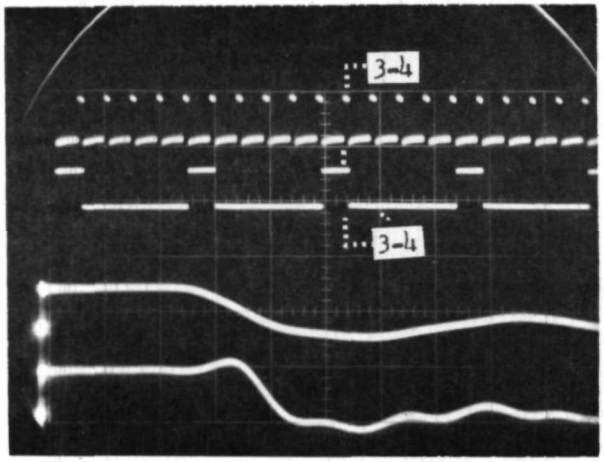


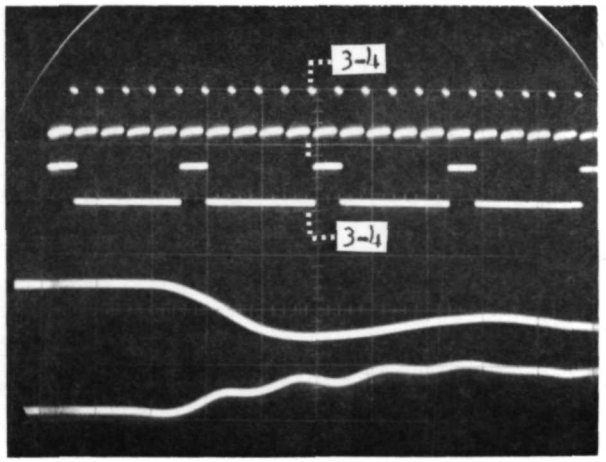
(e) Top 2 - 50 microsec/cm; bottom 2 - 20 nanosec/cm



(f) Top 2 - 50 microsec/cm; bottom 2 - 20 nanosec/cm
20 KHZ to 4 KHZ Counter

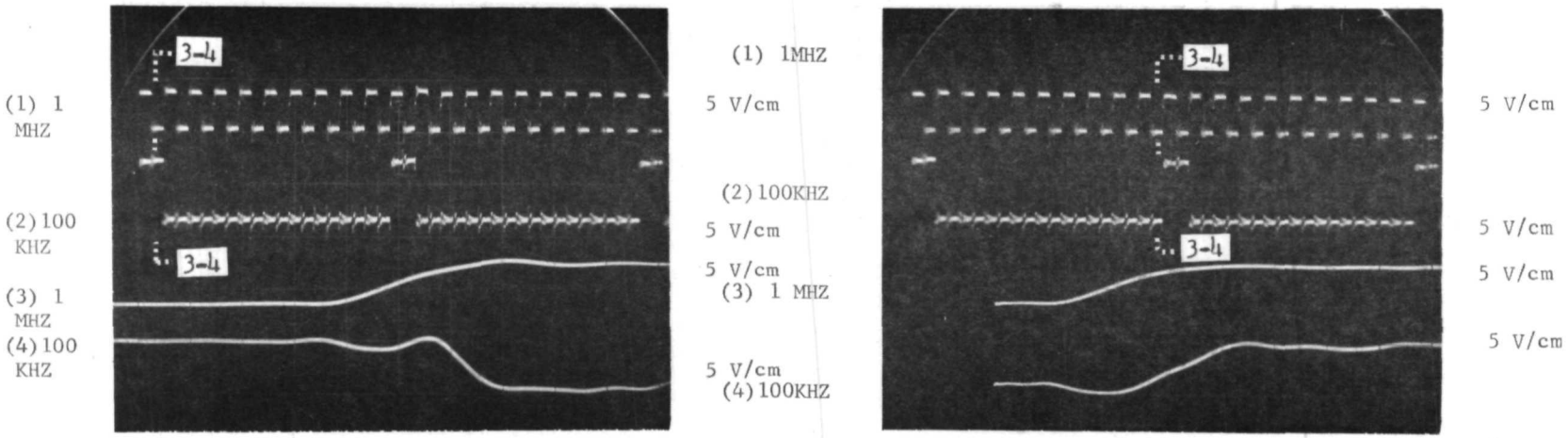


(g) Top 2 - 0.5 millisec/cm; bottom 2 - 20 nanosec/cm



(h) Top 2 - 0.5 millisec/cm; bottom 2 - 20 nanosec/cm
4 KHZ to 800 Hz Counter

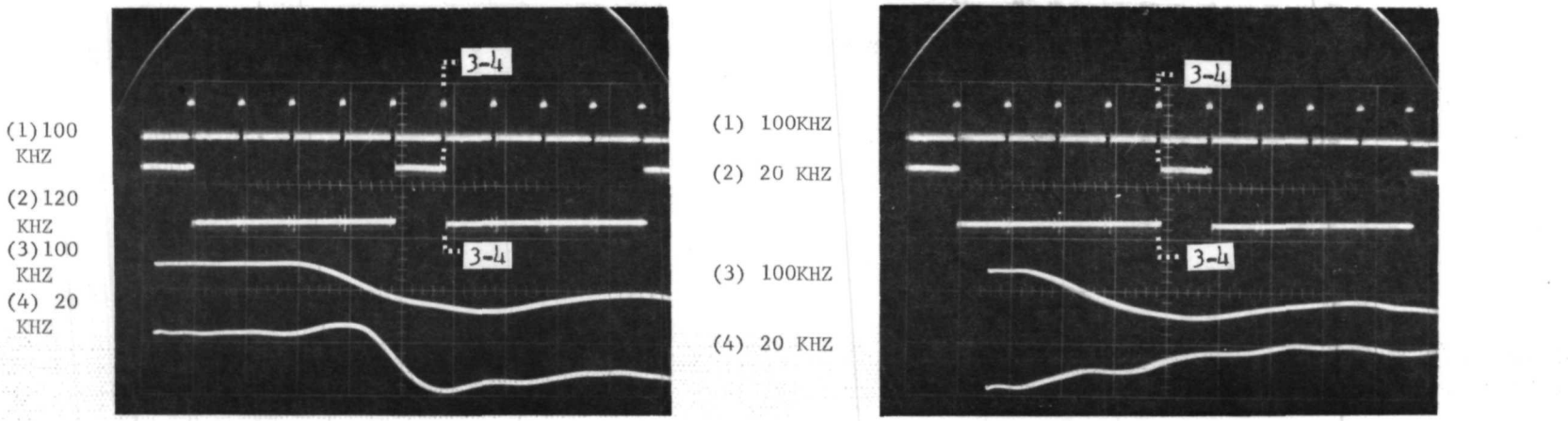
Figure 7 (Cont.)



(a) Top 2 - 2 microsec/cm; bottom 2 - 20 nanosec/cm

(b) Top 2 - 2 microsec/cm; bottom 2 - 20 nanosec/cm

1 MHZ to 100 KHZ Counter

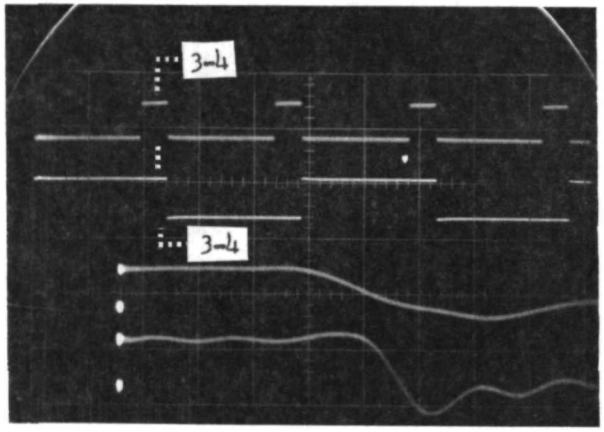


(c) Top 2 - 10 microsec/cm; bottom 2 - 20 nanosec/cm

(d) Top 2 - 10 microsec/cm; bottom 2 - 20 nanosec/cm

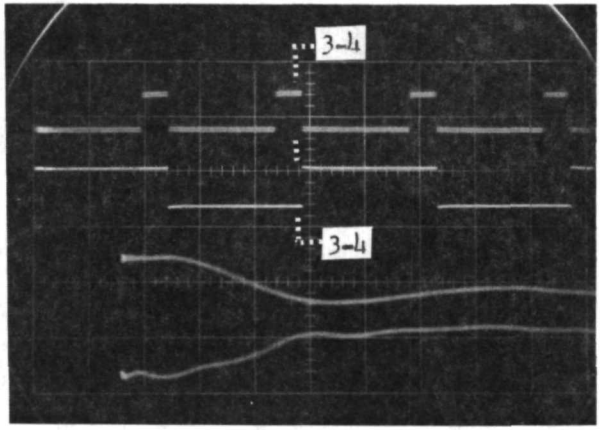
100 KHZ to 20 KHZ Counter

Figure 7 - Input/Output Relationship of Frequency Reference Counters



(1) 800 Hz
(2) 400 Hz
(3) 800 Hz
(4) 400 Hz

(i) Top 2 - 0.5 millisec/cm; bottom 2 - 20 nanosec/cm

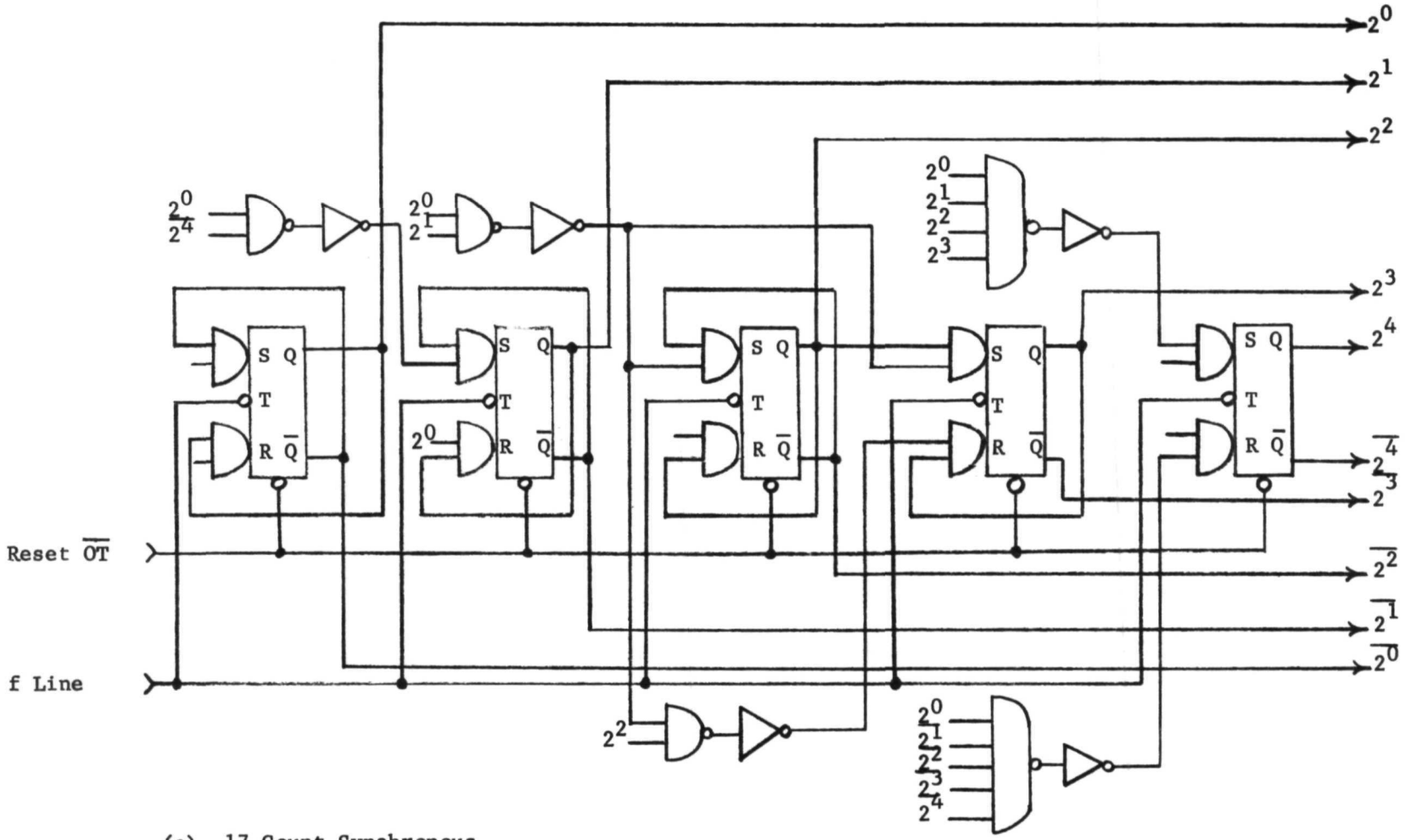


(1) 800 Hz
(2) 400 Hz
(3) 800 Hz
(4) 400 Hz

(j) Top 2 - 0.5 millisec/cm; bottom 2 - 20 nanosec/cm

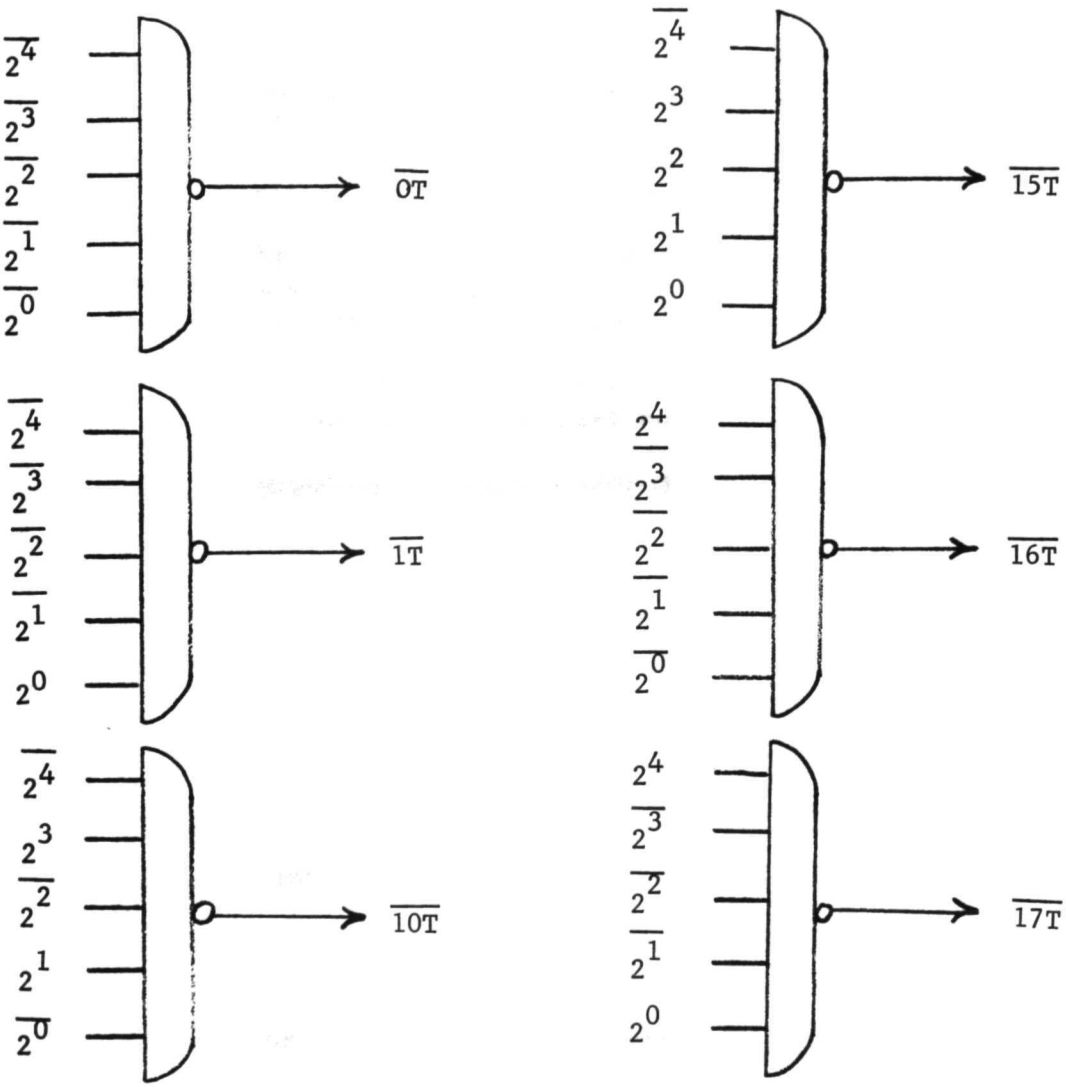
800 Hz to 400 Hz Counter

Figure 7 (Cont.)



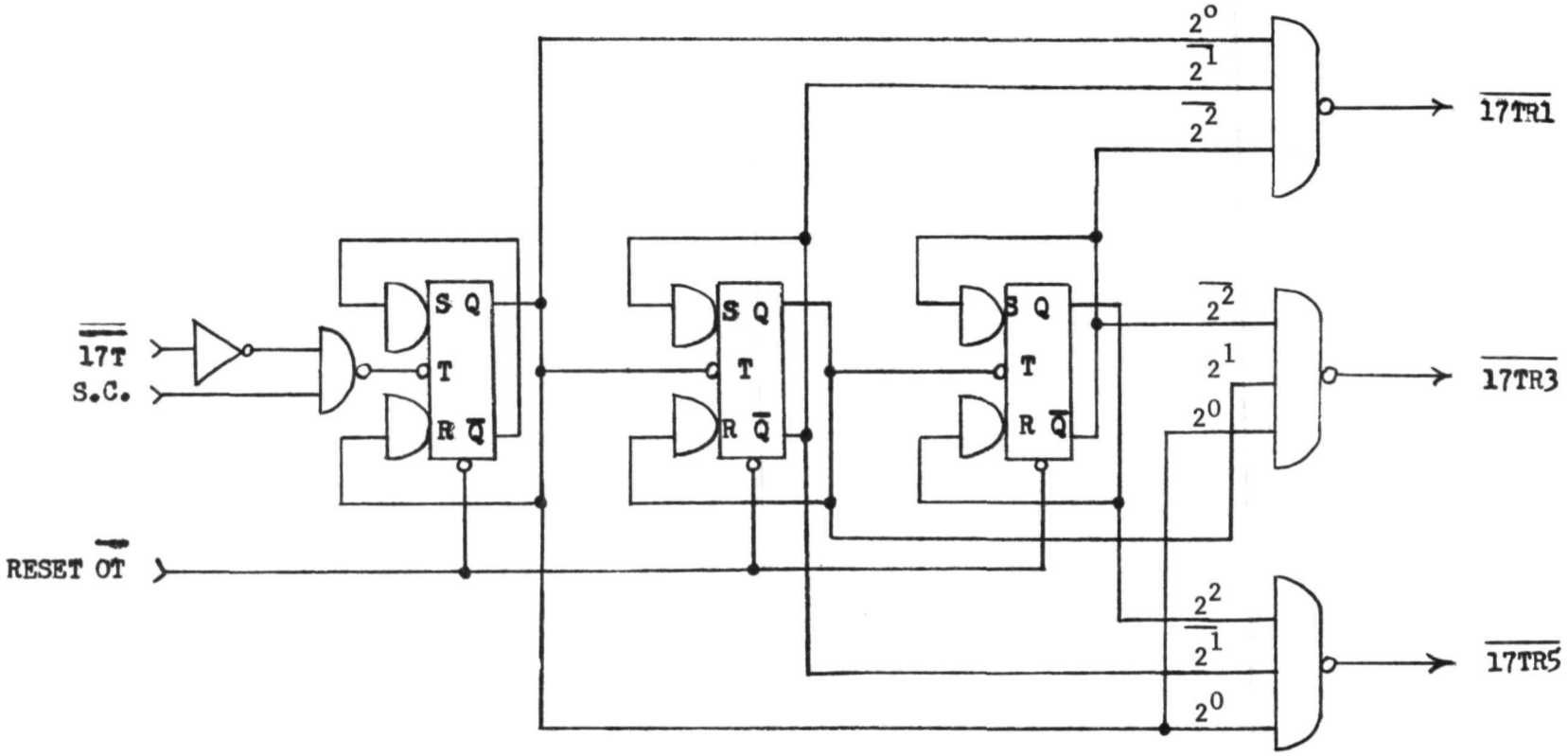
(a) 17 Count Synchronous

Figure 8 - f Line Period Counter Logic Diagram



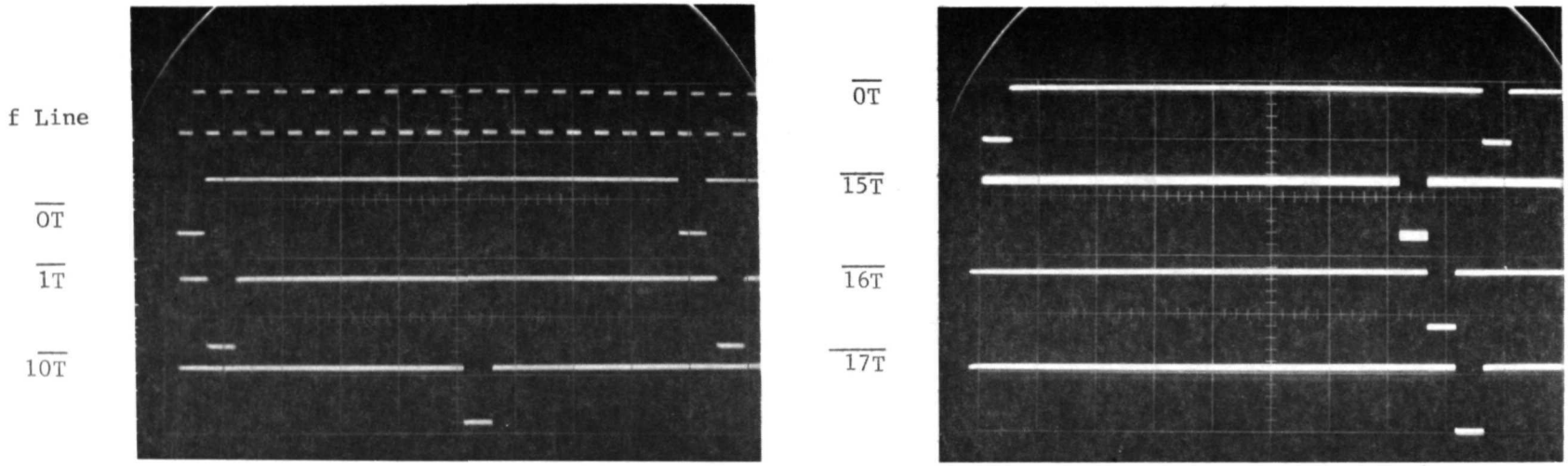
(b) Function Generator

Figure 8 (Cont.)



(c) Strobe Generator

Figure 8 (Cont.)



(a) 5 millisec/cm (b) 5 millisec/cm

Figure 9 - f Line Period Counter Function Generator

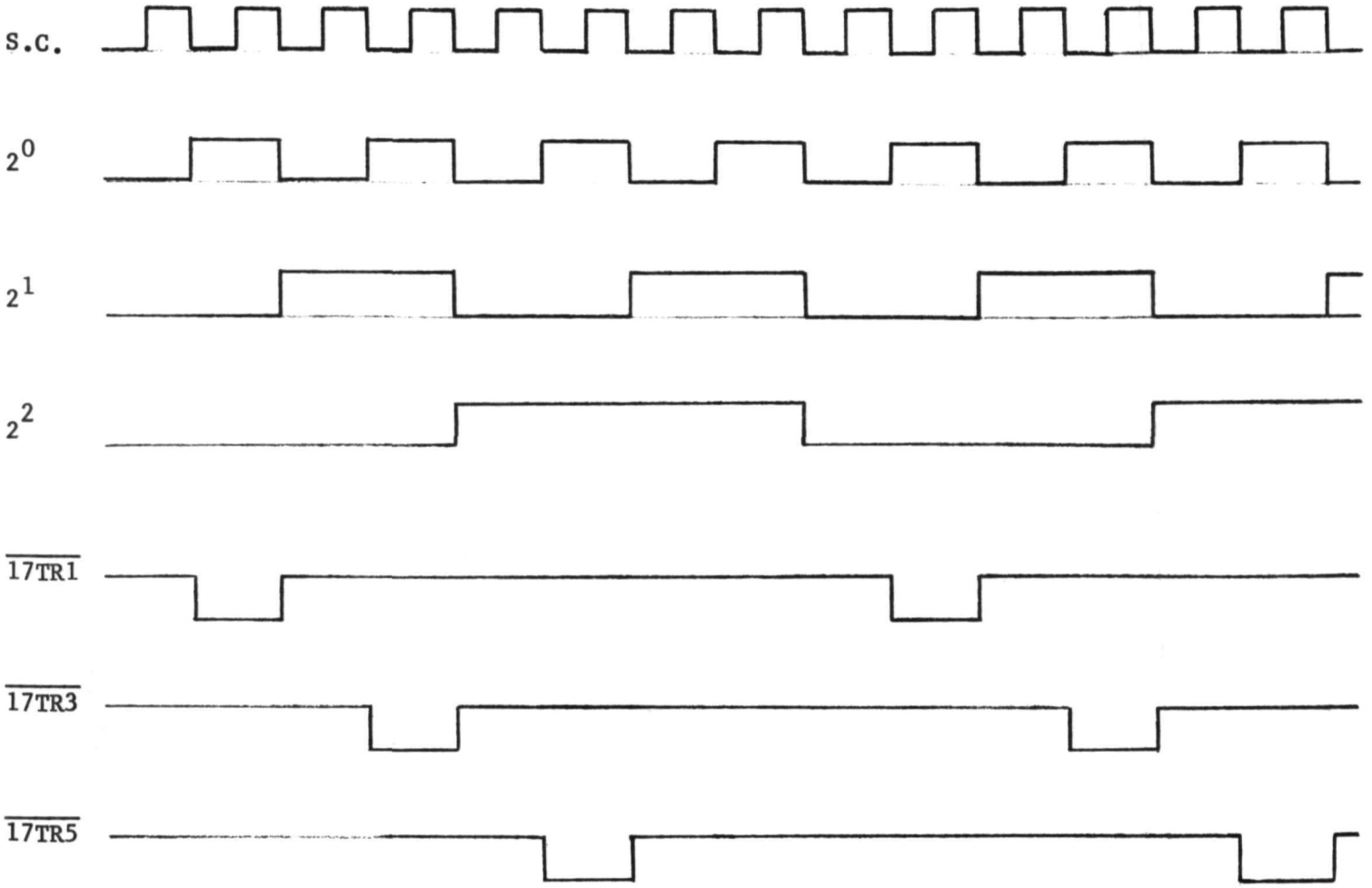


Figure 10 - f Line Period Counter Strobe Generator Timing Diagram

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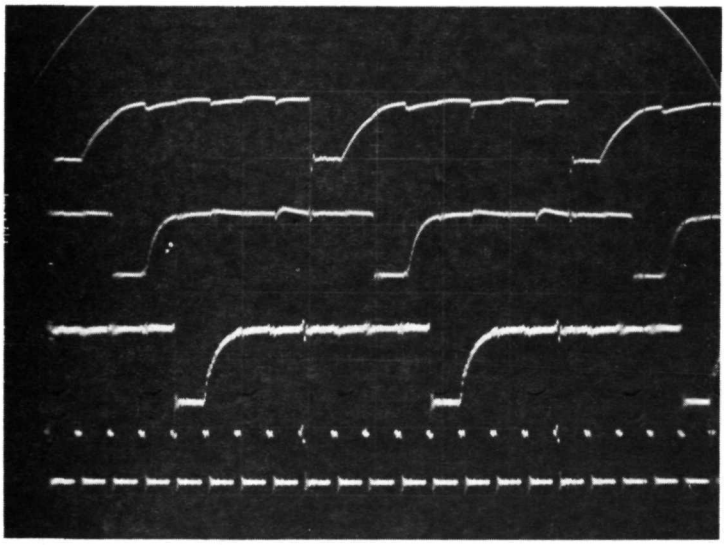

Figure 11 - f Line Period Counter Strobe Generator

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