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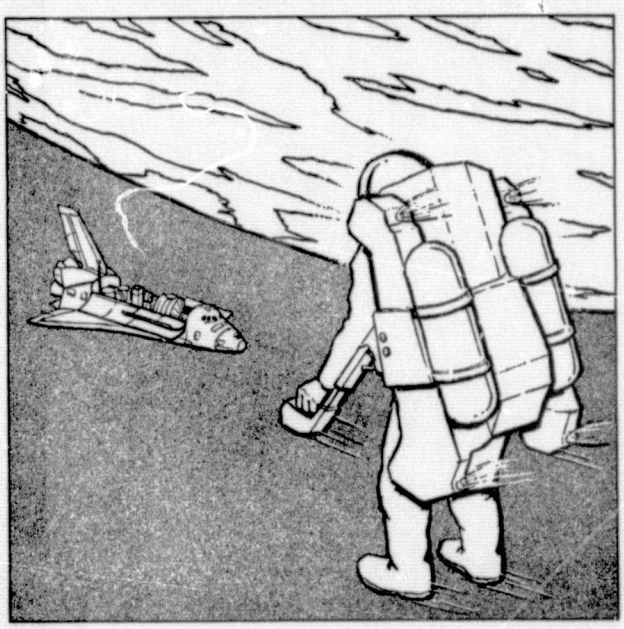

MARTIN MARIETTA

MANNED MANEUVERING UNIT TECHNOLOGY SURVEY

Contract NAS9-14593
Contract S/W
Item Paragraph 3-2

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FOREWORD

This document has been prepared by the Martin Marietta Corporation and is submitted in accordance with Exhibit "A", Statement of Work, Paragraph 3.2 of Contract NAS9-14593.

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1.0 INTRODUCTION AND SUMMARY

Man's utility in space has been demonstrated on many space missions and his need for effective EVA maneuvering aids has become apparent. Skylab Experiment M509 evaluated and proved the feasibility of backpack mounted maneuvering units. The preliminary design of the Manned Maneuvering Unit (MMU) for the Shuttle era is now underway. The purpose of this survey is to examine the current state of the art in certain technology areas that may find application on the operational EVA Shuttle MMU.

This survey covers three broad areas of technology, namely:

1) Mechanical energy storage - i.e., the practicality of utilizing the energy storage capability of either a reaction wheel or a control moment gyro;

2) Numerical and alphanumerical displays;

3) Recent electronics developments such as microprocessors and integrated injection logic.

Section 2 of this survey, that on momentum exchangers and energy wheels incorporates a paper furnished through the courtesy of Sperry Flight Systems Division, and a tabulation, Table 2-1, of some reaction wheels made by both Bendix and Sperry.

Section 3 of this report is a survey of the latest developments in numerical and alphanumerical displays.

Finally, a survey of new electronic components is presented in Section 4.

2.0 MECHANICAL ENERGY STORAGE, REACTION WHEEL SIZING, AND CMG SIZING FOR MMU

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June 4, 1975

2.1 MECHANICAL ENERGY STORAGE FOR MMU

The practicality of utilizing the energy storage capability of either a reaction wheel or a CMG system in the MMU was considered. The primary battery system consists of two 16.8 volt, 25 amp-hr units weighing 9-1/2 lb each. Total energy storage of the battery system is therefore 840 watt-hrs and the energy density is 44.2 watt-hrs/lb. It was against these parameters that mechanical energy storage was compared.

The energy density of a rotating wheel may be expressed as:

$$\text{Energy Density} = E/W = K_s \frac{\sigma}{\rho} \times \frac{1}{31{,}800} \frac{\text{watt-hr}}{\text{lb}}$$

where K_s = classical stress shape factor

σ = rotor maximum working stress (lbs/in.^{2})

ρ = rotor density (lbs/in.^{3})

31,800 = (12 in./ft)(2650 ft-lb/watt-hr)

The above equation relates the maximum energy stored in a wheel to the weight of the wheel. The available energy from the wheel, E^1, is related to E by various efficiencies.

$$E^1/W = E/W \times \eta_s \times \eta_{sg} \times \eta_r$$

where η_s = delivered/stored energy ratio = $1 - \left[\frac{N_{min}}{N_{max}}\right]^2$

η_{sg} = generator efficiency

η_r = rotor efficiency = $1 - \frac{P_{drag}}{P_{max}}$.

Typically, $\eta_s = 1 - \left(\frac{1}{3}\right)^2 = .89$

$\eta_{sg} = .83$

$\eta_r = .95$

so that, $\frac{E^1}{W} \approx .702 \frac{E}{W}$.

If the rotor radius is known, the maximum speed may be calculated from

$$\omega_{max} = \frac{1}{R} \sqrt{\frac{\sigma}{\rho} \frac{g}{K_v} \frac{K_s}{}}$$

where ω_{max} = maximum speed (rad/sec)

R = radius (in.)

g = 386 in./sec^2

K_v = classical velocity shape factor

From the above equations, the energy storage capacity and density were calculated for the eight cases listed in Table 2-1. The material assumed for cases 1, 2, 3, and 7 was PRD-49 fiber with PRD-49-III epoxy having a working stress of 170,000 psi and density of .048 lb/in.^{3}. The isotropic material used for the other four cases was maraging steel with σ = 90,000 psi and ρ = .289 lb/in.^{3}. Cases 1 and 4 correspond to the infinite diameter, constant stress tapered rotor where K_s = 1.0. A disk rotor having diameter D and thickness H was considered in cases 2 and 5. Note that the energy density drops by 40% (K_s = .6 and K_v = .25). If the diameter is constrained to 3 in. corresponding to the maximum allowable gimballed wheel size, the maximum speed and available energy capacity may be calculated (cases 3 and 6). Similarly, if the diameter is restricted to 6 inches (reaction wheel), cases 7 and 8 result. It should be noted that the momentum capacity of any of these cases is far in excess of the 1 ft-lb-sec requirement.

Within the volume constraint required for gimballing a CMG, the amount of deliverable energy storage is small (15.9 watt-hrs) and it requires an extremely high speed composite rotor design. With an isotropic rotor, the recoverable energy is approximately half that of the composite rotor and the weight is six times greater.

If reaction wheels are used, the rotor diameter may be doubled thereby permitting more rotor mass to be added for energy storage. The best which can be achieved with a 6 in. composite rotor is 63.6 watt-hrs recoverable energy, which is less than 10% that of the battery.

Because of the volume constraint, mechanical energy storage does not appear feasible for the MMU. Note however that without this constraint, the recoverable energy density with a composite rotor of 46.9 watt-hrs/lb is competitive with that of the battery (44.2 watt hrs/lb).

2.2 REACTION WHEEL SIZING FOR MMU

Information for sizing the reaction wheel in less than 1 ft-lb-sec momentum range is provided by Figures 2-1 and 2-2. Figure 2-1 provides peak power consumption for a single wheel as a function of output torque. Figure 2-2 provides rotor weight from which total package weight can be calculated for a given output torque requirement. The curves on this figure are in terms of the speed/momentum ratio; practical rotor designs fall between the two shaded areas.

Table 2-1 Energy Storage Characteristics of MMU Rotors

Case	N_{max} (RPM)	Rotor Size D x H (in.)	Rotor Weight (lbs)	Material	E/W (watt-hr/lb)	E^1/W (watt-hr/lb)	E (watt-hr)	E^1 (watt-hr)	H (ft-lb-sec)
1	-	∞ Taper	-	Comp.	111.4	78.2	-	-	-
2	-	D x H Disk	-	Comp.	66.8	46.9	-	-	-
3	364, 841	3 x 1 Disk	.339	Comp.	66.8	46.9	22.6	15.9	3.14
4	-	∞ Taper	-	Iso.	9.79	6.87	-	-	-
5	-	D x H Disk	-	Iso.	5.87	4.12	-	-	-
6	108, 186	3 x 1 Disk	2.04	Iso.	5.87	4.12	12.0	8.4	5.6
7	182, 422	6 x 1 Disk	1.356	Comp.	66.8	46.9	90.6	63.6	25.1
8	54, 091	6 x 1 Disk	8.16	Iso.	5.87	4.12	47.9	33.6	44.8

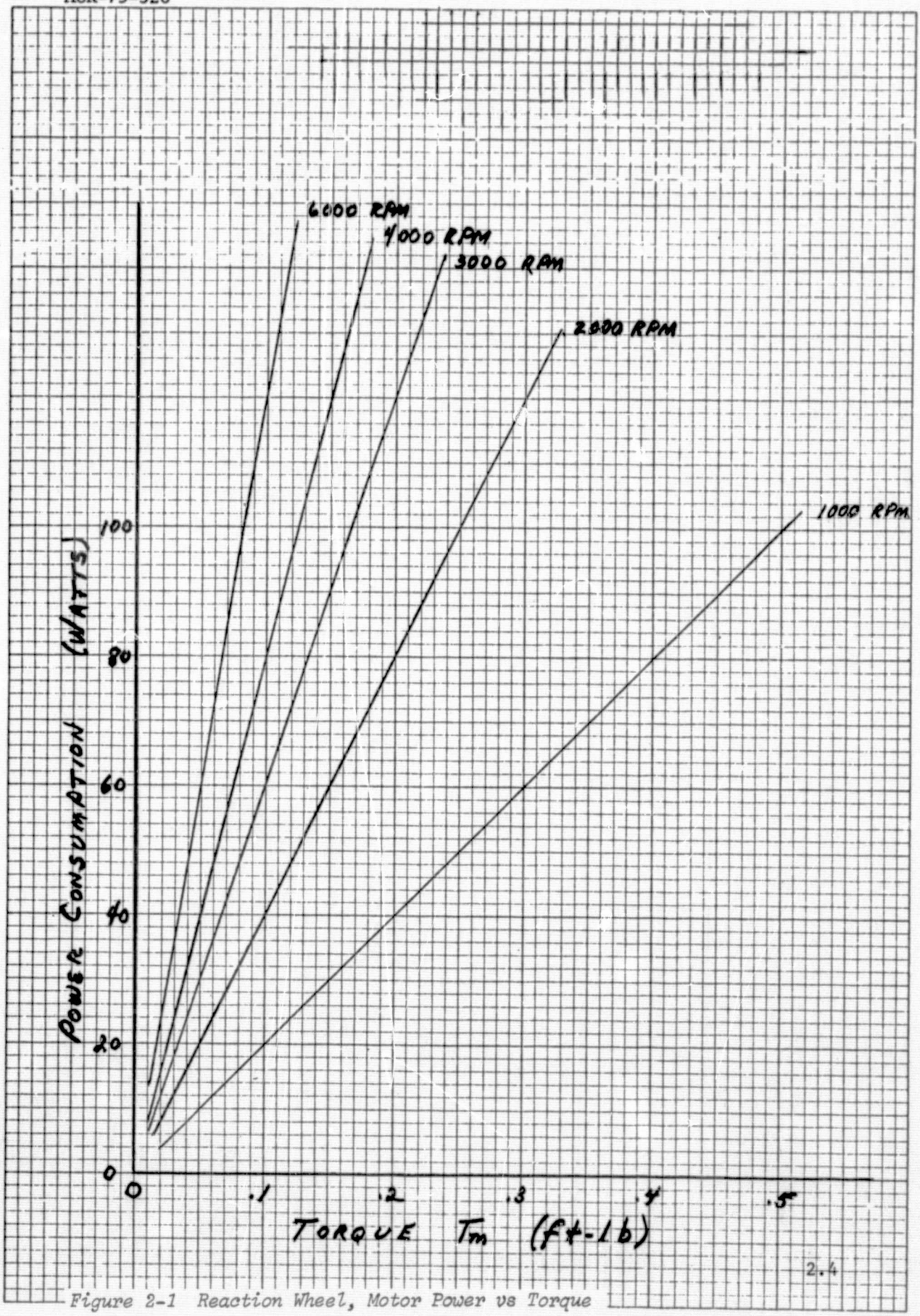

Figure 2-1 Reaction Wheel, Motor Power vs Torque

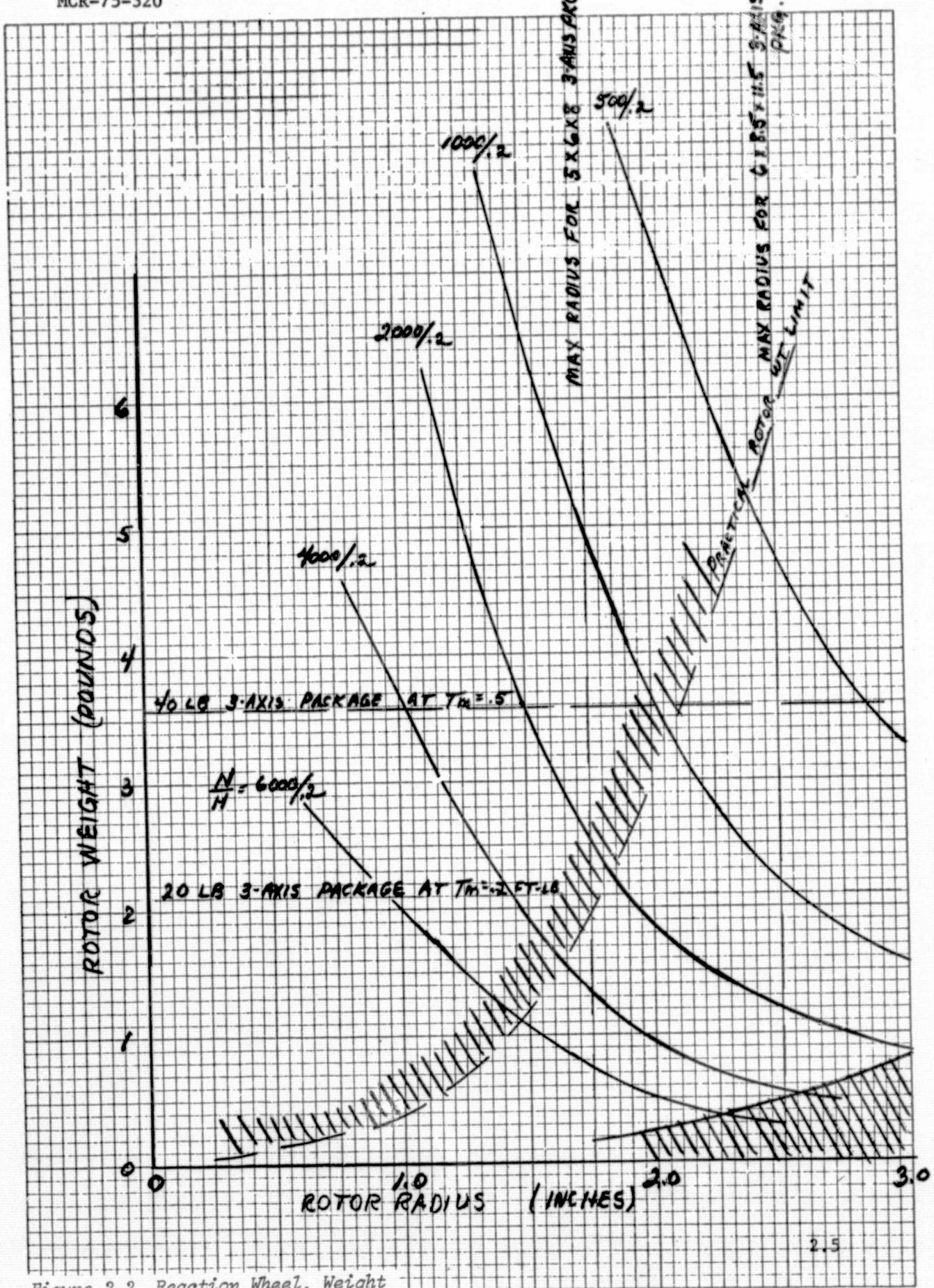

Figure 2-2 Reaction Wheel, Weight

To size a particular design the torque, maximum power, and momentum requirements should be known. To obtain the lightest, smallest design, determine from Figure 2-1 the maximum speed at which the torque can be produced without exceeding power consumption limits. Then calculate the speed to momentum ratio and select the proper curve on Figure 2-2. On this curve select the best compromise between weight and size. The following equation can be used to estimate size and weight.

$$P = \frac{.144\ N\ T_m}{.72}$$

$$W_r = \frac{73{,}720\ H}{N\ R^2}$$

$$W_p = 3\ (2\ W_r + 12\ T_m)$$

where P = power consumption in watts

T_m = motor torque in foot-pounds

W_r = rotor weight in pounds

H = angular momentum in foot-pound-seconds

N = rotor speed in RPM

R = rotor radius in inches

W_p = three-axis package weight in pounds

An example will illustrate the procedure. For

$$P = 125 \text{ watts};\ T = .5 \text{ ft-lb};\ H = .5 \text{ ft-lb-sec.}$$

From Figure 2-1, N = 1,250 RPM; $\frac{N}{H} = 2{,}500$.

Using the 500/.2 curve the rotor radius must be 2.4 inches and the rotor weight will be about 5 lbs.

$$W_p = 3(2\ W_r + 12\ T_m) = 48 \text{ pounds}$$

The package size will be approximately 5 x 9 x 11 for a three-axis package. A partial cross-section of the RWA is shown in Figure 2-3 and the package layout in Figure 2-4.

The above estimate is based on the use of conventional (ball bearing) rotor suspension. For the radial loads present in this application, it

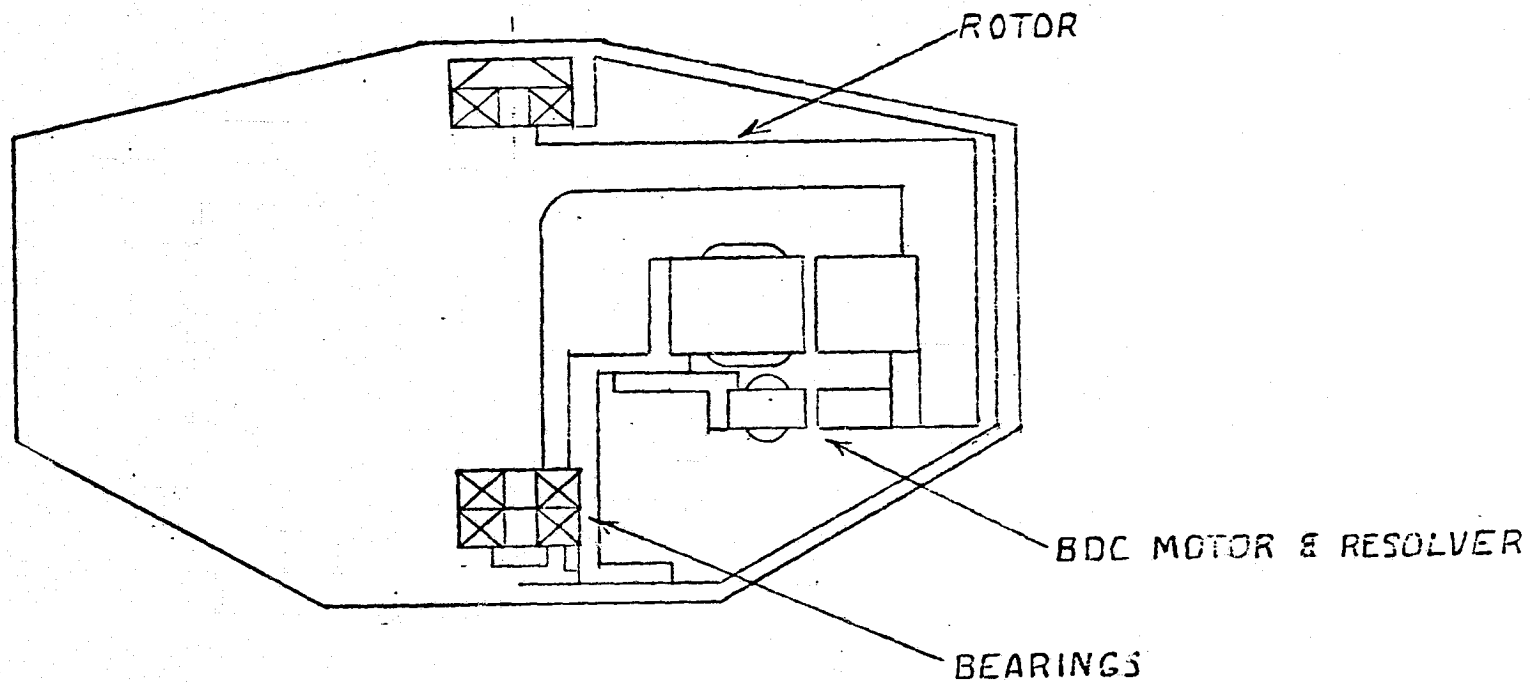

Figure 2-3 Reaction Wheel Assembly, Partial Cross Section

SCALE 1:1
R = 2.4

Figure 2-4 Three-Axis RWA

SCALE 1:2
R = 2.4"
5.5 × 9 × 11 PACKAGE

was estimated that the use of magnetic suspension would add approximately one pound to the weight of each rotor. Magnetic suspension is generally favored where very long life is required or where low running power at high rotor speed is desired. In this case, however, the high torque to momentum ratio necessitates the use of a relatively low speed rotor to keep the torquing power reasonable. Since long life is also not required, the added weight and complexity of magnetic suspension is not justified.

2.3 CMG SIZING FOR MMU

System Description - A three axis CMG configuration was considered for purposes of comparison with the reaction wheel system. Although many different configurations can (and should) be considered, the gimballed pair originally studied by Kennedy [1] was selected because it requires only two wheels and three gimbals to provide three axis attitude control.

The unit consists of a double rotor double gimbal unit shown in Figure 2-5. Rotors 1 and 2 are controlled to the same speed and momentum and gimballed independently through angles β_1 and β_2 respectively. The steering law can be derived readily if a change in variables is made.

$$\beta = (\beta_1 + \beta_2)/2 = \text{angle of resultant momentum vector}$$

$$\delta = |\beta_1 - \beta_2|/2 = \text{scissor angle}$$

A derivation of the steering law is given in reference [2].

The block diagram in Figure 2-6 shows that the CMG system acts in parallel with the reaction jet system. Depending on the torque and momentum sizing of the gyros, the momentum exchange capability can be used either in place of the reaction jets to conserve fuel, or within the reaction jet deadband to provide finer control. Calculation of the gimbal rate commands, $\dot{\alpha}_c$, $\dot{\beta}_c$ and $\dot{\delta}_c$ requires knowledge of the current momentum state (α, β and δ angles) and the three axis torque commands (M_{xc}, M_{yc}, and M_{zc}):

$$\dot{\alpha}_c = \frac{-T_{x''}}{H_t \cos\beta} = \frac{-\cos\alpha\, M_{xc} + \sin\alpha\, M_{zc}}{2H \cos\delta \cos\beta}$$

$$\dot{\beta}_c = \frac{T_{y''}}{H_t} = \frac{\sin\alpha \sin\beta\, M_{xc} + \cos\beta\, M_{yc} + \cos\alpha \sin\beta\, M_{zc}}{2H \cos\delta}$$

$$\dot{\delta}_c = \frac{-T_{z''}}{2H \sin\delta} = \frac{-\sin\alpha \cos\beta\, M_{xc} + \sin\beta\, M_{yc} - \cos\alpha \cos\beta\, M_{zc}}{2H \sin\delta}$$

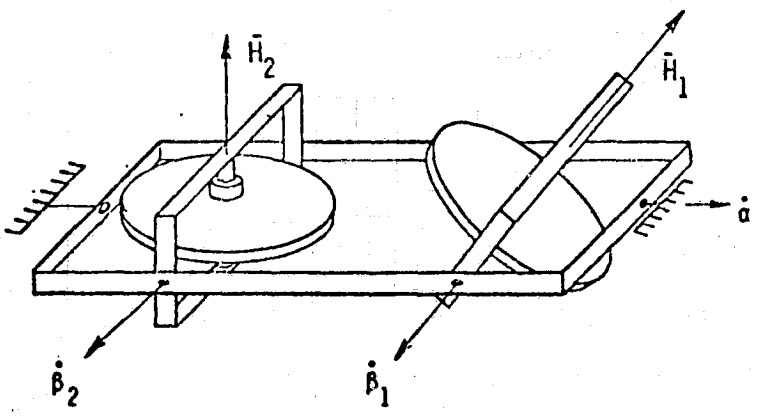

Figure 2-5 Mechanical Schematic, Gimballed Pair CMG

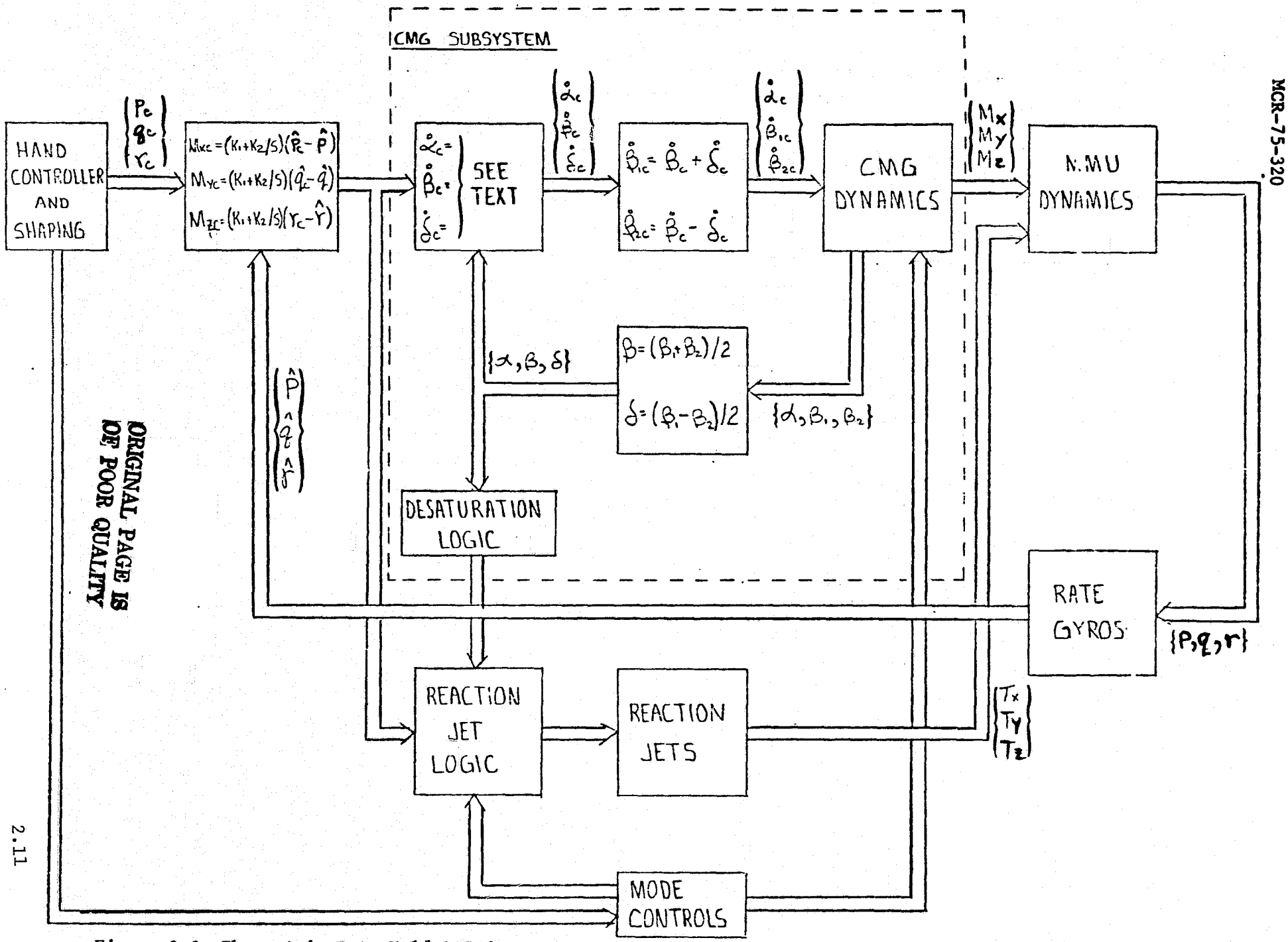

Figure 2-6 Three-Axis Rate Hold ACS for MMU

As can be seen from the control law equations, two types of nonlinearities are present. When the two momentum vectors are colinear ($\delta = 0$) no further momentum may be transferred and the CMG must be desaturated by the reaction jets. As indicated in the block diagram, this would be performed automatically by commanding the appropriate reaction jets while leaving the CMG system engaged. Also apparent in the control law equations are singularities which occur when the inner gimbal angles δ and β approach 90 degrees. These singularities may be avoided by adding additional logic to the steering law and by over-sizing the momentum of each rotor.

Present technology applicable to the required steering law control functions includes MSI and LSI semiconductor functions, LSI microprocessors, RAM and ROM memory devices, and hybrid devices. The CMG interface will require both A/D and D/A conversion. System control logic requirements such as mode control and desaturation logic would be programmed into the system executive software.

The configuration shown lends itself to compact packaging as described in the following section.

Size, Weight and Speed - The three axis gimballed pair CMG configuration described previously is considered here in terms of size, weight and rotor speed. The AMRV/CMG design was used as a basis for sizing the two wheels and their gimbal structure. For this case, there are three torque motors instead of two, three gimbal position sensors instead of two, and the addition of three gimbal rate sensors, all of which constitute the gimbal control system. A conceptual sketch of the gimballed pair CMG configuration for this application is shown in Figure 2-7. The rotors shown are three inches in diameter. As mentioned, the sketch is conceptual and the torquers, rate sensor, position sensor, and electronics sizing are estimates.

The housing and electromagnetic weights were assumed constant with the resulting equation for total system weight being

$$W_s = 8.0 + \frac{7.3 \times 10^5 \, H}{N \, D^2}$$

where W_s = system weight, lbs

H = angular momentum, ft-lb-sec

N = rotor speed, rpm

D = rotor diameter, inches

This equation does not include electronics weight which is estimated to be approximately 5 lbs for 5 power stations (three torquer power and two spin motor power) and EMI filtering.

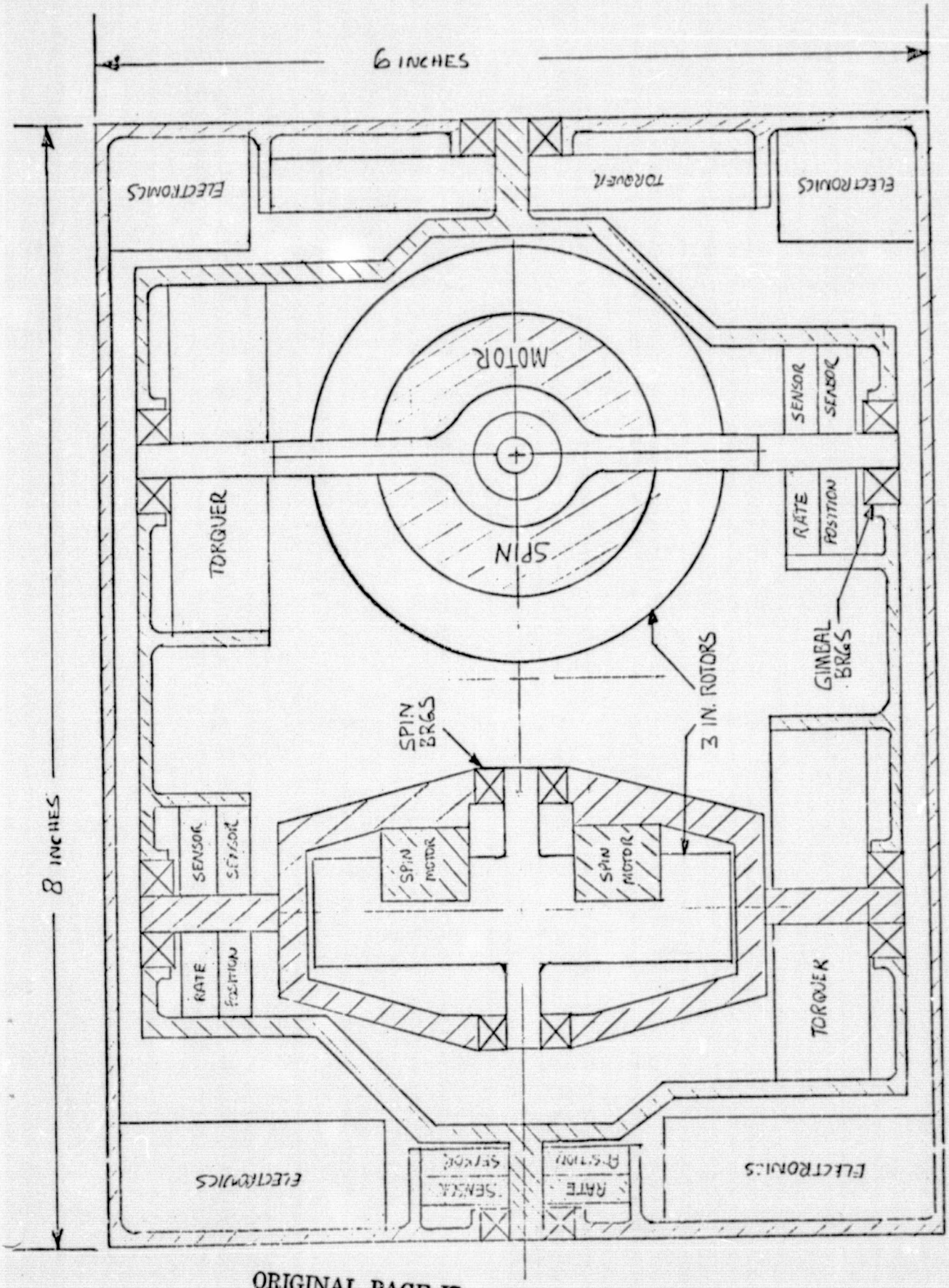

Figure 2-7 Conceptual Sketch, MMU Gimballed Pair CMGs

Because of the volume constraint of 6 in. x 8 in. x 6 in., the rotor diameter was allowed to vary between 1.5 in. and 3.5 in. Rotor speed varied from 10,000 rpm to 50,000 rpm. Figure 2-8 presents the system tradeoff parameters. System weight/rotor diameter is plotted against angular momentum/rotor speed. These parameters were normalized so that the data could be presented in a concise form. To cover the possible range of angular momentums, H was varied between 0.2 and 1.0 ft-lb-sec. As an example of the use of Figure 8, suppose the weight of a 3.0-in. diameter rotor with a single CMG angular momentum of 1.0 ft-lb-sec at 30,000 rpm is desired (potential of 2 ft-lb-sec total output of system). The H/speed ratio is 3.33×10^{-5} ft-lb-sec/rpm. From this point on the abscissa move vertically to the D = 3 in. curve and determine the weight diameter ratio on the ordinate of approximately 3.6 which gives a system weight of 10.8 lbs. This rotor size, speed, and angular momentum appear to be reasonable values in view of the requirements. The total weight including electronics would be approximately 15.8 lbs.

Power - A tradeoff exists between torquer sizing (weight) and CMG peak input power. A rough estimate of the peak power can be obtained from the following:

$$P_{shaft} = 1.356 \times \dot{\sigma}_{max} \times T_{max} \text{ (watts)}$$

relates the peak shaft output power to the maximum gimbal rate and torque. The motor winding losses can be computed from the motor constant, K_m (foot-pounds per square-root-watt) using:

$$P_w = (T_{max}/K_m)^2 \text{ (watts)} \quad .$$

A survey of currently available permanent magnet torquers indicates that the motor constant is related to the motor weight by $K_m = .152\ W$, where W is the weight in pounds. Therefore:

$$P_w = (T_{max}/.152\ W)^2 \text{ (watts)} \quad .$$

Electronic losses are attributable to both resistive losses, semiconductor junction drops, and standby power. On the basis of similarity to existing designs, it is estimated that the overall voltage drop at the minimum input voltage (assumed to be 24 VDC) and at the peak gimbal rate and torque will be approximately 7 volts. Therefore *at this condition* (peak power and minimum bus voltage), the electronic losses are:

$$P_{elec} = 7\ I_{max} + P_{run}$$

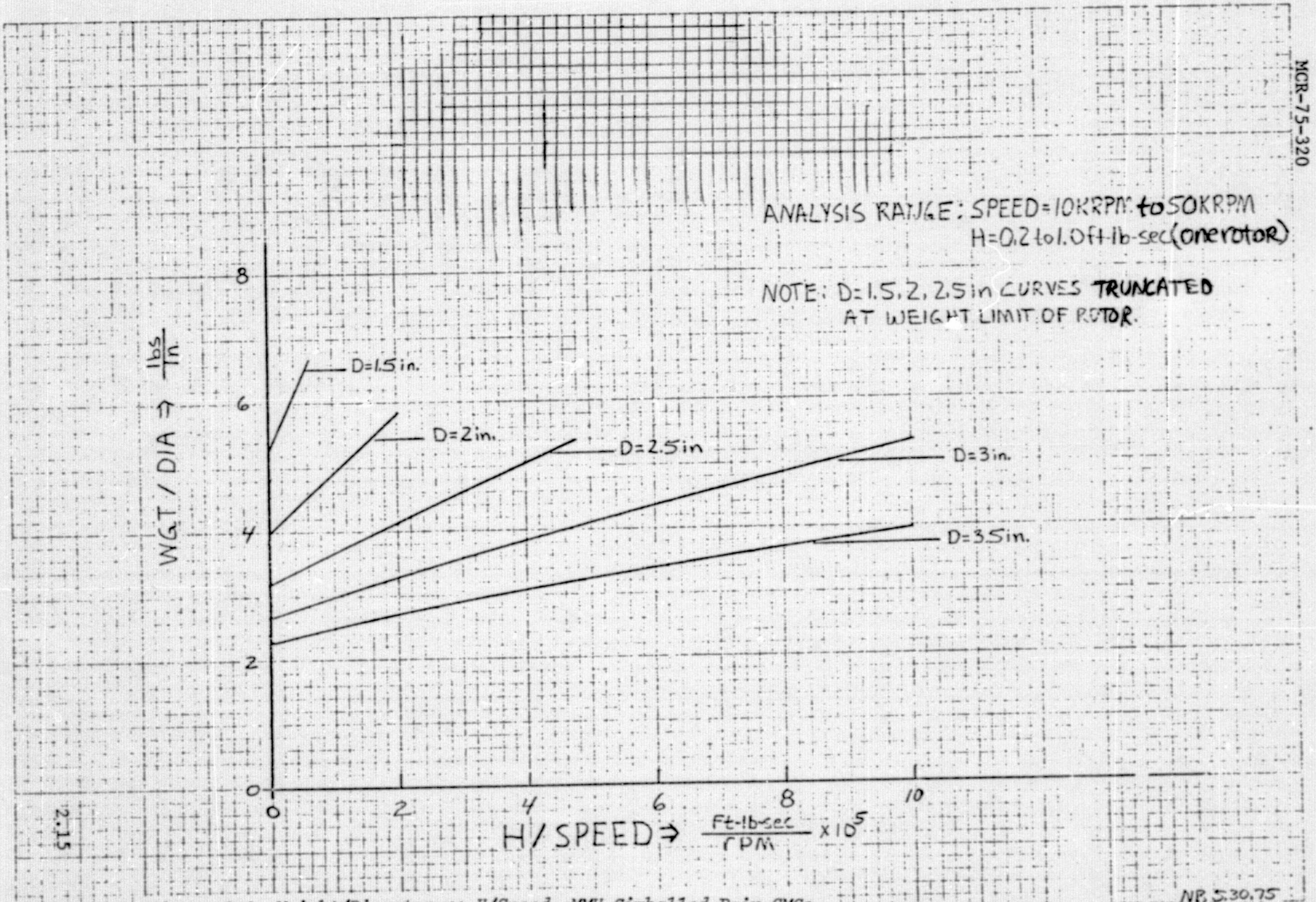

Figure 2-8 Weight/Diameter vs H/Speed, MMU Gimballed Pair CMGs

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where $I_{max} = (P_w + P_{shaft})/(24 - 7)$

Adding P_{elec}, P_w, and P_{shaft} gives the peak CMG input power:

$$P_{CMG} = \frac{7}{17}(P_w + P_{shaft}) + P_w + P_{shaft} + P_{run}$$

$$= 1.412\ [1.356\ \sigma_{max}\ T_{max} + (T_{max}/.152\ W)^2] + P_{run}$$

For the MMU, the peak torque is understood to be .5 ft-lbs and the peak momentum 1.0 ft-lb-sec. For a rough sizing, let $\sigma_{max} = T_{max}/H_{max} = 0.5$ rad/sec and let $T_{max} = .5$ ft-lbs (neglecting friction and acceleration terms).

This leads to a highly conservative peak power estimation since in a CMG of this configuration, the peak shaft rate and torque tend to occur about different axes at the same time.

$$P_{CMG} = 1.412\ [1.356\ (.5)(.5) + (.5/.152\ W)^2] + P_{run}$$

$$= 0.479 + P_{run} + 15.28/W^2$$

This equation is plotted in Figure 2-9.

The estimated running power of the gimballed pair system is expressed as

$$P_{run} = 5.8 \times 10^{-7}\ (N)^{1.667}$$

where P_{run} = running power, watts

N = rotor speed, rpm

P_{run} is plotted vs N in Figure 2-10. A reasonable rotor speed for this application would be around 30,000 rpm which results in an estimated running power of 17.3 watts. The standby power of the electronics is estimated to be 3 watts. For a one pound torque motor, which is compatible with the weight tradeoff, the total power for one channel of operation is 15.8 + 17.3 + 3 = 36.1 watts. A rotor speed of 20,000 rpm would yield a total power of 27.6 watts.

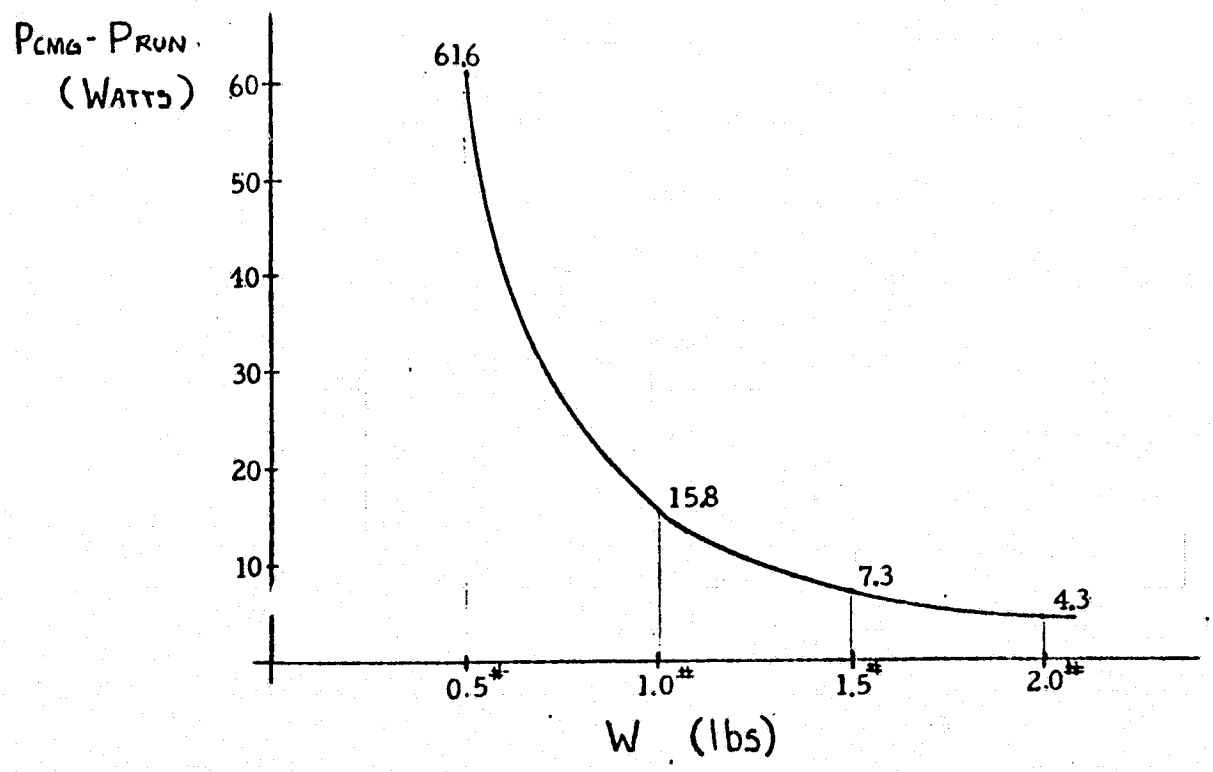


Figure 2-9 CMG Torquing Power vs Torquer Weight

Figure 2-10 Running Power vs Speed, MMU Gimballed Pair CMGs

REFERENCES (Section 2.0)

1. *A Gyro Momentum Exchange Device for Space Vehicle Attitude Control*, H. B. Kennedy, AIAA Journal, May 1963.

2. *Description and Simulation of an Integrated Power and Attitude Control System Concept for Space Vehicle Application*, R. W. Will, C. R. Keckler, K. L. Jacobs, NASA TN D-7459.

Table 2-2 Reaction Wheel Data

	BENDIX NIMBUS ERTS	BENDIX OAO	BENDIX OGO	BENDIX VELA	BENDIX ATS F&G	BENDIX NIMBUS YAW/ ERTS ADV	BENDIX NIMBUS (PITCH/ ERTS)	SPERRY (HIGH TORQUE)	SPERRY MODEL 45	SPERRY MODEL 15	SPERRY MODEL 1	SPERRY FLEET SAT COM
Inertia	0.00365 slug-ft^2	0.034 slug-ft^2	0.011 slug-ft^2	0.065 slug-ft^2		0.0025 slug-ft^2						
Momentum, (ft-lb-sec)	0.575	2.06 Fine 3.56 Coarse	1.44 Two 7.2 Ranges	8.5	4.7	0.327	1.37	7.5	45	15	1	7
Stall Torque (ft-lb)	2 oz-in. (0.104)	2 oz-in. (.0104) 32.7	6.5 oz-in. (.0323) 20	20 oz-in. (.104)	6.25 (.032)	4 oz-in. (.021)	4 oz-in. (.021)	50 oz-in. (.26)	8 oz-in. (.042)	7 oz-in. (.036)	5 oz-in. (.026)	24 oz-in. (0.125)
Watts Power at Runup	5	60 Coarse 4 Fine	27	28		13	13	108	70	50	20	Not Specified
Weight, Total Lb Rotor Lb	4.8 2.9	17 7.7	9.8 5.5	19.5 12.5		5.2 2.1	9.0 5.1	15	25	18	7.0	12.5
Synch. or Max Speed Motor Type	1500 rpm AC Induction	1200 rpm AC Induction	1500 rpm AC	1500 rpm AC	1500 rpm AC	1500 rpm AC	1500 rpm AC	2000 rpm		2750 rpm AC Induc-tion	2000 rpm DC Brush-less	3100 rpm
Environment	Vib .2g^2/Hz 20-7000 Acc 15g Temp +14°F to 58°F Vib 10g^2, 20-2000	Vib .03g 75-2000 Acc 11.5g Shock 30g 6,11 msec Vib 7.5g 5-2000	Vib .1g^2 20-2000 Acc 13g Shock 45g Vib 3.5, 6.5, 13g's 5-3000 Hz	Vib .03g^2 12g^2 20-2000 3.5, 5g 20-2000 Acc 30g, Shock 80g	Complex Spectrum					Complex Spectrum		
Power	26V 400 Hz 2Ø	26V 400 Hz 2Ø		36V 400 Hz 2Ø		26V 400 Hz	21.6V 400Hz 2Ø					
Application	Nimbus ERTS Has flown	OAO Has flown	OGO Flown	VELA Flown				Not Used As Yet				
Size, (D=Diameter, W=Width)	6D, 3W	Coarse 12D, 5W Fine 10D, 5W	7D 4W	12D, 4.6W		6D, 3.5W			15D, 10W	10D, 8.5W	7.5D, 5W	
Growth Potential H	1.2 ft-lb-sec	Fine 6 ft-lb-sec	6 ft-lb-sec									

MCR-75-320

3.0 SURVEY OF NUMERICAL AND ALPHANUMERICAL DISPLAY TECHNOLOGY

By: A. M. Ray
J. J. Leonard

3 July 1975

3.1 INTRODUCTION

The MMU pilot will need a certain degree of autonomy in his EVA activities. This requirement indicates that a display system is required which presents the pilot with all necessary information for MMU checkout, donning, maneuvering, servicing, doffing, and stowage. For efficiency of weight, volume, and crew workloading, the display may be integrated with the life support system displays. In either case, the display must be low power, meet a large range of temperature extremes, and be legible under all conditions from direct orbital altitude sunlight to almost total darkness. It should be highly reliable and compatible with state of the art electronic logic circuits.

Display technology is advancing very rapidly. There are numerous display alternatives for the MMU. Because of the severe MMU display requirements and the large number of alternatives, a display technology survey was undertaken. Display manufacturers supplied information (including performance parameters) on their product lines. Performance parameters were summarized for each type of display and some observations and general conclusions were drawn. Final display selection will require further definition of data processing requirements for the data to be displayed.

3.2 NUMERICAL READOUTS

Numerical readouts of various life support and maneuvering unit subsystem parameters are a very attractive way to display a large amount of data in a small volume allowing the pilot a degree of autonomy in his EVA activities without relying on TLM for subsystem status and performance data.

This report is limited in scope to numerical readouts which display from one to eight digits. A digit can be a number from zero up to and including nine, a hexadecimal character which includes numbers from zero to nine and the letters A through F; or an alphanumeric which includes up to 64 characters and numbers similar to those on a typewriter keyboard.

3.2.1 MMU Display Requirements

Maneuvering units and life support systems have a large number of parameters that should be displayed to the EVA astronaut. A means of minimizing the size of the display package is to utilize one numerical readout display that can present each of the parameters to the crewman. The display would be in conjunction with a caution and warning type bilevel or trilevel display which displays the qualitative status of each system to the pilot. In the event of a malfunction or for the purpose of real time mission planning, the pilot can control the readout to display quantitatively the parameter that he needs. The pilot's selection of parameters to be displayed could be accomplished in various ways; for

example, push button switches, one or more rotary switches, or lever switches.

The challenge to the display technology is a display which is legible under all lighting conditions with high reliability, broad band storage and operating temperatures, low power, and small size and weight.

3.2.2 Candidate Displays

Based on the survey of display manufacturers, the following displays should be considered for numerical readout:

Light emitting diodes - LED

Liquid crystal display - LCD

Planar gas discharge displays - PGDD

Plasma panels

Incandescent flat packs

Incandescent tube displays

Incandescent fiber optic and rear projected displays

Fluorescent tubes

Electro-mechanical

Miniature CRT-type displays

Voice synthesizers

These display types are summarized in Table 3-1 and discussed below in terms of their performance characteristics and EVA applicability. Mention is also made of some expected advances in the state of the art.

3.2.2.1 Light Emitting Diode

The LED is probably the most popular numerical display in use today. However, it will probably not be able to meet the EVA lighting and environmental requirements unless it is used inside the helmet or with specialized filters.

LEDs are solid state devices which have extremely fast response and high reliability. They are small, low-cost devices capable of very long service life. Brightness is from 200 to 400 foot-lamberts depending on the forward current. However, without special filters they are not visible in direct sunlight. Storage temperatures are -55°C to 100°C with operating temperatures from 0°C to 70°C.

Principal manufacturers of LED readouts include Monsanto, Dialight, Hewlett Packard, Chicago Miniature Lamp, and about twenty others. The larger readouts incorporate waveguides, fiber optics, or magnification in order to keep the actual LEDs as small as possible.

Table 3-1 Alphanumeric, Hexadecimal, and Numeric Displays*

Parameter	Light Emitting Diode	Liquid Crystal Display				Gas Discharge Flat Packs
		Scattering		Field Effect		
		Transmissive**	Reflective**	Transmissive**	Reflective**	
Operating Principle	Junction - electro-luminescence (7 segment, 9 segment, or 36 dot matrix)	In the quiescent state, the crystal is clear and passes light. Voltage gradients create discontinuities that scatter light (irradiantly reflect) and active areas appear bright. Typically, scattering type displays have dark digits (normally clear).		In the quiescent state, field effect crystals rotate incident light 90 deg. When current is applied, the molecules between the electrodes are rotated 90 deg so they no longer rotate the light.		Neon gas ionization with either pulsed or "key alive" voltages
		Backlighting	Mirror Backing	For lighted digits, backlighting and crossed polarized front and back filters are used.	For lighted digits, a mirror backing and crossed polarized filters are used.	
Light Output	300 ft-L typical 800 ft-L maximum	20 to 1 contrast ratio		Up to 40 to 1 contrast ratio; 25 to 1 typical		50 lm/ft^2 neon orange
Operating Voltage	1.5 V typical 5 V maximum	Greater than 5V minimum***;15 to 20V typical (AC for optimum life, 30 to 1000 Hz)		Less than or equal to 5V minimum***; 15 to 20 V typical (AC for optimum life, 30 to 1000 Hz)		180V dc typical
Operating Current for Six "8's"	1440 mA for 7 segment, 2880 mA for matrix, maximum ~ 5A	Nanowatts to Microwatts		Nanowatts (22 microwatts maximum)		About 2 mA typical
Life (at rated current)	.1 to 100 Mhrs	3K hours to 30K hours; 20K hours typical				50K hours
Operating Temperature	0°C to 70°C	5°C to 55°C; typically -10 to 65°C				0°C to +70°C
Storage Temperature	-55°C to 100°C	-20°C to +70°C		-20°C to +70°C		-55°C to +125°C
Viewing Angle		60 to 80 degree maximum				130 deg typical
Flight Qualified						
Character Height		.2 in. to 1.2 in.				.33 in. to .4 in. typical
Comments	Dialight 745-0005, 745-0006 Contrast washes out in direct sunlight	Multiplexing for up to 8 digits with only 16 leads and drivers required		Multiplexing for only 4 digits, not quite as bright but response is much faster than light scattering LCDs.		Similar to neon tube digital displays. May require electrostatic shielding.

* 0 through 9 and A through F
** There is also a dual mode operation with a semi-reflective mirror with backlighting.
*** Multiplexing requires 40V ac power with some sacrifice of contrast and operating life. LCDs contrast improves under sunlight conditions. Below 10°C LCDs do not respond quickly to excitation. Low wattage heating elements may be required for low temperature applications.

Table 3-1 Continued

Parameter	Incandescent Projected Segment Display	Incandescent Tubes	Incandescent Flat Packs	Plasma Panels	Special Miniature CRTs ("NIMO")
Operating Principle	Seven or sixteen segments with each segment illuminated with a separate miniature lamp	Seven luminescent segments in a single plane arrangement on a black ceramic base sealed in a glass tube	Seven segment tungsten filmanet mounted on a black ceramic base in a 14 pin DIP packaging	Neon or helium gas discharge	The IEE "NIMO" is a 10 gun cathode ray display tube with the characters generated in a single plane on the face of the tube
Light Output	500 ft-L; 1.5 minimum contrast in 8,000 f.c.	85,000 ft-L at 12 volts; any color filter	4,500 ft-L	60 ft-L	100 ft-L normal; 500 ft-L maximum.
Operating Voltage	4.5V dc	3.5 to 12 volts, AC or DC	5 volts	300 volts	Anode, 1750V dc; filament 1.1V AC or DC
Operating Current for Six "8's"	.7 Amps	.4 Amps to 1.26 Amps	.6 Amps	.75 mA/dot; characters are 35 dot	Anode, 30 μA; filament .2 A
Life (at rated current)	5000 hours	From 10K hrs to 100K hrs	100K hours	50K hours	10K hours to 200K hours
Operating Temperature	TBD	-50°C to +125°C	-55°C to +70°C	-10°C to +55°C	+5°C to +55°C
Storage Temperature	TBD	TBD	TBD	-65°C to +70°C	+85°C maximum
Viewing Angle	150 deg	140 deg	120 deg	120 deg approximately	160 deg
Flight Qualified	MIL-STD-202	MIL-STD-202D (201A) for Vibration (213A, Cond. J) for Shock		Not	TBD
Character Height	.4 in.	.4 in. to .6 in.	.47 in. to .614 in.	.2 in. or .3 in.	.625 in. typical
Comments:	Aerospace Optics Incorporated			Not bright enough	Less than 30 mW total power consumption. Brightness is marginal

Table 3-1 Concluded

Parameter	Electromechanical	Neon Tube Digital Displays	Fiber Optic Displays
Operating Prinicple	Display window with either moving drum, belt, or tape with the characters positioned by electric motor	Cold cathode single plane gas ionization, seven segments	Seven incandescent bulbs each illuminating three dots per segment. Similar displays for 16 segment alphanumerics.
Light Output	Reflective phosphorescent or backlighted	500 ft-L	1200 ft-L, contrast 7 to 1 minimum
Operating Voltage	24 to 28V typical (6 - 8 volts for backlighted)	160 to 190V dc	5 volts
Operating Current for Six "8's"	Starting, .5A*; Running, .125A (56 mA for backlighted)	14.7 mA to 25 mA	840 mA
Life (at rated current)	10^6 random indications	100K hours	10K hours
Operating Temperature	-54°C to +71°C	-10°C to +55°C	-54°C to +80°C
Storage Temperature	-62°C to +95°C	-65°C to +70°C	To + 95°C
Viewing Angle	120 deg	120 deg	Up to 120 deg
Flight Qualified	MIL-E-5422D, Environment	MIL-STD-202D (201A), Vibration and (213A, Cond. J), Shock	Hughes, F18 MDAC, MIL-E-5400, Canada Helicopter
Character Height	No limit, typically .21 in. to .37 in.	.38 in. to .59 in.	
Comments:	*Once positioned, they consume no power until the displayed information is changed, except for backlighting. Specifications are for 10 digit display with BCD decoder and display driver. 64 character display requires about 100% more power with one-half the life.	Similar to planar gas discharge can be operated in either a direct DC or time-shared, multiplexed mode, and can be used with standard TTL-compatible BCD to seven circuit driver/decoders	20 mA decoder driver available. Wire leads. Sperry flight testing. Seems to be brightest.

For the MMU applications viewing angle requirements are small thus allowing for use of louvered or other narrow field of view filters to increase the display contrast ratio and directional brightness.

The following were identified in the manufacturers' survey as providing display lenses, filters and louvers:

3M Visual Products Division

Polaroid

Panelgraphic Corp.

Optical Coating Laboratory

3M manufacturers a louvered light control film in either clear or red with louvers at 0, 18, 30, 94 45 deg. The louvers and filters are applicable to all types of displays. They are commonly used with LEDs to prevent sunlight washout, but they are not yet proven for use in direct sunlight.

3.2.2.2 Liquid Crystal Display

The LCD has been the logical choice for many applications which require sunlight legibility. However, multiplexing is not presently feasible for more than a couple of digits. Also, LCDs will probably not meet the environmental temperature extremes during on-orbit stowage. A big advantage of this type of display is that it requires no intensity adjustment over a large range of lighting conditions. They do however require either some ambient lighting or backlighting for use in extremely low light levels.

There are numerous manufacturers of LCDs; however, Hamlin of Lake Mills, Wisconsin, has acquired a large portion of the LCD market. LCDs can be made using two different types of crystal structure. The "light scattering" LCDs employ a thin film crystal that is normally clear but appears frosted when an electronic current is present. This frosted appearance is because of a type of turbulence set up in the film by the presence of the current. The "field effect" LCDs employ a crystalline structure that normally rotates light waves 90 deg due to its helical arrangement of molecules. An electric current realigns these molecules so that no rotation of the light waves occurs.

Either type of LCD can be made either transmissive requiring backlighting, reflective using only ambient lighting, or more recently a "trans-flective" back surface in which most of the ambient light is reflected; however, backlighting is used for low ambient light levels.

In any case, the digits can be made to appear dark or light through proper orientation of polarizing filters for field effect LCDs and through proper electrode placement for light scattering LCDs. Typical

light scattering displays use white characters as do typical transmissive field effect LCDs, whereas reflective field effect LCDs typically have dark characters. This is because it is more efficient to energize only the characters than it is to energize the surrounding background.

3.2.2.3 Planar Gas Discharge Displays (PGDD)

The PGDD are brighter than LEDs and less susceptible to the EVA environmental temperature extremes. Unlike the original Nixie tube, they are segmented numbers. They are becoming more popular for interfacing with MOS/LSI for use in DC or multiplexed applications. They typically require 180 volts dc but with less than 1 milliamp of current per digit. It is a visually attractive display because the seven segments blend into a line which appears continuous. Minimum storage temperature is -55°C.

The Helipot Division of Beckman Instruments (previously a subsidiary of Sperry) in Scottsdale, Arizona, has become the front runner of a relatively few manufacturers of PGDDs. These include Cherry Electrical Products Corporation, National Electronics, and Burroughs, who made the original Nixie tube twenty years ago. (Nixie tubes were the first display that was compatible with solid-state, high-speed decoding and driving electronics.) Beckman offers an economical dc to dc converter to operate the displays from a 5v dc source. Burroughs offers a Panaplex II series which are multiple digit displays from 4 to 12 digits. Whereas a discrete 12 digit LED display would require 132 connections, a 12-digit Panaplex II unit requires only 19 connections. Cherry and National Electronics also make similar multiple digit displays.

3.2.2.4 Plasma Panels

Plasma panels are used to display from 10 to 4000 characters and bridge the gap between the CRT and single character readouts. These are typically composed of a series of 5 x 7 dot matrices with each dot a neon cell with a constant sustaining voltage and switching voltage required for illumination. Principal manufacturers are Burroughs, Owens-Illinois, and Industrial Electronic Engineers.

3.2.2.5 Incandescent Flat Packs

Neil Schlater in the December 1974 issue of *Instruments and Control Systems* says that "... the emphasis on display life, reliability and compatiblity with integrated switching circuitry has virtually eliminated the incandescent display from serious consideration ... however, where there are special requirements for high visibility and adjustable brightness level, the incandescent display in its many forms retains its superiority."

The first form to be discussed is the incandescent flat pack constructed of seven (or more) segment characters with an incandescent filament for each separate segment. Industrial Electronic Engineers have such a display which they rate at 85,000 ft-L. Yet their engineer as well as an Aerospace Optics, Inc. engineer claim that these are not sunlight-readable. The 85,000 ft-L is probably a misuse of lighting units in that only a small point on each segment is 85,000 ft-L. (Candela is the appropriate measure for brightness for a point source whereas ft-L which is brightness per unit area should be used to measure brightness of a total segment or digit.)

3.2.2.6 Incandescent Tube Displays

Industrial Electronic Engineers, Inc. is the only manufacturer of this display that was identified in the survey of manufacturers. The display has no apparent advantages over the incandescent flat pack and is larger in size.

3.2.2.7 Incandescent Fiber Optic and Rear-Projected Displays

For sunlight readability, the incandescent projected displays are very promising according to Industrial Electronic Engineers, Inc. and Aerospace Optics. They require relatively large amounts of power (about 2.5 watts for six digit display), with decoder/drivers available from several manufacturers.

The IEE display has been chosen by MDAC for the F-18 and by Hughes, Sperry, and a Canadian helicopter manufacturer for NASA and military specification testing.

The higher power requirements, wire leads, and solid state logic compatibility appear to be the biggest drawbacks.

The sunlight readability is obtained by projecting, with optics or waveguides, a relatively bright incandescent light source onto a very small area or segment. This collects the light into a small area for brightness amplification and contrast enhancement since no light is transmitted to the surrounding area.

3.2.2.8 Fluorescent Tubes

While only a few U. S. manufacturers build fluorescent seven-segment display tubes and panels, these devices are competitive with the neon devices. They offer a pleasing blue-green presentation in place of the orange-red glow of the neon gas. Tung Sol, a division of Wagner, was the only manufacturer of fluorescent tube displays that we identified in our manufacturers' survey and have not yet received their catalogs.

3.2.2.9 Electromechanical

The major emphasis of this display survey has been on lighted displays because of their simplicity and increased reliability over typical electromechanical displays. However, there are a few electromechanical displays which are military flight qualified and should be considered in this survey.

An electromechanical device has several advantages for sunlight legibility and was therefore used on the Apollo life support system on the lunar surface for a cuation and warning device with a deflection pressure gauge for a quantitative display. The scale marks were phosphorescent for low ambient lighting but were also legible in direct sunlight.

Union Switch and Signal Division of Westinghouse Air Brake manufacturers 10, 12, and 64 character readouts with or without internal backlighting and with binary to digital decoders. They require from 3 to 7.5 watts to run per digit with 0.0 watts steady state except for backlighting when supplied. Character height is from 0.21 in. to 0.38 in.

3.2.2.10 Miniature CRT-Type Displays

Industrial Electronic Engineers manufactrers a 10 gun CRT with single plane 0.62 in. high characters (numerals, letters, symbols, and messages) consuming less than 30 mW of power and producing up to 500 ft-L. They also have recently introduced a 64 character display to this series. The biggest drawback is the high voltages required (1,750 v dc) and flight qualifications.

3.2.2.11 Voice Synthesizers

Master Specialties Company manufactures special purpose voice synthesizers primarily for Western Electric Telephone systems. Applications to displays for real time control are under investigation. The present systems are all solid-state system with 10 numeric words (0 - 9) stored in read-only memories (ROM). One model accepts multi-frequency inputs, stores the data, decodes the data into digital signals, and provides output in voice readout of the desired numbers.

3.2.2.12 Future Display Technology

Among the display technologies which have not yet been commercially introduced are electrophoretic and electroluminescent readout panels. The electroluminescent technology was introduced about 10 years ago for edge lit panels but still awaits readout capability. The electrophoretic offers some promise for MMU applications with a variety of colors, and like the LCD, is a passive display dependent on ambient lighting for visibility in most applications. Further upstream in the technology

development are erasable light-addressed light valves and flat panel CRTs. It is doubtful that any of this technology will yield flight qualified hardware before 1980, but may have potential advantages for later MMU applications.

3.2.3 Results and Conclusions

It is apparent that LEDs would be the most desirable display because they require low power, are very reliable, and are the most compatible with modern logic circuitry. However, LEDs are not bright enough without brightness and contrast enhancers which are yet unproven for sunlight legibility.

Liquid crystals are difficult to integrate into the modern logic circuits and function only in a small temperature range. Their big advantage is that they rely only on ambient light, require no intensity adjustment, use almost no power, and maintain high contrast ratio over all lighting levels.

Gas discharge displays require 180 volts but very little power and show little promise of legibility in direct sunlight.

The only display being really pushed as legible in direct sunlight are the rear projected and fiber optic incandescent displays. They however use a lot of power (~ 2.5 watts for six digits) and are difficult to integrate into modern logic circuits. Their reliability is low with only one lamp per segment. A program of lamp burn in and early replacement would most likely be required for sufficient reliability. For annunciator or lighted switch applications, two lamps could be utilized for each message, (whereas display size may not permit two lamps for every segment on the segmented character readouts).

There is no present requirement for lighted switches. For typical application, simple lighted displays can display status of automatic systems and caution and warning indicators. Toggle or rotary switches can be used to indicate status of pilot selectable functions. Lighted switches can be used to indicate status of automatic systems which also have a pilot override capability.

From the data gathered in this survey, fiber optic incandescent displays are the most promising approach for meeting the requirement for readability in direct sunlight.

MCR-75-320

4.0 SURVEY OF ELECTRONIC DEVELOPMENT TRENDS

By: J. Wathen

1 August 1975

4.1 SUMMARY

A survey of the dynamic electronics field since the astronaut maneuvering equipment was designed for the Skylab experimental program circa 1970 reveals many new developments applicable to future MMUs. The most significant recent development has been the microprocessor. For the MMU, microprocessors make possible the realization of more complex and sophisticated functions easily modified by programming (true hardware adaptability). Some possible MMU functions with microprocessors are:

- More efficient control modes such as retrace or repeat maneuvers;
- Routine maneuver programs;
- Rendezvous capability;
- Automatic astronaut retrieval;
- Self-test;
- Emergency interrupt;
- Gyro parameter correction.

There are many microprocessors to choose from. Two low power candidates are the COSMAC (RCA), a CMOS unit, and the SBP0400 (TI), an integrated injection logic (I^2L) unit. The two candidates are a study in contrasts, except that they both have low power requirements. COSMAC has a fixed, though varied, instruction set with a great deal of hardware and software backup provided by the manufacturer. The SBP0400 has a user defined instruction set (it is microprogrammable) and virtually no manufacturer backup. Good backup decreases the main microprocessor system cost--software. Microprogrammability means greater potential for tailoring the instructions to the requirements, in a word--performance.

There are two low power technologies, CMOS and integrated injection logic (I^2L). CMOS is much further along with a large selection of units to choose from. It has many advantages for MMU use: low power dissipation, high noise immunity, insensitivity to temperature variations, good switching speeds, and single, unregulated power supply operation. One of the big advantages of CMOS is its use in memory devices, where the quiescent power dissipations will run two to three orders of magnitude less than other technologies (except integrated injection logic). CMOS programmable (by the user) read only memories have recently appeared. They will be especially important to Aerospace needs for low power, short design time, and reduced programming cost. RCA is the only company qualified to the high reliability specification MIL-M-38510, but National Semiconductor expects this level qualification by August, 1975. Also by August, 1975, Motorola has plans for NASA line certification (a big step to MIL-M-38510

qualification). I^2L, the other low power technology (actually a bipolar process) has CMOS dissipation and Schottky TTL speeds. A relative newcomer, I^2L is gathering momentum fast both in new units and improved processing with higher performance. Although most of the work has been custom up to now, 1976 should see many new standard I^2L circuits.

4.2 MICROPROCESSORS

4.2.1 Applicability

Probably the most significant development in electronics in recent times is the microprocessor. A microprocessor or microcomputer may contain one integrated circuit or it may contain as many (or more than) 30 integrated circuits. Functionally, a microprocessor contains a programmable data-processing system consisting, at a minimum, of an arithmetic logic unit (ALU), some registers, and some type of control. It may also contain a register stack or a random access memory, data buses, and most significantly, a read-only memory containing microprograms or microoperations. Hardware costs are becoming a small part of the total cost of microprocessors. Since software is the major cost, it is usually advantageous to put more money into the hardware to save on software cost.

Guidelines for Using a Microprocessor: (Reference 4.6.1)

- More than 30 integrated circuit chips required;
- Programming required for expected system changes;
- Complex logic and arithmetic functions required.

When not to Use Microprocessors:

- If great speed is required, hardwired ECL and Schottky controller processors are an order of magnitude faster than present microprocessors. However, Motorola has recently announced an ECL microprocessor. Raytheon had plans for a 16-bit ECL microprocessor with a cycle time of 1.0 μ, but will probably not produce it;
- If large word lengths are necessary (greater than 32 bits);
- If memory size is very large (greater than 64 kilobits), there is an address line limitation.

Whether or not microprocessors are appropriate for future MMUs depends on the complexity and number of functions added to the M509 concept. A microprocessor in the MMU would provide the astronaut the power and efficiency of a personal computer. New functions can be realized that increase the operating efficiency and the safety of the astronaut. Possible MMU microprocessor applications are:

- Control logic for MMU - providing that control is more complicated than combinatorial logic or programming is required.
- More efficient control modes - more efficient thruster control modes where retrace or repeat maneuvers could automatically be carried out for a specific set of commands. The retrace commands could be stored in a last-in-first-out (LIFO) stack and the repeat commands stored in a first-in-first-out (FIFO) stack. A more efficient storage method would store the resultant of the commands to be retraced or repeated. However, the retention of the exact commands vs time might also be desirable.
- Routine maneuver programs - another microprocessor use with an increase in efficiency could be the storing of routine maneuvers in read only memory (ROM). Increased efficiency would mean less fatigue for the astronaut, allowing him to operate longer, faster and with more intelligence.
- Rendezvous capability - a rendezvous capability could be incorporated in the MMU with a microprocessor, enabling the astronaut to intercept objects in space. With the aid of radar or beacon sensing, a microcomputer could calculate and display range and range rate information to a destination. This information could also be used for automatic interception, providing thruster control for proper interception in space.
- Automatic astronaut retrieval - automatic return to the space ship could also be accomplished with beacon and microprocessor control. This could be initiated by command and by emergency conditions indicating a disabled astronaut. Microprocessors can monitor many items, combine and compare arithmetic/logical operations, and initiate and control appropriate action to be taken.
- Self-test capability -
  - Preflight test routine can be stored in ROM and called up by a command switch to give a go/no-go status.
  - Continuous self-test is possible during normal operation.
- Emergency interrupt - critical parameters can be constantly monitored and if limits (programmable) exceeded, emergency interrupt can call up a corrective subroutine. The subroutine can involve a number of decisions based on measurements, arithmetic operations, and logic operations.
- Gyro parameter correction - a microprocessor would provide a programmable means of enhancing gyro operation by sensing and correcting for parameter variations such as scale factor and bias. This could provide a means of reducing power consumption by the use of small, low powered gyros without the need of temperature control. In a pulse rebalance gyro loop, the pulse generator

must produce pulses of constant areas under changing conditions. Temperature variations can cause parameter changes that affect bandwidth of the loop as well as scale factor. A bias error, generated by the electronics, also changes with temperature and time. Microprocessors could provide a convenient and accurate means of compensation for these errors.

4.2.2 Microprocessor Candidates for the MMU

For low power operation, CMOS and integrated injection logic (I^2L) microprocessors are the leaders (see Table 4-1). I^2L is not yet available in standard circuits, but Texas Instruments' first microprocessor, the SBP0400, uses I^2L technology. Additional registers and memories could be custom I^2L (standard I^2L circuits will be out in 1976) or could be picked from the large assortment of CMOS memory units.

The SBP0400 architecture is that of a bit-slice microprocessor (Figure 4-1). These microprocessors are now available in 2-bit and 4-bit fully parallelable architectures. Typical of I^2L operation, the SBP0400 has a large range of power dissipation vs propagation delay. Propagation times of 110-530 ns can be obtained at 128 mw. The unit can be powered down by 5 or more orders of magnitude (which puts it in the range of quiescent CMOS) and with typical I^2L operation will not lose functions or memory data (Figure 4-2).

Other features of the SBP0400 include:

- 16 function symmetrical arithmetic logic unit with full carry look-ahead logic;
- An 8-word general register file that includes a program counter and incrementer;
- Two 4-bit working registers that can handle both single and double length operations;
- A factory programmable logic array (PLA) providing 512 standard operations--the PLA is often more powerful and efficient than a control ROM.

The CMOS microprocessor to be considered is the RCA COSMAC. This is an 8-bit, register-oriented central processing unit designed for use as a general-purpose computing element. COSMAC is implemented as two LSI devices and belongs to the chip family architecture. The strong points of this microprocessor are:

- Low power dissipation;
- Can be powered by unregulated power supplies;

Table 4-1 Microprocessor Comparison Chart

Manufacturers	Device	Technology	Bit Slice	CPU[1]		Memory Family		Data Word Size	Memory Capacity	Microprogrammed	Instructions	Stack	Interrupts	DIP Pins	Voltage
				One Chip	Chip Set	RAM	ROM PROM								
Burroughs	Mini D	PMOS	No	√		On Chip	On Chip	8	256	No		-	No	16	12, +5
Fairchild Semiconductor	F 8	NMOS	No		√	√	√	4/8	64K	No	101	64	Multilevel	40	12, +5
	PPS-25	PMOS	No		√	√	√	4	12K	No	32	4	No	16/18/ 24/40	-10, +5
General Instrument	CP-1600	NMOS	No		√	√	√	16	64K	No	68	8	Multilevel	40	12, +5
Intel	4004	PMOS	No		√	√	√	4	4K	No	45	3	No	16/24	-10, +5
	8008	PMOS	No		√	√	√	8	16K	No	48	7	Multilevel	18	-10, +5
	8080	NMOS	No		√	√	√	8	64K	No	78	RAM	Multilevel	40	-5, +5, -9
	3000	Schottky Bipolar	Yes		√			2 Bit Slice	64K	Yes	512	RAM	Multilevel	28	+5
Intersil	6100	CMOS	No		√	√	√	12	4K	No	40+	-	1	40	+5
Monolithic Memories	5701/6701	Schottky Bipolar	Yes		√	√	√	4-Bit Slice	64K	No	36	16	1	40	+5
Mostek	5065	PMOS	No		√	√	√	8	32K	No	51+	RAM	3	40	+5, 12
Motorola	M6800	NMOS	No		√	√	√	8	64K	No	72	RAM	1	40	+5
National	IMP4	PMOS	Yes		√	√	√	4	64K	Yes	43+	16	2	24	-12, +5
	IMP8	PMOS	Yes		√	√	√	8	64K	Yes	43+	16	2	24	-12, +5
	IMP16	PMOS	Yes		√	√	√	16	64K	Yes	43+	16	2	24	-12, +5
	PACE	PMOS	No		√	√	√	8/16	64K	No	337	10	Multilevel	40	-12, +5
RCA	COSMAC	CMOS	No		√	√	√	8	64K	No	37	RAM	Multilevel	28/40	+12
Raytheon	RP16	ECL Bipolar	Yes		√	√	√	4 Bit Slice	64K	No	32	RAM	2	48	+5
Rockwell	PPS-4	PMOS	No		√	√	√	4	12K	No	50	3	No	42	-17
	PPS-8	PMOS	No		√	√	√	8	12K	No	90+	2	Multilevel	42	-17
Signetics	2650	NMOS	No		√	√	√	8	32K	No	72+	8	Multilevel	40	+5
Texas Instruments	TMS 1000	PMOS	No	√		On Chip	On Chip	4	8K	No	43	1	No	28/40	+15
	SBP 0400	I^2L Bipolar	Yes		√	√	√	4-Bit Slice	64K	Yes	512	RAM	Multilevel	40	+4
Toshiba Transistor Works	TLCS-12	NMOS	No		√	√	√	12	4K	Yes	18	RAM	Multilevel	16/24/ 26/42	-5, +5

Notes 1) CPU includes ALU, controller, and control memory

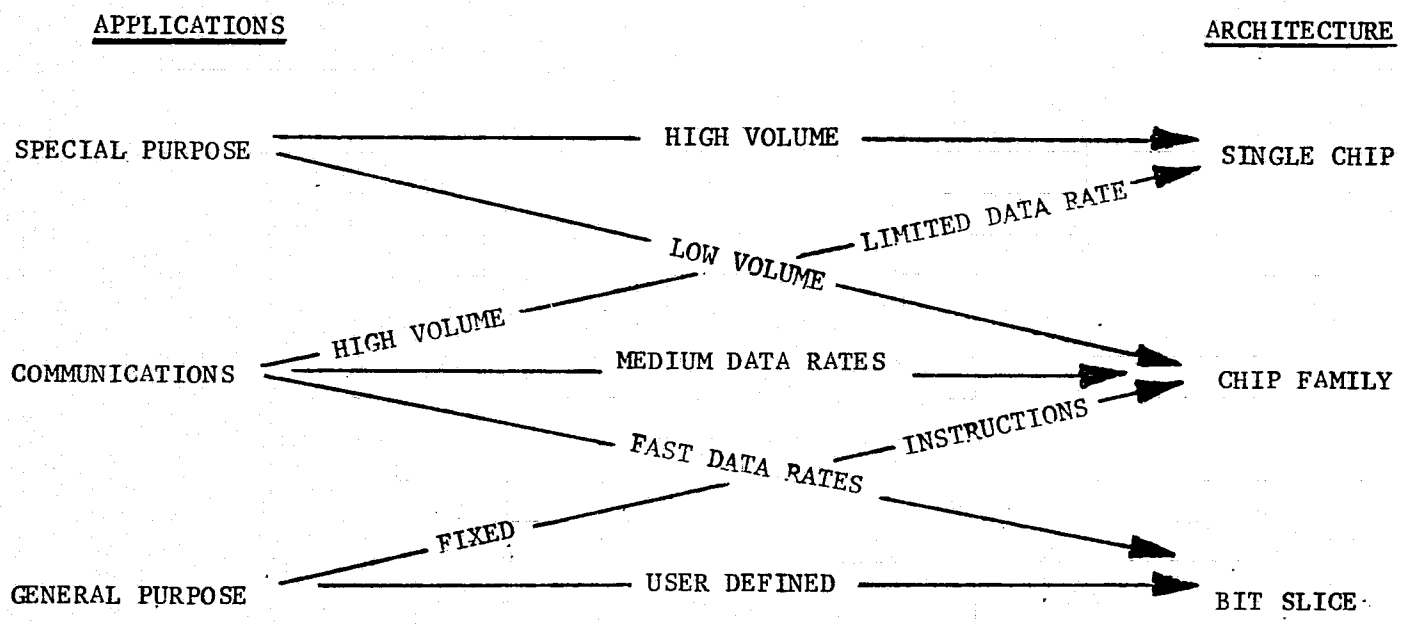


Figure 4-1 Microprocessor Architecture vs Application

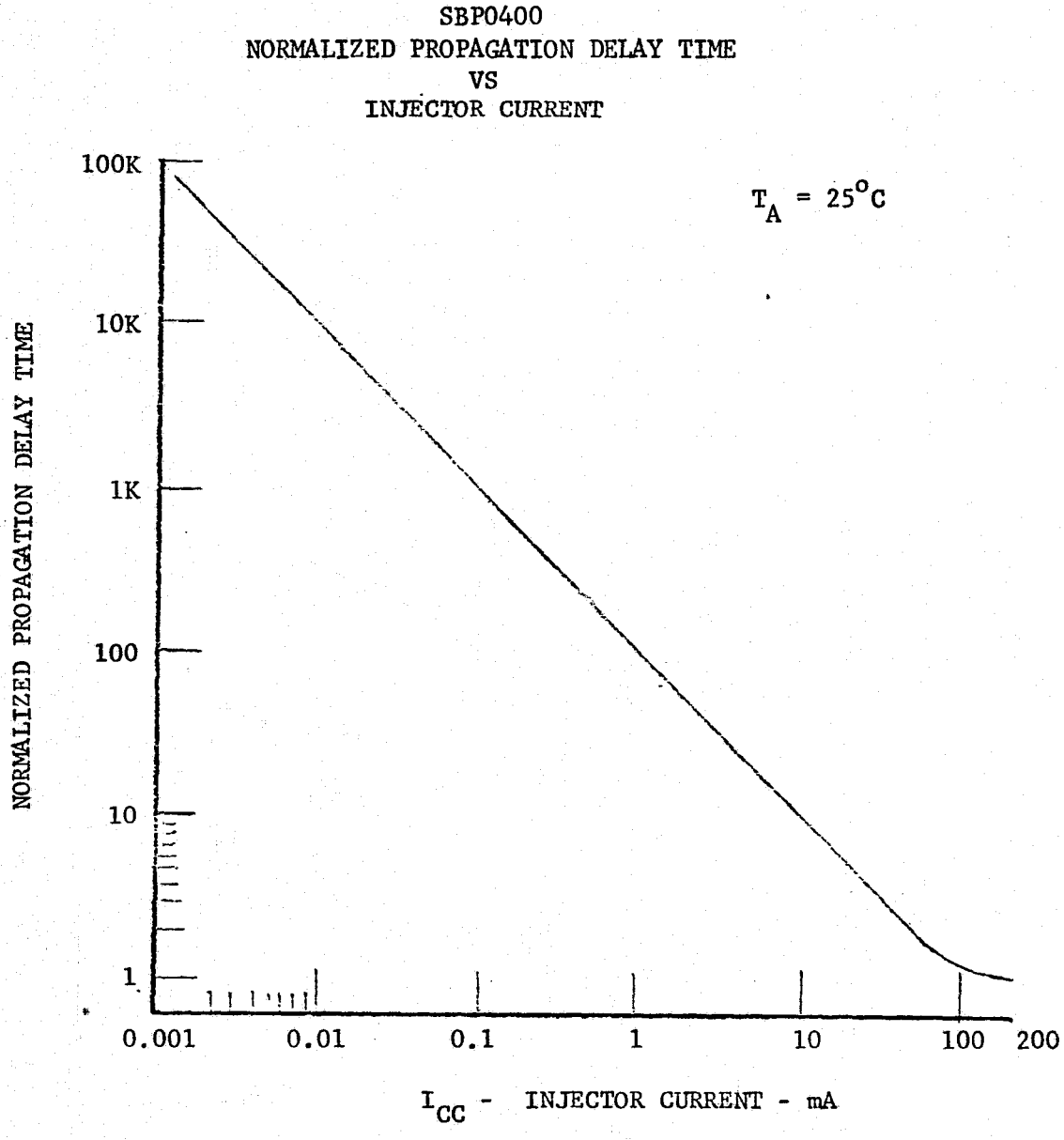


Figure 4-2 I^2L SBP0400 Characteristics

- High noise immunity;
- Completely static--its clock can be controlled to interface with very slow memories or I/O devices;
- And very important--design aids:
  - Assembler;
  - Simulator/debugger;
  - Editor;
  - Hardware Support Kit.

Other features of COSMAC are:

- 4-12V dc operating range (single voltage operation);
- 59 instructions (fixed instructions);
- Multilevel interrupts;
- RAM stack;
- I/O interface handles devices in polled interrupt drive and direct memory access modes;
- 64K bits of memory.

The following table summarizes the characteristics of the two candidate microprocessors.

Table 4-2 Candidate Microprocessors

Parameter	TI SBP0400	RCA COSMAC
Word Length	4 bit slice	8 bit
Technology	I^2L	CMOS
Cycle Time (μs)	1	3
Inst. Time Min. (μs)	1	6
Number Instructions	512	59
Power Supply (volts)	+ 4V	+ 5 to + 12
CPU Configuration	40 pin chip	28 pin 40 pin (2 chips)
Chip Family	RAM ROM, PROM	RAM ROM, PROM
Memory Capacity	64K	64K
Microprogrammed	Yes	No
Stack	RAM	RAM
Interrupts	Multilevel	Multilevel
Bit Slice	Yes	No
Support Components		
Software Support	No	Yes
Program Development Support	No	Yes

In summary, both units have the low power operation required for MMU. A realistic comparison of power consumed would require final configuration definition including number and kinds of registers, memories, input/output as well as operating speed and power up/down circuitry for the SBP0400. On the one hand, there is the SBP's bit-slice design and microprogramming capability, enabling the user to determine data length, register allocation, instruction set and I/O interfacing. This makes it possible to optimize the characteristics of the processor for a particular application. Not only does this reduce instruction execution times by more efficient operation, but allows the synthesis of instructions not available in the fixed instruction machine. However, the price for this instructional power and efficiency is the need for a greater degree of skill and the lack of design aids. On the other hand, COSMAC has an instruction set with many strong features and outstanding design and debugging aids. Good backup for program assemby, editing, simulation, and debugging is a very important consideration.

If more than 8 bits are needed there is also a 12-bit CMOS microprocessor recently available from Intersil, the IM6100. It has a very handy feature in that the processor recognizes the instruction set of Digital Equipment Corporation's PDP8/E minicomputer. The IM6100 has a fixed instruction set, as does COSMAC, with good software and hardware development backup. Many of the remarks concerning good backup vs microprogrammability are also appropriate to the IM6100.

None of the microprocessors are qualified to MIL-M-38510 and the SBP0400 is presently available only in samples (engineering evaluation units). All these microprocessors are aimed at the military/aerospace market with RCA (COSMAC) having the best record for CMOS qualification. This could boil down to a choice between performance and cost. A proper choice would have to wait until design requirements and goals are more specifically defined. See Table 4-3.

Conclusions:

- Microprocessors will be available to the MMU if complex functions or programmability are required. Low power units are available in CMOS and I^2L technologies. The CMOS units, the RCA COSMAC, and the Intersil IM6100 have good software and hardware backup by the manufacturer. The TI SBP0400 can be tailored to performance by microprogramming. The CMOS units are recommended for first consideration due to the savings in time and money that good backup would provide. The user-defined instruction set of the SBP0400, however, would provide the potential for high performance if it became necessary.

Table 4-3 Microprocessor Manufacturers

Advanced Micro Devices
901 Thompson Road
Sunnyvale, California 94086
(408) 732-2400

American Microsystems, Inc.
3800 Homestead Road
Santa Clara, California 95051
(408) 255-3651

Applied Computing Technology
17961 Sky Park Circle
Irvine, California 92707
(714) 557-9972

Burroughs
P. O. Box 517
Paoli, Pennsylvania 19301
(215) 648-2000

Computer Automation, Inc.
18651 VonKarman Avenue
Irvine, California 92664
(714) 833-8330

Comstar Corporation
7413 Washington
S. Minneapolis, Minnesota 55435
(612) 941-4454

Control Logic Incorporated
9 Tech Circle
Natick, Massachusetts 01760
(617) 655-1170

Data Architects, Incorporated
460 Totten Pond Road
Waltham, Massachusetts 02154
(617) 890-7730

Digital Equipment Corporation
One Iron Way
Marlborough, Massachusetts 01720
(617) 481-7400

Digital Laboratories
377 Putnam Avenue
Cambridge, Massachusetts 02139
(617) 876-6220

Dynamic Data Systems Corporation
533 Stevens Avenue
Solana Beach, California 92075
(714) 755-5161

Electronic Arrays
550 Middlefield Road
Mountain View, California 94043
(415) 964-4321

Fabri-Tek Incorporated
5901 South County Road 18
Minneapolis, Minnesota 55436
(612) 935-8811

Fairchild Semiconductor
464 Ellis Street
Mountain View, California 94042
(415) 962-5011

General Automation, Incorporated
1055 South East Street
Anaheim, California 92805
(714) 778-4800

General Instruments
600 West John Street
Hicksville, New York 11802
(516) 733-3097

Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051
(408) 246-7501

Intersil, Incorporated
10900 North Tantau Avenue
Cupertino, California 95014
(408) 257-5450

Microdata Corporation
17481 Red Hill Avenue
Irvine, California 92705
(714) 540-6730

Microsystems International Ltd.
P. O. Box 3529 Station C
Ottawa, Canada KIY, 4JI

Table 4-3 (Continued)

Monolithic Memories, Incorporated
1165 East Arques Avenue
Sunnyvale, California 94086
(408) 739-3535

MOSTEK
1215 W. Crosby Road
Carrollton, Texas 75006
(214) 242-0444

Motorola Semiconductor Products
5005 East McDowell
Phoenix, Arizona 85062
(602) 244-6228

National Semiconductor Incorporated
2900 Semiconductor
Santa Clara, California 95051
(408) 732-5000

Process Computer Systems (PCS)
5467 Hill 23 Drive
Flint, Michigan 48507
(313) 744-0225

Pro-Log Corporation
852 Airport Road
Monterey, California 93940
(408) 372-4593

Raytheon Semiconductor
350 Ellis Street
Mountain View, California
(415) 968-9211

RCA Solid-State Division
Route 202
Somerville, New Jersey 08876
(201) 722-3200

R2E Micro Computers
38 Garden Road
Wellesley Hills, Massachusetts 02181
(617) 235-3130

Rockwell Microelectronic Device Div.
3310 Miraloma Avenue
Anaheim, California 92803
(714) 632-3729

Scientific Micro Systems
520 Clyde Avenue
Mountain View, California 94043
(415) 964-5700

Signetics Corporation
811 E. Arques Avenue
Sunnyvale, California 94086
(408) 739-7700

Standard Logic, Incorporated
2215 South Standard Avenue
Santa Ana, California 92707
(714) 979-4770

Teledyne Systems Company
19601 Nordhoff Street
Northridge, California 91324
(213) 886-2111

Texas Instruments Incorporated
P. O. Box 1443
Houston, Texas 77001
(713) 494-5115

Three Phoenix Company
10632 North 21st Avenue
Phoenix, Arizona 85029
(602) 944-2223

Transitron
168 Albion Street
Wakefield, Massachusetts 01880
(617) 245-4500

Toshiba Transistor Works
1-Komukai
Toshiba-Cho
Kawasaki-Chi, Japan

Varitel Incorporated
8857 Olympic
Beverly Hills, California 90211
(213) 659-5914

Western Digital Corporation
3128 Red Hill
Newport Beach, California 95051
(714) 557-3550

Xerox Corporation
Dept. 15-02
701 S. Aviation Boulevard
El Segundo, California 90245
(213) 679-4511

- CMOS vs I^2L - For the near future, CMOS should be used for low power needs. It has wide availability and the selection is growing fast. For requirements more than a year or two ahead, I^2L might be far enough along to be a serious competitor to CMOS. I^2L has the best speed-power characteristics, smallest size and simplest fabrication process, implying high reliability as well as cost savings.

- Programmable Read Only Memory (PROM) - PROM should be used for cost savings and design convenience with fast programming turn-around times. Reprogrammable Read Only Memories are very handy for program development, but presently have questionable reliability in space radiation.

4.3 CMOS

4.3.1 CMOS Advantages

CMOS has some notable advantages, especially applicable to an MMU. CMOS has very low power dissipation, high noise immunity, relative insensitivity to temperature variations, and good switching speeds (see references 4.6.10 through 4.6.13). CMOS operates well from a single unregulated supply voltage. Power dissipation does go up with switching speed, but CMOS maintains an advantage over low power TTL up to the mega Hz region as shown in Figure 4-3. The industry has not been producing CMOS memories long, but there are a number available. Motorola has a 1024-bit ROM, MCM 14524, and Rockwell has a 4096-bit CMOS/SOS ROM. A significant recent development in CMOS memories is the appearance of PROMs (Programmable Read-Only Memories). PROMs should be much more economical than ROMs because of the mask cost savings, especially in low volume production memories.

The power savings with CMOS memories can be huge. Quiescent power dissipation levels of CMOS run two to three orders of magnitude less than other technologies with the exception of I^2L. A CMOS memory of 100K bits would typically have a quiescent power dissipation of about 1.1 μwatts at 5 volts (5 mw maximum).

CMOS uses N-channel and P-channel MOS on the same substrate with the N-channel device usually driving the P-channel device. This configuration allows only one transistor to be "on" in a quiescent logic state with a very low quiescent power dissipation of a few nanowatts per gate. The a-c power dissipation increases directly with frequency according to the formula $Pd(a\text{-}c) = CV^2_{DD}f$. In a sense, CMOS power dissipation is self-programmed. This is in contrast to the operation of integrated injection logic in which the speed and power are programmed by the amount of current injected. Although CMOS has an advantage over TTL up into the megahertz region, the big advantage of CMOS is standby power which is especially true for large memories.

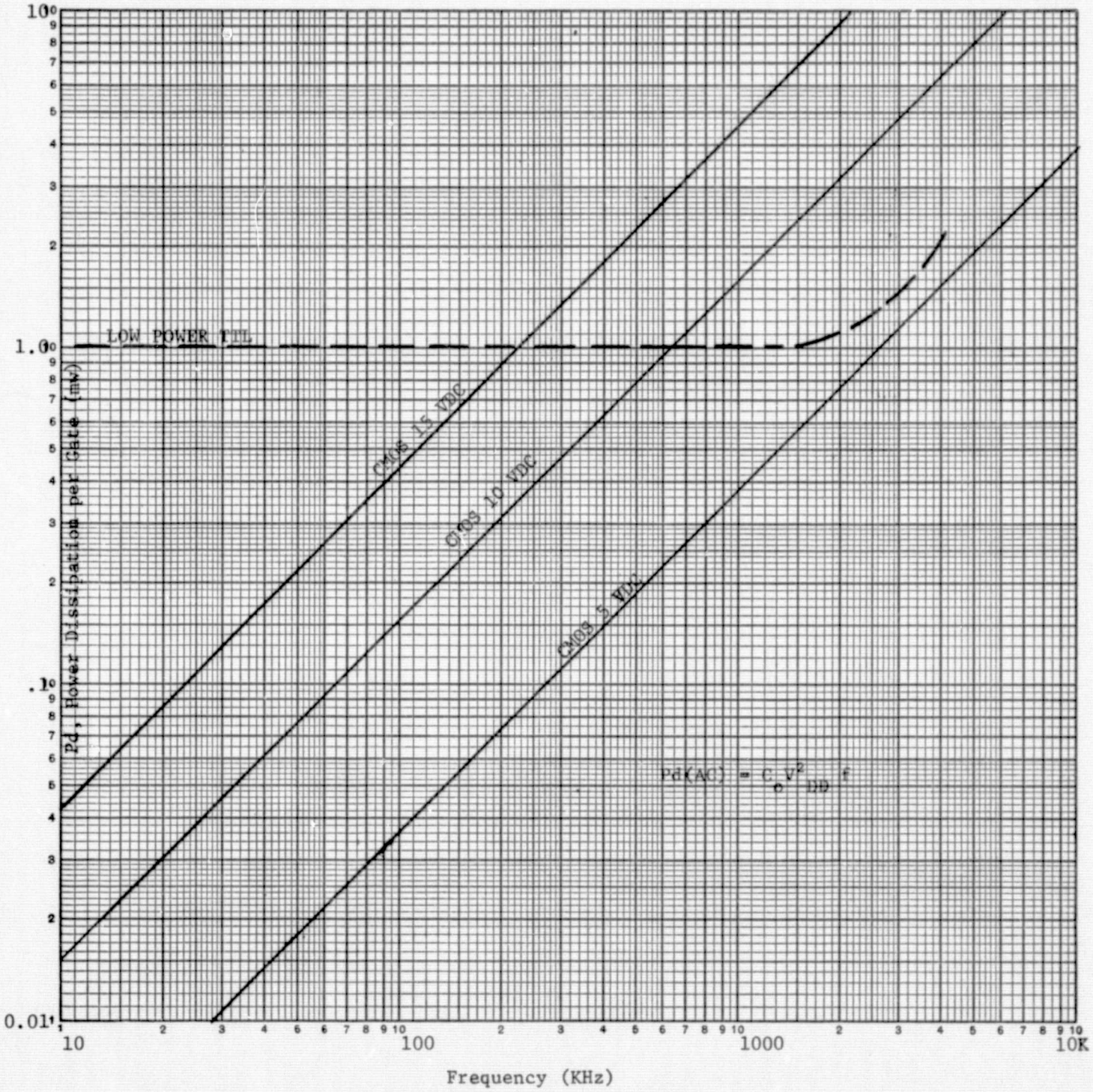


Figure 4-3 Typical Gate Power vs Speed, CMOS and TTL (low power)

4.3.2 High-Reliability Sources

As of June, 1975, RCA is the only company which has qualified CMOS parts to the high reliability specification MIL-M-38510. Several companies have indicated they intend to qkalify to that specification in the near future. National Semiconductor expects to have Hi Rel (MIL-M-38510) CMOS by August 1975. Motorola has plans for NASA Line Certification, also in August 1975. Line certification is one of the requirements for obtaining Class A qualification approval. TI's qualification is not scheduled before January 1976. CMOS has developed into a general purpose logic family with a large assortment of MSI and LSI parts. CMOS units now available include:

- 128-bit to 1,024-bit shift registers;
- Full adders;
- Counters of many types--binary, BCD, up/down and programmable; and
- Arithmetic Logic Units (ALUs) of 4 bits and 8 bits.

In the CMOS microprocessor area, there are:

- An 8-bit parallel processor by RCA that will ultimately use silicon-on-sapphire substrate to get microinstructions down to microsecond time and micropower operation, and an 8-bit microprocessor by Solid-State Scientific which is also using SOS/CMOS to obtain these speeds.

Available CMOS memory devices include:

- Read only memories, random access memories, and recently, programmable read only memories. By the end of 1975, read only memories of 1,024 to 8,192 bits will be available. With such minute quiescent power dissipations, the addition of a small battery can solve the volatile-memory problem.

4.3.3 Problems with CMOS

Besides the slow pace for CMOS qualification to the high-reliability specification of MIL-M-38510, there are some other problems with this technology.

- In the 4000 Series (originated by RCA and the most popular), there is a lack of uniformity in the device specifications. Speed and output drive capability can vary by a factor of 3 from circuit to circuit. However, this problem is largely overcome by the fact that the 4000 series has been around long enough to have its peculiarities discovered and many application notes published.

- CMOS buffers are available to drive TTL loads, but some must be current limited to avoid exceeding the rated dissipation.

- To obtain TTL compatibility on some CMOS units, external resistors are used from input to power supply. This can negate the typical CMOS low power operation.

- Propagation - delay can be misleading; it is usually measured at the point where the signal crosses fifty percent of the supply voltage. The actual switching point can range from 30% to 70% of the supply voltage.

- There is an electrostatic (burnout) handling problem with CMOS. The problem is exacerbated by dryness and synthetic clothing. Some CMOS user companies report very few failures with a minimum of handling procedures--perhaps only storing the units in conductive wrapping. HP medical laboratories report a very low failure rate (< 1%) with no special handling procedure for CMOS. Other companies advise not only conductive wrapping, but also grounding straps for tools and personnel, ionized-air blowers, and humidity control.

4.4 INTEGRATED INJECTION LOGIC (I^2L)

Integrated injection logic is a new bipolar process with CMOS dissipation and Schottky TTL speeds (recently announced by TI). TI uses a new process which will give propagation delays of 10 to 20 nanoseconds at 100 μA. The theoretical I^2L gate limit is 1 nanosecond at 1 μwatt.

"The advanced process, when applied to TI's microprocessor chip SBP0400 could result in microinstruction execution times about as fast as the Schottky T^2L processor slices that are now on the market." (Reference 4.6.2).

To get the low quiescent power that makes CMOS so good for memories, the injected current must be reduced. The additional circuitry for this would have to be considered. I^2L, however, does have the best speed-power product of any process (Table 4-4) with a theoretical limit of 0.001 picojoules.

Added to the speed and power advantages are compactness and process simplicity which imply low cost and high reliability as shown in Table 4-5.

The small area of I^2L comes from the pure digital, nonisolated technique. In the linear, isolated technique, space-consuming pn junctions are used to separate elements within the gate. This is not necessary in the nonisolated case, where commonality between the pnp injector and the npn inverter is used to good advantage as shown in Figure 4-4. In the nonisolated process, gates shrink to transistor size and with the low power required, thousands of gates can be made on a single chip.

To date there is not much to choose from in I^2L as most of the work has been on a custom basis. In 1976 I^2L standard circuits should start appearing in some volume. A significant recent development by Fairchild is an I^2L 4096-bit random-access memory. The device has nominal access times of 100 ns, making it more than twice as fast as today's N-MOS, 4-kilobit dynamic RAMS.

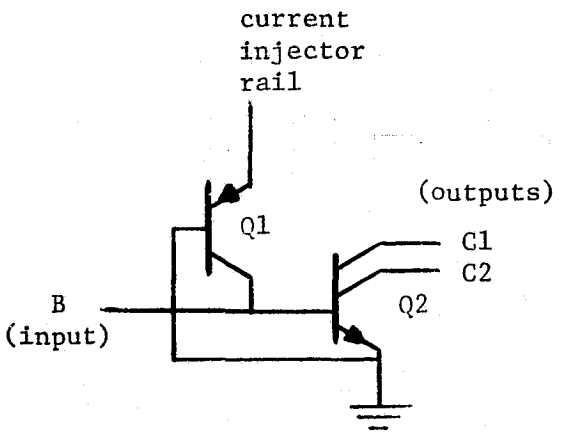
Table 4-4 Performances of Various Technologies

Type of Logic	t_P (ns)	P_D (mw)	Speed-Power Product (picojoules)
TTL	10	10	100
TTL(H)	5	20	100
TTL(L)	30	1	30
TTL(S)	3	20	60
TTL(LS)	10	2	20
ECL(10K)	2	30	60
ECL(D1)	0.7	43	30
PMOS	200	0.1	20
NMOS	100	0.1	10
CMOS	30*	1.0*	30*
SOS	15	0.05*	7.5*
*At 1 MHz			
I^2L(1975)	35	0.085	3.0
I^2L(1976)	20	0.05	1.0

Table 4-5 Size and Process Comparisons (All structures are 4-wide gates)

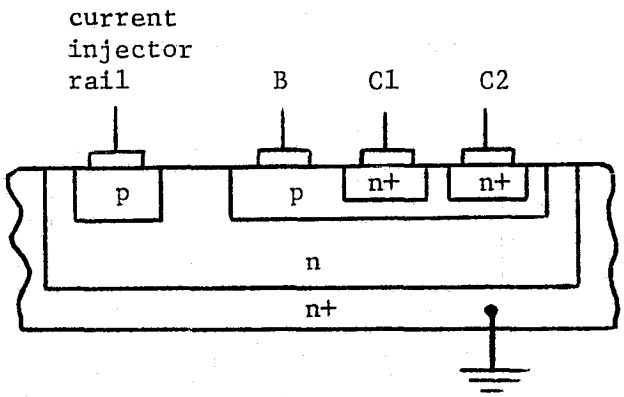
Technology	Gate Area ($mils^2$)	Number of Components	Mask Steps	Number of Diffusions
STD TTL MSI	52.8	3	7	4
CMOS	49.8	3	6	3
TTL LSI	19.9	3	7	4
PMOS	10.6	2	4	1
SG-NMOS	5.6	2	7	3
I^2L	4.8	1	4	2

Schematic



Vertical npn transistor Q_2 with multiple collectors C1 and C2 operates as inverter and lateral pnp transistor Q1 acts as current source.

Construction



- The n+ region acts as the structural base and as a ground plane common to all grounded emitters (eliminates ground metalization).
- The n region acts as grounded emitter of npn and grounded base of pnp transistors.
- The right-hand p region acts as connected base of npn and collector of pnp transistors.

Figure 4-4 I^2L Schematic and Construction

4.5 PROGRAMMABLE READ ONLY MEMORIES (PROMs)

Programmable refers to field programmable by the user instead of the manufacturer. There are two main divisions of PROMs: permanently programmable and *re*programmable. Permanently programmable PROMs use an irreversible process; an example is the fusible-link type. A reprogrammable type can be programmed many times such as the ultraviolet-erasable PROM. CMOS PROMs have only recently become available. They are very attractive for space use, especially for large memories built in small quantities. The huge power savings of CMOS memories, which are primarily in the stand-by low-power state, are now combined in PROMs with reasonable programming costs and design convenience.

First, consider the *permanently* programmable read only memory. There are the following:

1) Fusible Link Nichrome (NiCr), also called PROM. In this type the nichrome fuse is "blown" in the programming process to set the "1's" or "0's" into memory.

   These PROMs come as all "1's" or all "0's". The desired changes are made by supplying enough current through the links to cause separation of the metal in a manner similar to that of a conventional fuse. The programming of course is irreversible, or is meant to be. There has been concern for "growback" of the fusible link and a number of articles written on the subject. (See references 4.6.6 through 4.6.8.) This problem has led to considerable study and design changes.

   Signetics has changed the geometry of the link and with a closer control of programming conditions, claims that growback will not occur.

2) Polysilicon Fusible Link PROM - There is a fusible link PROM made with polysilicon by Intel that is supposed to be immune to growback (see reference 4.6.9).

3) Avalanche induced migration (AIM) is another permanent programming method. This is a diode-shorting technique used by Intersil to accomplish the programming. This method has good reliability data and should be a prime candidate for space work.

The *re*programmable read only memories are:

1) Program or write in electrically and erase with ultraviolet. This type is unsuitable for space since the erasure can also be done by x-rays. However, this type is very handy for breadboarding purposes.

2) Write in and erase electrically. Another reprogrammable ROM, which has a questionable space application due to space radiation environments. It is also very handy for breadboarding use.

The following is a survey of available PROMs and a brief description of the units.

PROMs (prices are for the commercial version)

Permanently Programmable

- Intersil (AIM technology)

  5603/5623 OC/TS (open collector/three state)
  - 1024 (256, X4)
  - Bipolar, 50 ns access time
  - $22/2days
  - 5604/5624 OC/TS
  - 2048-bit (512 x 4)
  - Bipolar, 50 ns access time
  - $45/2 days (unit price/delivery)

- Harris Semiconductor (fusible nichrome links)

  HPROM-8256
  - 256 bit (32 x 8)
  - Bipolar
  - 40 ns access time
  - Expendable - "wired-OR" outputs
  - $9/2 days

  HPROM-0512
  - 512 bit (64 x 8)
  - Bipolar
  - 55 ns access time
  - Expandable - "wired-OR" outputs
  - "AND" enable inputs
  - $18/3-4 weeks

  HPROM-2048
  - 2048 bit (512 x 4)
  - Bipolar
  - 50 ns access time
  - TS-2048, OC-2048A

- Monolithic Memories (fusible nichrome links and Schottky TTI)

  6305
  - 2048 bit (512 x 4)
  - $58/1 week

6340
- 4096 bit (512 x 8)
- $98/1 week, 5340 military version, $140

- Fairchild (fusible nichrome link)

  93416/93426 OC/TS
  - 1024 bit (256 x 4)
  - Bipolar, access time 45 ns
  - Wired-OR

- National Semiconductor

  DM 8574 Fusible Link
  - 1024 bit (256 x 4)
  - Bipolar
  - $17.50/shelf

- Intel

  8604 (polyfuse, polycrystalline silicon link)
  - 4096 bit (512 x 8)
  - Schottky bipolar, 100 ns access time
  - No growback or dissimilar metals problem (Intel's claim)

Reprogrammable

- Intel - Ultraviolet Light Erasable and Electrically Programmable

  8702 Silicon Gate MOS
  - 2048 bit (256 x 8)
  - Transparent quartz lid for ultraviolet light erasable
  - 3-state output (or tie) capability
  - 500 ns access time
  - Three state output (or tie) capability
  - $45/shelf

  5704 Silicon Gate MOS
  - 4096 bit (512 x 8)
  - 500 ns access time
  - Three-state output (or tie) capability
  - Quartz lid

- National Semiconductor - Ultraviolet Light Erasable, Electrically Programmable (Programmed on MM5203 Programmer with 50V pulse)

  MM5202A
  - 2048 bit (256 x 8)
  - MOS P-channel, 1 μs access time
  - Quartz lid
  - Common data busing (tri-state output)

MM4203/MM5203
- 2048 bit (256 x 8 or 512 x 4)
- Same as above, MM4203 greater temperature range

MM5204
- 4096 bit (512 x 8)
- 750 ns access time
- Tri-state output, chip select input
- Power saver control (5:1 decrease in power when memory not accessed)

- National Cash Register, Electrically Erasable and Electrically Programmable

1105 MNOS P-Channel
- 1024 bit (256 x 4)
- 2 μs access time
- Electrically erasable by row
- Unpowered nonvolatile data storage - 10 years
- 40.25/shelf

4.6 REFERENCES AND BIBLIOGRAPHY

4.6.1 *Designing with Microprocessors*, Texas Instruments (a course).

4.6.2 *Electronics*, June 26, 1975, pg 25.

4.6.3 Horton, R. L., Englade, J., and McGee, G.: *I^2L Takes Bipolar Integration a Significant Step Forward*, Electronics, February 6, 1975.

4.6.4 *What's New in Solid State*, RCA Issue 3/75.

4.6.5 RCA Microprocessor Products (COMSAC) 2M1122A, B, C, D, E, 3/75.

4.6.6 Barnes, D. E., and Thomas, J. E.: *Reliability Assessment of a Semiconductor Memory by Design Analysis*, Hughes Aircraft.

4.6.7 Franklin, P. G., and Burgus, D. L.: *Reliability Aspects of Nichrome Fusible Link PROMs*, Monolithic Memories, Inc.

4.6.8 Eisenberg, P. H., and Nolder, R.: *Nichrome Resistors in Programmable Read Only Memory Integrated Circuits*, Litton G/CSD.

4.6.9 Parker, G., Carnet, J. C., and Pinter, W.: *Reliability Considerations in the Design and Fabrication of Polysilicon Fusible Link PROMs*, Intel Corporation.

4.6.10 Torrero, E. A.: *Focus on CMOS*, Electronic Design 6, March 15, 1974.

4.6.11 *CMOS Electronics*, 15 May 1975.

4.6.12 Dinzl, R. A.: MMC Memorandum PE-74-23, 14 June 1974.

4.6.13 *McMOS Handbook*, Motorola, First Edition, 1974.

4.6.14 *The Microprocessor Handbook*, Bibliography - pages 119 - 123, Texas Instruments, Dallas, Texas.