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FINAL REPORT

DEMONSTRATION OF THE FEASIBILITY OF AUTOMATED SILICON SOLAR CELL FABRICATION

By

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16. Abstract

Final Technical Report under Contract NAS3-18566 demonstrating the feasibility of automated silicon solar cell fabrication. An analysis of estimated costs indicate that for an annual output of 4,747,000 hexagonal cells (38 mm. on a side) a total factory cost of $0.866 per cell could be achieved. For cells with 14% efficiency at AMO intensity (1353 watts per square meter), this annual production rate is equivalent to 3,373 kilowatts and a manufacturing cost of $1.22 per watt of electrical output. A laboratory model of such a facility was operated to produce a series of demonstration runs, producing hexagonal cells, 2 x 2 cm cells and 2 x 4 cm cells.

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ABSTRACT

The process steps and design requirements for an automated solar cell production facility were determined, utilizing a baseline sequence which excluded high energy, limited batch size operations. Processes were selected which could be readily automated and were compatible with continuous flow production. Based on these processes a conceptual automated solar cell production facility was designed for producing hexagonal cells, 38 mm. on a side. An analysis of estimated costs indicated that for an annual output of 4,747,000 cells, a total factory cost of $0.866 per cell could be achieved. For cells having a 14% efficiency at AM0 intensity (1353 W/m^2), this annual production rate is equivalent to 3,373 kW, with a manufacturing cost of $1.22 per watt of electrical output. A laboratory model of such a facility was designed, constructed, and operated to produce a series of demonstration runs, fabricating hexagonal cells, 2 x 2 cm cells, and 2 x 4 cm cells.

I. SUMMARY

This program was instigated to demonstrate the feasibility of automating a major portion of solar cell processing and fabrication. Studies were made to establish the process steps and design requirements of an automated facility. Key process steps were identified and a laboratory model to demonstrate solar cell automated production was conceived and designed in detail. This model was then assembled and operated to produce a series of demonstration runs.

The baseline process established utilized screen printed aluminum to produce a P+ back surface field, and screen printed front and back contacts. The AR coating was spun on, thus avoiding the use of any high vacuum processing in the cell production.

A portion of the program was devoted to various processing options and selecting those processes which could be integrated into a pilot line capable of processing the demonstration runs and which were capable of being readily automated. From the processes selected and the process sequence chosen, a conceptual automated solar cell production facility was established. Estimates were made of the capacity, yields, operating costs, and investments necessary for such a facility. These calculations indicated that a capital investment of $3,086,000 would be required to set up an automated facility capable of producing 4,747,000 cells annually having a manufacturing cost of $0.866 per cell, such cells being hexagonal in shape with 38 mm. sides. This annual production rate is equivalent to 3,373 kW and a manufacturing cost of $1.22 per watt for cells having an efficiency of 14% at AMO intensity (1353 kW/m^2)

A total of forty-one 100-wafer lots were processed in the demonstration runs made to show the feasibility of the laboratory model. During these operations it was established that additional technological development should

be devoted to improving the effectiveness of the printed and alloyed back field layer, to improve the adhesion of the printed-on contacts, and to improve the efficiency of the cells produced. The hexagonal cells produced had an average efficiency of 10.7%, with an average open circuit voltage of 583 millivolts, and an average short circuit current of 567 milliamperes.

II. INTRODUCTION

A. BACKGROUND

Arrays of silicon solar cells have been used to produce electrical energy for some time. Such systems are particularly well suited for situations requiring long life and high reliability, and in locations where the costs and availability of fuel supplies for other energy sources are prohibitive. Spacecraft, with the conditions imposed by the space environment, are a logical area for the application of solar cells.

Generally, however, the manufacturing techniques and practices used in the production of today's space-type solar cells results in their being expensive. Processing is characterized by many relatively complex steps, limited batch sizes, and a considerable number of hand operations. Major reductions in the cost of solar cells should result if mechanized or automated processing could be utilized with the accompanying reduction in hand labor. Also, if continuous flow operations could be maintained, there should be marked improvements in product uniformity.

B. PROGRAM OBJECTIVES

This program was instigated to demonstrate the feasibility of automating a major portion of solar cell processing, and concentrated on the processing sequence extending from starting silicon wafer to completed space-quality cells. The program required not only a demonstration of the feasibility of automating key fabrication processes, but also the integration of these process steps into a functioning pilot production line having a potentially high production rate, reduced energy consumption, and lower operating costs.

This effort also was intended to pinpoint those processes where marked cost reductions could be realized, and where further technological developments would result in additional cost reductions.

C. PROGRAM ORGANIZATION

The technical effort of this program was organized and separated into the following listed tasks:

Task I-A — A study effort to determine the process steps and design requirements of an automated solar cell production facility.

Task I-B — Identification of key process steps and the conceptual design of a laboratory model to demonstrate the feasibility of automating silicon solar cell fabrication processes.

Task II — Develop a detailed design of a laboratory model to demonstrate those functions most critical to the question of the feasibility of automating solar cell fabrications processes, such model to be based upon the conceptual design of Task I-B.

Task III — Construct, assemble, and operate the laboratory model; analyze the operation of the model; ascertain process cost reduction areas and recommend needed technological developments.

III. PROCESS EVALUATION AND SELECTION

A. BASELINE PROCESS

To demonstrate the feasibility of automated silicon solar cell fabrication it was decided to utilize the Spectrolab low cost solar power facility and processes as a point of departure. This facility had been established using techniques and processes selected as being compatible with eventual mechanization.

A major innovation in this facility was the use of screen printed thick film contacts to replace the relatively costly vacuum deposited contacts. Additional cost advantages were obtained by the use of larger silicon wafers (51 mm diameter) cut directly from the single crystal ingot.

Since this program was directed towards producing space-type solar cells rather than terrestrial-type, the standard process was also modified to:

a) Use high resistivity silicon (7-13 ohm-cm or higher).
b) Reduce the diffusion temperature to produce a shallow junction, as in our high-efficiency "Helios" space cells.
c) Incorporate a back-surface field by including a simultaneous P+ diffusion.
d) Re-design the contact pattern to assure optimization for higher diffused layer sheet resistance.
e) Maximize the possible packing factor by adding a shaping operation to produce square, rectangular, or hexagonal cells.

It was also proposed to evaluate and identify alternative processes for junction formation and AR coating which would be amenable to automation. A generalized flow diagram of the baseline process sequence, based on these considerations, is given in Figure III-1.

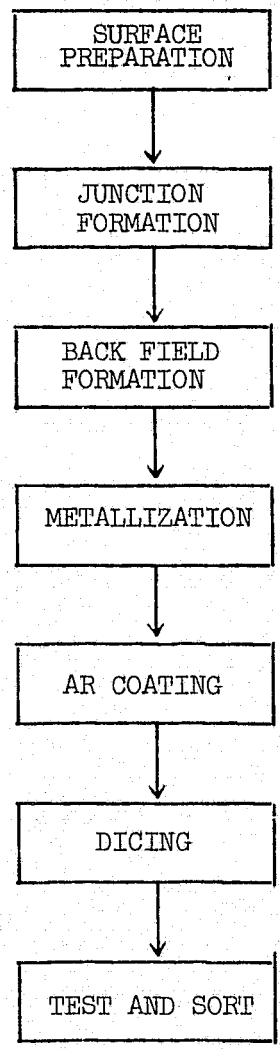


Figure III-1

BASELINE PROCESS SEQUENCE

B. PROCESS STUDIES AND SELECTION

1. Surface Preparation

Sodium hydroxide solutions had been used for some time for wafer etching in the production of low cost solar cells, and offered several advantages as compared to acid etching. Sodium hydroxide etching is a milder process and more easily controlled than acid etching. Also, the silicon surface resulting from hydroxide etching is texturized and exhibits lower reflectance. The adhesion of metallized contacts to such a surface is somewhat greater, and the AR coating requirements are less critical.

This process was investigated using as-cut silicon wafers and sodium hydroxide/water solutions containing 3%, 10%, and 30% NaOH by weight. It was found that:

a. The variation of etch rate with temperature corresponded to an activation energy of 0.56 eV, as found in the literature.

b. The etch rate at a given temperature is a direct function of the square root of the hydroxyl ion concentration.

c. Adding a detergent to the etch reduces the etch rate, to a greater extent at lower NaOH concentrations.

d. The etch rate is only slightly increased by ultrasonic agitation.

e. For equal amounts of material removed, the 30% solutions of NaOH gave substantially more uniform etching than the lower concentrations.

f. As the NaOH concentration is lowered, smaller, deeper, and better defined crystallographic etch pits are obtained, an effect that appears to be independent of etch temperature.

g. The depth of mechanical damage resulting from the sawing process, as determined by microscopic examination of samples etched to various depths and by noting the etch rate as a function of depth, appears to be about 15 micrometers.

Therefore the surface preparation process was set up to utilize a two step etching process. Wafers are first etched in a hot 30% NaOH solution to remove 15-25 micrometers of silicon, thus removing most of the mechanical saw damage. An additional 15-25 micrometers are then removed in a hot 1% NaOH solution to produce a texturized surface.

2. Junction Formation

Junction formation by diffusion from spin-on dopant sources was evaluated as a possible alternative to tube furnace diffusion using phosphine. The simultaneous diffusion of both boron, to produce a P+ back field region, and phosphorous or arsenic, to form the front surface junction (giving a sheet resistance of 20-25 ohms/square), held obvious attractions for process simplification. These studies were unsuccessful in establishing a simultaneous diffusion process using spin-on dopants. Therefore, since sequential operations were necessary for front junction formation and back field generation, the phosphine diffusion process was selected as the process to be used in the demonstration.

Inherent to the phosphine diffusion process is the formation of a low resistivity, heavily doped N-type layer on all surfaces of the wafer. This layer must be removed from the reverse side of the wafer where the P+ back field region is to be located and where any back metallization is to be applied. It was therefore necessary to devise and construct a back etching facility to remove the N+ layer on the reverse side of the wafer. This back etch process exposes the starting wafer material on the back of the wafer without affecting the N+ front surface by utilizing a water spray "curtain" to isolate the front from the back during the etching step.

3. Back Field Formation

It was found that the P+ back field region could be formed on the back etched wafer by screen printing a layer of aluminum paste and a subsequent alloy firing. It was necessary that this process follow the N+ diffusion, since the aluminum paste, or possibly some of its constituents adversely affected the N+ diffusion. The aluminum paste used required an alloying temperature of 850°C for a period of at least fifteen minutes. Thus there was a resulting increase in the depth of the N+ layer on the front of the wafer during the alloy step.

It was also found that the aluminum paste used led to the formation of small aluminum balls and lumps on the back of the wafer during alloying. Sometimes these were quite firmly attached to the silicon. This was objectionable since it caused problems in subsequent screen printing operations and in mounting finished cells. Prefiring the paste 630°C prevented these irregularities, but tended to decrease the effectiveness of the back field layer. It was anticipated that firing in the aluminum paste layer could set up thermal stresses which might cause troublesome warpage of the wafers. However, except in a few instances, the 12 mil thick wafers used did not give this problem when printed with an aluminum paste layer approximately one mil thick.

4. Metallization

Contacts to the cells have been made using metal pastes, which were screen printed onto the wafers in appropriate patterns, and then fired onto the wurface. These contacts appear to be satisfactory. However, the sequence of applying first the front, and then the back contacts seems to minimize possible damage to the silicon tetrahedrons on the texturized front surface. The screened-on front contacts appear to protect the front of the wafer from possible microfractures and damage during the printing of the back contacts.

Therefore the contact metallization process consists of sequentially printing on the front contact, drying it, printing on the back contact, drying it, and then firing both contacts in a belt furnace simultaneously. Attempts to cofire the silver back contact and the aluminum layer were unsuccessful.

After the contacts have been fired, a dilute hydrofluoric acid cleaning step is required to optimize cell characteristics and to improve the electrical behavior. This cleaning must be done with considerable care, since insufficient cleaning will not optimize the electrical behavior of the cell, and excessive treatment will adversely affect the adhesion of the metallization.

5. AR Coating

In order to satisfy the requirements for readily automated processing, a different method for applying antireflective coatings was investigated. The most common method for coating solar cells with antireflective layers is to evaporate a layer of silicon monoxide or tantalum pentoxide onto the front surface of the cells to a carefully controlled thickness. A process that did not require high vacuum equipment, small batch processing, and critical control was therefore needed.

It was found that a coating material manufactured by the Emulsitone Company was attractive for service as an AR coating. This material consisted of a mixture of silicon and titanium organometallic compounds in an alcohol based vehicle. The manufacturer specified that this coating had an index of refraction of 1.96. The liquid could be spun on using standard spin-on equipment and then baked, a process that could be easily automated.

Since the cells had texturized surfaces, the requirements for the AR coating were somewhat less critical. Tests also indicated that once the cell was covered by a layer of silicone resin and topped by a layer of glass, the spun-on AR coating gave nearly as great an enhancement of short circuit current as vacuum applied AR coatings.

6. Dicing

In order to improve the packing factor when solar cells are used in modules and arrays a shaping operation was required to produce square, rectangular, or hexagonal cells from the round wafers. A process was therefore devised utilizing a high speed dicing saw to score wafers on the reverse side, through the fired-on aluminum layer, in a pattern matching the metallization and the desired cell configuration. The final cell could then be achieved by breaking away the unwanted portions of the wafer. A rotating vacuum table was designed and built to hold the wafers in place during the scoring operation and to enable indexing.

Since a commercial dicing saw was not readily available, a K. O. Lee grinder was fitted with a high speed air motor to drive the diamond dicing saw. Recirculating water was used as the coolant, since an attempt to use gas as a coolant was unsuccessful.

It was found that the 0.5" flat on the wafers was not capable of completely accurate registration at the time of printing the contact metallization. Since the wafers were scored in a face-down position, it was necessary to use transparent plastic templates for this operation. The wafers were placed on the templates so that the metallization was accurately registered on a matrix of guidelines and taped into place. The template was then placed on the vacuum table against stops and the cutting was then done. While this was a relatively slow manual operation, it was considered to prove the validity of the step, which would be easily automated in actual production.

Several advantages are realized by scoring the wafers from the back side and then breaking away the unwanted portions. Since the cut does not extend all the way through the wafer, the P - N junction does not receive any mechanical damage from the saw. This eliminates the need for edge etching the finished cell. Aluminum that may be picked up by the saw blade from the back field layer cannot get to the junction. The intersection between the junction and the edge of the cell is essentially at a freshly cleaved surface.

IV. DESIGN CONCEPTS

A. AUTOMATED SOLAR CELL PRODUCTION FACILITY

Based upon the process studies and selections made in the earlier portion of the program, a conceptual design for an automated solar cell production facility was established. This facility was designed around the process sequence shown in block diagram form in Figure IV-1. The detailed design, expanded to indicate both the final automated method, as well as the method to be used in the demonstration laboratory model, is given in Table IV-1.

A suggested factory organization, showing labor, capital, and space requirements is given in Table IV-2. The estimated capital costs for this conceptual factory are presented in Table IV-3. Tables IV-4, IV-5, and IV-6 show elements of the manufacturing costs and are combined in Table IV-7. This analysis estimates a manufacturing cost of $0.866 per cell, or $1.22 per watt, based on a factory processing 21,973 kilograms of silicon crystal into 4,747,000 hexagonal solar cells, having 38 mm. sides, per year on a three shift, 49 week basis. If the nominal cell produced has an efficiency of 14%, the cells manufactured would have a power capability of 3,373 kilowatts at AMO, assuming an input of 1,353 watts per square meter.

The proposed processing starts with 76 mm. diameter round wafers cut from P-type Czochralski crystals. The successful development of ribbon crystals for a starting material would result in the substitution of finite length ribbon strips for sawed round wafers. The round wafers would be etched to remove saw damage, a step that would not be necessary for the ribbon material. Etching to develop a texturized tetrahedral surface would then be done. Some modification of the etching facility would be required for processing silicon ribbon, and the texturizing step would not be used if the strips did not have (100) surfaces.

Figure IV-1

PRODUCTION PROCESS SEQUENCE

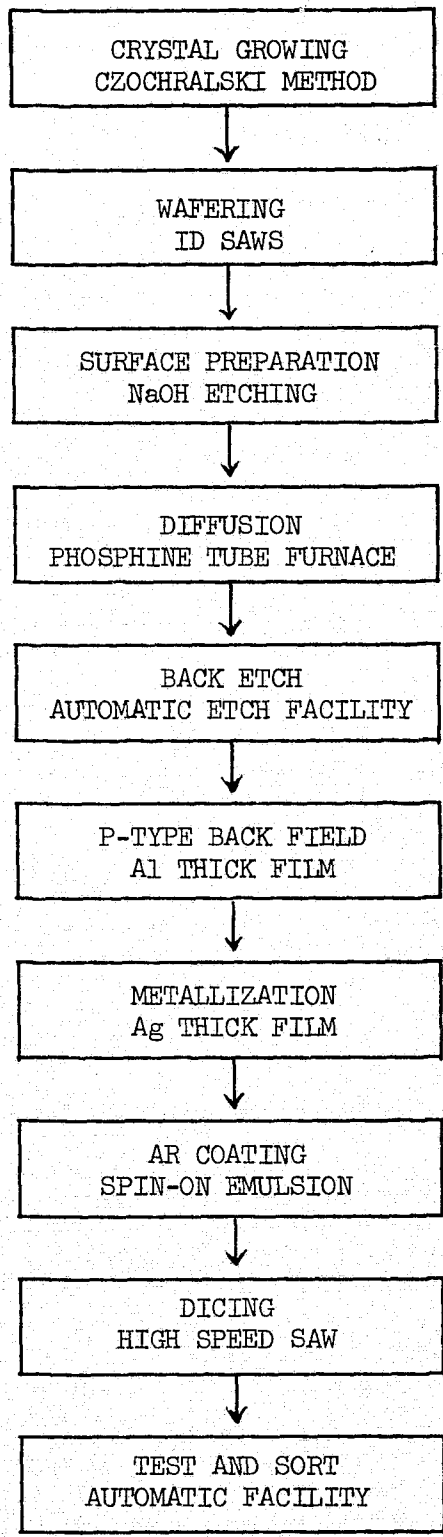


Table IV-1

PRODUCTION PROCESS SEQUENCE DETAIL

Process Step	Automated Production Method	Demonstration Model Method
Crystal Growing	Czochralski Furnace	Czochralski Furnace
Mounting	Hot Plate	
Sawing	ID Saw	
Basket Load	Mechanical	Hand
Clean	Basket Dip	Basket Dip
Basket Transfer	Mechanical	Hand
Saw Damage Removal	Basket Dip 30% Hot NaOH	Basket Dip 30% Hot NaOH
Basket Transfer	Mechanical	Hand
Texture Etch	Basket Dip 1% Hot NaOH	Basket Dip 1% Hot NaOH
Basket Transfer	Mechanical	Hand
Rinse	Basket Dip	Basket Dip
Dry	Centrifuge	Centrifuge
Unload	Hand Dump	Hand Dump
Quartz Boat Load	Mechanical	Hand
N+ Diffusion	Tube Furnace (Phosphine)	Tube Furnace (Phosphine)
Boat Unload	Hand Dump	Hand Dump
Back Etch	Water-Cooled Mechanically Loaded Fixture	Water-Cooled Hand Loaded Fixture
Dry	Centrifuge	Centrifuge

Table IV-1 (cont'd)

PRODUCTION PROCESS SEQUENCE DETAIL

Process Step	Automated Production Method	Demonstration Model Method
Print Aluminum Back Field Source	Automatic Screen Printer	Manual Screen Printer
Dry Paste	Belt Furnace	Electric Oven
Quartz Boat Load	Mechanical	Hand
Alloy and Diffuse	Tube Furnace	Tube Furnace
Unload Boat	Hand Dump	Hand Dump
Print Front Contact	Automatic Screen Printer	Manual Screen Printer
Dry Paste	Belt Furnace	Electric Oven
Print Back Contact	Automatic Screen Printer	Manual Screen Printer
Dry Paste	Belt Furnace	Electric Oven
Fire Contacts	Belt Furnace	Belt Furnace
HF Clean and Rinse	Water-Cooled Mechanized Fixture	Water-Cooled Hand Load Fixture
Dry	Centrifuge	Centrifuge
AR Coat	Automatic Spinner	Hand Loaded Spinner
Bake AR Coating	Belt Furnace	Electric Oven
Dice	Automatic Diamond Blade High Speed Saw	Manual High Speed Saw
Test and Sort	Solar Simulator with Automatic Cell Handler	Solar Simulator Hand Load and Test
Interprocess Transfer	Mechanical	Hand Load

Table IV-2

Conceptual Factory Organization

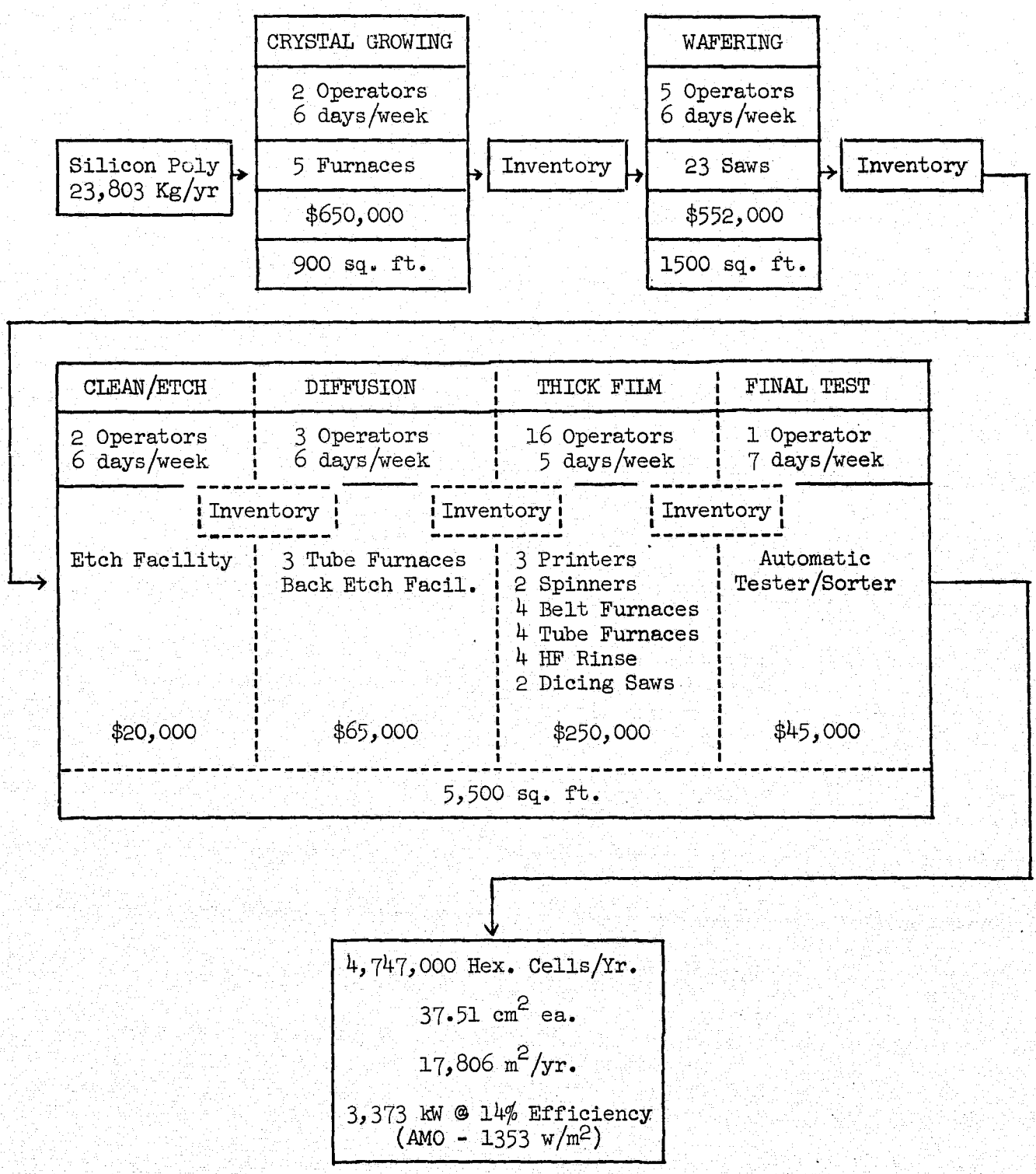


Table IV-4

CAPITAL EQUIPMENT SUMMARY

EQUIPMENT:	Crystal Growing Area	$ 650,000
	Wafering	552,000
	Cleaning and Etching	20,000
	Diffusion	65,000
	Thick Film and Dicing	250,000
	Final Test	45,000
	Miscellaneous	58,000
		$1,640,000
	Equipment Installation	240,000
		$1,880,000
SPACE:	Crystal Growing 900 ft^2 @ $40	$ 36,000
	Wafering 1500 ft^2 @ $40	60,000
	Cell Fabrication 5500 ft^2 @ $40	220,000
	Office and Laboratory 2000 ft^2 @ $30	60,000
	Storage 4000 ft^2 @ $20	80,000
		$ 456,000
TOTAL FACILITY COST:		$2,336,000
WORKING CAPITAL:		750,000
TOTAL CAPITAL INVESTMENT		$3,086,000

Table IV-5

LABOR REQUIREMENTS

CRYSTAL GROWING:

2 Opr x 24 hr. x 6 days x 49 wks.	14,112 hrs.

WAFERING:

5 Opr x 24 hr. x 6 days x 49 wks.	35,280 hrs.

CELL FABRICATION:

5 Opr x 24 hr. x 6 days x 49 wks. = 35,280	
16 Opr x 24 hr. x 5 days x 49 wks. = 94,080	
1 Opr x 24 hr. x 7 days x 49 wks. = 8,232	137,592 hrs.

TOTAL FACTORY LABOR HOURS:

@ $3.00 per hour	$560,952

UNIT LABOR COST:

$560,952 ÷ 4,747,000 Cells = $0.118/Cell

Table IV-6

MATERIALS AND SUPPLIES

CRYSTAL GROWING:	
Silicon (23,803 Kg @ $37.00)	$ 880,711
Power	41,250
Argon	26,500
Crucibles (@ $50.00)	137,500
Spare Parts	100,000
	$1,185,961
WAFERING:	
Saw Blades (@ $80.00 - 2000 waf/blade)	$ 237,420
Chemicals	10,000
	$ 247,420
CELL FABRICATION:	
Pastes and Chemicals	$ 471,000
Miscellaneous Materials	100,000
TOTAL MATERIAL COSTS	$2,004,381

UNIT MATERIAL COST:

$2,004,381 ÷ 4,747,000 Cells = $0.422/Cell

Table IV-7

MANUFACTURING COST SUMMARY

	Annual Total	Per Cell
Labor	$ 560,952	$0.118
Overhead @ 150%	841,428	0.177
Material	2,004,381	0.422
Equipment Depreciation (5 years)	376,000	0.083
Building Depreciation (25 years)	18,240	
Interest on Capital @ 10%	308,600	0.065
TOTAL FACTORY COST	$4,109,601	$0.866

The silicon substrates would then be diffused in a batch type gaseous phosphorous diffusion facility capable of handling either the 76 mm. wafers or ribbon strips up to three inches wide and two feet long. After back etching the material would be processed through the thick film facility to apply the aluminum back field and the solderable front and back contacts. This facility would use screen printers and belt furnaces capable of processing either wafers or silicon ribbon strips.

The AR coating would be applied by spinning, in the case of round wafers. Spraying or flood coating would be utilized for strip materials. Finally the material would be shaped into hexagonal, square, or rectangular cells to provide an optimum packing factor. Testing and sorting into categories would also be automated to minimize hand labor in these operations.

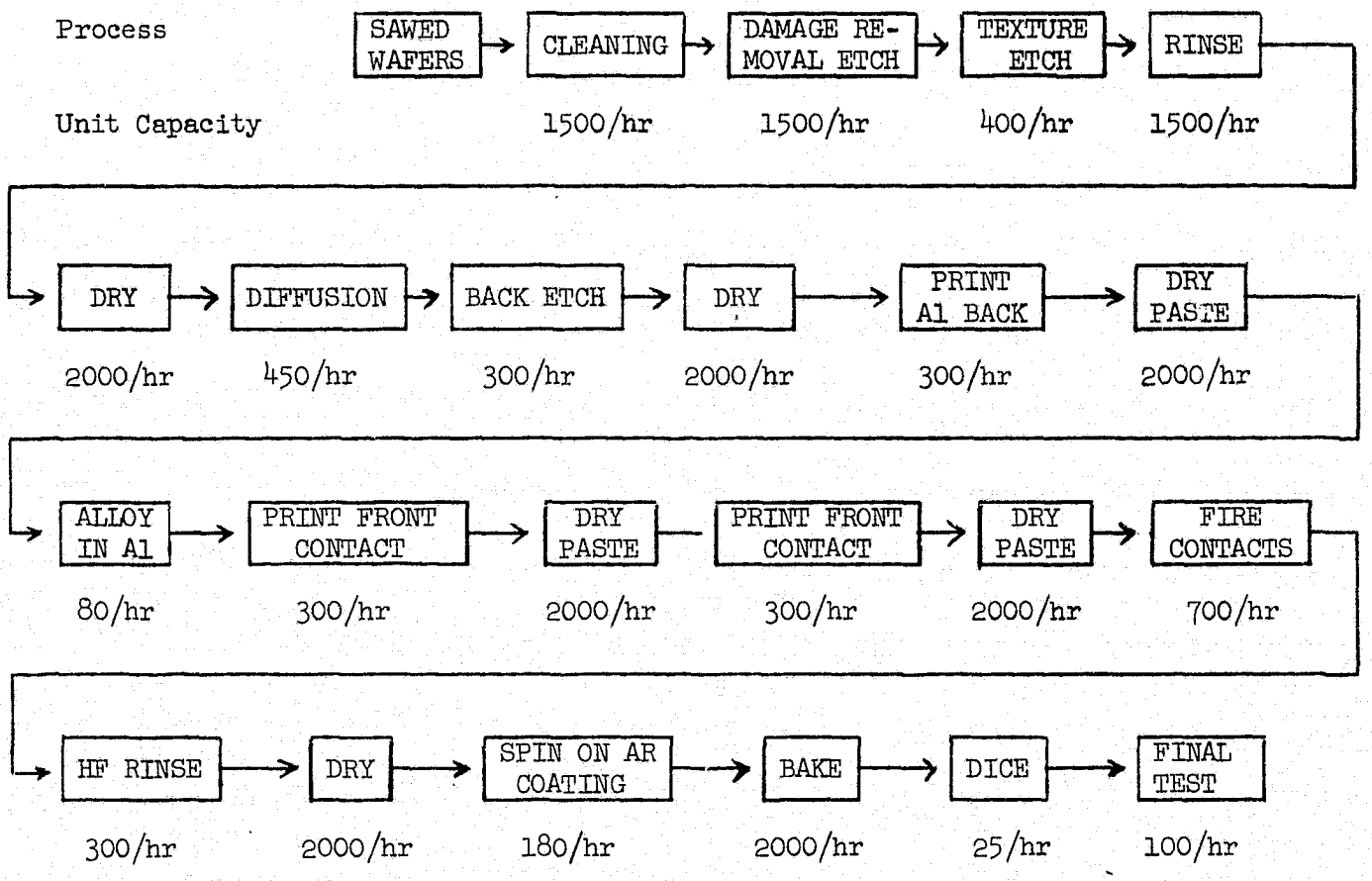
B. LABORATORY DEMONSTRATION MODEL

In order to demonstrate the feasibility of these concepts a laboratory demonstration model was designed. This model shared the facilities, personnel, and equipment of the Spectrolab low cost solar cell production facility. This approach allowed the use of actual production equipment without requiring extra time, effort, and capital expenditures that would be needed to establish an entirely new and separate facility.

The process steps and components that were used in the demonstration model, along with production capabilities, are shown in Figure IV-2. The production capabilities envisioned during the design of the laboratory model were generally correct for most of the process steps. However, the manual operation of certain steps, while satisfactory in demonstrating the feasibility of a process for an automated facility, were sufficiently low to limit the size and scope of the demonstration runs. In particular the alloy step, used to establish the back field P+ layer, and the dicing step, used to shape the round wafers into the final cell configuration were severely limiting. The following paragraphs discuss each step in turn and compare the laboratory model process with a properly automated facility.

Figure IV-2

BLOCK DIAGRAM - LABORATORY MODEL



While the conceptual design of the automated solar cell production facility was based on utilizing 76 mm. diameter wafers, the most common wafer processed in the Spectrolab low cost solar cell line was 52.5 $\pm$ 1.5 mm. in diameter. Therefore it was decided to use the smaller size wafer for the demonstration. Fixtures and equipment for handling the larger wafers are readily available, and much of the capital equipment used for this program can handle either size. Wafers used in the demonstration were made with a half-inch flat on the edge of the wafer in the < 110 > direction to allow repeatable contact pattern registrations, to optimize the score-and-break shaping operation, and to identify the wafers from the low resistivity wafers of the production line in places where mixing might occur.

Cleaning, etching, and diffusion steps used the same fixtures and equipment that would be used in an automated facility with the exception that automated transfer mechanisms would be used to minimize wafer handling. Such mechanisms are commonly used in various small parts manufacturing industries and in many cases have been used in portions of the semiconductor industry. Commercial equipment would require some adaptation and modification, but this should be minimal.

The back etch equipment used was hand loaded and operated, and was considered adequate for establishing the technological feasibility of the step. There is no known commercially available equipment for this operation, but there appears to be no significant problem in utilizing commercially available components in building an automated facility to perform this operation.

The several steps of printing, baking, and firing the thick film elements for the back field, and the front and back contacts utilized non-automated equipment for printing and baking. In an automated facility automatic printers, belt driers, and automated feed equipment would be used. This equipment has been developed and its use is well established in the thick film industry. A

belt furnace was used in establishing the feasibility of the contact firing operation step utilizing manual feed and unload.

Alloying the aluminum to the backs of the wafers was done in small batches in a tube furnace. Nominally this would be done in a properly profiled belt furnace, however none was immediately available, and the tube furnace operation was considered adequate for establishing the validity of the process for future automation.

The AR coating was done on a manually loaded and operated Headway single head spinner. This sufficed to establish technical feasibility, and commercial automatic equipment for performing this operation is readily available.

A K. O. Lee grinder was modified by the addition of a high speed air turbine, a recirculating coolant system, and an indexing vacuum table to perform the dicing step. Loading and unloading, as well as indexing, was done manually for the demonstration. Commercial dicing equipment is commonly available in the semiconductor industry; however automated loading and unloading would require the addition of automated wafer handling equipment and possibly some design and modification.

The final test facility consisted of a manually operated test station utilizing a temperature controlled holding fixture, a Spectrolab Model X-25 Mark III Solar Simulator, an X-Y curve plotter, a digital voltmeter, and a Spectrolab designed test set. Illumination levels were set by using a NASA calibrated solar cell. Final test conditions were AMO, 25°C, and an incident energy level of 135.3 mW/cm^2. An automated test facility would require the design and construction of automatic cell handling equipment, provisions for automatic periodic calibration checks, and data registering and recording facilities. Cells produced by the demonstration runs were checked for open circuit voltage, short circuit current, and current at 0.450 volt, a voltage level slightly lower than that for peak power point. I-V curves were plotted for several randomly selected cells from each lot.

In general, the laboratory model used hand loading of boats, fixtures, and equipment. Mechanized loading and transfer equipment for performing most of these operations is currently commercially available. The design requirements, production performance, and estimated cost of items of equipment with no commercial availability are given in Table IV-8.

Table IV-8

AUTOMATED PRODUCTION FACILITY

EQUIPMENT DESIGN REQUIREMENTS

Description	Steps for which required	Criteria	Estimated Cost
Etch facility	Back etch HF rinse	1. May consist of multiple stations 2. Shall be designed to accomodate the use of hydrofluric and hydrofluric-nitric acid solutions to the etching of two or three inch diameter silicon wafer structures on one side only. 3. Shall maintain the wafer temperature constant within $\pm$ 0.5°C during the prescribed etching cycle. 4. Shall have adjustable etch cycle times covering the range of 15 sec. to 1 minute followed by a cascade deionized water rinse. 5. Shall have mechanized feed and discharge using standard semiconductor wafer cartridges. 6. Shall be capable of a minimum thruput rate of 240 wafers per hour.	$12,000
Dice saw	Dicing	1. Shall be capable of cutting hexagonal or square cells from two or three inch diameter wafers. 2. Shall have mechanized feed and discharge using standard wafer cartridges. 3. Shall have a maximum cycle time.	$12,000
Automatic Tester/Sorter	Final test	1. Shall test hexagonal, square or round cells for current at a preset voltage in the range of 0.4 to 0.5 volts under standard conditions of solar simulation illumination. 2. Shall sort tested cells into reject and 3 acceptable groups determined by adjustable current output settings. 3. Shall have mechanized feed from standard wafer cartridges. 4. Shall have a minimum thruput rate of 590 cells per hour.	$45,000

V. DEMONSTRATION OF THE LABORATORY MODEL

A. DEMONSTRATION RUN PLAN

Initially the automation demonstration runs were scheduled in accordance with the planned starts schedule shown in Table V-1. Material was grouped into lots of 100 wafers with lot identity maintained throughout the cell fabrication process. At first the releases were kept low to allow process steps to be debugged and refined. As the schedule progressed the releases were increased to allow higher and higher volumes.

Data for each process step, necessary to the analysis of the process sequence was logged after each operation on a combination data log sheet and lot traveler which accompanied each lot through the line. A sample data log sheet is shown in Figure V-1.

The material used in the demonstration runs consisted of 51 mm. diameter wafers, which were ultimately diced into hexagonal cells measuring 25 mm. on a side. Six lots were made into rectangular 20 x 20 mm. cells and 20 x 40 mm. cells.

B. PLAN MODIFICATIONS

Once the demonstration runs were started it soon became evident that several factors were emerging that would require some modification to the original starts schedule. Since the laboratory model shared equipment, facilities, and personnel with the Spectrolab low cost solar cell production facility, the demonstration runs added to the throughput requirements of nearly all processing stations. In some cases these stations were already at or near capacity operation, and overload situations began to occur. This was temporarily relieved by processing the demonstration runs during overtime periods.

Table V-1

INITIAL DEMONSTRATION RUN STARTS SCHEDULE

Week Ending	No. of Days	No. of Starts	Cum. Starts
October 24, 1975	1	500	500
November 7, 1975	1	500	1,000
November 21, 1975	2	1,000	2,000
December 5, 1975	2	1,000	3,000
December 19, 1975	3	1,500	4,500
January 9, 1976	3	1,500	6,000
January 30, 1976	4	2,000	8,000
February 20, 1976	5	2,500	10,500
March 12, 1976	5	2,500	13,000
March 19, 1976	5	2,500	15,500

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AUTOMATION DEMONSTRATION Figure V-3

Prod. Lot No. _____ Start Date _____

No.	Phase	Date	Opr.	Time In	Time Out	Start	Good	Rej.	Remarks
01	Thickness Check					X	X	X	5 Random - Enter Below
	Etch								
	Thickness Check					X	X	X	5 Random - Enter Below
02	Diffusion								
	Sheet Res. Check					X	X	X	5 Random - Enter Below
03	Back Etch								
04	Print Al Back								Jar No.
05	Alloy								
	Clean								
06	Print Front								Jar No.
07	Print Back								Jar No.
08	Sinter								
09	Clean								
	Current Check								5 Random - Enter Below
10	Dice								
11	AR Coat								
12	Test								Enter Below

In-Process Checks:		1	2	3	4	5
01	Thickness Before Etch					
01	Thickness After Etch					
02	Sheet Resistance					
09	I @ .45V After Clean					

FINAL TEST DATA

(Current @ .45V - 1 Sun @ AMO/25°C)

Lows	420	430	440	450	460	470
480	490	500	510	520	530	540
550	560	570	580	590	600	610
620	630	640	650	660	670	680

It also became apparent, after the production volumes began to increase, that some of the process steps, while satisfactory for demonstrating an operation that could be readily automated, did not have the rate capacity to keep pace with the initial demonstration run starts schedule. In particular the steps having a lower production rate than originally planned were alloying, AR coating, and dicing.

It had been planned that the alloying would be done in a tube furnace, using a quartz ladder boat, and batches of fifty wafers. It was found that alloying in a ladder boat, with that high a density of wafers, gave unsatisfactory P+ layer formation. It was therefore necessary to return to the use of low heat mass quartz lattice boats and batches of eleven wafers for each alloying operation. This limited the throughput to only about eighty wafers per hour using the two furnace tubes available, instead of the 450 wafers per hour originally planned.

The AR coating step, using manual loading and a single head spinner could process only approximately 180 wafers per hour, rather than the considerably higher quantities initially used in planning the demonstration run schedules. Finally, the process step creating the greatest rate problem was the dicing operation. First, there were problems that had to be overcome in converting the K. O. Lee surface grinder into a high speed dicing saw, capable of producing satisfactory cuts on the wafers. Then it became apparent that the accuracy of locating the printed contacts on the wafer by using the half-inch flat, was not sufficient to allow "blind" scoring with the saw, positioning the wafers face down on the vacuum chuck. Templates had to be utilized, with a resulting throughput of only 25 wafers per hour. Therefore the modified demonstration run schedule shown in Table V-2 was established.

Table V-2

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MODIFIED AUTOMATION DEMONSTRATION RUN SCHEDULE

	PLANNED QUANTITIES PER WEEK										
PROCESS STEP	2-14	2-21	2-28	3-06	3-13	3-20	3-27	4-03	4-10	4-17	4-24
ETCH	***	***	***	***	500	500	500	500			
DIFFUSE	200	500	500	500	500	500	500	500			
BACK ETCH	200	500	500	500	500	500	500	500			
PRINT AL BACK	200	500	500	500	500	500	500	500			
ALLOY		200	500	500	500	500	500	500	500		
PRINT Ag FRONT		200	500	500	500	500	500	500	500		
PRINT Ag BACK		200	500	500	500	500	500	500	500		
SINTER			200	500	500	500	500	500	500	500	
CLEAN			200	500	500	500	500	500	500	500	
AR COAT			200	500	500	500	500	500	500	500	
DICE				200	500	500	500	500	500	500	500

***Wafers already on hand for these runs that have been through the etch process step.

B. PROCESS OPTIMIZATION

Once the demonstration runs had been started, several process steps were found where the results were not satisfactory. This required some readjustments in processing parameters and caused some delays in continuing the runs until the problems could be analyzed, tests performed, and the difficulties alleviated. In the time available not all problems were completely eliminated. The following portions of this section discuss those process steps that worked well during the demonstration runs, those that presented problems which were overcome, and those where further investigation will be needed.

Satisfactory Process Steps

Wafer processing through the back etch step was judged as generally satisfactory and no modifications in either the processes or sequences were made, with the following exceptions. The N+ layer diffusion time was shortened in order to compensate for the time the wafers would be held at the elevated alloy temperature. Also the removal of the doped oxide from the fronts of the wafers was postponed from the back etch step until after the alloying operation. A short (10 second) dip in 10% hydrofluoric acid was performed on the wafers after alloying to remove oxide layers prior to printing on the contact patterns.

Screen Printing Operations

No serious problems appeared in the screen printing steps other than the difficulty in accurately locating the patterns on each wafer. The printers used were shared with the low cost solar cell production facility, and used a retracting V-block for positioning the round wafers of that operation. The wafers being used in the demonstration runs were made with a half-inch flat on a $< 110 >$ edge. It proved to be more difficult than expected to accurately and repeatably position the wafers. Wafers were located prior to printing

by placing the wafer flat against one side of the V-block and sliding the wafer until its edge just touched the other side of the V-block. It was found that using this method only a fair geometrical accuracy could be maintained. It was decided that inaccuracies in pattern location could be corrected in the dicing step by scoring the wafer with respect to the pattern, rather than the wafer itself. In actual automated production the wafers used could be made with a larger flat (say 3/4-inch) and/or a notch to provide precise locating, a practice common in many automated semiconductor operations.

Alloying

Early lots processed through the laboratory model were found to either not exhibit the enhancement of open circuit voltage normal for cells having a P+ layer back field structure, or only partial enhancement. Attempts to use quartz ladder boats and relatively high density loading (50 wafers per load) resulted in wafers having discolored aluminum layers, sometimes coated with white powder-like material, which would not provide a satisfactory substrate for contact printing.

A series of test runs were therefore processed in 10 wafer batches performing the alloy step in the tube furnace using a low heat mass quartz lattice boat. Wafers were loaded face down on the boat. Insertion into the furnace was done at a rate of two inches per second (mad.) and withdrawal was as rapid as possible. Test groups were alloyed for periods of 5, 10, 15, 20, and 25 minutes. After metallization and HF rinsing the groups were tested at AM1 and 26°C for open circuit voltage with the following results:

Alloy Time	Average V_{oc}
5 min.	560 mV
10 min.	570 mV
15 min.	580 mV (590 mV @ AM0)
20 min.	560 mV
25 min.	560 mV

These data indicated that an alloy time of 15 minutes gave the best back field structure, and this was the period adopted for subsequent alloy processing.

Attempts to attain higher density loadings with ladder boats were unsuccessful. In the initial studies for this process wafers were loaded face down on a lattice boat. While results were satisfactory using the low heat mass lattice boats, capacity per load was limited, and vertical loading in ladder boats was desirable, since up to fifty wafers could be alloyed per cycle. However, tests seemed to indicate cross doping from wafer to wafer in the ladder boats and it was decided to accept the lower throughput limitation in favor of better back field behavior. Thus the use of lattice boats was continued throughout the demonstration runs.

Insufficient time was available to perform a complete and thorough investigation of alloying, since there are many factors affecting the process. This appears to be an area where further technical study is warranted.

Contact Firing

After both front and back contact patterns had been screen printed and baked at 150°C in air for fifteen minutes, the wafers were air fired in a conveyor belt furnace, where the temperature was elevated to 630°C and then gradually cooled to room temperature. This firing is necessary to drive off organic materials remaining in the contact paste. This operation elevated the temperature of the wafers above the aluminum-silicon eutectic temperature, remelting some of the eutectic, however, since it was well below the alloy temperature, there was no adverse effect on the back field structure.

Insufficient time was available to attempt different temperature programs for this firing step. Also the necessity for sharing the belt furnace with an ongoing production facility precluded modifying this step. As a result no changes were made in this step of the processing.

HF Rinse (Cleaning)

The 10% hydrofluoric acid rinse following the contact firing appears to be a critical operation. This process improves the shape of the I-V curve markedly. However the duration of the acid rinse (10 seconds) must be carefully controlled. Insufficient treatment results in inferior I-V curve shapes and correspondingly low curve factors, while excessive treatment causes detrimental effects on contact adhesion. It was found that some lots exhibited poor contact adhesion, yet had satisfactory electrical performance, yet demonstrated satisfactory contact adhesion. Fortunately the majority of the lots processed were satisfactory electrically and also had adequate contact integrity.

The presence of the alloyed aluminum layer appears to be a factor, for wafers without a P+ layer were given the HF rinse in the same boats and at the same time as wafers from the demonstration runs. The wafers without the P+ layer had satisfactory contacts, while the wafers with the back field layers had barely acceptable adhesion.

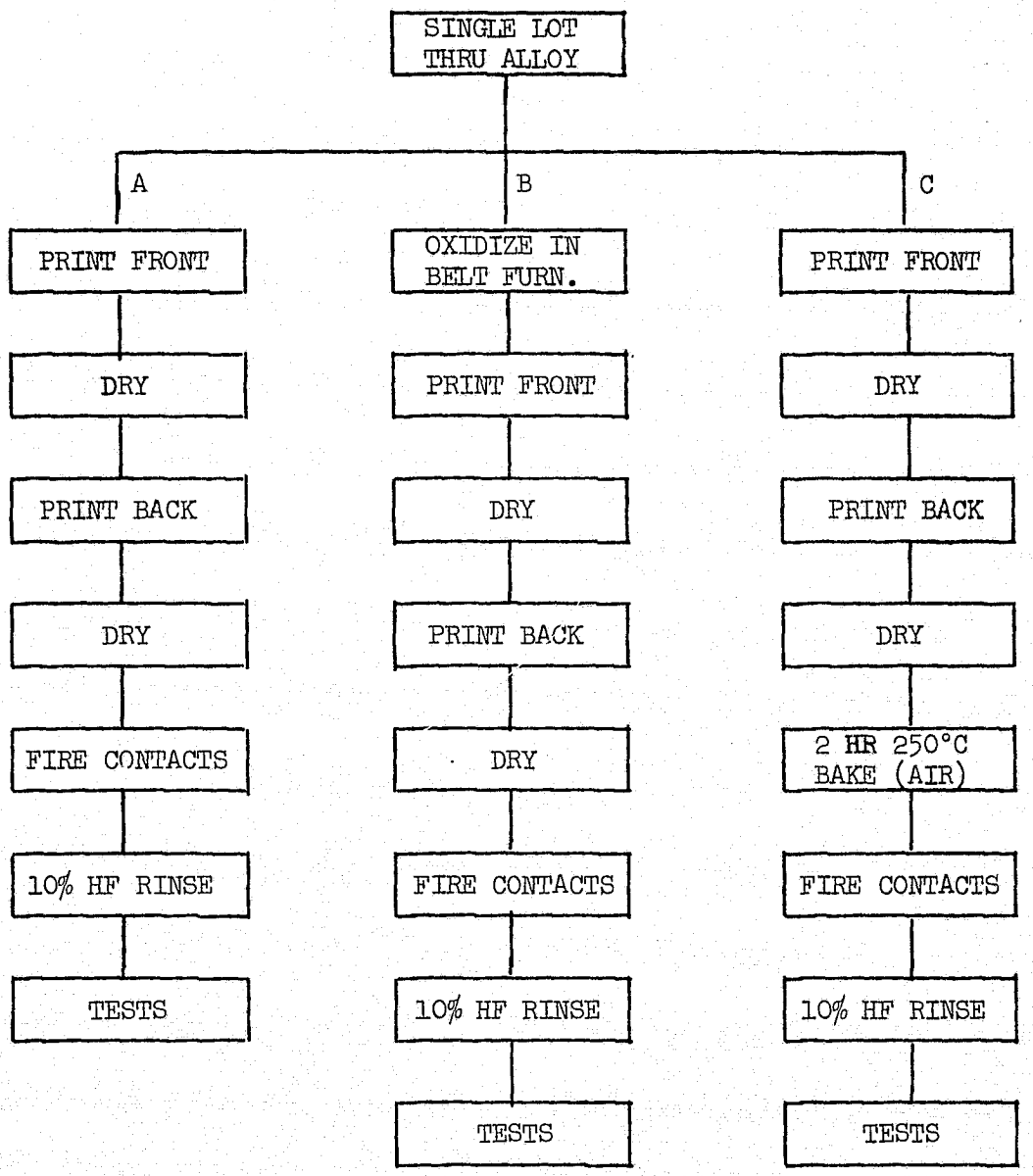
Refiring wafers with poor contact adhesion by passing them through the belt furnace a second time made the contacts quite satisfactory, but at the expense of curve factor. Another 10% HF rinse improved the curve shape, but did not attain the curve factor realized after the first processing.

Within the limited time available an experiment was performed to determine if a controlled oxide layer on the wafers prior to contact printing would improve adhesion without detrimentally affecting cell performance. A wafer lot that had been processed through the alloy step was split into three sublots A, B, and C. These were then processed through the sequences shown in Figure V-2. Ten random wafers from each group were then tested electrically and given pull tests using a Unitek Model 6-092-03 tester.

Figure V-2

PROCESSING BLOCK DIAGRAM

FOR ADHESION TESTS



It was found that Group A, the control group, that had had normal processing, had pull strengths at the front solder pad ranging from 0 to 250 gms (average 153 gms). Group B, which had been slightly oxidized by passing through the belt furnace prior to contact printing, had pull strengths ranging from 25 gms to 550 gms (average 305 gms). Group C, which had been given a 250°C bake in air for two hours after contact printing and prior to the belt furnace contact firing, had strengths ranging from 75 gms to 500 gms (average 340 gms).

Group A had the better electrical behavior, with average values of V_{oc} of 587 mV, I_{sc} of 676 mA, and $I_{.45V}$ of 569 mA. Group B had an average V_{oc} of 581 mV, I_{sc} of 669 mA, and an $I_{.45V}$ of 543 mA. Group C was found to have an average V_{oc} of 566 mV, I_{sc} of 652 mA, and $I_{.45V}$ of 478 mA. This seemed to indicate that the normally processed wafers had the best electrical characteristics with the poorest contact adhesion.

Five random wafers were then taken from each of five normally processed lots and given pull strength tests at the solder pad and at a point midway down the central ohmic stripe. The following data were obtained:

Lot Number	Average Pad Strength	Average Mid-Stripe Strength
1219-01-75	735 gms (550 to 975 gms)	750 gms (650 to 850 gms)
1216-03-75	645 gms (125 to 1100 gms)	640 gms (500 to 700 gms)
1217-03-75	880 gms (25 to 1600 gms)	770 gms (25 to 1300 gms)
1218-01-75	410 gms (200 to 700 gms)	515 gms (325 to 800 gms)
1218-03-75	290 gms (150 to 375 gms)	995 gms (400 to 1650 gms)

These measurements indicated a wide variation from lot to lot in contact adhesion, as well as some cases where there was a wide variation across a single wafer. In only one case (Lot 1217-03-75) did the lowest pull strength at the solder pad occur on the same wafer as the lowest pull strength midway down the ohmic stripe. With additional time for further investigations unavailable, it was decided to continue processing the demonstration runs as planned without a process change, rejecting inferior wafers on an individual basis. However, this is an area where further technical study and development is needed.

Dicing

The dicing process offered no particular problems except for a relatively slow rate of throughput. This was caused by the necessity of manually loading cells face-down on transparent templates so that the contact patterns were precisely positioned on guide line, loading the templates on the vacuum chuck, and making the necessary scoring cuts. Indexing of the vacuum chuck was done manually after each cut. Wafers were then cleaned in a trichlorethylene ultrasonic bath and rinsed in alcohol.

The inherent slowness of this operation is only a characterization of the equipment and method used in the laboratory model. In an automated facility, mechanized loading, positioning, indexing, and unloading would allow an adequate throughput rate which could be increased further by the use of ganged saw blades allowing multiple cuts per pass.

AR Coating

The earlier lots processed in the demonstration runs had the titanium oxide - silicon oxide spin-on AR coatings applied prior to the dicing operation. In order to avoid possible damage to such coatings during the mechanical handling necessary during the dicing step, later lots were not coated until after dicing. Subsequent electrical testing did not show any noticeable difference.

To check on the effectiveness of the spun-on AR coatings as applied in the laboratory model, as well as to compare these coatings with a conventional evaporated AR coating, a series of measurements were made using three groups of similar terrestrial cells.

Five cells were coated in the normal fashion with the spin-on AR coating, five were coated with the evaporated AR coating, and five cells were left uncoated. The short circuit currents of all cells were measured before and after coatings. All cells were then given a thin layer of silicone resin and attached to 2" x 3" microscope slides. This simulated actual mounting in a module. Short circuit current measurements were made at AM1 and 26°C. The results of these tests, shown in Table V-3, indicate that while the evaporated AR coatings are superior in enhancing the short circuit currents for unmounted cells, the spun-on AR coatings are nearly as effective when the cells are placed under a layer of resin and glass. Both groups of AR coated cells were superior to the uncoated cells under the conditions of a simulated module mounting.

The AR coating procedure adopted for the demonstration runs consisted of manually loading and unloading a single position spinner, coating the cells with the titanium oxide-silicon oxide liquid, spinning at 4,000 rpm for 15 seconds, and baking at 250°C for 30 minutes.

Table V-3

AR COATING EFFECTS ON SHORT CIRCUIT CURRENTS

Cell Group	AR Coating Used	Av. Percent I_{sc} Increase* (AR coating only)	Av. Percent I_{sc} Increase* (AR coating + Resin + Glass)
A	None	-------	+11.12%
B	Spin-on	+ 7.13%	+14.52%
C	Evaporated	+17.54%	+15.98%

* Compared to uncoated values

C. ANALYSIS AND REVIEW

General

Since the laboratory model shared equipment and facilities with an ongoing production operation, it was necessary to process the demonstration runs during intermittent periods. Lots were passed through the processing sequence in "bubble" fashion with the result that bunching would occur when equipment was not available. This effect was made more pronounced by the process steps having relatively low throughput capacities. Balanced operations, with a continuous flow of material through the pilot line, were not possible.

Forty-one lots were processed during the demonstration runs, following as closely as possible to the schedule of Table V-2. Each lot started out with 100 2-inch silicon wafers as-cut from the sawing process. Six of these lots were made into 20 x 40 mm. and 20 x 20 mm. rectangular cells, while all other lots were made into hexagonal cells. Two lots were terminated after the 10% HF rince step because of poor contact adhesion. Two lots were used for test purposes in attempts to improve back field effectiveness and contact adhesion.

All lots were processed through the 10% HF rinse step, however the slowness of the dicing operation became an obstacle to processing all lots into the hexagonal cells. Since insufficient time was available to complete all lots, it was decided to dice ten random wafers from each lot into the hexagonal shape and thus get electrical data on all lots processed. Thus twenty lots were sampled in this fashion, and ten lots were 100% tested electrically.

Process Yields

Because of the discontinuous nature of the operations, yield data should be viewed as more of an indication of potential than a significant measure of actual capability. Generally continuous operations are necessary to allow processing to be optimized and thus achieve maximum yields. Since some

process steps were identical with the shared production line, yields are probably quite accurate. Other steps which were unique to the demonstration runs did not attain the consistency or operating efficiency of automated continuous processing.

Yield data for the various process steps is given in Table V-4. Yields for the electrical testing are not shown, since in the absence of a specification, none were rejected. The electrical testing served primarily to establish the general electrical behavior of cells fabricated by this particular process sequence. Losses were generally due to mechanical breakage in the early process steps, and in particular in the printing steps where aluminum lumps that had not been removed after the alloy step did not allow the wafer to lie flat during printing.

Breakage was initially severe during the dicing operation, primarily because the operation required considerable mechanical handling of the wafers. As experience was accumulated in operating the dicing saw, breakage became less and less, until it was well within acceptable levels.

Electrical Performance

Ten lots of demonstration run cells were completely diced into hexagonal cells, AR coated, and then tested 100% for electrical performance. Six lots were made into rectangular cells, with the first fifty wafers of each lot being diced into 20 x 40 mm. cells, and the remaining wafers of the lot being made into 20 x 20 mm. cells. These were also tested 100% after AR coating. Because of time limitations the remaining lots were not completely diced and tested. Instead, ten wafers were selected at random from each lot, and these were diced into hexagons, AR coated, and electrically tested.

While no specifications had been established for solar cells made by this process sequence, measurements made on small groups of cells during the early process studies gave indications as to what general level of performance to

Table V-4

YIELDS FOR PROCESS STEPS

Process Step	Percentage Yield
Wafer Etch	99.4
Diffusion	98.0
Back Etch	99.5
Print Aluminum	98.3
Alloy	99.5
Print Front	96.0
Print Back	98.0
Fire Contacts	98.3
HF Rinse	77.3
AR Coat	94.9
Dice to Shape	84.9

expect. All tests were made at AMO using a Spectrolab Model X-25 Mark III Solar Simulator adjusted to an illumination level of 135.3 milliwatts per square centimeter using a NASA calibrated standard cell. All tests were made at a cell temperature of 25°C. Cells were measured for open circuit voltage, short circuit current, and current at 450 millivolts. Plots of the IV-curves were made for five random cells from each lot. A typical set of I-V curves for one lot of hexagonal cells is shown in Figure V-2. Also shown are segments of the constant power curves for three different efficiencies for hexagonal cells of this size under the above test conditions. It was found that the characteristic I-V curves for any given lot were fairly tightly grouped.

Data from these tests are shown in Table V-5 for the hexagonal, 20 x 40 mm., and 20 x 20 mm. cells. Shown are the arithmetic mean and the standard deviations for each of the three parameters tested. In the case of the hexagonal cells, to avoid weighting of the data by the lots that were 100% tested, the table indicates the values for all cells tested, as well as values for the 100% tested lots and the sampled lots taken separately. Shown also are the ranges for the parameters measured.

It should be noted that the peak power point, as indicated by the I-V curves taken, is generally at 0.46 - 0.47 volt, rather than the 0.45 volt point where the current points were taken for the data of Table V-5. Average cell efficiency was 10.7% for the hexagonal cells, 10.4% for the 20 x 20 mm. cells, and 10.5% for the 20 x 40 mm. cells.

Figure V-2

CURRENT vs VOLTAGE CURVES

FOR A TYPICAL LOT OF HEXAGONAL CELLS

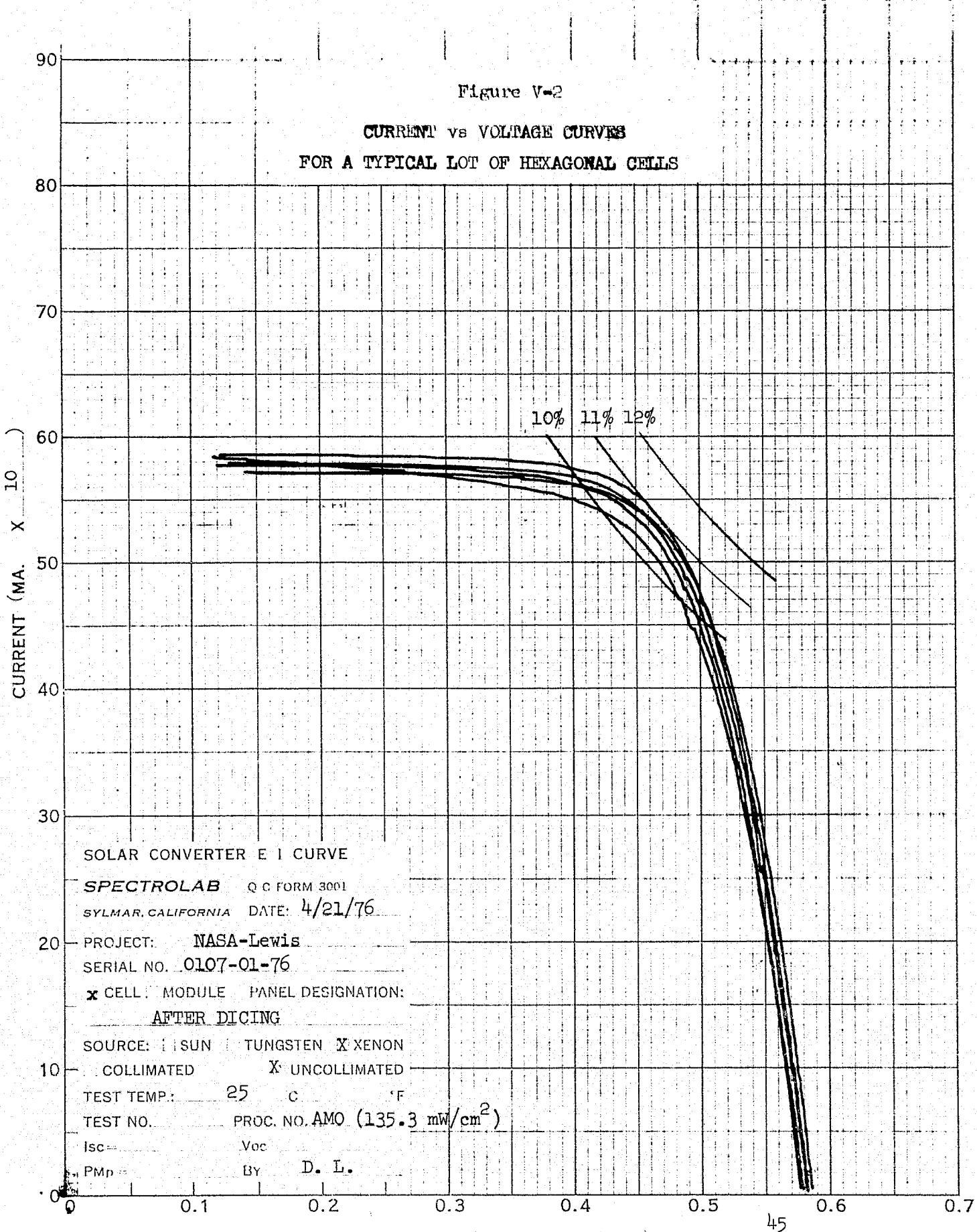


Table V-5

ELECTRICAL PERFORMANCE DATA

(All tests at AMO, 25°C, 135.3 mW/cm^2)

	Range of Values Found	All Cells Tested			100% Tested Lots Only			Sampled Lots Only		
		Number Tested	Arith. Mean	Std. Devia.	Number Tested	Arith. Mean	Std. Devia.	Number Tested	Arith. Mean	Std. Devia.
Hexagonal Cells*:										
V_{oc}(mV)	555-605	690	583	9.1	493	585	9.5	197	582	8.7
I_{sc}(mA)	510-610	690	567	14.8	493	569	13.3	197	560	16.1
$I_{.45V}$(mA)	420-565	690	510	27.9	493	513	26.4	197	502	29.9
20 X 40 mm. Cells:										
V_{oc}(mV)	515-600	264	569	19.5	---	---	----	---	---	----
I_{sc}(mA)	240-280	264	262	7.3	---	---	----	---	---	----
$I_{.45V}$(mA)	180-265	264	237	17.6	---	---	----	---	---	----
20 X 20 mm. Cells:										
V_{oc}(mV)	525-600	275	570	18.5	---	---	----	---	---	----
I_{sc}(mA)	110-140	275	130	4.3	---	---	----	---	---	----
$I_{.45V}$(mA)	95-135	275	119	8.2	---	---	----	---	---	----

* Frontal area of hexagonal cells is 16.76 cm^2.

VI. FURTHER TECHNOLOGICAL DEVELOPMENT

A. BACK FIELD FORMATION

While the present process used in the laboratory model was successful in obtaining a back field structure using screen printed aluminum paste which was then alloyed into the silicon, additional process refinement and study is needed. The aluminum paste used in the work to date includes a relatively low melting glass frit, which may well be useful in applications where alloying is not used, but quite possibly may interfere with the alloy process. There is some possibility that the glass prevents all of the aluminum particles from reaching the aluminum - silicon eutectic formed during the alloy step, and thus inhibits the alloying from being complete. Additional work is needed in this area using aluminum pastes that do not contain such materials.

There is some evidence that the back field structure can be formed by performing the alloy step in a period of only a few seconds duration, using a very fast heat/cool temperature spike. Penetration into the silicon under such conditions appears to be fairly uniform, and the P+/P- junction formed is quite abrupt. Additional development of the alloying thermal cycle to optimize the formation of the proper structure, without forming aluminum lumps and balls, would be most helpful.

Finally, the HF rinse step, used after firing on the metallization, produces a dark spongy layer on the printed aluminum material. This can be abraded off some wafers quite readily, while on others it is quite difficult to remove. Tests indicated that this material had good electrical conductivity, yet it may well have an adverse effect on the adhesion of the back metallization. It is quite possible that the removal of this spongy layer might improve the contact adhesion, as well as reducing the series resistance of the cell to some degree.

B. HF RINSE (CLEANING)

After the contact metallization is fired onto the solar cell wafers they are immersed in a 10% HF solution for ten seconds, rinsed in deionized water, washed in a dilute NaOH solution for a time to stop additional action by the HF, and then washed in deionized water. This step improves the shape of the characteristic I-V curve for the cells and gives a marked decrease in the series resistance of the cells.

If the HF rinse is at all prolonged beyond the ten seconds normally used, there will be a loss of contact adhesion to the surface of the cell. Cases were observed where contact adhesion became unsatisfactory before the improvement in curve shape had been completed.

It appears that effort to improve this process, by using a different chemical treatment, is warranted. The chemistry involved, and how it interacts with the contact pastes used and the firing cycles employed, make the problem a complex one. However, such investigations would be most beneficial in reducing yield losses because of poor contact adhesion.

C. AR COATING TECHNIQUES

Cells produced in the laboratory model during the demonstration runs were AR coated by a spin-on process. It is possible that similar coatings could be applied by a spray-on method that might well have some decided advantages. The spin-on coatings which were applied to the texturized front surface of the cells were found to enhance the short circuit currents still more if a second coating was applied and baked on over the first coating. The silicon tetrahedrons on the texturized surface may well cause some "shadowing" during the spinning step, thus leaving some of the front surface uncoated, or insufficiently coated. A spray-on process might enable a more effective coating thickness to be obtained in one step, and would have the additional advantage of allowing masking to be used to prevent AR coating material from covering the solder pad on the metallization.

VII. CONCLUSIONS

During the course of this program it was established that useful silicon solar cells could be fabricated using a sequence of processes that excluded small batch, high energy steps. Screen printed contacts and spin-on AR coatings were utilized in lieu of high vacuum evaporated techniques. Each process step was chosen so as to be capable of being automated in a continuous flow operation, to thereby offer marked cost reductions, as well as a more uniform product.

Using these processes and techniques, a conceptual design for an automated solar cell production facility was generated. This facility would be capable of producing 4.75-million hexagonal cells per year measuring 38 mm. on a side for an estimated manufacturing cost of $0.866 per cell. If these cells had an efficiency of 14%, they would have a power capacity of 3,373 kilowatts at AMO, assuming a one sun input of 1353 watts per square meter, and thus an energy cost of roughly $1.22 per watt.

In order to establish the validity of the processes and sequences developed a laboratory model production line was designed and assembled using these concepts, and a series of demonstration runs were processed through this line. These operations were primarily to establish the feasibility of the processes, each of which were chosen so as to be readily automated. The majority of the solar cells produced during these runs were hexagonal cells, 25.4 mm. on a side, however some 20 x 20 mm. and 20 x 40 mm. cells were also produced.

The cells produced in the demonstration runs had an average efficiency of 10.7%, when tested at AMO, 25°C, and an input energy level of 135.3 milliwatts per square centimeter. All of the processes appeared to be capable of producing satisfactory cells, however additional optimization, not undertaken because of time limitations, is needed to improve the

effectiveness of the P+ back field structure and the adhesion of the printed contacts after the HF rinse step. The yields obtained for the various process steps were generally satisfactory, however since the laboratory model was not operated on a continuous basis, no yield optimization effort could be mounted.

In general, the program established the validity of the concepts and design of a silicon solar cell production facility capable of being automated and capable of continuous flow operations with marked reductions in costs. Not unexpectedly, the effort also gave indications and guidance as to areas where further technological development is needed, namely in improving the back surface field structures, the quality of the printed contacts, and the effectiveness of the non-evaporated AR coatings.