NASA

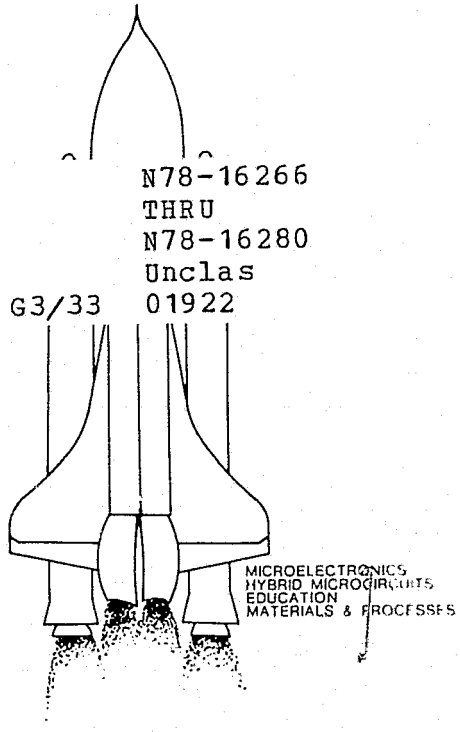
National Aeronautics and Space Administration

INTERNATIONAL HYBRID MICROELECTRONICS SOCIETY FOR

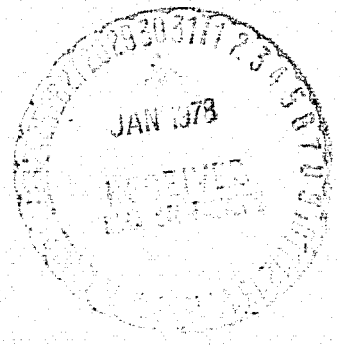
Tennessee Valley Chapter

George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

NASA CP 2027



Proceedings of the 1977 NASA/ISHM Microelectronics Conference



September 20—21,1977
Morris Auditorium
Marshall Space Flight Center, Alabama

TECHNICAL REPORT STANDARD TITLE PAGE

1. REPORT NO.	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.
NASA CP 2027		

4. TITLE AND SUBTITLE	5. REPORT DATE
MICROELECTRONICS CONFERENCE - Microelectronics for the Nineteen Eighties	November 1977
	6. PERFORMING ORGANIZATION CODE
7. AUTHOR(S) Compiled by S. V. Caruso	8. PERFORMING ORGANIZATION REPORT #
9. PERFORMING ORGANIZATION NAME AND ADDRESS Marshall Space Flight Center Marshall Space Flight Center, Alabama 35812	10. WORK UNIT NO.
	11. CONTRACT OR GRANT NO.
12. SPONSORING AGENCY NAME AND ADDRESS National Aeronautics and Space Administration Washington, D. C. 20546	13. TYPE OF REPORT & PERIOD COVERED Conference Publication
	14. SPONSORING AGENCY CODE

15. SUPPLEMENTARY NOTES

16. ABSTRACT

~~The objective of the Conference was~~ to provide a forum to discuss current and future requirements for research, development, manufacturing and education in the field of hybrid microelectronic technology. The Conference was held at the George C. Marshall Space Flight Center (MSFC) at Huntsville, Alabama, on September 20 and 21, 1977.

17. KEY WORDS	18. DISTRIBUTION STATEMENT
	Unclassified-Unlimited

19. SECURITY CLASSIF. (of this report)	20. SECURITY CLASSIF. (of this page)	21. NO. OF PAGES	22. PRICE
Unclassified	Unclassified	179	NTIS

For sale by National Technical Information Service, Springfield, Virginia 22151

OVERVIEW OF THE TRI-SERVICE MICROELECTRONIC MM&T PROGRAM

CHARLES E. McBURNEY

MANUFACTURING TECHNOLOGY DIVISION

US ARMY INDUSTRIAL BASE ENGINEERING ACTIVITY

ROCK ISLAND, ILLINOIS 61201

TABLE OF CONTENTS

D1

N78-16267

OVERVIEW OF THE TRI-SERVICE HYBRID MICROELECTRONICS MM&T PROGRAMS

For purposes of this overview, a hybrid circuit will be defined as one constructed on a thick or thin film substrate and having attached to it discrete components and/or integrated circuit chips. It may be packaged in a ceramic, metal or plastic housing. It's purpose is to provide a complete electronics function.

Within the MM&T program, Army has aggressively pursued new hybrid techniques more than either the Navy or Air Force. Army has 30 on-going hybrid projects in various stages of contracting and execution, 14 at Electronics Command, 13 at Missile Command, and three at Armament Command. Navy has six, and Air Force has two.

In FY79, Army is programming for eight hybrid projects, Navy for five, and Air Force none. In terms of dollars, Army's FY79 program is worth $2.25 million, and Navy is expected to spend about $1.7 million.

SHIFT IN EMPHASIS

Recently, the emphasis on hybrid circuit manufacturing processes has shifted from Army's Electronics Command to the Missile Command. Most of the Army's FY79 hybrid program is being done here at Missile R&D Command. Mr. Victor Ruwe, hybrids prototype laboratory manager, is the proponent of several of the projects proposed for FY79, all of which are listed here:

R 3146 High Density Multilayer Thick Film Hybrid Microcircuits.

R 3251 High Temperature Operating Tests for Microcircuits.

R 3410 Production Method for Heat Pipes for Hybrid/LSI.

R 3436 Development of Ceramic Circuit Boards and Large Area Hybrids.

R 3438 Delidding Parallel Seam Sealed Hybrid Microcircuit Packages.

R 3081 Radar Monopulse Seekers Using PC and Stripline Techniques.

R 3956 Low Cost Protection for Fuze Electronics.

R 9869 Rapid Removal of Plastic Encapsulants.

ARMY'S PROPOSED HYBRID PROGRAM FOR FY79

R3436	DEVELOPMENT OF CERAMIC CIRCUIT BOARDS AND LARGE AREA HYBRIDS
R3146	HIGH DENSITY MULTILAYER THICK FILM HYBRIDS
R3410	PRODUCTION METHOD FOR HEAT PIPES FOR HYBRID/LSI
R3438	DELIDDING PARALLEL SEAM SEALED HYBRID PACKAGES
R3251	HIGH TEMPERATURE OPERATING TESTS FOR MICROCIRCUITS
R3081	RADAR MONOPULSE SEEKERS USING PC AND STRIPLINE TECHNIQUES
53956	LOW COST PROTECTION FOR FUZE ELECTRONICS
H9869	RAPID REMOVAL OF PLASTIC ENCAPSULANTS

NAVY'S PROPOSED FY79 HYBRID PROGRAM

DNA-053	DEVELOPMENT OF COMPUTERIZED THICK FILM PRINTER
DNA-366	HIGHER DENSITY THIN FILM HYBRIDS
DNA-414	AUTOMATED SELF-TEST WIRE BONDER
DNA-557	INTEGRATED CIRCUIT CHIP CARRIER PACKAGE
DNE-034	EXTRA HIGH FREQUENCY INTEGRATED CIRCUITS

AIR FORCE ON-GOING HYBRID PROJECTS

71E 08512-8B MICROWAVE HYBRID PROCESSES

78E 08511-8B STANDARD ELECTRONIC MODULES FOR AVIONICS

AS OF SEP 77

ELECTRONICS COMMAND ON-GOING HYBRID PROJECTS

274 9656	SUPERFINE FINISH BERYLLIA SUBSTRATES
274 9411	SILK SCREENING AND LAYERIZING CERAMIC DIELECTRIC CAPACITORS
274 9767	DEPOSITING THICK FILM CIRCUITS FOR CRYSTAL OSCILLATORS
274 9575	AUTOMATIC ASSEMBLY OF HYBRIDS FOR FUZES
276 9749	THICK FILM PROCESSING OF MICROWAVE ICS
276 9766	DEPOSITING HIGH VOLTAGE INSULATING LAYERS ON THICK FILM CIRCUITS
276 9781	THIN FILM TRANSISTOR-ADDRESSED DISPLAY

AS OF SEP 77

ELECTRONICS COMMAND FY77 AND FY78 HYBRID PROJECTS

277 9857	AUTOMATIC SEPARATION, CARRIER MOUNTING AND TESTING OF SEMICONDUCTOR DICE
277 9808	AUTOMATIC IN-PROCESS EVALUATION OF THICK FILM PRINTING AND HYBRID CIRCUIT ASSEMBLY
277 9835	INTEGRATED CONTROL CIRCUIT FOR THIN FILM TRANSISTOR DISPLAY
278 9837	HIGH DENSITY MEMORY PROCESSING AND PACKAGING TECHNIQUES
278 9869	RAPID REMOVAL OF PLASTIC ENCAPSULANTS
278 9871	AUTOMATED PRODUCTION OF MILITARY ICS
278 9877	LIGHT EMITTING DIODE ARRAY COMMON MODULES

AS OF SEP 77

MISSILE COMMAND ON-GOING HYBRID PROJECTS

376 3147	ADDITIVE PROCESS FOR FABRICATION OF PRINTED CIRCUIT BOARDS
376 3224	SCREENING OF ELECTRONIC COMPONENTS
376 3227	LOW COST PRODUCTION METHOD FOR HANDLING HYBRID CHIPS VIA A TAPE CARRIER LEAD FRAME
377 3165	SEALING HYBRID MICROCIRCUIT PACKAGES

AS OF SEP 77

MISSILE COMMAND FY78 HYBRID PROJECTS

378 3075	INFRARED TESTING OF PC BOARDS AND MICROCIRCUITS
378 3146	PHOTOLITHOGRAPHIC PROCESS FOR THICK FILM MULTI-LAYER CIRCUITS
378 3165	SEALING HYBRID MICROCIRCUIT PACKAGES
378 3219	AUTOMATIC POLYMER ATTACHMENT PRODUCTION METHODS
378 3227	HANDLING HYBRID CHIPS VIA A TAPE CARRIER LEAD FRAME
378 3254	LOW COST SEMI-FLEXIBLE THIN FILM SEMICONDUCTORS
378 3405	THICK FILM MICROELECTRONICS PROCESSING EQUIPMENT FOR BASE METAL CONDUCTORS
378 9406	LOW COST PRODUCTION OF MULTILAYER HYBRIDS

AS OF SEP 77

ARMAMENT COMMAND ON-GOING HYBRID PROJECTS

577 3947	THICK FILM HYBRID CIRCUITS FOR M587/M724 FUZES
578 3925	PROTOTYPE PRODUCING EQUIPMENT FOR FUZE HYBRIDS
578 3947	THICK FILM HYBRID CIRCUITS FOR M587/M724 FUZES

AS OF SEP 77

NAVY'S PROPOSED AND ON-GOING HYBRID PROJECTS

DNA 363	DEVELOPMENT OF LOW COST THICK FILM MIC
DNA 053	COMPUTERIZED THICK FILM PRINTER
DNA 504	PILOT PRODUCTION OF IMPROVED AIMS ENCODER
DNA 366	HIGH DENSITY THIN FILM HYBRIDS
DNA 414	AUTOMATED SELF TEST HYBRID WIRE BONDER
DNA 557	INTEGRATED CIRCUIT CHIP CARRIER PACKAGE

AS OF SEP 77

ARMY'S BUDGETED FY79 HYBRID PROGRAM

R 3146 High Density Multilayer Thick Film Hybrid Microcircuits.

Present screening technology is generally limited to 6 mil lines on 12 mil centers, with 12 mil (.012) via holes. Present methods also require firing each layer separately after screening and drying. This project will scale up R&D methods for multilayer circuits which require only one firing and can produce 4 mil lines on 8 mil centers. Drilling and plating 10 mil via holes will also be addressed.

Narrower lines and spaces can reduce the number of layers or circuitry required and thus may improve yield rather than reduce it.

R 3436 Development of Ceramic Circuit Boards and Large Area Hybrids.

Large scale hybrids (LSH) are expected to be needed to meet near future requirements for electronic systems. LSH's will increase system reliability because they reduce the number of substrates and interconnections. This project will investigate several ceramic base circuit boards and substrates manufacturing methods, and can lead to integration at the system level.

R 3410 Production Method for Heat Pipes for Hybrid/LSI.

Work here will optimize:

a. The design of the substrate for maximum heat transfer,

b. methods for assembling the heat pipe casing, wick, and hydrocarbon fluid, and

c. methods for sealing the circuit and housing to prevent leakage.

The project envisions the circuit package as forming a heat pipe. The heat-generating circuit substrate is in one end and is protected by surface passivation; the cooling medium surrounds the circuitry and moves by wicking action to the cooler, radiating end of the package. This method greatly improves heat transfer capability and efficiency.

R 3081 Production of Radar Monopulse Seekers Using PC and Stripline Techniques

Besides applying stripline photo-etching techniques to slot array antennas, the contractor will work on hybrid networks for forming sum and difference patterns of received signals, and on the receiver front end using PC and stripline techniques. Will work on smooth conductor surfaces on low loss materials.

R 3438 Delidding Parallel Seam Sealed Hybrid Microcircuit Packages.

Lids are now removed by grinding or cutting the flange, or lapping away the lid. This project will develop semiautomatic equipment to cut or lap the lid to a controlled depth. Prior to breakthrough, the package will be removed from the device and the lid removed by hand to prevent abrasion particles from entering the package. A documentable procedure should result.

R 3251 High Temperature Operating Tests for Microcircuits.

Accelerated life testing of unpackaged hybrid circuit components can increase the reliability of hybrid circuits. This project will document a procedure for applying high temperature operating tests to unencapsulated semiconductor devices to be used in hybrid circuits.

Use of well tested hybrid circuit components can appreciably increase the yield and reliability of the hybrid circuit in which they are used.

R 3956 Low Cost Protection for Fuze Electronics.

Hybrid thick film circuitry used in low cost, high "g" fuzes will be injection molded with plastic to form electronic modules. The modules may be metal plated for electrical shielding. Unpackaged semiconductor chips may be bonded to the substrate and coated with protective material prior to injection molding.

This system is expected to replace foamed-in-place encapsulation or poured solid potting methods.

2 9869 Rapid Removal of Plastic Encapsulants.

Will vacuum form a plastic film over a printed or hybrid circuit prior to foam encapsulation, to permit easy removal of the foam.

NAVY'S PROPOSED FY79 HYBRID PROGRAM

DNA-053	DEVELOPMENT OF COMPUTERIZED THICK FILM PRINTER
DNA-366	HIGHER DENSITY THIN FILM HYBRIDS
DNA-414	AUTOMATED SELF-TEST WIRE BONDER
DNA-557	INTEGRATED CIRCUIT CHIP CARRIER PACKAGE
DNE-034	EXTRA HIGH FREQUENCY INTEGRATED CIRCUITS

NAVY'S PROPOSED FY79 HYBRID PROGRAM

DNA 557 Integrated Circuit Chip Carrier Package.

Complex hybrid circuits will benefit from the use of chip carriers for applying IC's to the film circuit. This is the third phase of a three year effort to production engineer small multilayer ceramic packages. A metallization pattern is formed on top surface of the ceramic and is connected by "vias" to pads formed on the bottom of the ceramic. The pads are placed on 40 mil or 50 mil centers; 40 mil centers can be used with metric spacing — 1 millimeter or 39.39 mil centers.

DNA 053 Development of Computerized Thick Film Printer.

This is the third phase of a three year effort to develop a high speed computer controlled applicator that will actually "write" the desired conductor and resistor thick film patterns onto substrates. The system will use a minicomputer and teletype, an X-Y table with stepping motors, a TV viewing system, and a fluid dispensing system. It will use some of the components of a laser trimming system, except the epoxy dispensing system will replace the laser; a bonding tool capillary with 0.2 mil opening will form part of the inking system.

DNA 366 Higher Density Thin Film Hybrids.

This is a continuation of a FY78 project to

1. Selectively etch multiple resistance layers,
2. fabricate air-isolated microbridges, and
3. plasma deposit monomer (teflon) films.

In part 1, thin films of different sheet resistivity will be laid down and will then be selectively etched. Part 2 will adapt RCA and Bell Labs techniques for making microbridges to comply with military standards. Part 3 will develop plasma deposition techniques for monomer films to protect the film circuitry from humidity.

DNE 034 MMT for Extra High Frequency Integrated Circuits.

On polished ceramic substrates, thin and thick film circuitry will be deposited with fine line definition and smooth surfaces and edges. These qualities are needed for extra high frequency (20 to 100 gigahertz) applications which include fuzing, surveillance, communications, and guidance systems.

DNA 414 Automated Self-Test Wire Bonder.

This is the third phase of a three year effort to apply a non-destructive pull tester (NDPT) to an automated wire bonder. Typical numerically controlled wire bonders are guided through a cycle of operation by an operator while the computer memory "learns" the cycle. Then the bonder is set to run the cycle itself. The new feature — a pull test of each wire — includes feedback to vary the bonding parameters to ensure specified bonding strength.

AIR FORCE ON-GOING HYBRID PROJECTS

9B0852X MT for Conformal Coatings.

Air Force Materials Labs has planned no work in hybrid circuitry for FY79, but some of the results of their 2nd year effort on conformal coatings may apply. AFML is classifying different coatings and looking at their removal and repair techniques.

9X0852X MT for Printed Wiring Boards.

While this is obviously not a hybrid circuit project, some of the techniques established for computer aided design, conductor routing, and circuit test techniques apply also to hybrid circuit layout. This is the second phase of a polyimide PWB contract at McDonnell Douglas, St. Louis, and the techniques developed are applicable to hybrid manufacture.

AIR FORCE ON-GOING HYBRID RELATED PROJECTS

9B 0852X	MT FOR CONFORMAL COATING
9X 0852X	MT FOR PRINTED WIRING BOARDS
9A 0851X	MT FOR I.C. ENCAPSULATION

9A0851X MT for IC Encapsulation.

This project will assess newly developed polymeric compounds for integrated circuit protection. Use of plastic encapsulation in fuze circuitry is expected to save 15% over ceramic or metal packages. While AFML will work on semiconductor IC protection, the polymerics may be usable for high quality, high density hybrids.

ELECTRONICS COMMAND ON-GOING HYBRID PROJECTS

274 9656 Beryllia Substrates.

Brush Wellman Co. ground and polished beryllia substrates to a 4 micro inch finish. ECOM intended that they level the material in the slurry state, but Brush decided to use polishing methods because they were cheaper.

274 9411 Silk Screening and Layerizing Ceramic Dielectric Capacitors.

Centralabs is using thick film techniques to build up multilayer ceramic capacitors.

274 9767 Depositing Thick Film Circuits for Crystal Oscillators.

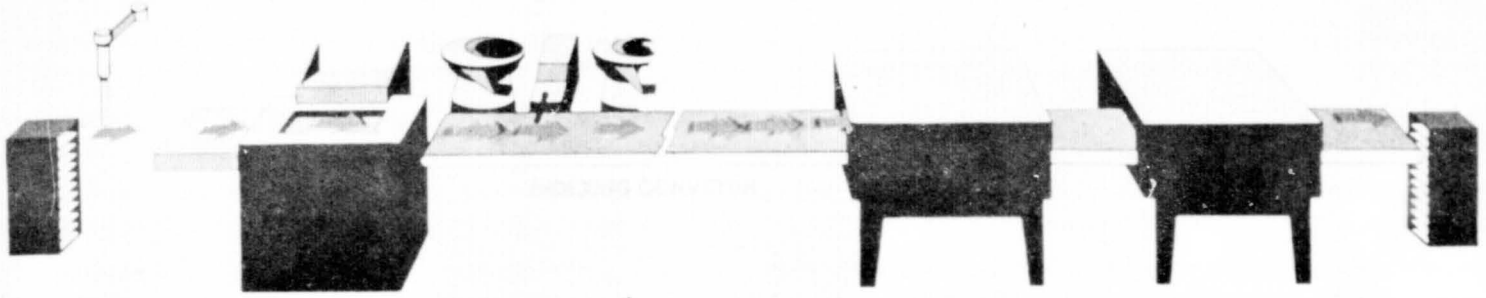
Raytheon is working on fine lines and high quality edges and surfaces for higher frequency work. An oscillator with one mil thick lines was breadboarded.

274 9575 Automatic Assembly of Hybrids for Fuzes.

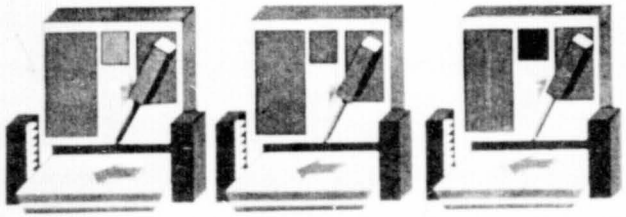
RCA is producing hybrid circuits using CMOS amplifiers for M734 fuzes. A Dixon robot is used to wire-bond the circuit into its package. Circuit prices were cut from $250 for lab models to $10 for production units.

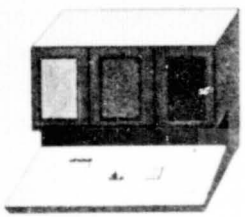
Automated Hybrid Assembly

Passive Component Attach Module (PCAM)

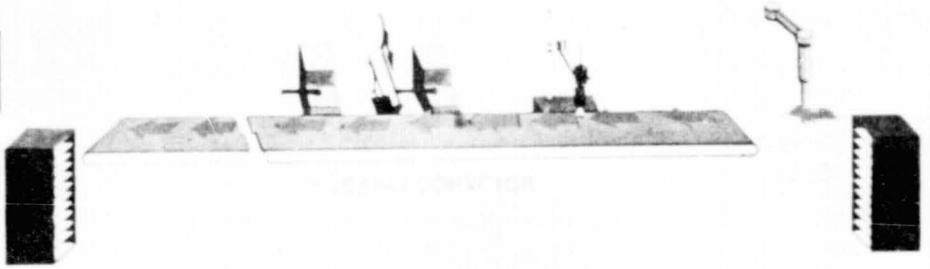


Auto·Bonding System





Active Component Attach Module (ACAM)



RCA Burlington

276 9749 Thick Film Processing of Microwave IC's.

Rockwell International, Collins Radio Division, is working on 3 to 5 mil lines on 6 to 10 mil spacing with high quality surface finish for microwave circuits. Fritless material is used; they are working on a linear amplifier.

276 9766 Depositing High Voltage Insulating Layers on Thick Film Circuits.

Erie Technical Products will varnish selected areas and not the pad areas. Erie built a multiplier on ceramic and it is operating efficiently.

276 9781 Thin Film Transistor-Addressed Display.

Will connect multiplexed input leads to a light emitting diode LED display.

277 9857 Automatic Separation, Carrier Mounting and Testing of Semiconductor Dice.

Will work on automating the entire dicing, taping, testing, and mounting operations. The taped semiconductors can be used readily on hybrid circuits.

277 9808 Automatic In-Process Evaluation of Thick Film Printing and Hybrid Circuit Assembly.

Will employ an image orthicon (TV camera) to scan a film circuit and compare it with a good circuit. Will look for opens, shorts, etc.

277 9835 Integrated Control Circuit for Thin Film Transistor Display.

Will develop mask mounting and changing techniques in a multichamber vacuum system for thin film circuitry. Will adapt methods for cleaning and reinserting masks without disturbing their indexing configuration. Will put peripheral circuitry on display panels.

278 9837 High Density Memory Processing and Packaging Techniques.

Will overcome the high cost of attaching and wirebonding 20 IC memory chips to a hybrid substrate. Will use automatic alignment and bonding equipment to mount and bond IC chips to hybrid circuit substrates. Film carrier bonding equipment will be procured or developed.

278 9869 Rapid Removal of Plastic Encapsulants.

Will vacuum form a thin film of polypropelene over circuit assemblies including hybrids and then foam an encapsulating material over the film. The latter permits easy removal of the foam during repair.

278 9871 Automated Production of Military IC's.

Although this work involves mounting silicon chips on ceramic headers and wire-bonding between the chip pads and the output posts, the equipment and techniques may be applicable to hybrid circuit assembly.

278 9877 Light Emitting Diode Array Common Modules.

Will develop methods for handling ceramic substrates through thick film screening to deposit and bake 180 resistors and conductors, to attach 180 LED's, and to trim the resistors for uniform LED output.

MISSILE COMMAND ON-GOING HYBRID PROJECTS

376 3147 Additive Process for Fabrication of Printed Circuit Boards.

The additive process of plating circuit tracer on boards may be applicable to thick film circuits.

376 3224 Screening of Electronic Components.

Rockwell is developing more efficient screening and inspecting methods. They are looking at less costly test procedures for characterizing component reliability.

376 3227 Low Cost Production Method for Handling Hybrid Chips via a Tape Carrier Lead Frame.

Honeywell will bond inner leads of the frame to the chip, and outer leads of the frame to the carrier. Will burn-in, test, and later attach the carrier to the substrate.

377 3165 Production Processes and Techniques for Sealing Hybrid Microcircuit Packages.

Will establish methods for production sealing large quantities of hybrids. Will look at cap welding, cold welding, seam welding, furnace brazing, and hand and atmosphere soldering.

Will develop a matrix including method, material, and quality of seal.

378 3075 Infrared Testing of PC Boards and Microcircuits.

Will develop an IR testing setup for checking energized PC boards and hybrids. Will use a computer to check a new unit against a proven unit. An IR detector will locate hot spots.

378 3146 Photolithographic Process for Thick Film Multilayer Circuits.

The screening process will be improved by using finer stainless masks to permit 4 mil lines on 8 mil centers. The green ceramic drilling process will be revised to provide 4 mil holes in place of 12 mil holes. The small holes will be plated through to establish "vias." Insulating layers will permit 10 to 12 layers to be laid up with reasonable (50%) yield. Martin obtained 2 mil lines on 4 mil centers in R&D, but with low yield.

378 3165 Production Processes and Techniques for Sealing Hybrid Microcircuit Packages.

This is the second year of a project to establish volume sealing methods for hybrids. Will look at cold welding, seam welding, cap welding, brazing and soldering.

378 3219 Automatic Polymer Attachment Production Methods.

Will develop an automated process for attaching chips to substrates via adhesive bonding.

378 3227 Low Cost Production Methods for Handling Hybrid Chips via a Tape Carrier Lead Frame.

This is the second phase of a two-phase effort to adapt the Eastman Kodak tape carrier lead frame to military circuits. This second year effort concentrates on validating fabrication and assembly methods, cost and specifications data.

378 3254 Low Cost Semi-Flexible Thin Film Semiconductors.

Will apply Computer Aided Design techniques to the design and layout of thin film circuits, and will batch produce them in a vacuum system. FY78 will select thin film evaporation equipment and a CAD setup. FY79 will integrate the equipment and demonstrate the system.

378 3405 Thick Film Microelectronics Processing Equipment for Base Metal Conductors.

Will screen, dry, and fire aluminum conductor paste and barrier pastes. Use of aluminum will reduce the need for gold, palladium, and other noble metal inks.

378 9406 Low Cost Production of Multilayer Hybrids.

Will develop a method of screening on alternate layers of conductors and insulators and then firing the entire circuit. Non-running inks will be needed.

ARMAMENT COMMAND ON-GOING HYBRID PROJECTS

577 3947 Thick Film Hybrid Circuits for M582/M724 Fuzes.

578 3925 Prototype Producing Equipment for Fuze Hybrids.

A volume thick film screening and firing facility at HDL would produce short run high rate production on factory type equipment to prove out the circuitry.

578 3947 Thick Film Hybrid Circuits for M587/M724 Fuzes.

Will select non-noble metal inks and work on ink application for small sized resistors.

Will apply hybrid assembly methods developed by competent firms to the thick film circuitry needed for fuzes that must withstand 20,000 to 30,000 G's shock.

NAVY'S PROPOSED AND ON-GOING HYBRID PROJECTS

DNA 363 Development of Low Cost Thick Film MIC.

Will apply thick film technology and low cost commercially available materials to high volume production of hybrid microwave IC's.

DNA 053 Computerized Thick Film Printer.

Will use a numerically controlled X-Y table with a capillary over it to write the ink directly on the substrate. Is aimed at 4 mil lines. Several firms are already screening on 4 mil lines. Will eliminate the need for artwork and mask sets.

DNA 504 Pilot Production of Improved AIMS Encoder.

Part of work is on a hybrid IC having two MOS chips, 22 transistor chips, and 4 resistor or capacitor chips. Will use gold ribbon bonding. Will concentrate on automatic test methods to check out the hybrid before it is put into the encoder.

DNA 366 High Density Thin Film Hybrids.

A contractor will establish guidelines for thin film hybrids; will include materials, processes, packages, and testing. Will look at selectively etchable multiple resistance layers, air-isolated microbridges, and plasma deposition of monomer films.

DNA 414 Automated Self Test Hybrid Wire Bonder.

First year of a contract at Kulick and Soffa to apply pull test to a wire bonder. Bonder is aluminum ultrasonic bonder controlled by NC.

Will use feedback from pull strength test to adjust bonding parameters as subsequent bonds are made. Will also use pattern recognition to locate the bonding head.

DNA 557 Integrated Circuit Chip Carrier Package.

Will develop sources for ceramic chip carriers for use in hybrid circuits as well as MSI and LSI integrated circuits.

The ceramic carrier employs hybrid techniques in its manufacture: a multilayer ceramic base, base metallization, vias and pads, and a metallized frame and lid.

AIR FORCE ON-GOING HYBRID PROJECTS

71E 08512-8B Microwave Hybrid Processes.

Identifying cost drivers in hybrid processes. Looking at thin films, automated wire bonding, sealing, and automated testing.

78E 08511-8B Standard Electronic Modules for Avionics.

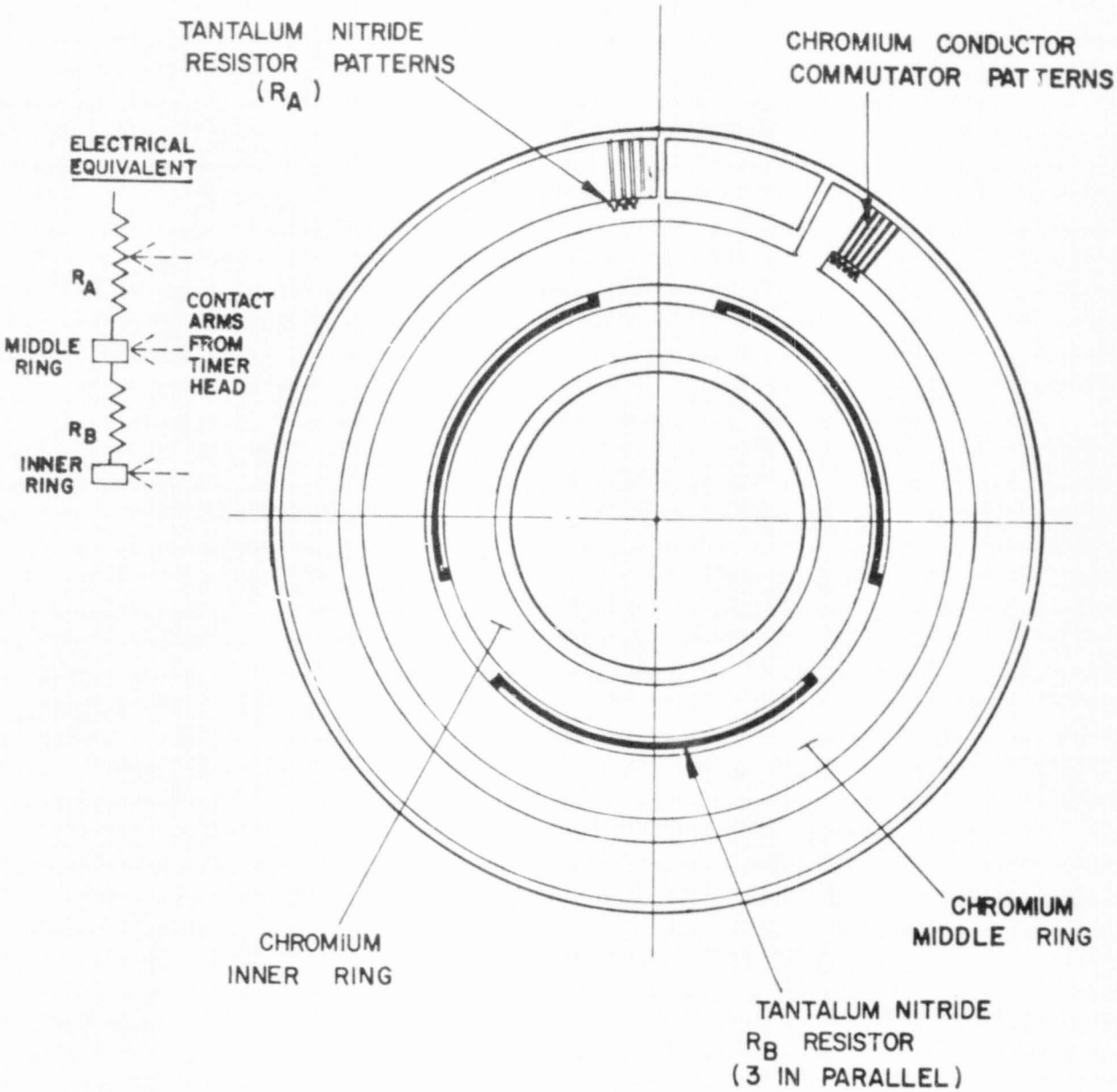
May be some hybrid circuitry involved in the control circuits.

EXAMPLES OF COMPLETED WORK

273 9605 Thin Film Ratiometer.

TRW employed thin film techniques to build ratiometers — concentric potentiometers — in groups of six on pre-punched substrates. See Vugraph. Resistor films are sputtered tantalum nitride, anodized and photo etched into a complex pattern. Conductor films are sputtered chromium, photo etched in concentric pattern. The base is a 2" x 3" American Lava (3M) ceramic substrate which is later divided into six discs after laser scribing. Note the thin film processes here.

RATIOMETER
RESISTOR AND CONDUCTOR PATTERN

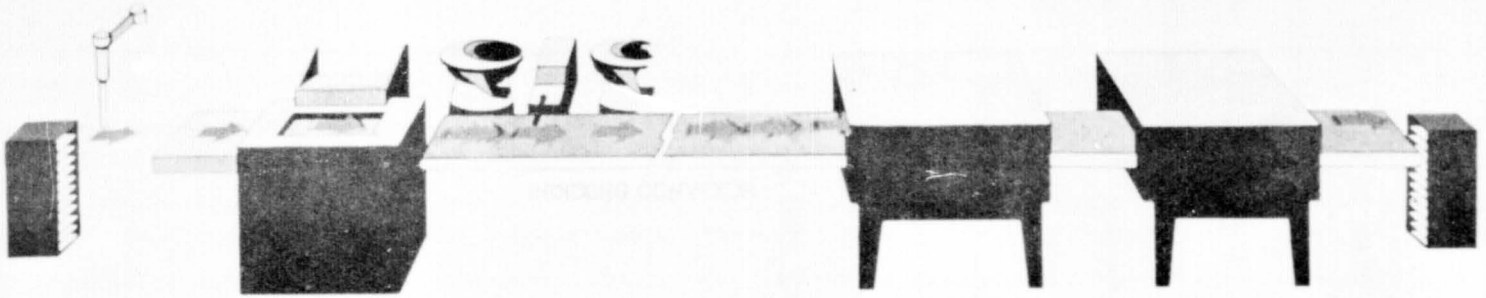


AUTOMATED HYBRID ASSEMBLY

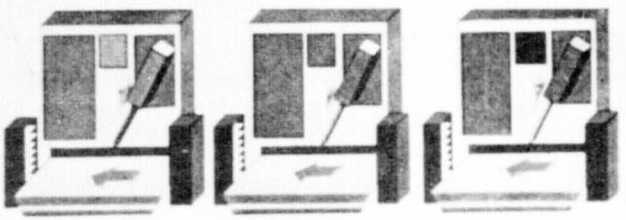
Of particular importance to Harry Diamond Labs fuze component procurers is the automated hybrid assembly facility at RCA Burlington, which is diagrammed here. The capability was put together through a contract funded by Electronics Command. In addition to automatically screening, drying, firing, and trimming the thick film circuitry on the substrate disks, the equipment is set to insert or attach discrete components by solder reflow. The versatility of the line is limited, however, by the pickup heads; more universal type pick, place and attach equipment must be added to make the facility usable on different circuit types.

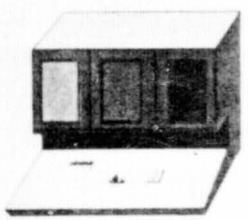
Automated Hybrid Assembly

Passive Component Attach Module (PCAM)

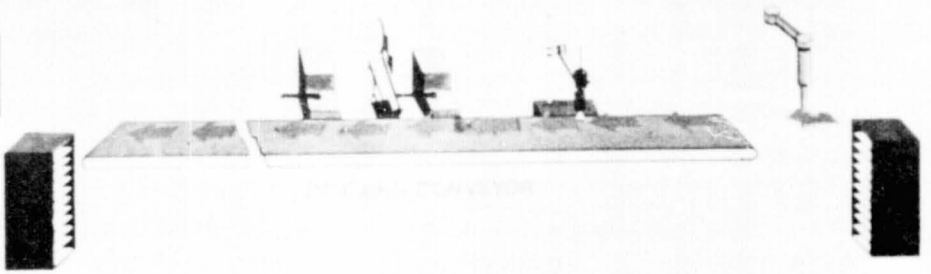


Auto·Bonding System





Active Component Attach Module (ACAM)

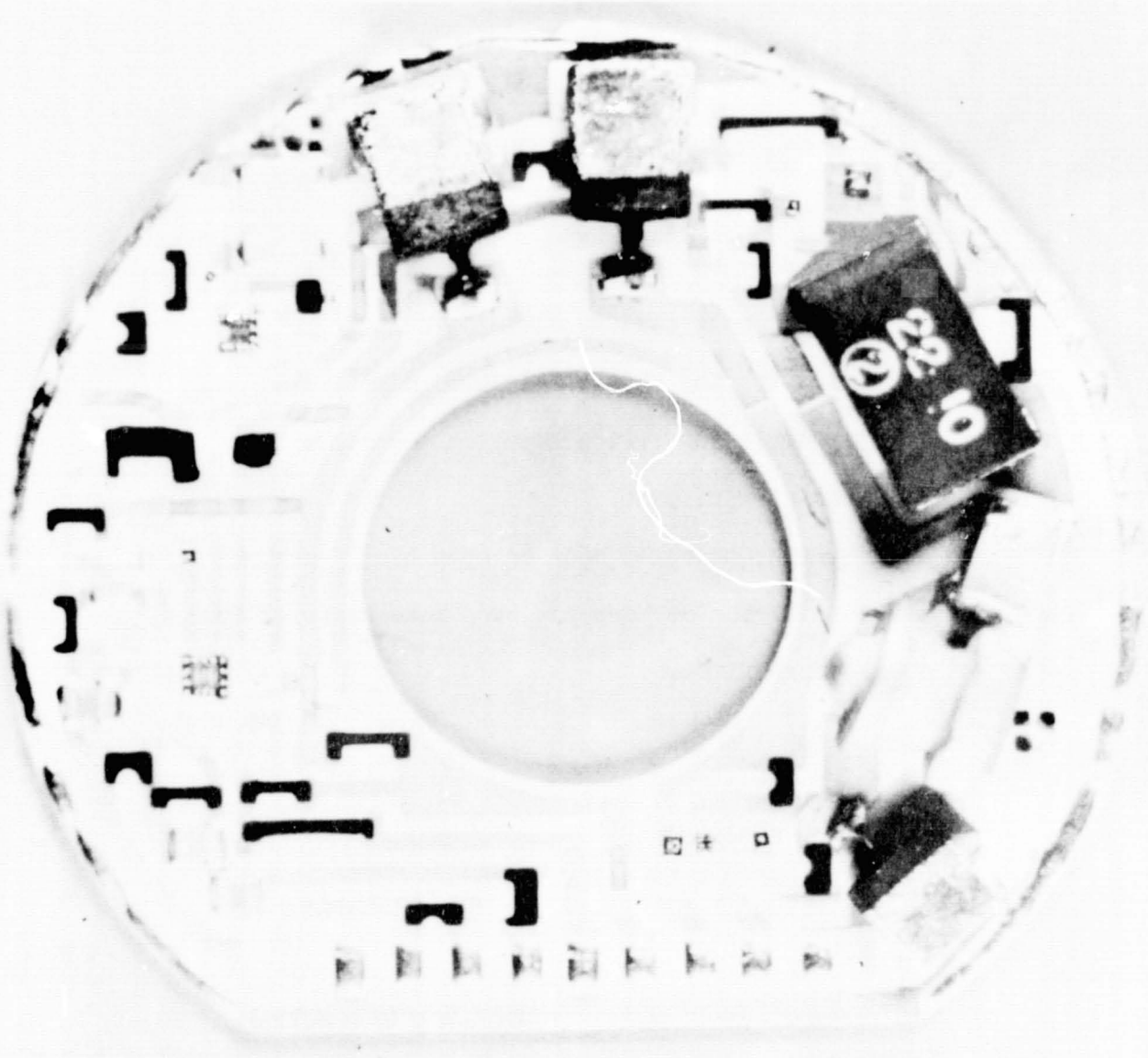


RCA Burlington

AMPLIFIER-FIRING CIRCUIT

A circuit of the type which might be assembled on the automatic equipment shown previously is illustrated here. The washer-shaped disc contains thick film circuitry, several capacitors, and an impact switch. This circuit forms part of the electronics for the M734 Multioption mortar fuze and performs the amplifier-firing function. Another disc contains an oscillator circuit.

This fuze will be procured soon on open bid; Kodak was prime contractor for the development, and subcontracted the electronics to other firms.



CIRCUIT INSPECTION SYSTEM

Electronics Command, in conjunction with RCA, is developing a substrate inspection system that checks the ink pattern on snap-strates before they are fired. This permits easy removal of the inks and rescreening and saves substrates and firing time.

At the left is shown a Return Beam Vidicon which has the capability of viewing the substrates and enlarging any portion of its field of view. Output of the tube is digital and is compared with a stored program obtained from a reference or acceptable substrate. A comparison of signals from the tube and the memory is made in a circuit. A zero output means an identical match, and a quantative output determines the amount of difference. Limits are predetermined to set acceptance limits for the unit under test.

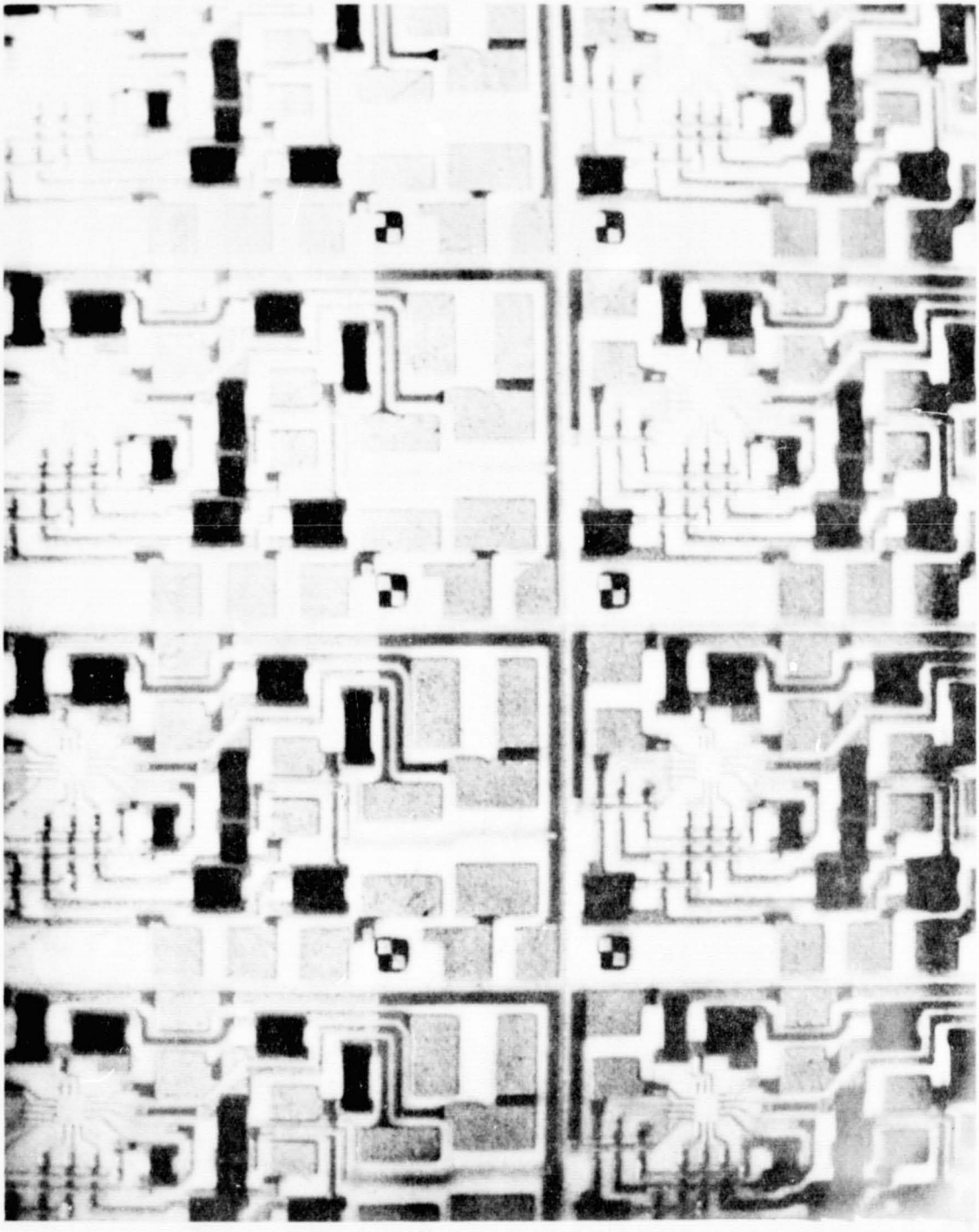
Defective substrates are wiped clean of inks and are rescreened. On a snap-strate having a number of identical patterns, one defective pattern may be recorded and discarded after firing.

This system is designed to save substrates and prevent the firing of defective units.

2779808

TV CAMERA

ENLARGED THICK FILM CIRCUIT



D2

N78-16268

THE ROLE OF APPLICATIONS ENGINEERING IN HYBRID MICROELECTRONICS

C. E. Jones
MCDONNELL DOUGLAS ELECTRONICS COMPANY

I. INTRODUCTION:

Hybrid microcircuits occupy a peculiar place in the electronic packaging spectrum. I suppose that is one of the reasons, among others, that they are called hybrids. This paper addresses itself to that "peculiar place" and addresses the problem of why hybrids are not as widely used as they should be.

Circuit designers and packaging engineers have been familiar with discrete components on printed wiring boards for a long time, twenty-five years or more. Microelectronics as a separately defined area, however, is relatively recent. The packaged integrated circuit, as a standard item did not affect printed wiring board implementation because it is just another component mounted on the board. If discrete components including IC's on printed wiring boards can satisfy a requirement, this is usually the path taken. Custom monolithic devices are usually specified by system engineers. If the circuit function is breadboarded by a circuit designer, and this is not always possible, what the monolithic designer comes up with bears no relationship to the circuit breadboard except by function. A laboratory circuit "breadboarder" would have difficulty recognizing his circuit when he saw the monolithic schematic. Custom monolithics are entertained if non-recurring costs can be justified or if space forces the issue.

Hybrids are a different breed implemented by a different process. Usually they are the last alternative considered for a system and we in ISHM should find out why.

II. THE APPLICATIONS ENGINEER:

1. The need - As stated above, the Printed Wiring Technology is very familiar to designers and monolithic design, at present, is beyond the control of the system and circuit designer.

In the typical program scenario, the responsible design engineer begins his functional layouts or logic diagrams, etc., and directs the electrical and packaging engineers. The physical implementation is thus in the hands of circuit designers and mechanical engineers. The process breaks down into form, fit, and function and there are several iterations to attempt to make everything go into whatever box or boxes the system must fit. If, at this point, discrete components or P.C. cards, in line packaging, motherboards, etc., no matter what monstrous multilayer requirements are put on the P.C. system, no matter what interconnect problems are present, this is usually the way the system is implemented. It's up to the reliability, thermal and environmental people to work their way out of the mess. If at this time space restraints are encountered, that cannot be circumvented, then the microelectronics people will be called. This step usually occurs when the schedule constraints are pushing the system into the panic mode, with little time left in the design cycle to solve the problem with hybrid microcircuits. This is sad. For many prototype units and small production runs, hybrid circuitry is the best solution to the packaging problem. Of course, after prototyping, certain of the functions may be implemented monolithic technologies provided the quantities are sufficient to justify the non-recurring costs. For many limited quantity systems, however, hybrid packages on P.C. cards is the best solution. The reason this hybrid approach is not taken is simply that

users and hybrid fabricators cannot reasonably talk to one another. What is needed is a function between users and fabricators to interpret requirements and see that the requirements are implemented into hardware.

2. Applications Engineering - The successful implementation of hybrid microcircuits requires a function which is not clearly defined in the other methods of implementation. I call this function applications engineering. The engineering service performed is interpretation between the users and the fabricators of hybrids. The qualifications for applications engineers are as follows:

1) Good circuit designer.

2) Total knowledge of hybrid fabrication and test.

3) Good system sense for partitioning the electronic circuit functions into packages.

4) Fully knowledgeable of MIL Specs for hybrids.

5) Also knowledgeable in monolithic and conventional packaging methods.

6) Able to deal with outside suppliers acting as a component engineer.

The applications engineer thus sits between the users and the fabrication group. It is he who must partition the circuitry into packages, choose package types, determine technology such as thick film, thin film, etc. An important part of the task is to determine the impact of hybrid implementation on the circuit performance. Circuit designers will not usually be aware of the impact of the geometry and topology on the circuit performance. In this task it is also important that errors or marginal operation in the circuits be corrected. The applications engineer can perform this review very well. He must also determine producibility, set the acceptance criteria, and test requirements for the circuit. He should determine the trade-off among the technologies for implementation, i.e., the mix of discrete, hybrid and custom monolithic.

3. Reporting - Where the applications engineers report in the organization will have an impact on the effectiveness of the function. Most in-house hybrid facilities are set up as functional organizations because of the necessity to serve many programs. The applications engineering function should report to the head of this operation. Where no in-house capability exists the best place is in the component engineering group since he will be dealing with outside suppliers. If the organization is large enough and versatile enough, then perhaps the most likely position is in an organization including monolithic, hybrid, and conventional packaging so the necessary trade-off decisions can be made, without bias, for the most cost effective packaging methods using a mix of the various technologies.

If the reporting levels are correct, then the application group is usually into the game early enough to determine where hybrids are the best solution to the important system requirements rather than later when things do not fit and time really does not permit an elegant solution.

4. Professional Societies - Something should be said about professional societies. Where does the hybrid applications engineer fit? In my opinion, certainly he must use ISHM for the Materials and Process portions of his knowledge. He will not get much else. PHP and Manufacturing Technology of the IEEE are probably just as biased as ISHM toward Materials and Processes.

III. RECOMMENDATIONS:

1. Organizations concerned with implementing systems into hardware should revamp their present thinking and institute policies which encourage hybrid microelectronics as one of the technologies to be seriously considered

for implementing hardware. This can be accomplished by establishment of a strong microelectronics application group reporting to a level in the organization sufficiently high enough to have influence.

2. The societies which represent microelectronic interests should establish sub-groups on application engineering and should encourage seminars and additions to the literature of microelectronics on this subject.

3. The role of the applications engineer in Microelectronics should be clearly defined both in the industry and in the societies so the visibility to the need is established.

I would like to emphasize that nothing in this paper should be interpreted as criticism of the excellent materials and process work done in this society and other societies. I fully understand the role of the material and process scientist and engineer. However, Material and Processes is one-half of the puzzle. Bad design is just as bad as a bad process, and we will all lose unless both areas are well covered.

D3

N78-16269

MICROELECTRONICS/ELECTRONIC PACKAGING POTENTIAL

Rene F. Sandeau

Martin Marietta Corporation
Orlando, Florida 32805

Electronic assemblies in the 1980's should be an order of magnitude lighter and smaller than the average package being produced today. There may be new technological developments in the near future which will accelerate the process, however the technology is available today to achieve this potential.

The path to the 1980's appears to involve extensive utilization of microelectronics. Achievement of the full potential is almost guaranteed if we couple large scale usage of microelectronics with overall electronic packaging technology. It also appears that total integration of microelectronics and electronic packaging is a logical natural progression. Engineers working in both disciplines are taking off their blinders and developing a broad attitude toward the affect their respective efforts will have on the final product. Also, teamwork is becoming more prevalent among the engineers working in both disciplines and is a welcome and necessary ingredient required to produce the ultimate end product.

What may have appeared as tunnel vision in the past was a necessary step in the total process of evaluation. The vision was necessarily inward in an effort to broaden the base of both technologies. At this point the maturity of both is such that we can take time out to seek innovative methods to utilize our knowledge in ways that enhance the overall end product.

Industry is already feeling the military demand for reductions in volume and weight. System sophistication is steadily increasing at the same time weapon size is decreasing. The challenge will be met, but it is further complicated by the need to reduce cost and maintain reliability.

The trend toward smaller and lighter electronic packages is in full swing at Martin Marietta. Electronic packaging engineers and microelectronic designers are closely associated and give full attention to optimization of both disciplines on all product lines. Also extensive research and development work is underway to explore innovative ideas and make new inroads into the technology base that will satisfy the demands of the 1980's.

HYBRIDS IN THE 1980'S

Common practice today is to utilize hybrid packages integrated with discrete components stuffed in a printed wiring board. It is true that this practice utilizes volume to better advantage than does exclusive use of discrete components. However, thick film technology can be utilized to incorporate entire functional circuits that are contained in unique large scale hybrid packages that fully utilize all available volume.

Large scale thick film hybrids of four to nine square inches in area will become common place. In order to achieve this goal acceptable yields at reasonable cost will be dependent upon several factors. One most important factor is to test all active devices to the fullest extent possible. Second, a pre-lid burn-in and test procedure must be established which exposes all possible modes of failure. Third, adequate rework procedures must be established to obtain maximum yield prior to sealing. A final requirement will be development of a practical lid removal, repair and resealing process to drive yield losses as low as possible.

The packaging engineer will configure the hybrid cases to uniquely satisfy the overall assembly needs. In many cases the large scale hybrid will replace printed wiring boards on a one to one basis. Thus whole banks of printed wiring boards containing conventional discrete components will be replaced by stacks of large scale hybrids.

Establishment of the procedures and processes above will lead to other innovative large scale hybrid assemblies. There will be no reason to package and seal each large scale hybrid substrate in an individual kovar case. Two to a dozen large scale hybrids may be stacked cordwood fashion in a single sealed container with a removable cover. Each ceramic substrate may be bonded to a planar structural support member to provide handling and environmental protection. The overall container will provide glass to metal sealed leads for assembly input/output functions. Since the container cover is removable, the entire stack can be withdrawn for repair,replacement or system changes, and reinserted and resealed.

LEADLESS DEVICES

Individual chip carriers will also see increased usage in some form. The two most popular forms today are the leadless inverted device and the ceramic chip carrier. These carriers offer many opportunities. They can be reflow soldered on ceramic using conventional thick film techniques, or onto other substrate materials utilizing conventional printed wiring techniques.

They offer several obvious advantages. Each active device can be individually sealed and therefore fully tested and burned in prior to assembly, thereby offering high assembly yields. Secondly, they can be removed or repaired by replacement without disrupting seals or requiring burn-in of the total assembly.

Higher usage of these carriers, the attendant yield increases, improved repair procedures and handling ruggedness, without sealed kovar cases will provide reasonable cost tradeoffs with pure thick film technology. It is obvious that die attach in the carriers must be automated. Inner and outer lead bonding to a film tape carrier or its equivalent will provide the low cost die attach necessary to increase utilization.

The conventional printed wiring board will still be with us as a substrate, or motherboard to accommodate smaller substrates containing leadless carriers and associated components. Daughter board substrates may be ceramic with screened resistors or non-ceramic using chip resistors.

INTERCONNECTIONS

The electronic packaging engineer must provide the interconnection schemes to maximize success of the microelectronic marriage. Typical interconnection schemes utilizing standard connectors may in fact size the overall package to the connector volume. A large scale hybrid or substrate containing chip carriers may in fact be smaller than the connector available to interconnect it to other circuit functions. The answer lies in creative utilization of flexible or rigi-flex interconnecting harnesses, thermal compression bonding, miniature stacking connectors or elastomeric connectors. Martin Marietta has fabricated assemblies in prototype quantities containing 480 components per cubic inch. The assemblies used leadless devices and chip components on small multilayer polyimide printed wiring boards. However, this was accomplished primarily due to an innovative interconnection scheme, using a flexible printed wiring harness and totally eliminating conventional connectors.

STRUCTURE

Miniaturization of circuitry permits a corresponding reduction of supporting or protective structure. The total assembly concept changes when weights decrease by an order of magnitude. Adverse dynamic environments can now be handled with ease. Lower individual component mass inherently provides assemblies with much more tolerance to adverse vibration and shock loads. Leadless device assemblies supported by light weight structure have been shock tested successfully without shock isolation to 25,000 g's.

It is also possible to utilize existing structure as a unique electronic assembly. Conventional printed wiring processes have been adapted to metal cored material. As such it is possible to install components directly on formed metal of irregular shapes. Leadless devices can now be reflow soldered to a supporting metal cored gusset or skin containing a printed wiring pattern, therefore eliminating the requirement for separate supporting structure.

It is also foreseeable that leadless devices will be applied to cylinders. This is an excellent opportunity to fully utilize the cylindrical volume of small missiles and projectiles that is presently so wasteful of packaging density. Concentric cylinders containing thick film or leadless devices on the outside surfaces can be inserted one inside the other and interconnected at the ends to provide a unique packaging concept for small missiles and projectiles. Circuitry printed on molded polycarbonate shapes is another distinct possibility.

THERMAL MANAGEMENT

Small highly dense electronic assemblies present another challenge to the packaging engineer. Reduction in size does not reduce heat dissipation,and confined in a smaller volume it demands close attention. Efficient thermal management techniques are a must.

However in most cases it can be handled by use of the proper substrate material or special heat sinks. In extreme cases air movement or cold plates may offer the solution. The metal core printed wiring board, structural chassis or metal cored substrate will provide the required thermal path for efficient management in some applications.

STANDARDIZATION

Do not minimize the subject of standardization. Although left until last, the position does not signify importance. A major goal that must be set and worked toward is that of standardization. The threshold of a totally new hardware concept is the place to begin standardization plans. It is far too late after many different hardware configurations have evolved.

Standardization in both disciplines is long overdue. Large scale hybrids or their equivalent offer a true building block approach. Designers must think ahead to the next program or task and conceive package geometry that is not dead-ended. Custom packages are expensive, therefore designs should permit continued usage in large volume. Standardization is a realizable goal, but only if it is an established goal from the beginning will we achieve the maximum benefit.

All of the technology is available today in which to achieve the concepts described herein by the 1980's, however this technology will not integrate itself. The task can only be accomplished by the teamwork of engineers in both the microelectronics and electronic packaging disciplines.

D4

N78-16270

Comparsion of DoD Tape Automated Bonding Programs

By: Robert F. Unger
U.S. Naval Ocean Systems Center
San Diego, California 92152

Abstract:

Tape Automated Bonding (TAB) shows promise of being the predominant assembly and interconnect technique for microcircuit devices in the 1980's. After briefly reviewing the evolution of TAB, this paper will give consideration to factors influencing and motivating TAB, including current major problem areas. Solutions to these problems are being investigated under five Department of Defense (DoD) programs. These complementary DoD efforts will be discussed and compared. The findings will be contrasted against recent improvements and advancements in automated wire bonding.

Evolution of TAB:

Tape Automated Bonding (TAB) has been evolving since its inception when General Electric announced its Mini-Mod concepts in the mid 1960's. Since then, it has been explored and further developed by others to become the promising processing technology for assembling the next generation of microelectronic devices, both single chip discretes and multi chip hybrids. It is reported that 48 major companies are currently involved in either production or R&D tape automated bonding efforts as illustrated in Figure 1. Appendix A, reference 1, identifies many of the specific companies and factors involved. The feasibility of TAB has thus been well established, but now optiminization of materials, processes, etc., are needed before its potential benefits can be fully realized. TAB is destined to become a universal assembly technology of the 1980's.

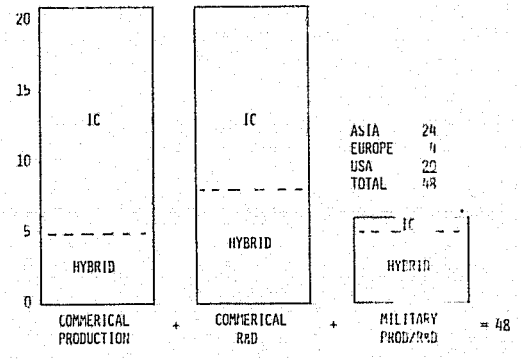


Figure 1. Estimated Number of International Companies involved in TAB for 1977

Figure 2 illustrates the various key factors involved in TAB. The most basic system uses a reel or strip of copper foil which is etched to form a specific connection pattern for eventual mating with bond pads of an integrated circuit (IC) chip. (See A in figure 2). The copper foil concept has the lowest potential cost, but does not permit chip testing later in the assembly process. Foil that has been laminated to a plastic film carrier,

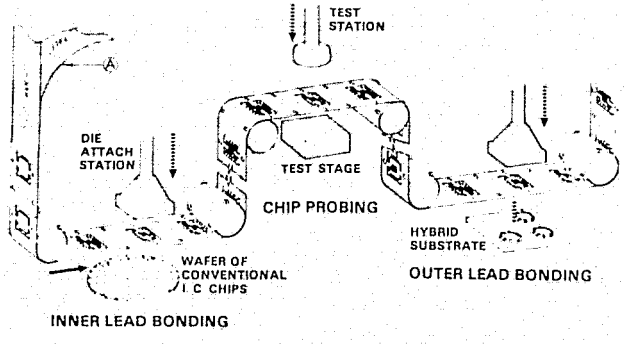


Figure 2. Key Factors Involved in TAB

however, does provide potential means for testing. Each etched foil pattern is classified as a lead frame.

Inner lead bonding (ILB), lower left portion of Figure 2, is usually accomplished via thermocompression bonding (TCB) techniques - the application of heat, time and pressure. This same basic process is used in wire TCB. The major difference with TAB is that all the etched foil contacts are bonded simultaneously to their mating IC bonding pads. To facilitate this bonding step, raised bonding pads or bumps must either be added to the chip or to the lead frame, as illustrated in Figure 3 and 4. The bumps provide the necessary clearance above the chips to prevent contact shorting or damage to the chips. Chips used for TAB are provided from wafers which have been subjected to the customary static probe testing and dicing. ILB essentially initiates the automatic handling and assembly process. Reels or strips of lead frames with chips attached can now be automatically tested and outer lead bond bonded.

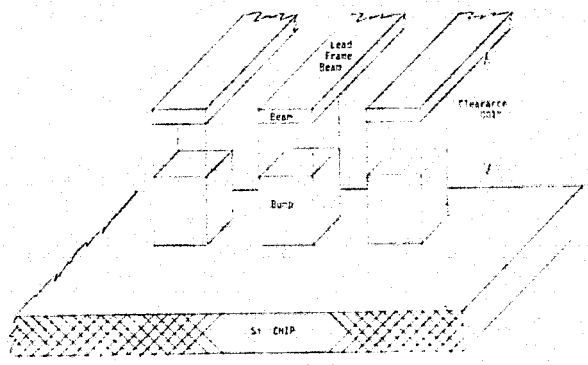


Figure 3. TAB Utilizing Bumps on Chips

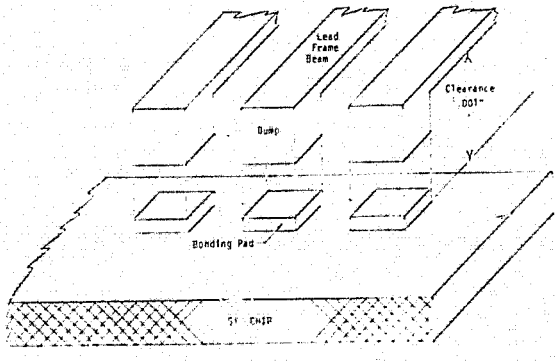


Figure 4. TAB Utilizing Bumps on Tape

The test station shown in the center portion of Figure 2, has the potential for subjecting each lead frame and chip (LFC) to various tests, necessary to provide greater confidence that the chip will function satisfactorily after final assembly. These may include dynamic testing, temperature stressing, automated computer comparsions, burn-in, etc.

Outer lead bonding, illustrated in the right side of Figure 2, separates a portion of the LFC and bonds the extended metal foil pattern or contact beams to mating bond pads on a substrate or discrete package frame. Thus, Figure 2 shows in sequence form how TAB will automate handling, bonding and testing. The potential rewards of TAB are great for reducing costs and for improving yield and reliability. The DoD programs to be discussed later will relate positive methods for achieving full TAB potential by addressing problems yet to be resolved.

Wire Bonding:

TAB technology essentially is a replacement or alternative for wire bonding, therefore, current wire bonding factors are generally used for a base line comparsion with TAB. Figure 5 illustrates

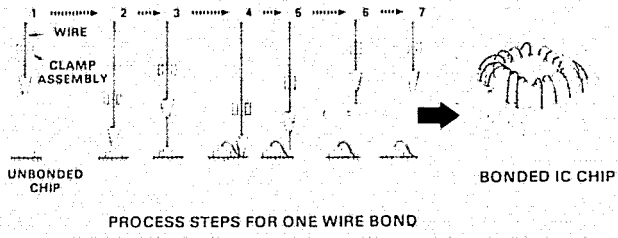


Figure 5. Wire Bond Process Sequence

seven separate steps necessary to make the two bonds required for each wire. Currently, the hybrid wire bonding rates vary from 800 to 1800 bonds/hour for manual operation and 10,000 to 13,000 bonds/hour for automated pattern recognition type bonding. The important benefits offered by wire bonding are:

1. Flexibility - can be bonded to practically any chip,
2. Low Material Costs - cost of the wire, and
3. Minimal Non-Recurring Costs - does not require special tooling and mask charges for each separate chip, which is the case for TAB.

The main disadvantage of wire bonding is the number of individual steps involved to bond a chip to a hybrid. Each DoD program compares TAB cost, reliability, yield and other factors with the wire bond assembly processes.

Influence Factors:

There are four major factors with have influenced or prompted the DoD programs:

1. Chip related failure,
2. Wire bond related failure,
3. Device yield, and
4. Insufficient reliability

Figure 6 illustrates two of these major failure modes, reference 2. Portion (a) shows that for those hybrid devices that failed during in-process assembly, 60% of those that failed were due to active device failures; i.e. inoperative, wrong type or damage chips during assembly, plus diagnostic errors. Wire bond failures attribute to 23% of the failures, specifically caused by loose, broken, incorrect or missing wires. For example, if 10,000 devices are processed and 100 devices fail during processing, 60 would be due to device related failure and 23 due to wire bond related failures. TAB has the potential to eliminate those two failure related factors, a definite motivation force for DoD efforts.

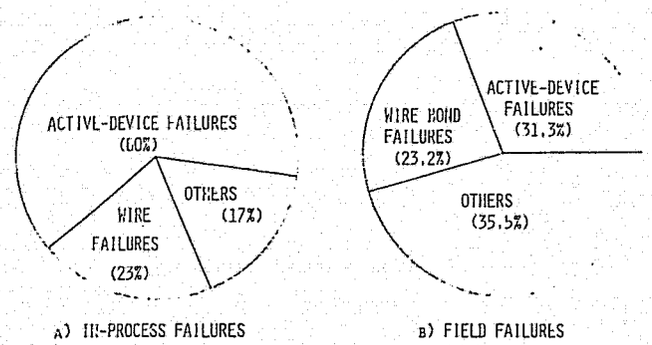


Figure 6. Major Causes of Hybrid Failures

Failures occurring during in-process assembly many times effect yield and are reflected in cost, since often it is necessary to fabricate more devices than required to compensate for those that fail during assembly and test and can not be reworked. In addition to the yield factor fault isolation must also be considered, because it can be an even greater cost item. Fault isolation to determine which IC chip is bad and which wire bond is defective can be very costly, and often exceeds the total assembly costs of a hybrid device. Again, TAB has the potential to eliminate many of these costly failure factors.

Portion (b) of Figure 6 shows the cause of those devices that failed in the field after successfully passing many specified MIL-Std screens. It indicates that screens are not 100% effective and other techniques are needed. TAB could be the answer by providing more effective test methods and provide the reliability urgently needed.

Chip yield, another powerful influencing factor, is shown by Figure 7.

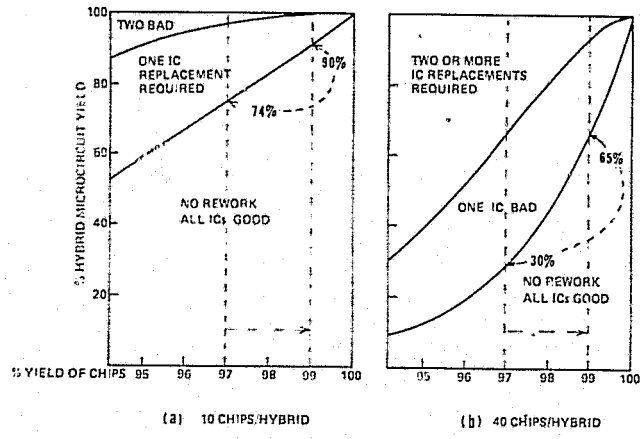


Figure 7. Chip Yield Dictates Hybrid Yield

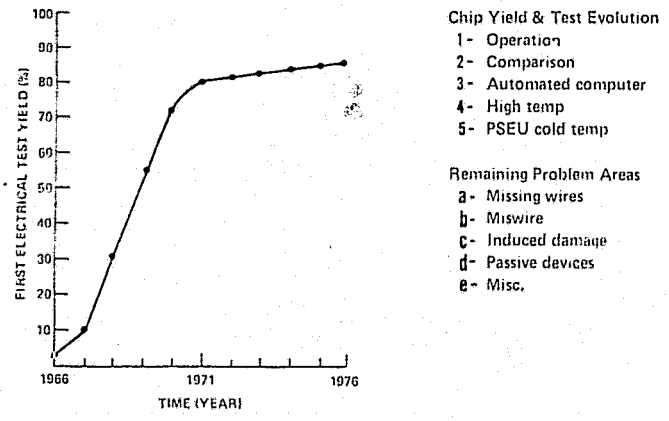


Figure 8. Hybrid First Electrical Test Yield History

To clarify this illustration, observe the dotted line above 97% in portion (7a). It shows that for a hybrid with 10 chips, 74% of the hybrids processed will have all good chips and will not require rework. However, 26% of the hybrids will require one or more chip replacements and of that 26% - 4% will require 2 or more replacements. Each chip in the above example has a 97% probability of functioning correctly in the hybrid circuit. TAB, through the use of dynamic chip testing, stress testing, burn-in, etc. can easily improve chip yield to 99%, thus improving hybrid yield from 74% to 90% as indicated. Examining portion (7b) under the same conditions shows that TAB has an even greater impact on yield when the complexity is increased to 40 chips. In this situation, TAB will increase yield from 30% to 65% --- a significant factor. Figure 8 further verifies the influence of chip testing over yield, reference 3. Items 1-5 of Figure 8, identify the evolving factors which eventually resulted in the indicated 85% yield. TAB can perform all five factors automatically, thus improving the current semi-automatic method. The factors a-e account for the remaining 15% yield. TAB also has the potential of reducing or eliminating factors a, b, and c.

Problems:

It has been shown thus far that TAB is a viable solution to current IC/Hybrid problems, but further development is required. The major problem areas to be resolved are:

Cost
Yield
Reliability

and the specific assembly factors to be addressed by the DoD efforts are:

Reduce bond failure
Reduce IC failure
Reduce handling failures by automation
Select and optimize TAB materials
Optimize TAB processes and specifications
Optimize testing and quality control techniques
Reduce non-recurring costs
Develop multi-chip type assembly techniques
Develop mass production techniques
Document reliability and cost
Standardization
Implement into DoD systems
Disseminate information to stimulate competition

DoD Programs:

There are five DoD efforts directly related to TAB and are summarized in Table 1. Note that each is concentrating on a

Programs and Key Factors	Activities	Bumped Chip	Bumped Tape	Start	Complete
IC Chips Tri-Metal System	Navy/NOSC-RCA	X		2/76	2/77 3/78 10/78
Hybrids Materials	Army/ECOM Honeywell	X		7/76	4/77
Hybrids Processes & Specifications	Army/MICOM Honeywell	X		7/76	12/77 12/78
Hybrids Mass Production	Army/ECOM Honeywell	X		6/77	9/79
Hybrid Missile Implementation	Navy/NOSC		X	9/77	1/79

Table 1. DoD Tape Carrier Complementary Programs

different key element. The five fields of emphasis are: the development and implementation of a tri-metal system for chips, the evaluation and selection of materials, the development of basic processes and specifications vital to hybrid assembly, the institution of mass production techniques, and the utilization of the broadened technology for a missile system. Therefore, in essence, they are complementary programs and the results from one program greatly benefits the others. Table 1 also lists the starting and completion dates, which indicates that much of the work is still in progress. However, sufficient data is available for a brief discussion of each.

Navy/NOSC/RCA Program:

"High Reliability, Low-Cost Integrated Circuits", (Contract Number N00039-76C-0240) has three major phases. Phase one is the development of process feasibility, process development and automated assembly. Phase two is devoted to quantity fabrication of eight selected different IC types. Phase three involves reliability analysis and verification.

The objective of this program is to investigate alternate approaches to MIL-M-38510 for achieving high-reliablity integrated cirucits at low cost. Emphasis is on adapting existing technology to industry mainstream products to achieve a reliability level of 0.005%/1000 hours at 125 with a 60% confidence level, a level that will meet military requirements without a cost penalty in excess of 20% over the cost of commercial, high-reliability plastic-packaged devices.

The approach to achievement of the goals of this program will be the integration and application of existing sealed-chip integrated-circuit processing with automated plastic packaging. In comparing this effort with other DoD programs the major difference is that this is the only program devoted to IC chips, or single chip discretes, the others concentrate on hybrids. The RCA chips are specifically developed for bumping using the tri-metal system illustrated in Figure 9. Note the unique passivation

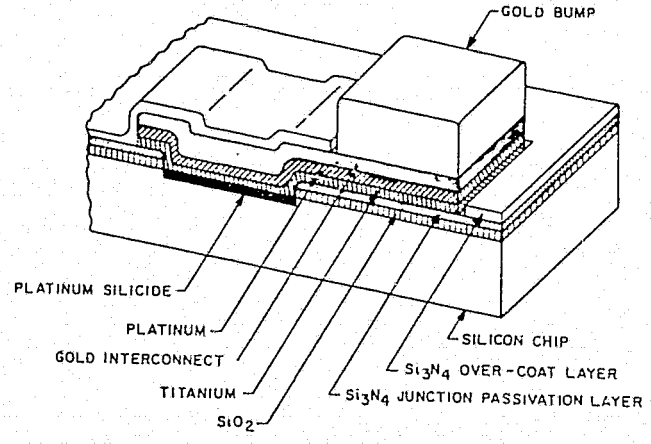


Figure 9. Navy/RCA Tri-Metal Bumped Chip

layers. These plus the plastic package provide protection for the chip.

Table 2 shows a cost comparsion of three different methods identified as systems A, B & C for assembling a CA 741 type device. System B serves as the base

System Number		I		II	III
System Processes	Passivation	SiO_2		SiO_2	Si_3N_4
	Metallization	Aluminum		Aluminum	Trimetal
	Dielectric overcoat	CVD PSG		CVD PSG	Si_3N_4
	Device bonding	Wire		Wire	Beam tape
	Assembly	Manual		Manual	Automated
	Packaging	Hermetic ceramic		Plastic	Plastic
Relative Cost Factors	Wafer process through passivation	15		15	15
	Metallization	2		2	6
	Dielectric overcoat	2		2	2
	Separation	11		11	5
		White	Frit seal		
	Assembly	250	65	48	22
	Encapsulation and test	38	30	22	22
	Total relative cost	318	125	100	72

Table 2. Navy/RCA Relative Cost Comparison for CA 741 Device

line wire bonding comparsion standard. Note than the total relative cost for system B is 100. The column on the left of system B, is system A, where the assembly involves hermetic ceramic packages. Note the relative comparative assembly cost of 250 as compared to 48 for system B. Now focus your attention to system C, where the assembly techniques involve TAB and plastic packages. Here the overall total relative cost is only 72, and the relative assembly costs, which included TAB, is only 22 - a substantial savings. The other major saving for system C involves die separation. This refers to separating the wafers into individual IC die. System C uses a diamond saw technique while the others use the scribe and break technique. Thus when volume production is ultimately developed and analyzed, system C should prove to be a viable solution to the major DoD goals; to reduce cost, and to improve yield and reliability. Figures 10, 11 and 12 serve to further illustrate accomplishments under the DoD program.

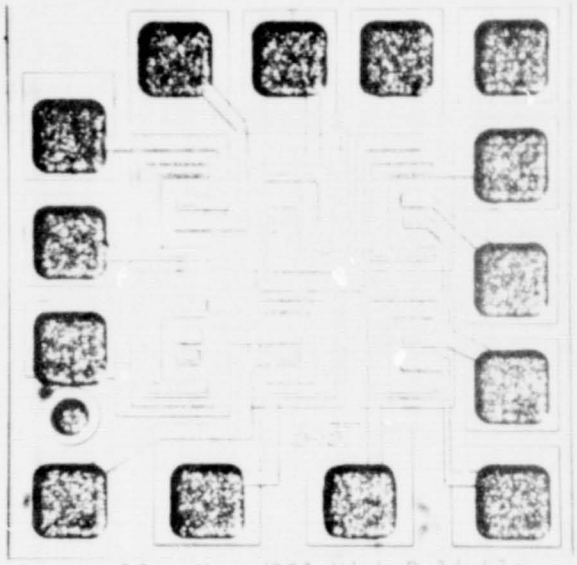


Figure 10. Navy/RCA High Reliable, Low Cost Bumped Chip

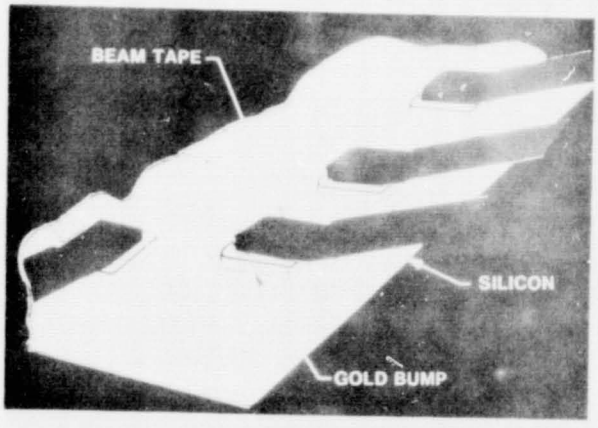


Figure 11. Navy/RCA Bumped Chip Bonded to Beams

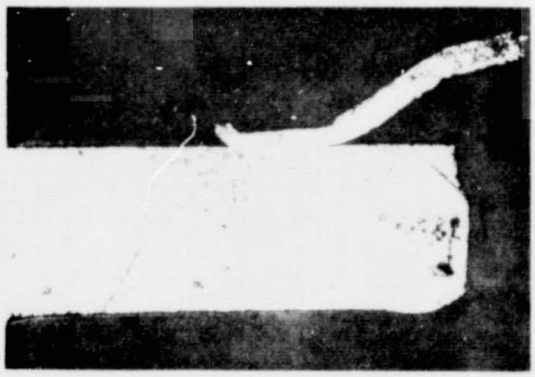


Figure 12. Cross-Section of Navy/ RCA Bonded Lead

Army/ECOM/Honeywell Program:

"Tape Chip Carrier for Hybrid Microcircuits", (Contract Number DAAB07-76-C-1401)

The purpose of this program is to select a suitable material system and establish the associated fabrication techniques to handle and test semiconductor chips and to assemble the chips into hybrid microcircuits. The objective is to replace wire bonding techniques in ECOM hybrid microcircuits by the Tape Chip Carrier (TCC) technology.

The program involves the bumping of conventional chips using the selected Ti-Pd-Au metal system as illustrated in Figure 13. The gold plated bump is one mil

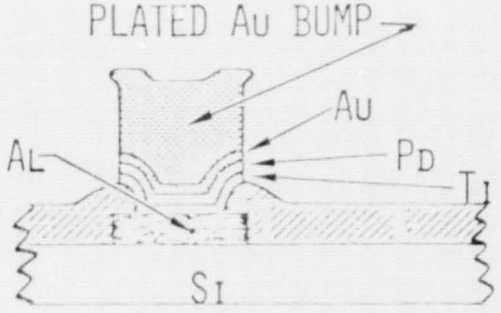


Figure 13. Army/Honeywell Metal System for Bumped Chips

(0.001") high. Other specific areas involve:

Plastic carrier materials
Metal system for carriers
Mechanisms for bonding

The final report of their R&D effort will be released shortly and will disclose the results of this program in more detail.

Army/MICOM/Honeywell Program:

Army/ECOM/Honeywell Program, Contract Number DAAH-01-76-C-1079, is titled "Production Methods for Handling Hybrid Chips via Tape Carrier Lead Frames."

The main objectives of this program are to develop processes and specifications for TAB that can be applied in fabricating missile systems. The key factors involved are:

Industrial Survey

Critical Processing Areas
- tape fabrication
- substrates
- die separation
- wafer metallization, bumped chips
- inner lead bonding
- outer lead bonding
- die testing & inspection
- rework methodology

Cost Analysis

Reports on this program are forthcoming and will reveal in detail the results and accomplishments of this program.

Army/ECOM/Honeywell Program:

Army/ECOM/Honeywell Program involves the development of mass production hybrid assembly techniques using TAB (Contract Number DAAB07-77-C-0526). The key factors involved are:

Technologies
- bumped chips-thick film substrates

Gold plated copper lead frames
reels or strips

Automated chip carriers
bonding
placement
testing
burn-in

Passivated IC's devices + dielectric overcoat

Pkg to provide mechanical protection
not hermeticity

Automated gold wire bonding
Used where TAB is uneconomical

Standardization

Demonstrate pilot production runs
government and industry

Note that this program also includes provisions for implementing automated gold wire where TAB assembly techniques prove to be uneconomicial. Also note in Table 1 that the program just started in June 1977, so only the preliminary data listed above is available at this time.

Navy/NOSC Program:

The prime objective of this program is to reduce the costs of hybrids used in a missile system. It differs greatly from the other DoD efforts by using a modified TAB technology termed Bumped Tape Automated Bonding (BTAB). In this approach the bumps are processed on the lead frame contacts as illustrated in Figure 14. Since all TAB approaches require special design and etching of lead frames for each chip type, adding the bumps to the lead frame eliminates the necessity for art work and processing to bump the chips, thereby reducing costs. In addition, since conventional chips can be used without added special processing, a greater variety of chip types can be utilized. The key

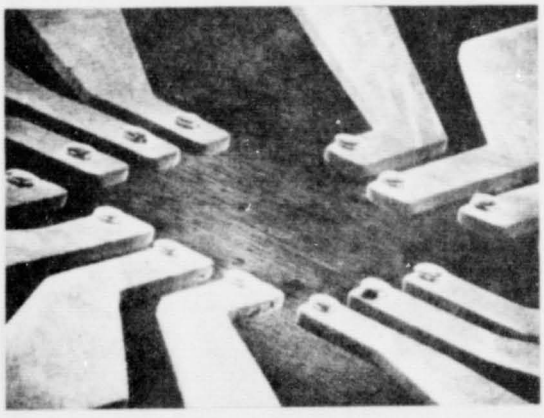


Figure 14. Bumps on Tape courtesy of General Dynamics

factors addressed by this program are:

conventional IC chip
bumped tape
reliability and quality assurance
multi chip type assembly techniques
non-recurring costs
chip testing prior to hybrid assembly
implementation into missile systems
cost analysis and verification
dissemination of information to stimulate competition
industry wide demonstration

Special attention is given to the factors dealing with multichip assembly techniques and non-recurring cost. To explain their great significance, consider the following example. It is desired to fabricate 200 hybrids, each containing an average of ten different chip types. This presents two major problems;

1. the non-recurring cost for each chip type - to provide tape masks, die masks and tooling; and
2. the technique for the cost effective assembly of the different types of chip.

Currently, the non-recurring costs for each chip ranges from $1,200 to $5,000.

For the above example it may require $5,000 x 10 = $50K to be amortized into the cost of the 200 hybrids. This gives rise to the possibility or necessity of reducing non-recurring costs or applying TAB/BTAB only to quantity production runs. Chip testing techniques developed by the DoD efforts could possibly be implemented with automated wire bonding - as was previously mentioned during the discussion of Army/ECOM/Honeywell program.

Assembling the 10 different chip types into a hybrid is the other consideration. When chips are die attached to substrates for wire bonding, the fact that they may be of different types is no major problem. But when TAB/BTAB is the assembly technique, the lead frames and chips are in reels or strips and may require multi-bonding units, changing of tooling, or some method yet to be developed. Therefore, considerable effort will be devoted in the DoD hybrid TAB programs to find a cost effective assembly technique where a variety of difference chip types are involved.

Figures 15, 16 & 17 illustrate the feasibility of the BTAB approach.

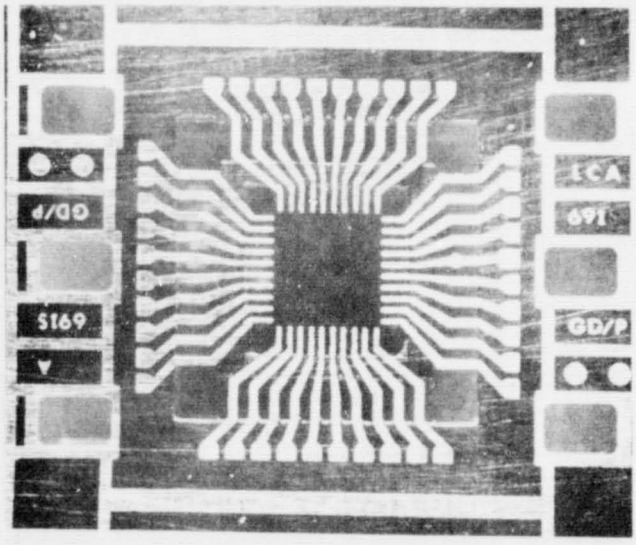


Figure 15. Lead Frame for BTAB courtesy of General Dynamics

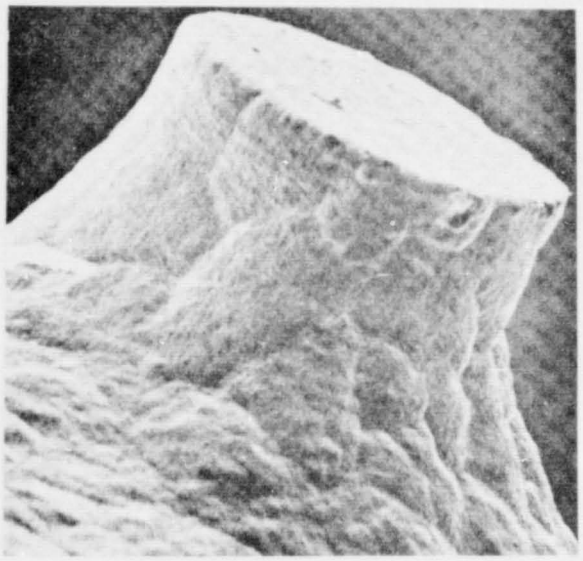


Figure 16. SEM of Bump Tape courtesy of General Dynamics

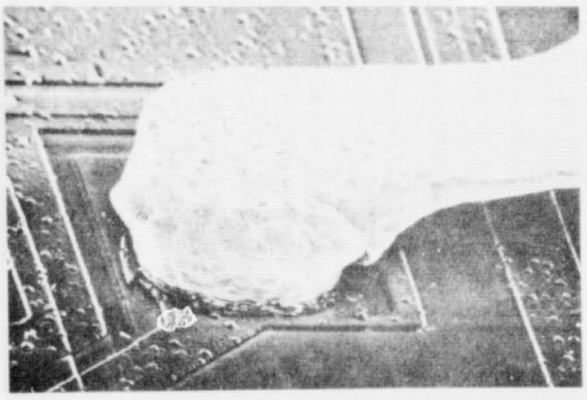


Figure 17. Bumped Tape Bonded to IC Chip courtesy of General Dynamics

Conclusions:

It has been shown that TAB and BTAB are viable, maturing technologies. Each shows great promise of resolving the major DoD goals; to reduce cost; to improve yield and to improve reliability. The complementary DoD efforts are destined to expedite benefits of TAB/BTAB into military systems. In addition, the DoD efforts will assist greatly in assuring that TAB/BTAB will be a major factor in microelectronics for the nineteen eighties.

References:

[1] Comparative Use of Gang Bonding Systems; Courtesy International Micro Industries, P.O. Box 604, Cherry Hill, New Jersey 08003

[2] R.P. Himmel and I.H. Pratt, "Analysis of Hybrid Microcircuit Failure Modes", Proceedings ISHM Symposium, pp. 347-352, 1976.

[3] H.L. Obright, "Electronic Testing of Bare Silicon Chips Prior to Hybrid Fabrication," 27th Annual Proceedings, Electronic Components Conference, Arlington, Virgina, pp. 141-145, 1977.

MILITARY REQUIREMENTS FOR MICROELECTRONICS - VIEW FROM THE FIELD

BY

LAWRENCE B. RESIDORI
LTC USA

This report represents the views, conclusions and recommendations of the author and does not necessarily reflect the official opinion of the US Army Missile Research and Development Command, the Department of the Army or the Department of Defense.

D5

INTRODUCTION

During the past decade, the field of military as well as commercial application of microelectronics has grown by leaps and bounds. The Department of Defense has been a key driver in expanding the state of the art by generating requirements for highly sophisticated electronic equipment to meet an ever increasing threat to our nation's security. Development of equipment to meet these requirements pushed the state of the art and placed a premium on innovative electronic designs. Cost to develop these systems took a secondary role to technology while operating and support costs as well as operation in a tactical environment were given only minor consideration. However, the climate today has changed dramatically and cost has become the major driver in system acquisition. This was aptly stated in an article in Electronics Magazine which noted.

> "Design-to-price--the Government's low price--is the chief bugaboo for engineers anxious to deploy their latest innovation throughout the military establishment. 'If they can't prove the costs to build and maintain, and guarantee its reliability, we don't want it,' says a specialist in the Directorate of Defense Research and Engineering (DDR&E)."[1]

In light of this recent change in the DOD climate, we have reached a point in the development of microelectronics where we need to pause, look forward, and ask "Where do we go from here?" The purpose of this paper is to reflect on that very question from the eyes of the military developer who must insure that a system is developed which cannot only meet the threat but can be operated and maintained in an economical manner in a field environment. Thus let us examine the military requirements for microelectronics with an eye towards its ultimate use on the battlefield.

FIELD ENVIRONMENT

In order to maintain a proper perspective, developers of microelectronics for military application must keep in mind the ultimate environment in which the electronic equipment will be utilized. In order to illustrate, let's look at the environment of a typical mobile Air Defense Missile System during combat.

The system is deployed forward in the division area where it moves over all types of terrain in all conditions of weather. Its tracked vehicle provides the mobility to keep up with rapidly advancing armor units. The crew operates around the clock maintaining vigilance monitoring the search radar display. Continued operation slows their reflexes and thought processes slowly diminishing their effectiveness. Rugged terrain causes severe shock and vibration to be transmitted to the systems electronic components. Missile resupply vehicles move slowly over the rugged terrain with their cargo of missiles exposed to the elements. Support test equipment vehicles move slowly over the roads to keep up with the advance elements to insure responsive supply and maintenance support. Maintenance crews are weary due to the continuous road marches caused by the fluid front. Maintenance personnel with soldering equipment work long hours repairing printed circuit boards needed to return fire units to a serviceable condition. Other maintenance teams canabalize a fire unit disabled by a direct hit from an enemy munition, parts are removed to replenish parts stocks depleted by the previous day's air battle.

Electronic repair parts are stored in bins in the supply vans where temperature soar to 125+ degrees. To the rear missile stocks are stored under canvas to protect them from the tropical sunlight.

This montage depicts some of the typical conditions an air defense missile system will face at some time in its life cycle. All the conditions described may not occur simultaneously. However, when any of the conditions do prevail, system availability will surely suffer. Climatic factors will result in increased probability of failure. Weariness of crew and maintenance personnel will exact its toll on system readiness through errors which result in equipment down time. These are some of the factors which cause fielded equipment to demonstrate lower levels of system availability than predicted during development. It is these conditions that equipment designers must keep continually in mind when developing equipment for use in the field environment.

REQUIREMENTS

Based upon the field environment depicted and the continued Department of Defense emphasis on reducing life cycle costs, a number of military requirements for microelectronics become readily apparent. Some of these requirements are inherent in microelectronics and are simply reiterated in this paper as a reminder of their importance and to suggested possible improvements for the future.

High Reliability. It is well understood that high reliability is an important characteristic of microelectronics circuits. However, it is an area that requires continual improvement to insure that reliability in the field is raised to much higher levels than is being achieved today.

The emphasis within the DOD is best summed up by the following statement:

> "There has always been emphasis on designing reliability into a system to meet operational mission needs, but only recently has similar emphasis been placed on system design reliability to meet O&S cost needs. This new emphasis developed when it was perceived that major weapon system complexity was leading to poor field reliability and that O&S costs had increased substantially."[2]

It appears ironic that such could occur, however, when the total field environment is considered one can well understand why field reliability is poor. Thus, a continual effort must be undertaken to insure that reliability improvements such as those listed below are investigated and implemented in microelectronic circuits.

- o Application of redundancy
- o Improved methods to interconnect circuits
- o Improved manufacturing processes
- o Better control of moisture

Efforts in these and other areas will contribute significantly toward the Service's goal of increased field reliability.

Expanded Built-in-Test-Equipment (BITE). When an electronic system fails, it becomes a crucial matter for the crew to restore the system in a minimal amount of time (i.e., under 30 minutes). The BITE must be simple and accurate and should allow the crew to isolate and repair 90-95% of all system malfunctions. This must be accomplished by the typical crew utilizing a repair manual written to a 5th grade reading level. One can recognize that proper electronics design techniques are required to obtain the required BITE capability and to insure that the BITE circuitry does not constitute an inordinately large percentage of

the system electronics. Designers of microelectronics must insure that components replaceable by the crew are designed such that BITE can readily and rapidly isolate most any given fault. The importance of and the need for properly designed and simple to operate BITE cannot be over stressed. Rapid and accurate repair at the organizational level is essential in maintaining a high level of operational readiness. An example of what can and will happen if BITE is not accurate and simple to operate was illustrated in an Air Force evaluation of the F-14 wherein it was reported that,

> The final analysis of the PSE indicated that approximately 23 percent additional Direct Maintenance Manhours (DMMH) were due to unverified faults . . ."[3]

These were indications which the crew suspected to be faults and when significant number of manhours were consumed attempting to correct them only to discover that they were not true faults at all. Properly designed BITE utilized to test properly designed microelectronic circuits can reduce this problem significantly thereby reducing the associated O&S cost.

International Standardization. Standardization is an attempt to minimize the number of items in the military inventory by developing items which can be used in a multitude of applications. Just recently the Department of Defense has undertaken a program to transfer European technology to build a complex electronic system in the US. One problem raised by this effort was the fact that, in some cases, a European component mounted on a printed circuit card could not be replaced by a US component which functioned in an identical manner. This was due

to the fact that US and European components were not constructed in a standard configuration to allow interchangeability. It appears that future cooperative development and production programs with European countries will be on the increase. To simplify this process, microelectronic manufacturers should proceed to develop international standards for microelectronic devices and then pursue a course to establish a mechanism to insure compliance by all countries involved. Such a program will help assure common configuration at the piece part repair level thus allowing full benefit to be derived from joint logistics strategies. Such benefits can be significant as Mr. R. E. Bredenbender reported in the Defense Management Journal when he stated that "...there can be little doubt that standardization can mean big savings."[4] One fine example of what can be accomplished is evident in the Raytheon developed "PATRIOT" air defense system where the RAY-PAC has been developed as a standard microelectronic circuit and used in multiple applications throughout the system. Similar efforts on a national and multinational basis can make a significant impact on O&S costs and open doors to international cooperation heretofore unheard of.

Ease of Repair. The Services have, over the past decade, strongly emphasized the need for improved maintainability in military equipment. This emphasis has resulted in major advances such as plug-in/plug-out modules, extensive built-in test, and improved maintenance technical documentation. As a result, prime system hardware of most of our modern military systems display very sound maintainability design. However, it

appears that little consideration of maintainability in design has occurred at the printed circuit card level. Most printed circuit cards present severe challenges to the repairman in the field. The concern over allowing printed circuit card repair of missile systems in the field was such in the US Army Missile Command that a policy was instituted some years ago which stated that no printed circuit card repair would be allowed in the field. Thus all electronic printed circuit cards had to be returned to US based depots for repair. Such a policy requires an increase in the supply pipeline quantities in order to maintain operational readiness. Printed circuit cards designed to facilitate repair in the field can lead to a reduced pipeline, more rapid supply response, and possible reduced O&S costs. Some items that should be considered in designing maintainability into printed circuit cards are:

- o Utilize innovative packaging and mounting techniques which allow defective components to be easily removed and replaced.
- o Reduce the amount of soldering/unsoldering required to effect repair.
- o Minimize the use of hard to remove epoxies and conformal coatings.

Maintainability design of repairable printed circuit cards and modules will reap great benefits in the field in the form of increased system availability.

Throw-Away. Over the past years, the services have had varying degrees of lack of success with so called "Throw-Away" logistics concepts. In such a concept, certain repair parts are categorized, due to low cost and low failure rate, as throw-away. That is, when the part fails in the system it is removed and replaced by a serviceable part and then thrown

away rather than repaired. This type of maintenance concept has an appealing aspect to it in that it could, if properly implemented, result in a reduction in the numbers of repair technicians required to support a fielded system. The past failures appear to be a result of three characteristics. First, the candidate item for throw away was too expensive and thus the economic soundness of the concept became questionable. This was exacerbated by the fact that the failure rates in the field environment were significantly lower than in the projections arrived at by the contractor. Secondly, adequate test equipment was not provided to allow verification that the part removed was actually unserviceable. Consequently, numbers of serviceable parts were discarded with a significant impact on the repair parts stocks. Finally, the throw away items were designed in such a manner that they could be repaired. Thus, repair personnel found it extremely difficult to throw the item away when they knew it could be repaired and that it may be difficult to get a replacement item through the supply system. It appears that a selective throw away policy would be extremely beneficial if the parts selected were low in cost, extremely reliable, and nonrepairable. Efforts in microelectronics design should consider these characteristics and implement them where feasible.

Environmental Protection. As described earlier in this report, the environment faced by a tactical weapon system in the field is severe at best. The need for equipment which can operate in all climates continues. The services continue to review and expand specifications and standards to insure that equipment is able to withstand the elements. One area which appears to offer great benefits is that of moisture resistance of micro-

electronics circuits. Recently released information indicates that moisture is a significant contributor to electronic failures. Attempts to develop new and improved methods to eliminate moisture in the construction of microelectronic circuits will result in improved life of fielded systems.

Replicability. Military systems usually remain in the active inventory for 10 to 20 years. Over this period, there are continual demands upon industry to provide repair parts. Unfortunately, many of the requirements are placed in extremely small quantities to one or more producers. Past experience indicates that it is extremely difficult to replicate microelectronics circuits from one manufacturer to another and, if the system is late in its life cycle, possibly extremely expensive even if purchased from the prime contractor. In order to alleviate part of this problem, it would be beneficial if documentation would be such to allow for competitive procurement of even the smallest microelectronic circuit.

SUMMARY

The areas of improvement mentioned above can and will have a favorable impact on the Services in their attempt to reduce costs in the life cycle of system development. As we all know, dollars are in short supply while requirements become increasingly complex in order to meet an increasingly sophisticated enemy threat. This environment will challenge all involved to develop innovative approaches to complex and challenging problems. The microelectronics industry has made significant contributions to the defense of our country through an innovative and pioneering spirit which

has taken us to levels of technology which were imagined by few just a decade ago. The challenge is clear, innovative ideas and the willingness to accept difficult challenges are required in our common efforts to increase system effectiveness and reduce life cycle costs. Total dedication to these efforts will surely result in future systems which can be maintained in a high state of readiness at costs affordable to the Services involved.

BIBLIOGRAPHY

1. "Technology Update-Government", Electronics, 17 Oct 74, pg 171.

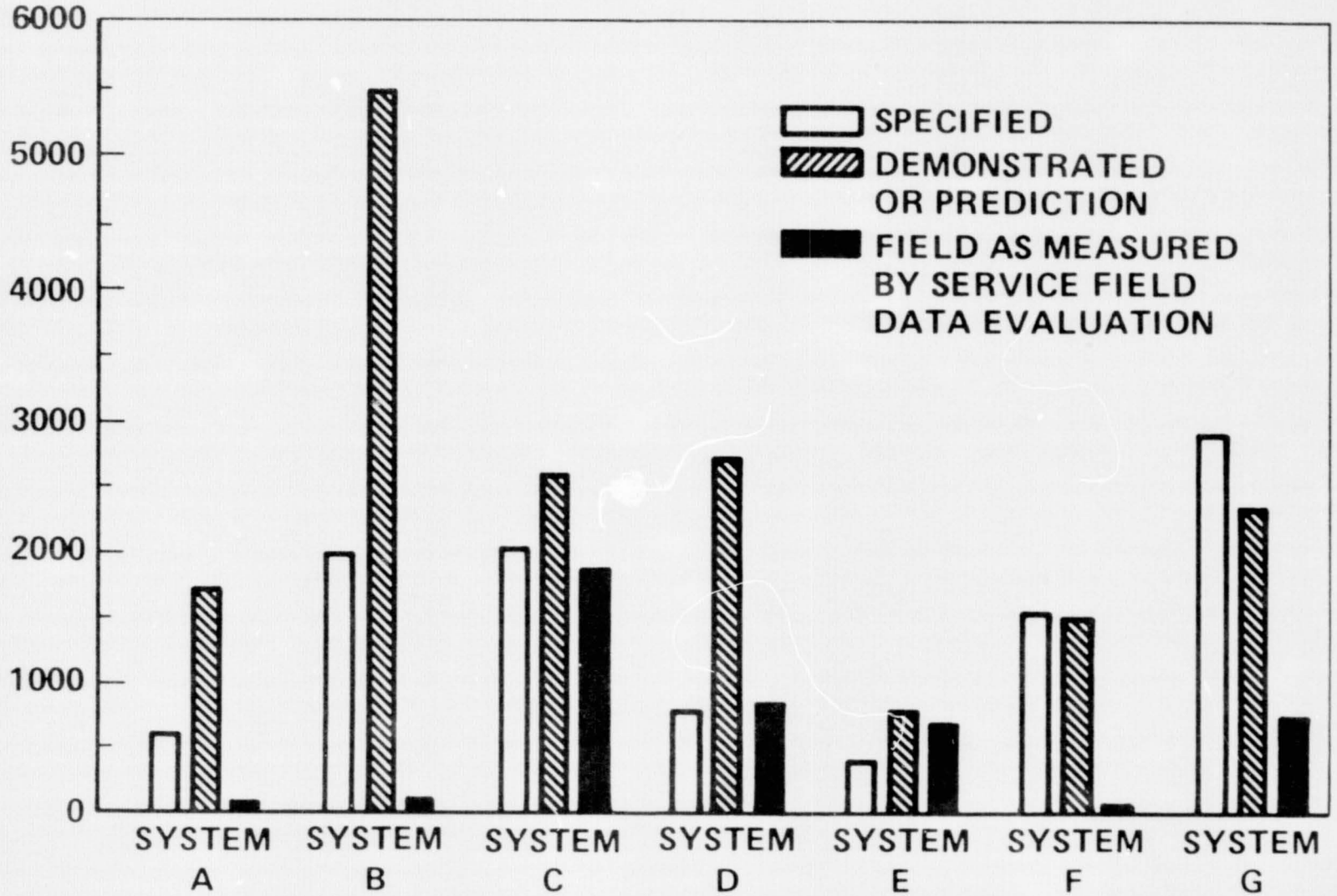
2. Meth, Martin A., "A DoD Approach to Establishing Weapon System Reliability Requirements," Defense Management Journal, Apr 76, pg 2.

3. Starr, H.I., "System Supportability--No Surprises Please," Society of Logistics Engineers, Maintainability Symposium, 22-25 Feb 77, pg 28.

4. Bredenbender, R.E., "Standardization Offers Economic Opportunities," Defense Management Journal, Apr 73, pg 25.

5. Department of the Air Force, "Evaluation of Environmental Profiles for Reliability Demonstration," Report RADC-TR-75-242, Rome Air Development Center, Griffiss Air Force Base, New York, Sep 75.

SELECTED EQUIPMENT RELIABILITY TREND FOR CONTEMPORARY WEAPON SYSTEMS



D6

*THE ROLE OF HYBRID CONSTRUCTION TECHNIQUES ON SEALED MOISTURE LEVELS

D. T. Somerville
Rockwell International
1200 North Alma Road
Richardson, Texas 75081
(214) 690-6438

Abstract

Residual gas analysis techniques are employed to measure the moisture in sealed hybrid packages as a function of substrate attach material, vacuum bake time and sequence, and sealing procedure. It is shown that, when room atmospheric exposure is eliminated following the vacuum bake-out, moisture levels of less than 1000 ppm may be achieved for modest bake times and solder substrate attach techniques. Suitable moisture levels were achieved for epoxy attached substrates only when seam sealing procedures were employed.

Introduction

Although moisture induced failure mechanisms in semiconductors and hybrids have been investigated and identified over the past several years, it has been only recently that conventional leak detection has been declared inadequate to insure low moisture levels in hermetically sealed hybrids and semiconductors. That is, although a hermetic seal insures that the external environment, including moisture, does not enter the package, it also insures that moisture internal to the package does not escape; this situation may not exist for less hermetic enclosures.

Recently Thomas[1] presented several less obvious factors contributing to high moisture levels in sealed packages. Included was the suggestion that extended vacuum baking, with no subsequent atmospheric exposure, was required to achieve moisture levels of less than 500 ppm; however, the role of several hybrid construction details was not presented. This paper presents the results of an empirical study that relates the effect of a selected group of hybrid process parameters and materials on the level of moisture in the sealed hybrid ambient.

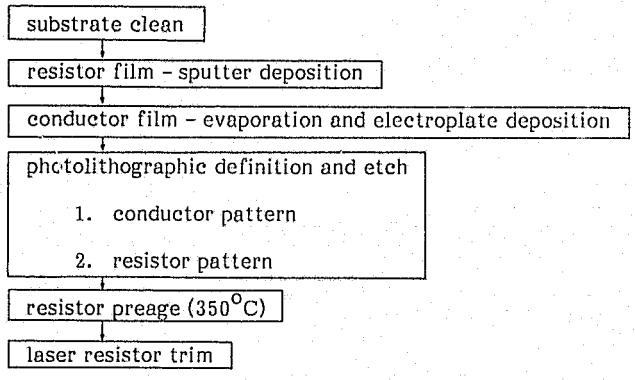
The study is divided into two parts. The initial data is the result of hybrids that were vacuum baked at 125°C, exposed to room atmosphere for various amounts of time, sealed on a gradient flat-pack sealer, and analyzed for moisture levels at Jet Propulsion Laboratories in Pasadena, California. The second portion of the study includes the same basic hybrid construction process; however, the semiconductors were omitted and the packages are vacuum baked at 150°C with no atmospheric exposure before sealing on both a gradient flat-pack sealer and a parallel seam sealer. Residual gas analysis of the second set of packages was obtained at Texas Instruments, Dallas, Texas.

Hybrid Construction

Substrate Fabrication

Conventional thin film subtractive processes utilizing tantalum nitride resistive films and titanium-palladium-gold conductive films were employed with the following generalized flow chart.

Fabrication Flow

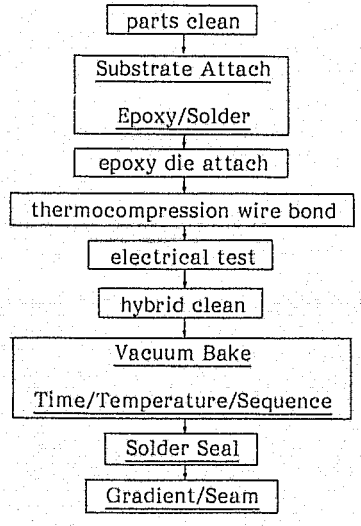


Previous characterization of this process utilizing Auger spectroscopy has demonstrated that the various rinse and bake steps are sufficient to leave no trace of ionic contaminants from cleaning solvents and chemical etches.

Assembly

After fabrication and inspection of the substrate, the packages and substrates were vapor degreased in electronic grade TMC and isopropyl alcohol as the first step in the assembly process. That process is described by the following flow chart.

Hybrid Assembly Flow



The substrates were then attached to the base of the 1 X 1 in. metal butterfly package in two ways, which represents the first variable of the study. Both 80/20 Au/Sn solder

*Published in the 15th Annual Proceedings, IEEE Reliability Physics Symposium, 1977.

and Ablebond 161-3® epoxy were used as attachment materials for mounting substrates. Package-substrate temperature exposure was approximately 300°C for Au/Sn attach and 170°C for 161-3 attach. Semiconductors (approximately 26 silicon die) were attached to the package mounted substrates with both Ablefilm 517® nonconductive epoxy and Ablebond 36-2® conductive epoxy. For the second part of the study, the same volume and type of epoxies were used, but no semiconductors were included. Although this change removed the potential moisture absorbing surfaces of silicon, it added more exposed epoxy surface area. The volume and uncovered surface area of epoxy were not specifically measured for this study; however, the volume for all epoxies per package is estimated as 25×10^{-4} in^3. This volume is reduced to an estimated 5×10^{-4} in^3 for soldered substrates.

Thermocompression wire bonding was simulated by mounting the package assembly on a hot plate at 230°C (the base temperature for Rockwell's thermocompression bonding process) for 30 minutes. Although the normal assembly flow would then include an electrical test, no electrical testing was performed on these parts. The package assembly and 80/20 Au/Sn preforms were then cleaned, prior to sealing with another TMC/isopropyl vapor degrease. The packages and preforms were vacuum baked prior to solder sealing. The vacuum bake time, temperature, and sequence represent the second major variables of the study. Bake times and temperatures varied from 30 minutes at 125°C to 36 hours at 150°C. In the first part of the study, which involved atmosphere exposure following the vacuum bake and prior to the sealing, packages were baked at 125°C for either 30 minutes or 16 hours. Packages were baked at 150°C, in the second portion of the study, for either 2, 3, 4, 5.5, 8, 16, 17, or 36 hours, with no atmospheric exposure between the bake cycle and the sealing process. The exception to this statement was a split cycle, in which the parts were baked for 3 hours, exposed to the atmosphere (for approximately 2 minutes), and again vacuum baked for 1 hour. The parts were then sealed without any atmospheric exposure following the second bake.

Sealing

Solder sealing was performed on a gradient sealer manufactured by Research Instruments Corporation and on a parallel seam sealer manufactured by Solid State Equipment Corporation. For this study, the primary significant difference between these two sealers is the technique of providing thermal energy to the sealing surface and subsequently raising the substrate or package base temperature. The gradient sealer features a flat heated surface, 1.500 X 1.375 in. that is typically brought in contact with the entire top surface of the package lid; an aluminum heat sink is likewise in contact with the package base. Thermocouple measurements of substrate temperature were made during sealing; these measurements indicated, with proper heat sinking, temperatures of 200°C at the hottest point of a solder attached substrate for Au/Sn sealing. Figure 1 shows the gradient sealer prior to enclosure of the unit in a dry box with attached vacuum oven; the unit is also used to solder attach substrates to the package base. The sealer is shown installed in the dry box in Figure 2. The parallel seam sealer (Figure 3) generates pulsed I^2R heating as two copper conical shaped electrodes roll along opposite perimeters of the lid surface. For flat pack sealing, the part is rotated after two opposite sides are reflowed, and the electrodes roll back along the two remaining sides of the lid. In this way, heat energy is kept primarily at the sealing surface. Similar temperature measurements were made of the substrate surface during seam sealing with Au/Sn solder, and these measurements indicated a temperature of approximately 120°C.

Figure 1
Gradient Sealer (Research Instruments Corp.)

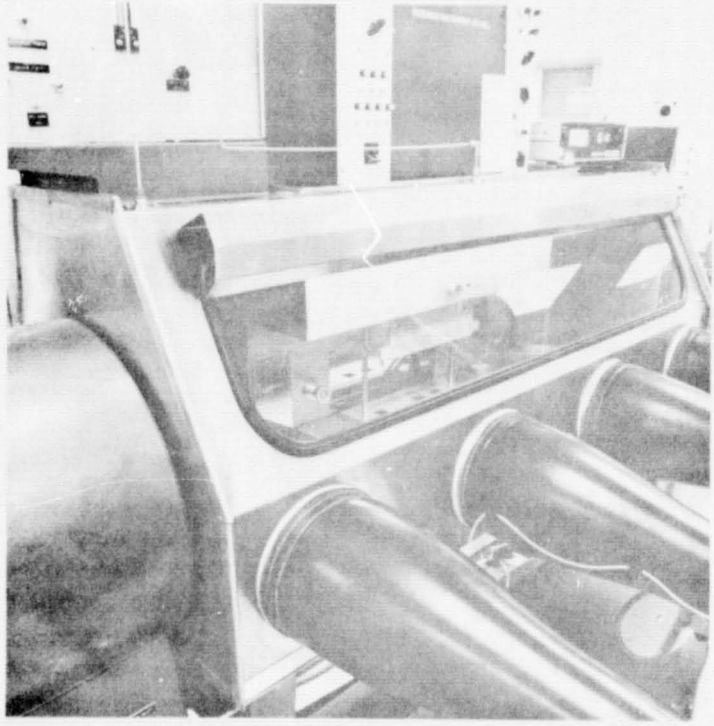


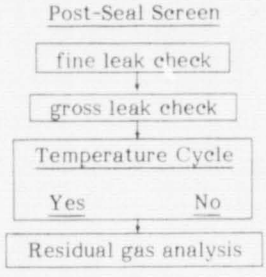
Figure 2
Gradient Sealer Enclosed with Attached Vacuum Oven

® Products of Ablestik Adhesive Co., Gardena, Calif.

Figure 3
Seam Sealer (Solid State Equipment Corp.)

In all cases, the moisture in the sealing gas atmosphere (80 percent N_2, 20 percent He) was less than 55 ppm and was typically less than 20 ppm, as measured by conventional phosphorous pentoxide monitors. In the case of the enclosed gradient sealer, both the dry box atmosphere and the sealer atmosphere was monitored.

The post-seal screen was minimized to a fine and gross leak check, followed by temperature cycling of a portion of the first phase packages. Because the initial work indicated the temperature cycling had no effect on sealed in moisture, it was omitted from the post-seal processing for the second part of the investigation.



Moisture Measurement

Facilities at Jet Propulsion Laboratory (JPL) and Texas Instruments (TI) utilized two analytical techniques to determine the moisture levels in the sealed packages. It is beyond the scope of this study to either detail or critique the measurement technologies; however, a partial comparison of the two methods follows.

Table 1
Residual Gas Analysis Technique

	JPL	TI
work preconditioning prior to lid puncture	vacuum evacuation for 16 hours at 125°C	He purge for 30 minutes at 120°C
analyzer (mass spectrometer)	quadrupole	magnetic sector
connecting plumbing from package to analyzer		
approx. length:	0.5 ft	3 ft
temperature:	100°C	120°C
data handling	computer	manual
"preconditioning" of package atmosphere prior to admission to analyzer	throttle down or sampling	He abstracted

The Jet Propulsion Laboratory technique essentially followed the procedures previously presented by Thomas.[2] Meyer[3] has reported on the basic methods utilized by Texas Instruments. In order to establish consistency between the two facilities, eight packages were identically processed and baked and sealed in the same lot. That is, the packages were exposed to identical environments and temperatures through the sealing process. The following results show reasonable consistency in the measured moisture levels.

Table 2
Results of Consistency Trials

Process Conditions	Moisture (in ppm)	
	JPL	TI
seam seal, epoxy substrate attach, 8 h bake	3000	800
seam seal, epoxy substrate attach, 16 h bake	<500	200 to 400
seam seal, solder substrate attach, 4 h bake	<500	200 to 400
seam seal, solder substrate attach, 16 h bake	<500	<200
(no atmosphere exposure)		

Results

More than 100 packaged "circuits" were analyzed for moisture during the investigation.

Table 3
Analysis of Circuits

	PKG. QTY.	TYPE	Residual Gas Analysis
Part 1	23	125°C bake, atmosphere exposure	JPL
Part 2	77	150°C bake, no atmosphere exposure	TI
Comparison	4	150°C bake, no atmosphere exposure	JPL

Part 1. Figures 4 through 7 show the moisture level, as a function of time of exposure to the atmosphere following the vacuum bake at 125°C. Although there is scatter in the data, there is an obvious increase in moisture with exposure time and no apparent dependence on thermal cycling. It may also be seen that the duration of the vacuum bake is of secondary significance when compared to atmospheric exposure. Solder attached substrates yield lower moisture levels and somewhat less dependence on exposure time. The empty packages (no substrate, components, or epoxies) all show less than 1000 ppm trapped moisture but measurement uncertainties masked exposure time dependence.

Part 2. Figure 8 compares moisture results between the gradient sealer and the parallel seam sealer for epoxy mounted substrates. Figure 9 makes the same comparison for solder attached substrates. The higher moisture levels for packages sealed with the gradient sealer may be attributed to the hotter substrate temperatures during sealing. This becomes dramatically apparent when the epoxy volume is increased by epoxy substrate attachment. Packages sealed on the seam sealer achieved moisture levels of less than 1000 ppm for both epoxy and solder attached substrates for bake times as low as 4 h at 150°C. The data plotted at 1 h bake time represents the split bake that included a short atmosphere exposure between an initial 3 h bake and the final 1 h bake. These samples were sealed on only the gradient sealer; however, satisfactory moisture levels were achieved for solder attached substrates.

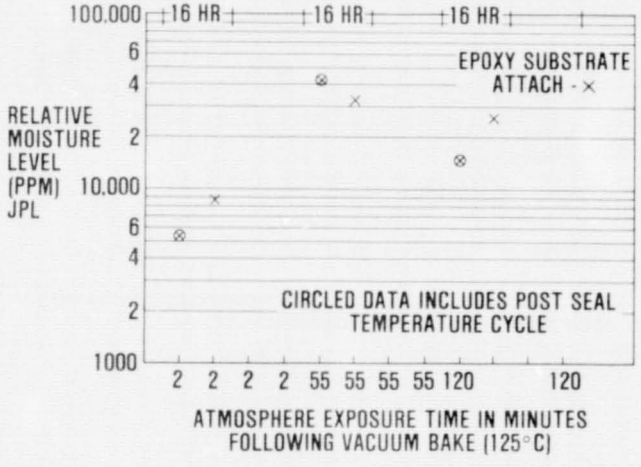


Figure 4
Moisture as a Function of Atmosphere Exposure - Epoxy Attach and 16 Hour Bake

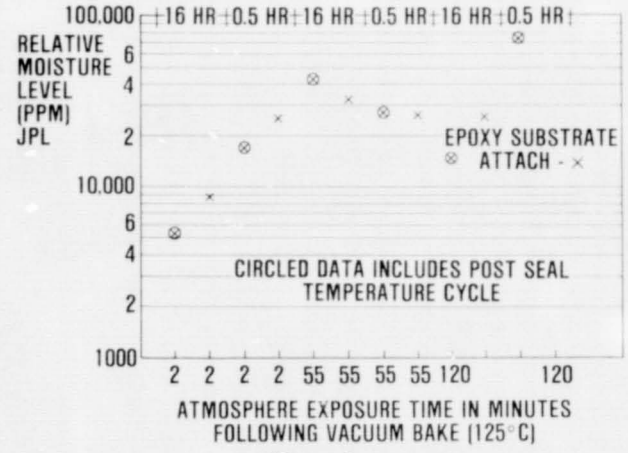


Figure 5
Moisture as a Function of Atmosphere Exposure - Epoxy Attach

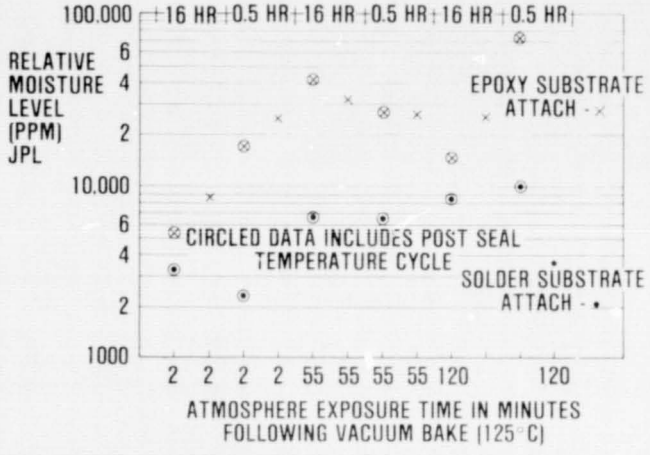


Figure 6
Moisture as a Function of Atmosphere Exposure - Epoxy and Solder Attach

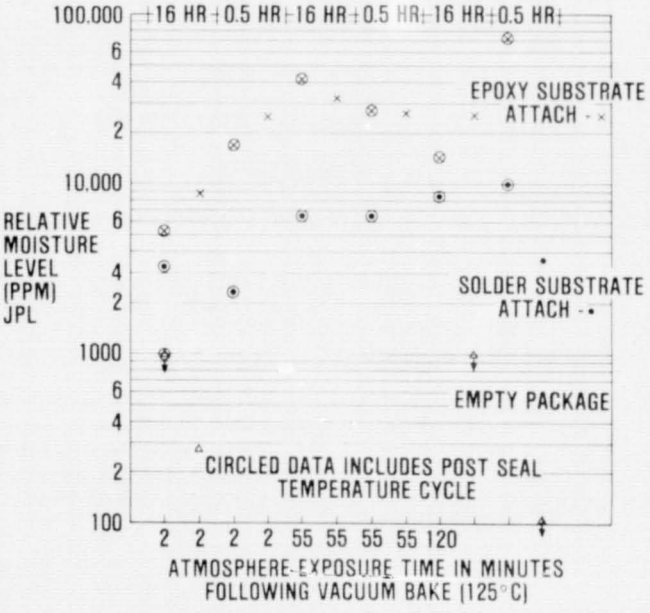


Figure 7
Moisture as a Function of Atmosphere Exposure Time

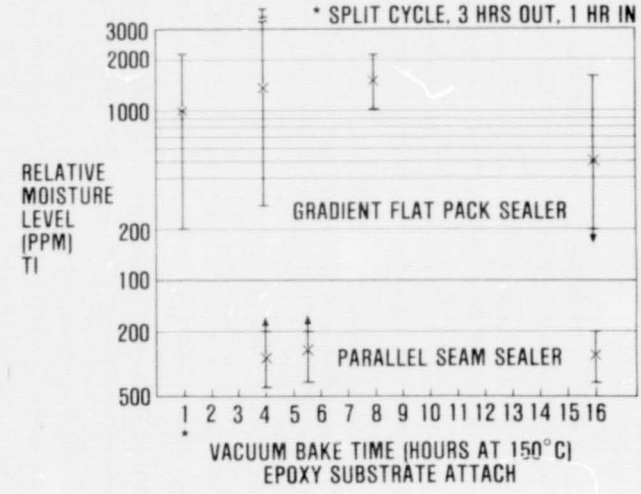


Figure 8
Moisture as a Function of Vacuum Bake Time and Sealer - Epoxy Attach

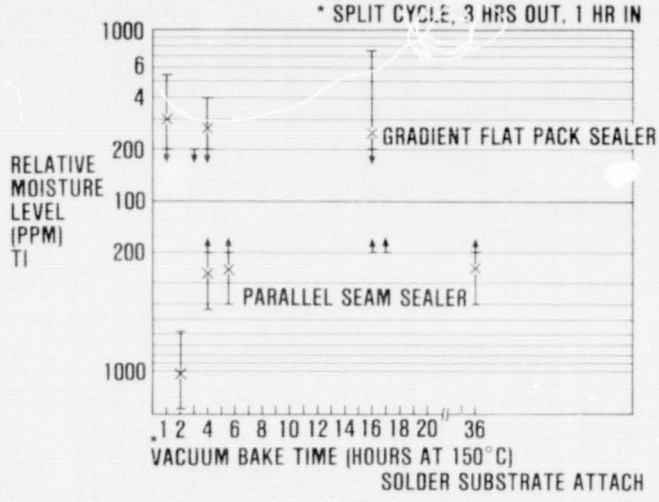


Figure 9
Moisture as a Function of Vacuum Bake Time and Sealer - Solder Attach

Conclusions

For the specific processes and materials described, the following conclusions are drawn.

- Room atmosphere exposure after preseal bake resulted in >1,000 ppm sealed-in moisture for exposures as low as 2 min and preseal bake times as long as 16 h.
- In general, room atmospheric exposure prior to sealing yielded moisture levels >10,000 ppm for hybrids with epoxy attached substrates and >1,000 ppm as measured at JPL for hybrids with solder attached ceramic.
- A split cycle with no room atmosphere exposure after the final bake resulted in adequate moisture levels only for hybrids with solder attached substrates.
- For hybrids with epoxy attached substrates, the gradient sealer yielded moisture levels, as measured at TI, >1,000 ppm with no atmosphere exposure and with bake times up to 16 h. Moisture levels <1,000 ppm were achieved for the same attachment process but for hybrids that had been sealed in a parallel seam sealer.
- For hybrids with solder attached substrates, bake times as short as 4 h yielded moisture levels, <1,000 ppm for either the gradient sealer or the parallel seam sealer.

Acknowledgements

The author recognizes and appreciates the efforts of Charles Totten, Walter Hollowell, Charles Burns, and Darrel Davis in preparation of the assemblies and package sealing, as well as the efforts in the Residual Gas Analysis provided by Dr. Alex Shumka of Jet Propulsion Labs and Jimmy Hosch and Vince Cordasco of Texas Instruments, Inc.

References

1. R. W. Thomas, "Moisture Myths and Microcircuits," Proceedings 1976 - 26th Electronic Components Conference, pp 272-276, San Francisco, California, April, 1976.

2. R. W. Thomas, "Microcircuit Package Gas Analysis," 14th Annual Proceedings Reliability Physics 1976, pp 283-294, Las Vegas, Nevada, April, 1976.

3. D. E. Meyer, "Measurement and Control of Atmosphere in Hermetically Sealed Semiconductor Packages," 1974 Int'l Microelectronics Symposium - ISHM, pp 293-296, Boston, Massachusetts, October, 1974.

N78-16273

INVESTIGATION OF PACKAGE SEALING USING ORGANIC ADHESIVES

K. L. Perkins
J. J. Licari
Rockwell International Corporation
Electronic Devices Division
Anaheim, California 92803

ABSTRACT

A systematic study was performed to evaluate the suitability of adhesives for sealing hybrid packages for NASA/MSFC applications. This study consisted of three parts.

(1) Screening ten selected adhesives on the basis of their ability to seal gold-plated Kovar butterfly-type packages that retain their seal integrity after individual exposures to the following four increasingly severe temperature-humidity environments:

   (a) Ten days at 50°C/60% RH
   (b) Ten days at 60°C/98% RH
   (c) The ten-day moisture test per Method 1004.1 of MIL-STD-883A
   (d) Ten days at 85°C/85% RH

(2) Screening the four best adhesives, as determined from the temperature-humidity screen, on the basis of their ability to seal gold-plated Kovar butterfly-type packages and ceramic packages that retain their seal integrity after both individual and sequential exposure to the following Class A test environments specified in Method 5004.2 of MIL-STD-883A:

   (a) Thermal Shock - Method 1011.1, Test Condition C (i.e., 15 cycles, -65°C to +150°C)
   (b) Temperature Cycling - Method 1010.1, Test Condition C (i.e., 15 cycles, -65°C to +150°C)
   (c) Mechanical Shock - Method 2002.1, Test Condition B (i.e., 5 shock pulses at 1500 g's in the Y_1 plane)
   (d) Constant Acceleration - Method 2001.1, Test Condition A (i.e., 5,000 g's in the Y_1 plane)
   (e) Temperature Aging corresponding to the temperature/time requirement associated with the burn-in test of Method 1015.1 (i.e., 240 hours at 125°C)

(3) Subjecting the best adhesive-package combination, as identified by the MIL-STD-883A screen, to a 60°C/98% RH environment and continuously monitoring the moisture content using Panametrics Aquamax-type moisture sensors to determine susceptibility to moisture permeation.

In all cases, seam-sealed gold-plated Kovar packages were used as controls. The ten adhesives selected for temperature-humidity screening were Ablefilm 507, Ablefilm 550, Ablebond 36-2, Ablebond 58-1, Epo-Tek H20E, Epo-Tek H81, Epo-Tek H77, Ablebond 789-1, Ablebond 873-1, and AF-30. The four best adhesives selected for MIL-STD-883A screening were Ablefilm 507, Ablebond 36-2, Epo-Tek H77, and Ablebond 789-1. Packages sealed with two of these, Ablefilm 507 and Ablebond 789-1, retained their seal integrity after exposure to all temperature-humidity environments. Packages sealed with the other two, Ablebond 36-2 and Epo-Tek H77, failed exposure to the 85°C/85% RH environment. The best adhesive-package combination selected for moisture permeation testing was the ceramic package sealed with Ablebond 789-1. All of the gold-plated Kovar packages sealed with the four adhesives failed sequential exposure to the MIL-STD-883A test environments, and all of the ceramic packages passed.

Results for two ceramic packages sealed with Ablebond 789-1 exposed to the 60°C/98% RH environment (moisture concentration of 193,000 ppm_v) for 15 days showed that the moisture content (which initially was only about 20 ppm_v) slowly increased to 1000 ppm_v after the first few days (3-3/4 days for one package and two days for the other), and thereafter steadily increased at constant rates to 14,600 ppm_v in one package and 19,000 ppm_v in the other by the end of the 15-day test. The moisture content was 6,000 ppm_v after eight days for one package, and after only a little over 5-1/2 days for the other. Permeabilities and times to half ambient were calculated to be of the order of 1.3 to 4.2 x 10^{-13} gm/cm sec Torr and 90 to 100 days, respectively.

The seam-sealed gold-plated Kovar packages used as controls passed all tests. In the case of the 15-day exposure to 60°C/98% RH, the moisture content of the seam-sealed gold-plated Kovar package remained unchanged at about 20 ppm_v.

CLUSTER SEAL FEATURES

RAYTHEON

- HIGH DENSITY / COST RATIO
- HERMETIC PROTECTION ONLY WHERE REQUIRED
- MINIMUM NUMBER OF INTERCONNECTS
- HIGH RADIATION RESISTANCE
- ADAPTABLE TO CLOSE TOLERANCE DISCRETE DEVICES
- OUTSTANDING THERMAL CHARACTERISTICS
- TAPE CARRIER, BEAM LEADS OR CHIP & WIRE
- COMBINES BEST FEATURES OF FIELD PROVEN TECHNOLOGIES
- UNIFORM ASSEMBLY PROCEDURE [MINIMUM DISTRIBUTION OF DEFECTIVE PARTS OR WORKMANSHIP]

CLUSTER SEAL

The cluster seal packaging technology represents a combination and extension of two well known technologies pioneered by the Raytheon Company. The first is the Raypack technology which is now an industry standard for a variety of military and commercial hybrid programs. The second is the hot cap seal technology which was developed by Raytheon as a discrete device packaging technology for the Poseidon and Trident programs. By combining these concepts we have achieved a packaging technology which can provide a higher performance to cost ratio than any competing packaging scheme. It should be stressed at the beginning that there is nothing "funny" about cluster seal. It involves no secret formulas, materials, or processes. It involves no organics, pseudo-organics, poisoning agents, or materials which are foreign to active devices. The concept is simple and it does work. There are refinements which can extend the usefulness of the concept to include a broader range of applications but we will start with the basic principle.

The philosophy on which the cluster seal concept is based and illustrated in this publication by way of a typical NAFI application, is that modern thick film technology is capable of providing passive networks which can be incorporated into a module without requiring hermetic protection. For systems or applications where this concept is not applicable, cluster seals cannot be effectively applied. Our position, however, is that if your system's module requirements will permit the use of multilayer PC boards and discrete passive components which are not hermetically sealed in either glass or metal and you require hermeticity only in your active devices (e.g., transistors, diodes, SSI, MSI, etc.) then from a cost, reliability and density standpoint your system is a good candidate for cluster seal packaging.

There is at present, mounting and almost overwhelming evidence that properly fabricated non-hermetic thick film networks comprised of conductors, resistors, and possibly capacitors are capable of highly reliable operation in multitude of hostile environments. The evidence stems from years of GEOS and other satellite operations, shipboard installations such as Aegis, RADC failure documentation, testing in missile applications such as Poseidon and Trident,automotive applications, and data from material vendors.

In cluster seal packaging, the active devices are arranged on the substrate in such a fashion that individual covers can be used to hermetically seal selected locations. Thus, a single 1/4 inch square cover may seal an .080 inch square MSI device or as many as four (4) transistors, four (4) or even more diodes. Various size covers are available to incorporate larger or more devices in a single seal site. The accompanying fabricating and process flow chart and photographs will clearly illustrate the application of cluster seal technology to a typical NAFI module. Layout and fabrication of the thick film substrate is identical to our standard thick film process. Sequence of screening and firings of a typical circuit is shown below.

STEP	SCREEN	MATERIAL	FIRING TEMP.(°C)
1	PtAu	ESL 5800 B	940
2	Au	Plessey 5025	940
3	Dielectric	ESL 4608 FB	850
4	Resistors	DuPont 1400 series	850
5	Seal Glass	Corning 7583	500

After the last standard thick film firing the seal rings are silk screened and fired to form a hermetic seal to the substrate. The glass used for this seal ring is a lead-zinc-borate solder glass which is available under the Corning code number 7583. The glass powder is mixed with various organic vehicles such as pine oil and ethyl cellulose to provide a suitable rheology for silk screening. All the sealing rings are silk screened

simultaneously to unfired thicknesses of about .009 inches. The simultaneous screening of seal rings provides precise seal ring location. The seal rings are then fired in an air furnace at about 500°C for a few minutes to drive off the organic vehicles and melt the glass to provide a hermetic seal to the substrate. The furnace profile and belt speed must be controlled to provide adequate fusion of the glass without promoting devitrification which would hinder the final seal operation. Resistors can now be trimmed to value. We employ laser trimming but abrasive trimming is also perfectly acceptable. After trimming, the active devices are die attached and wire bonded. Eutectic die attach is accomplished with an infrared die bonder made by Kulicke and Soffa Industries. The advantage of this machine is that the substrate and all previously attached chips can be maintained at a bias temperature well below the Au Si eutectic temperature (370°C) and only the particular die pad to which a device is currently being attached is heated to the eutectic temperature. Thus, the thermal history which each device sees during die attach, is the preheat bias temperature of 200 to 300°C plus the local thermal spike caused by the infrared heating lasting about 3 seconds which is required to achieve eutectic die attach. If a conventional die attach machine were employed, all semiconductors would sit in molten eutectic while subsequent devices were attached. This high temperature exposure for extended periods could cause large parameter shifts in device characteristics. The infrared die attach machine eliminates this problem.

Wire bonding is performed with ultrasonic wedge bonding equipment using .001 inch diameter 99% aluminum, 1% silicon wire. The cluster seal technology, however, is compatible with any of the standard wire bonding techniques. After wire bonding we generally perform an electrical test and repair as required. At this point the unit may go to burn-in (either powered or unpowered) or directly to sealing depending on the program requirements. Sometimes we perform a post seal burn-in to enable us to predict module reliability. If post-seal burn-in yields are high we may continue the burn-in but subtract the accumulated time from module burn-in.

If post seal burn-in yields are low, we may elect to do a pre-seal burn-in and repair any failures before sealing. Pre-seal burn-in is expensive because of the extra care required to handle unsealed devices. Although post seal failures are repairable we do not consider this to be a desirable procedure and prefer to consider the substrate a throw away item if it fails after sealing.

The sealing process is clearly illustrated in the accompanying charts and figures. Caps are fabricated from 92% Al_2O_3 by conventional dry pressing techniques. They are purchased to a source control drawing and carefully specified in terms of important physical and chemical parameters such as purity, gas permeability, water absorption, surface finish, expansion coefficient, etc. The seven degree taper on the sealing surface which is shown in the drawing serves to minimize glass flow inside the cap where it could damage wire bonds. It also serves to provide controlled seal glass thicknesses under the cap in the event that parameters such as seal ring glass thickness, seal force, temperature, etc. vary somewhat. The caps are loaded into a magazine and are fed automatically by the cap shuttle feed to the cap heater block where they are held by vacuum during the cap heating cycle which is automatically timed and is typically about seven seconds. When the cap heat cycle is over the cap heater block lowers the preheated cap and presses it into the glass seal ring on the substrate. The substrate has, of course, been pre-positioned by locating fixtures and pre-heated to a temperature substantially below the cap temperature and below the flow temperature of the seal glass. The contact of the cap (which has been pre-heated to above the flow temperature of the glass) with the seal ring instantly raises the temperature of the glass to a point where it flows, wets the cap and forms the hermetic seal. The cap heater block retracts after the seal cycle is completed and the substrate is ready to be repositioned for the next seal. The entire seal operation takes about 10 to 15 seconds per seal depending on the cap size and the use of the optional I.R. assist. A thermal profile (Figure 1) is illustrated for the first die attached to a substrate

via the normal mode and by the infrared assisted mode which lowers the average device temperature profile by about 100-150°C. Although subsequently

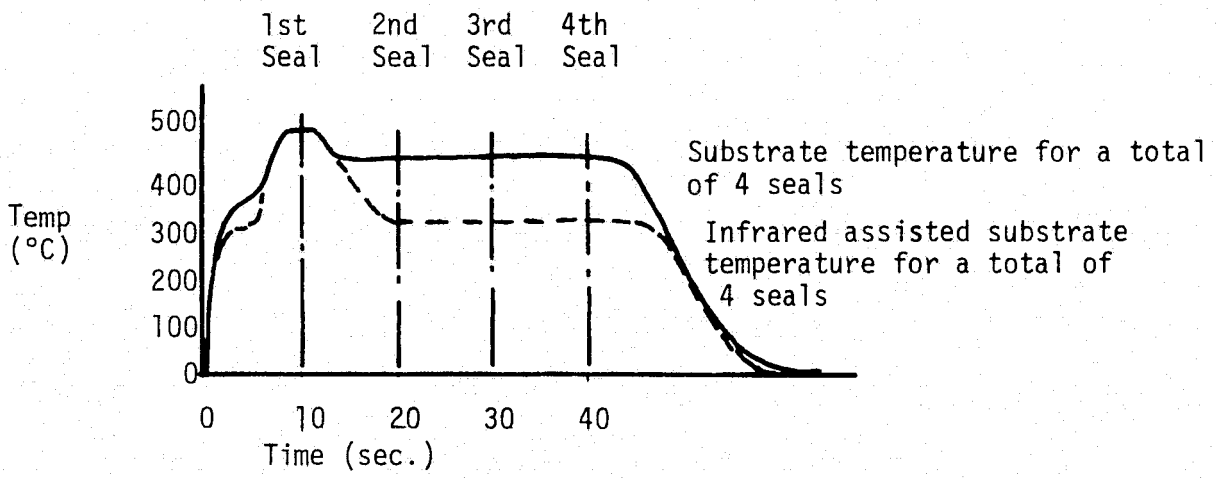


Figure 1

sealed die sites will undergo a similar thermal spike each die site will experience only one spike and the total substrate soak time at Ts will depend on how many sites are sealed. The limit to which bias temperature can be lowered when using infrared assist depends on the cap size, location on the substrate, etc. but is generally in the vicinity of about 100°C. Seal temperature for the seal glass we are currently using in production is about 500°C which means that we run the cap heater block at 600°C and the substrate heater block at 400°C. New glasses are currently being evaluated which could lower substrate temperature by 100-150°C but these glasses must be considered experimental at this time. Other schemes for lowering active device seal temperature have been evaluated. One promising technique involves the deposition of a resistive seal ring around the perimeter of the cap. During final seal, power is dissipated in this ring by impressing a voltage across it. The rapid and essentially adiabatic temperature rise in

cap perimeter heats the seal glass to its seal temperature with a minimal temperature rise of the active components.

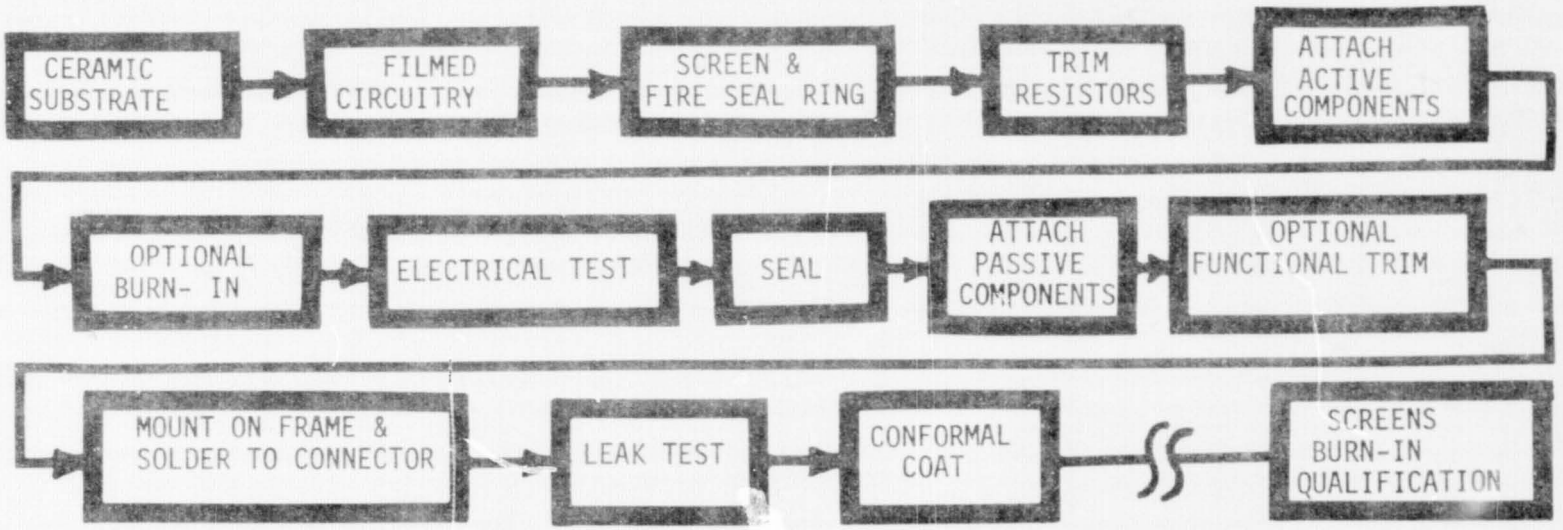
Attachment of passive or prepackaged active components can be performed either before or after the substrate has been bonded to the aluminum NAFI web. Also, functional trim can be performed anytime after sealing. The use of opaque caps for the cluster seal permits functional resistor trim when light sensitive active components are involved without having to resort to special precautions. Trimming may also be performed by any method without fear of contaminating the sealed circuitry. There are a number of adhesives which have been found suitable for bonding the substrates to the web. The most important adhesive parameter appears to be that it not be too rigid. There is a considerable difference in the expansion coefficients of the substrate and the web. The use of rigid adhesives can cause substrate cracking during thermal cycling or shock. A semi-rigid film adhesive such as Ablefilm 545 or a polysulfone adhesive filled with Al_2O_3 or BeO particles to improve thermal conductivity have both been used successfully. Silicone adhesives have also been used.

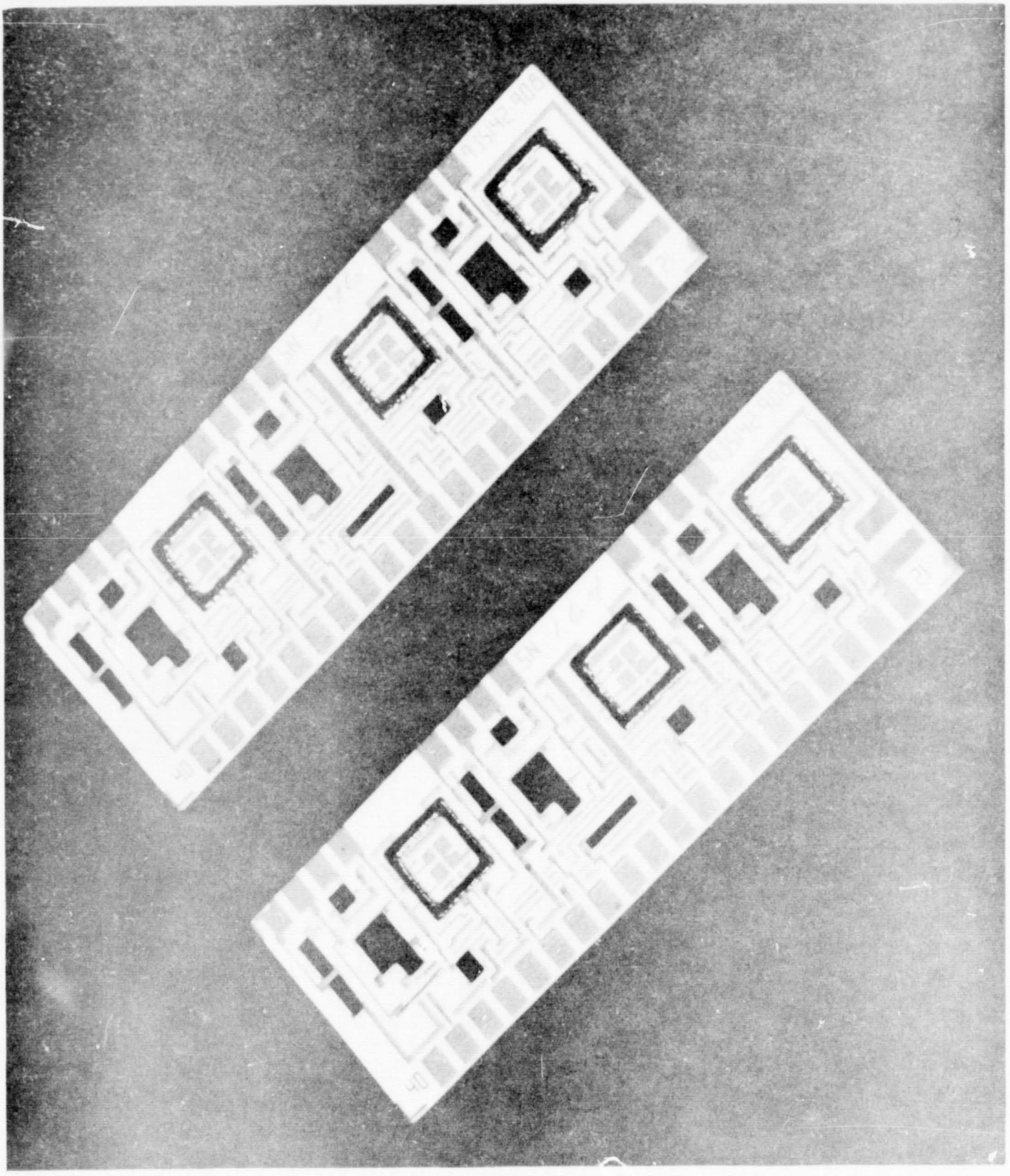
Soldering of the substrate termination pads to the NAFI I/O pins is accomplished by techniques similar to those used for terminating to multilayer boards. The only major process difference is that because of the high thermal conductivity of a substrate compared to a MLB it is recommended that the entire assembly be preheated to about 100°C to minimize the heat input required to reach the melting point of the solder.

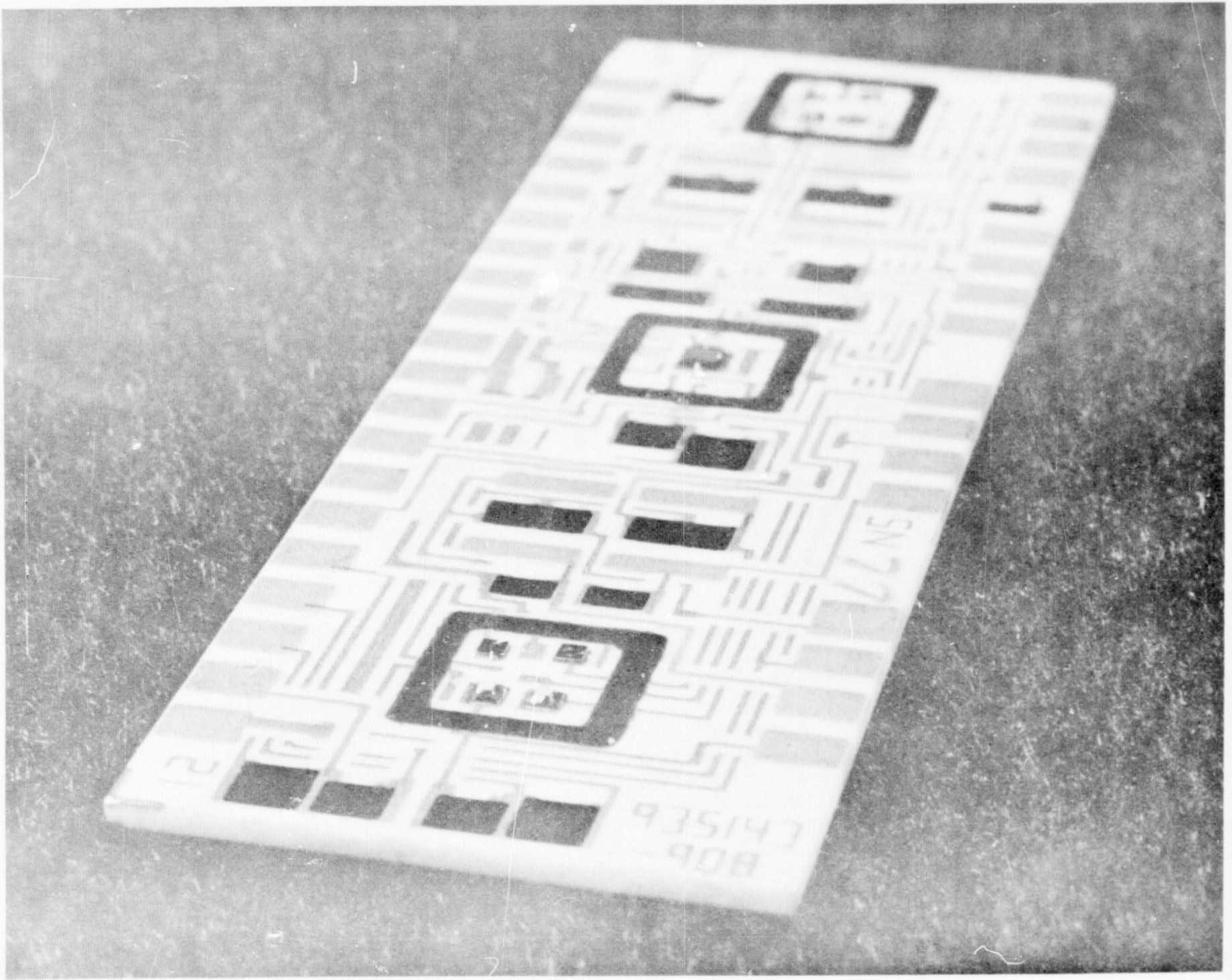
Conformal coating is usually applied to the finished substrate or module. Any of the coatings which can be applied to an MLB can be applied to a cluster sealed module. Raytheon has performed extensive evaluations of silicones, epoxies, urethanes, parylene and is in a position to recommend an appropriate coating for any application.

CLUSTER SEAL

FABRICATION PROCESS FLOW

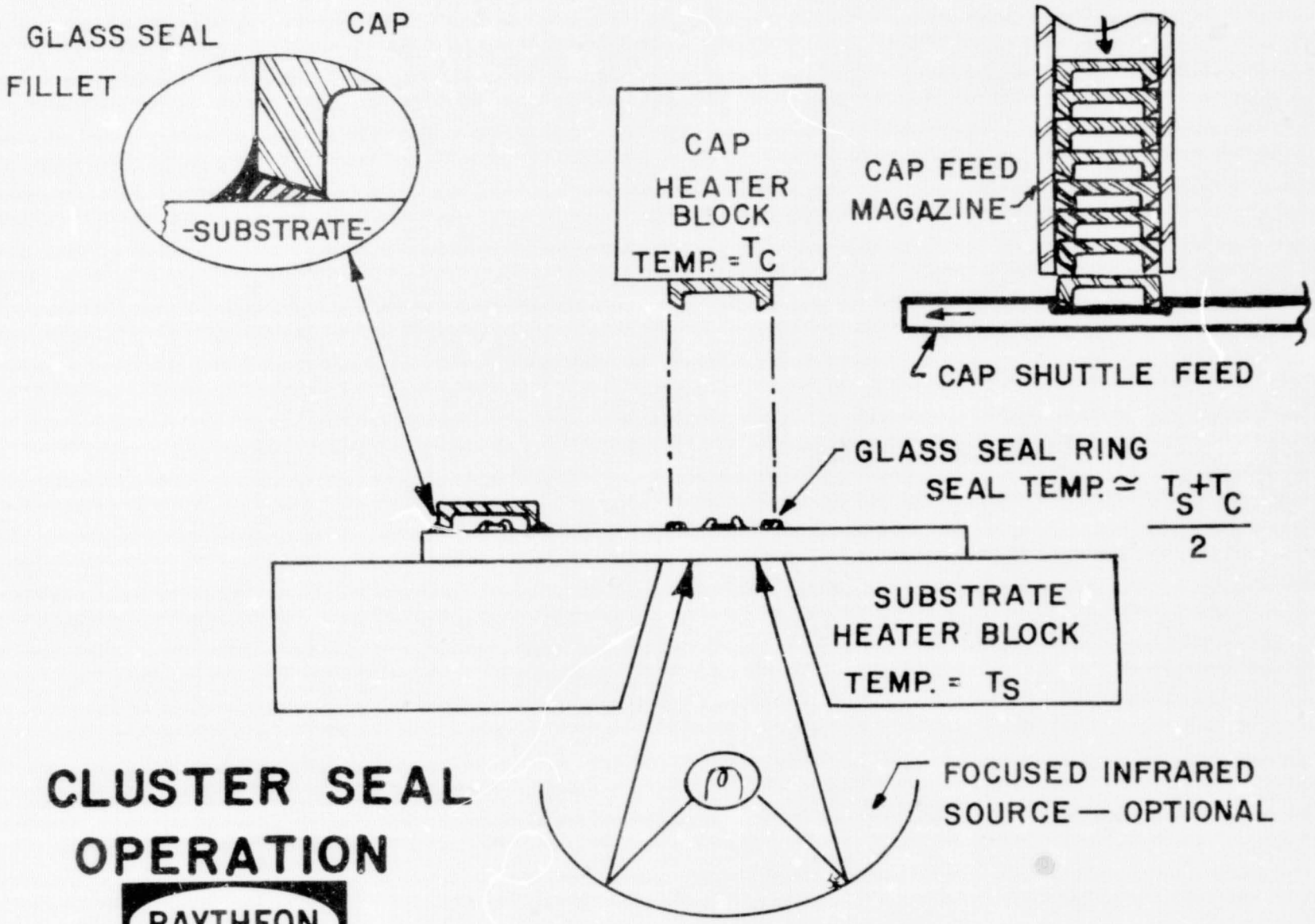






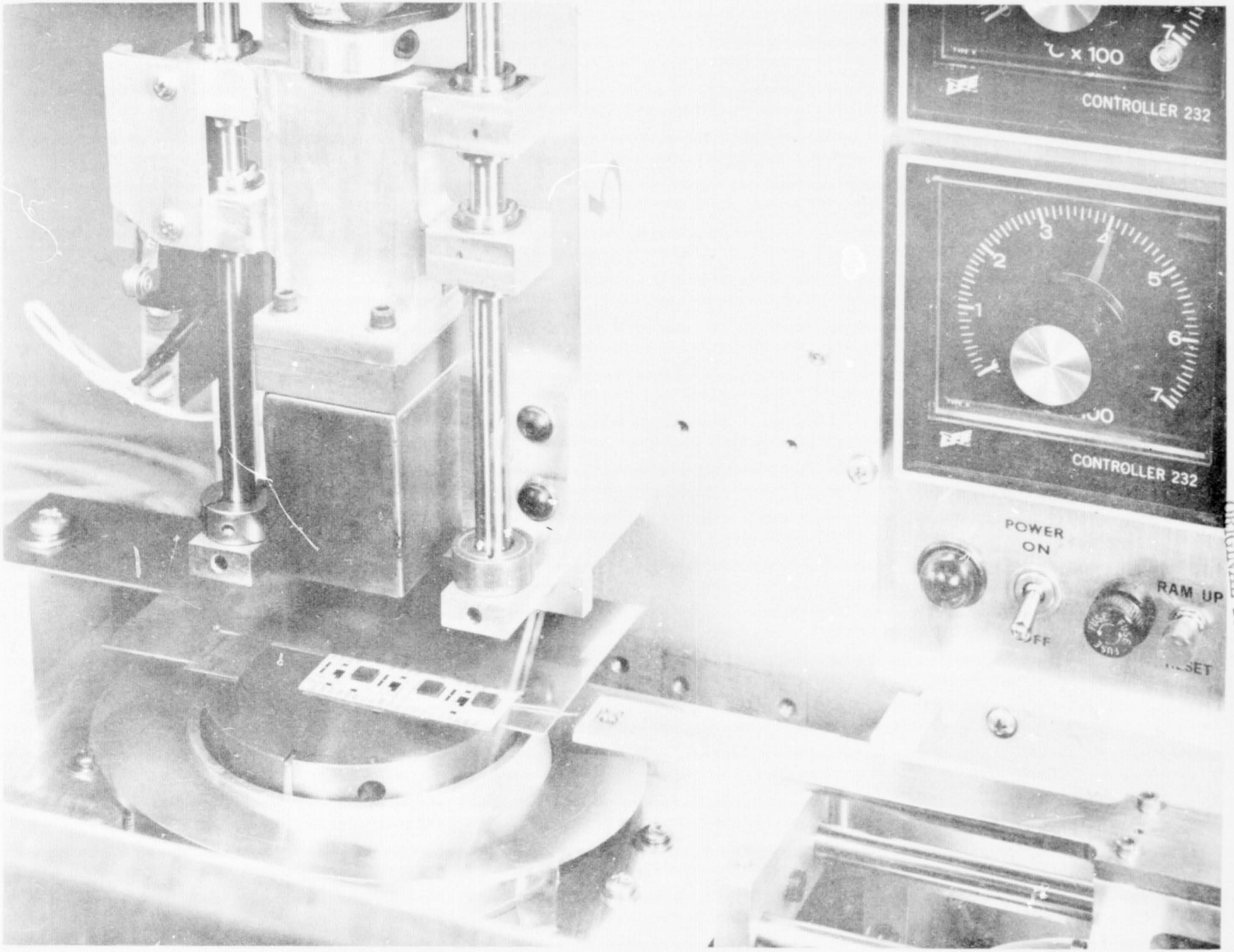
SUBSTRATE WITH ACTIVE DEVICES DIE AND WIRE BONDED READY FOR CLUSTER SEALING

DRY BOX SET UP FOR CLUSTER SEALING

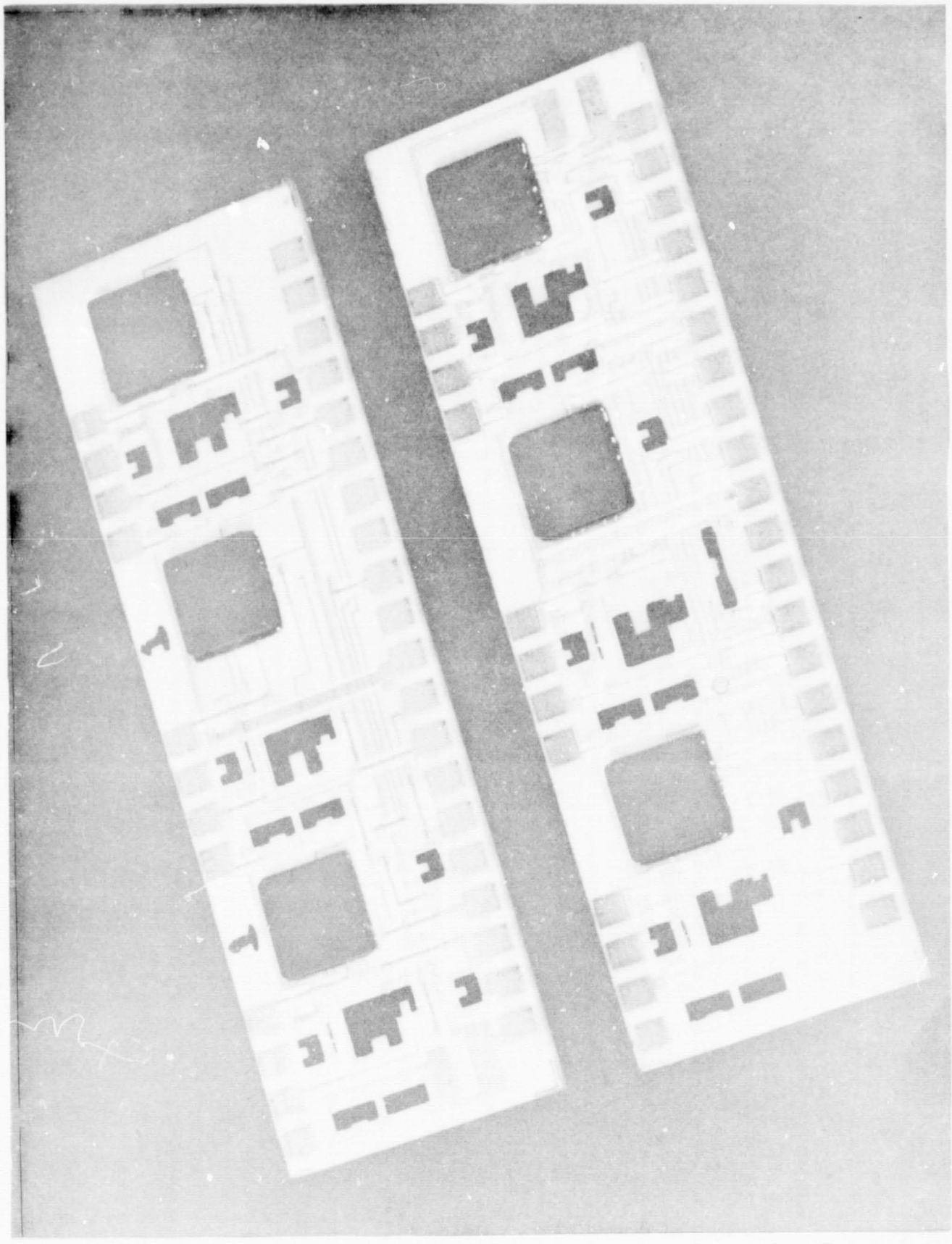


CLUSTER SEAL OPERATION

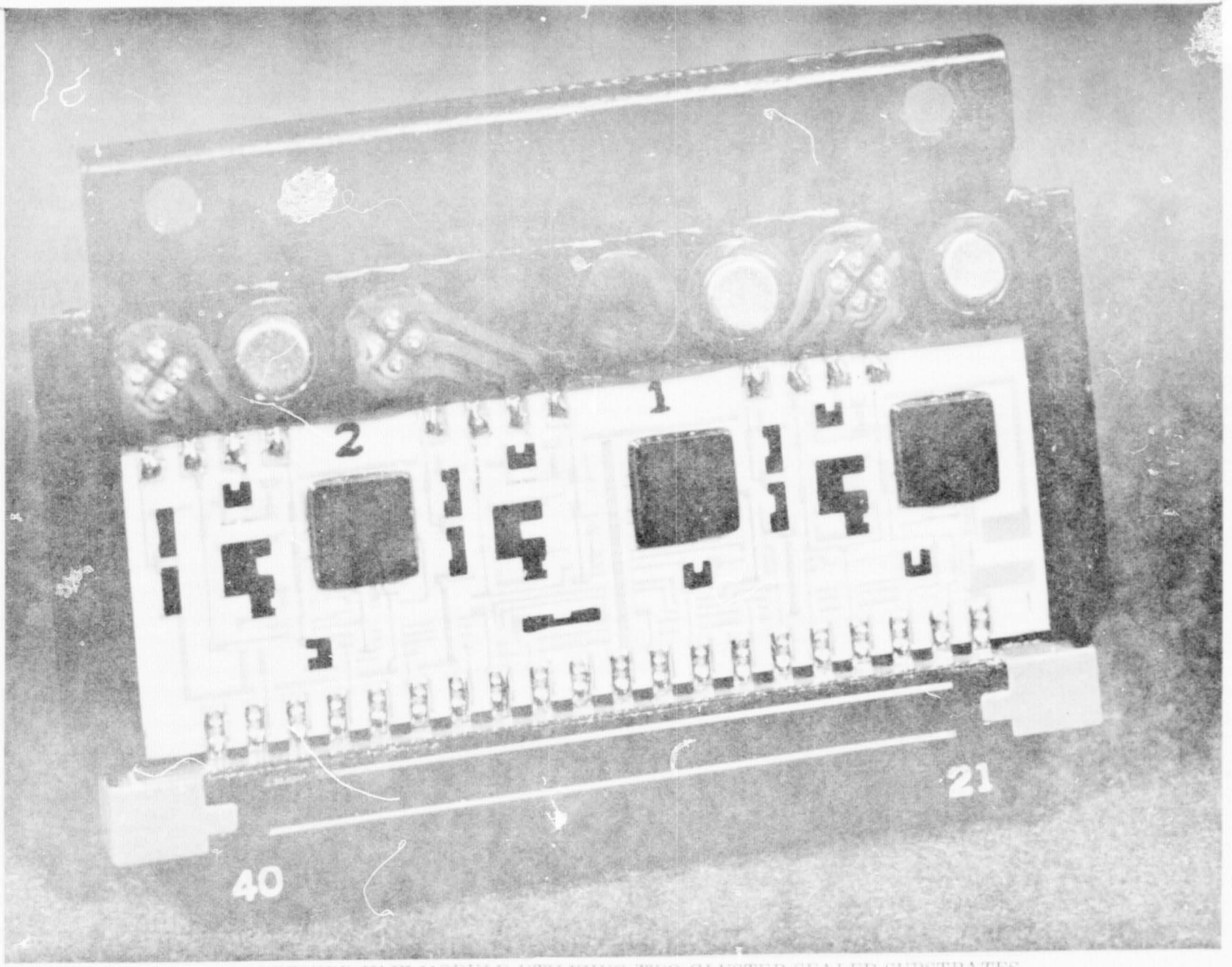
RAYTHEON



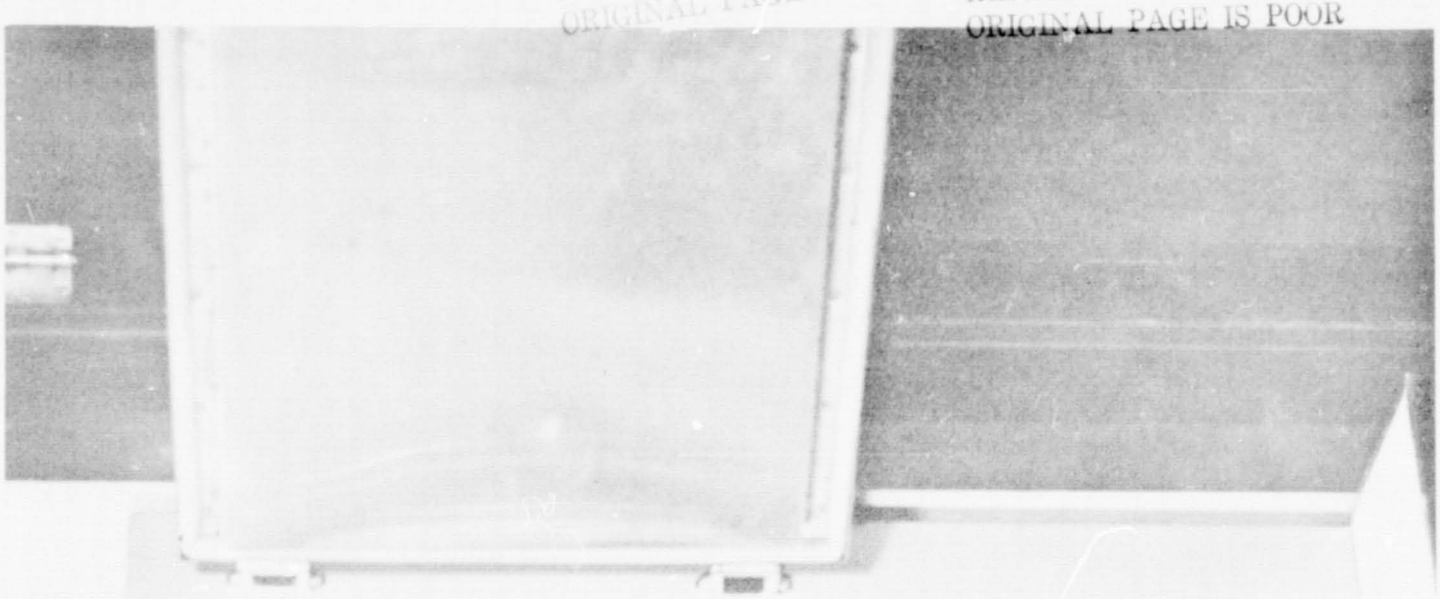
CLOSE-UP OF CLUSTER SEAL MACHINE

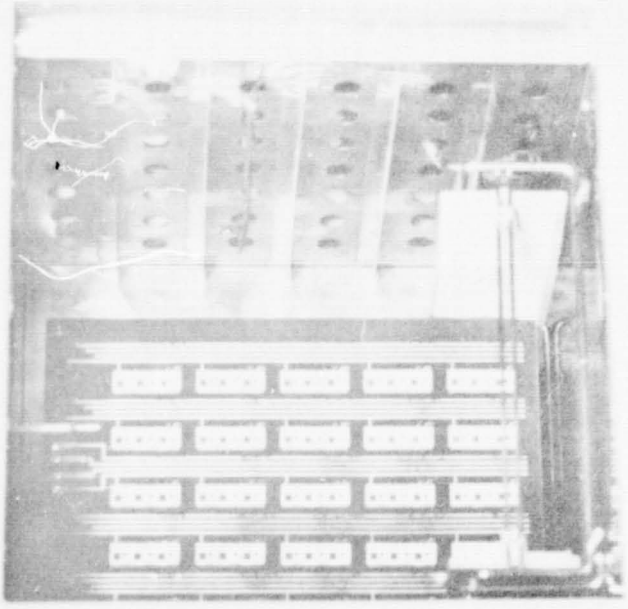


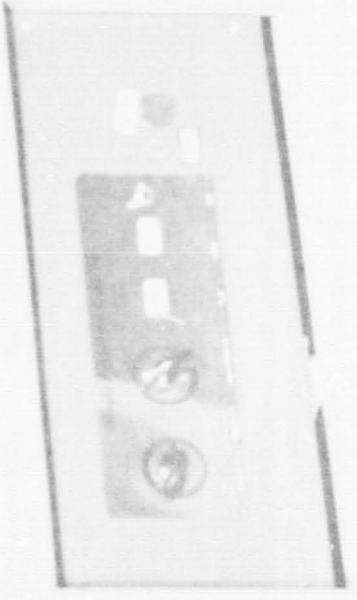
C-2

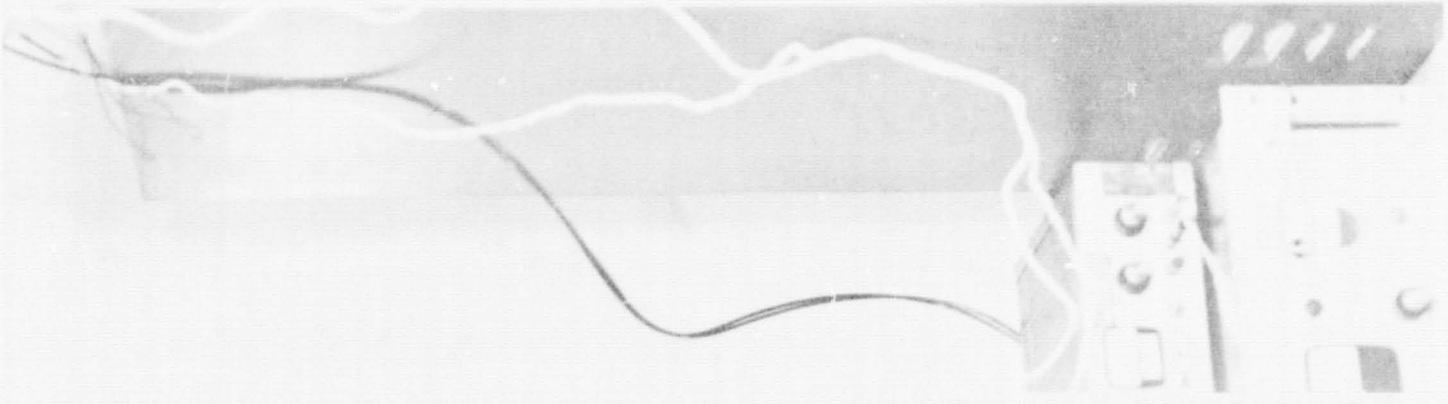


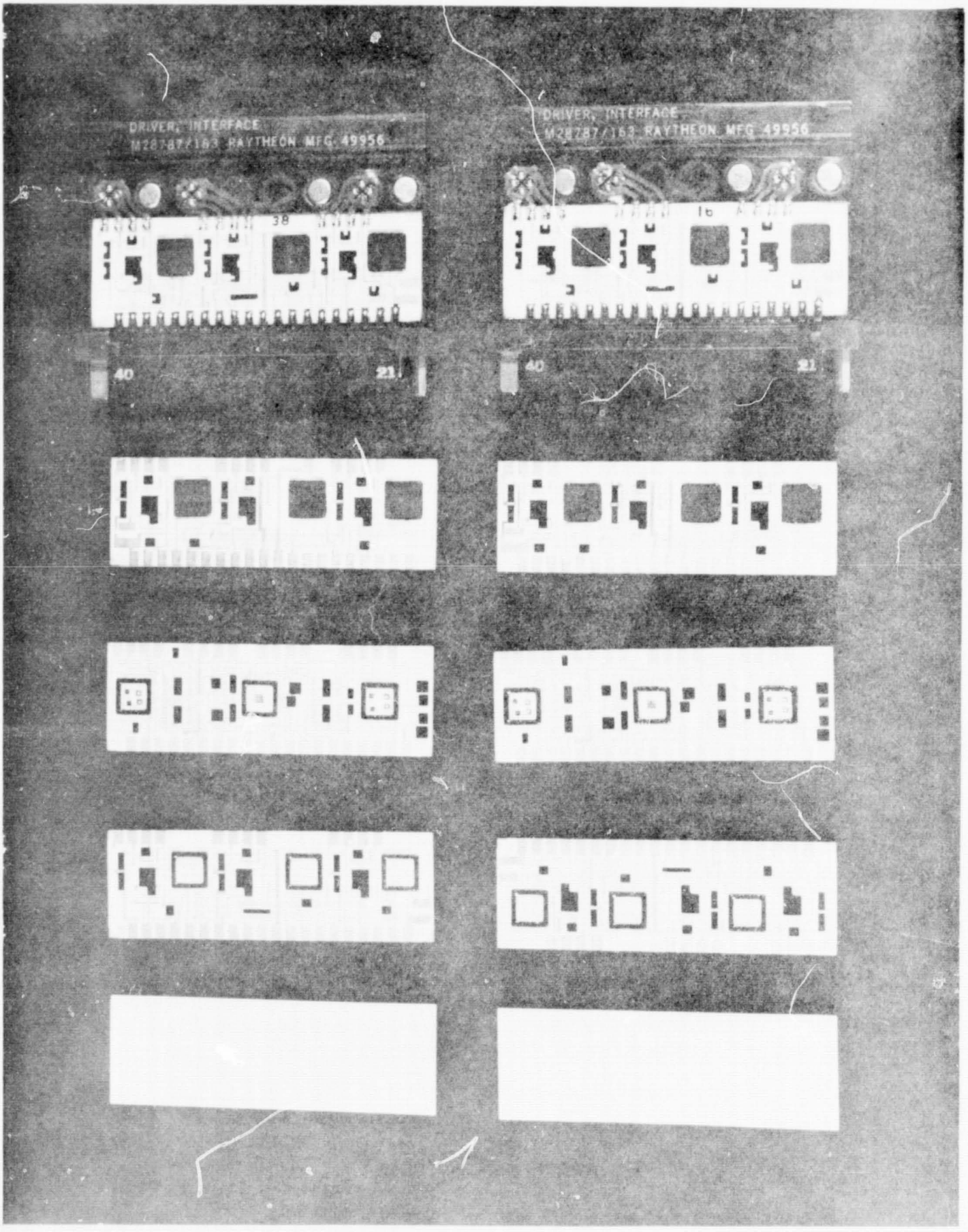
FINISHED NAFI MODULE UTILIZING TWO CLUSTER SEALED SUBSTRATES











FROM BARE SUBSTRATE TO CLUSTER SEALED MODULE

A HERMETIC SEALING PROCESS FOR LARGE IRREGULARLY SHAPED HYBRID MICROCIRCUIT ENCLOSURES

By M. R. Stahler
General Electric Space Division
Post Office Box 8555
Philadelphia, Pennsylvania 19101

TABLE OF CONTENTS

1.0 ABSTRACT

This paper describes a system for sealing vacuum baked hybrids in a dry inert atmosphere using an overlapping spot resistance weld. A unique electrode configuration and fixturing that permits sealing of large and irregularly shaped gold plated Kovar packages to the hermeticity requirements of MIL-STD-883 is discussed. Metallurgical considerations and comparisons to laser sealing are made.

Problems encountered during the development and optimization of the process are highlighted. Solutions to plating, fixturing, warpage, weld splatter and cracked bead problems are presented.

2.0 INTRODUCTION

The trend in microelectronic circuit packaging is to greater complexity and large area hybrids. The hybrids shown in Figure 1 and Figure 2 are representative of this trend. Indicators show that the hybrids of the 1980's will consist of a multilayer substrate (Ref. Figure 1) or multiple substrates (Ref. Figure 2) to which hundreds of silicon devices may be attached. For the hybrid shown in Figure 1 over three hundred devices and over three thousand 0.001 inch diameter wires are required to complete the electrical interconnections. The circuitry in both hybrids is housed in a gold plated* Kovar ® package.

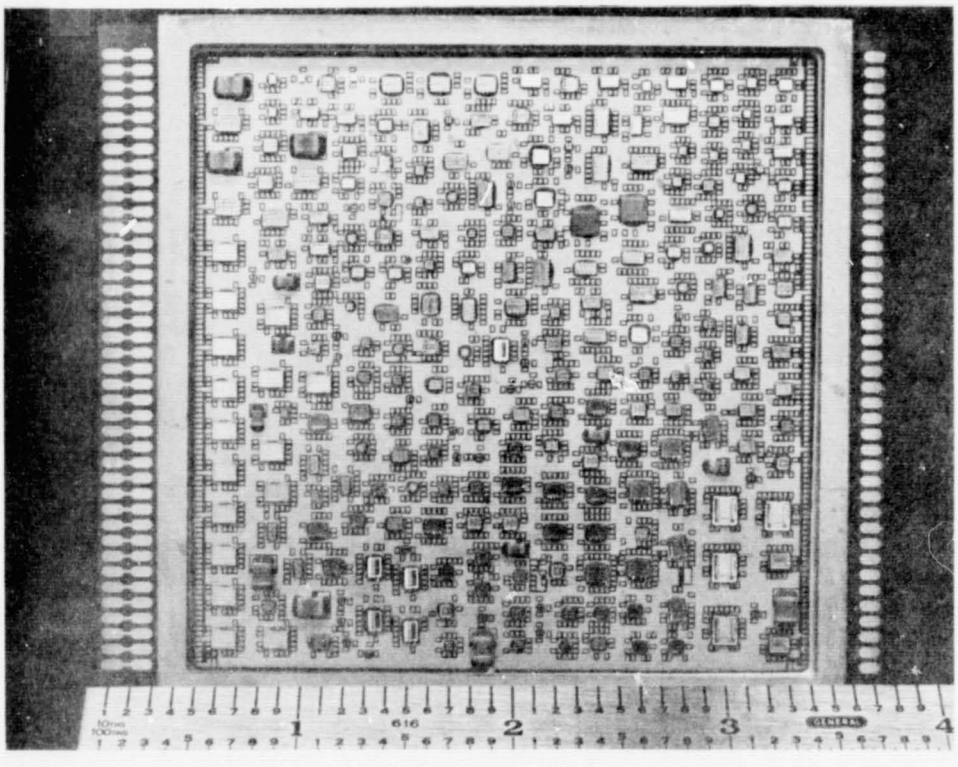


Figure 1. Data Formatter Hybrid

* Kovar is a registered trademark of the Westinghouse Electric Corporation for a Fe-Ni-Co composition.

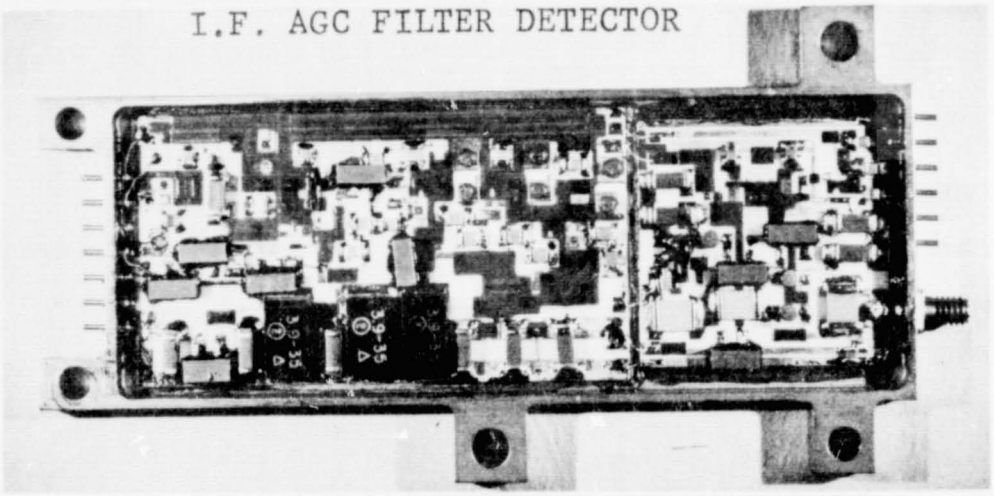


Figure 2. IF AGC Filter Detector

To achieve long reliable service life and to protect the circuitry of these large complex hybrids from deleterious environments such as moisture, the package must be hermetically sealed.

This paper deals with the sealing of these large and odd shaped packages to meet the leakage rates for hermetic seals specified in MIL-STD-883, Method 1014. There are several methods used to achieve hermetic seals and each has its own advantages and disadvantages (Ref. Table 1).

Table 1. Sealing Comparison for Large Packages

	Approx. Capital Inv.	Sealing Rate: Parts/Hr.	Maximum Component Temp.	Tooling Cost (Relative)	Repairability
dc Resistance Seam Welding	13K +	6-100	25°C	Low	Yes
Single Shot Resistance	35K +	200-600	25°C	Medium	No
Laser	25K +	10-60	100-175°C	Low	Yes
Electronbeam	50K +	50-300	25°C	High	Maybe
Furnace Solder AU/SN	5K	50-600	300°C	Medium	Maybe

However, for the large area hybrids, those greater than four square inches, resistance welding using the equipment, materials and processes described herein is highly recommended. The following advantages are realized with this sealing system:

- No preform needed
- Hermetic joints that withstand the most rigid environmental stresses are produced
- Process yields of 99 - 100% are achieved
- Circuitry is exposed to negligible process temperatures
- Reliable delidding and resealing procedures have been demonstrated
- Contamination potential is minimal
- Sealing of cover thicknesses up to 0.015 mils is readily achieved
- Package shapes may vary and sizes up to 6 by 6 inches have been successfully sealed
- No bead cracking.

These far outweigh the following disadvantages:

- Process is slow
- Equipment costs are high.

3.0 DESCRIPTION OF SEALING SYSTEM

The total sealing system is shown in Figure 3. It consists of a vacuum oven attached directly to a glove box to which a moisture monitor and an exit (inter-lock) chamber is attached. The resistance welder is housed within the glove box.

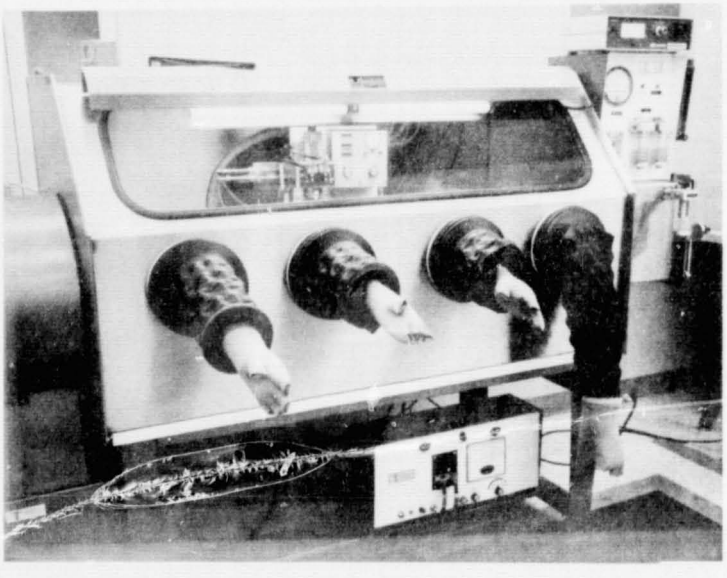


Figure 3. Resistance Welding System

Basically, two types of seam resistance welding machines exist, ac and dc. The dc welder was selected because of its great versatility. It has been used to seal packages up to 6.0 inches in length and width and lids to 0.015 inch thick, while the ac welder is limited to 3.0 inches in length and width and a lid thickness of 0.005 inch.

The Superior Varipulse dc Welder[1] operates on the capacitor discharge, stored energy principle. This welder insures reliable repetitive welds at any setting of the output level control, regardless of input voltage variations, by regulating the energy level stored in the internal capacitor banks.

The model used, combines the low distortion welding of capacitor discharge with the controllability of slope welding through the selection of 12 pulse widths ranging from 0.60 to 7.00 milliseconds through a normal impedance weld joint.

A storage range of 0.30 to 240 watt-seconds is obtained from two stored energy banks providing a choice of 120 or 240 watt-seconds operating range, each operatable in high or low voltage ranges.

A highly efficient pulse transformer is connected directly to the weld busses, which eliminates the impedance of high-current cables. Design of the welder provides efficient regulation (low ripple and extremely accurate voltage regulation). The primary circuitry giving this regulation is a two-stage transistorized amplifier which controls a solid-state regulator. No thyratrons or other vacuum tubes are used.

This welder combined with the vacuum oven, dry box and exit chamber allows the hybrid to be sealed within a monitored dry ($<$30 ppm moisture) environment without exposure of the circuitry to room environment after vacuum bake out.

A laser sealing process[2] for sealing the hybrid shown in Figure 2 was developed in parallel with this effort and comparisons will be made periodically in this report. One drawback at this time is that, with laser sealing, a vent hole is required in the cover which must be subsequently solder sealed. This adds extra processing costs and a source of contaminants such as flux and solder splash.

4.0 ELECTRODE CONFIGURATION AND FIXTURING FOR SPECIAL APPLICATIONS

The welder is extremely versatile. It may be used for parallel seam welding small packages ($\leq$ 3 inches in length and width), but with a linear converter and specially designed electrodes and fixturing, it has been used successfully to seal large and irregularly shaped packages such as the non-standard one shown in Figure 4.

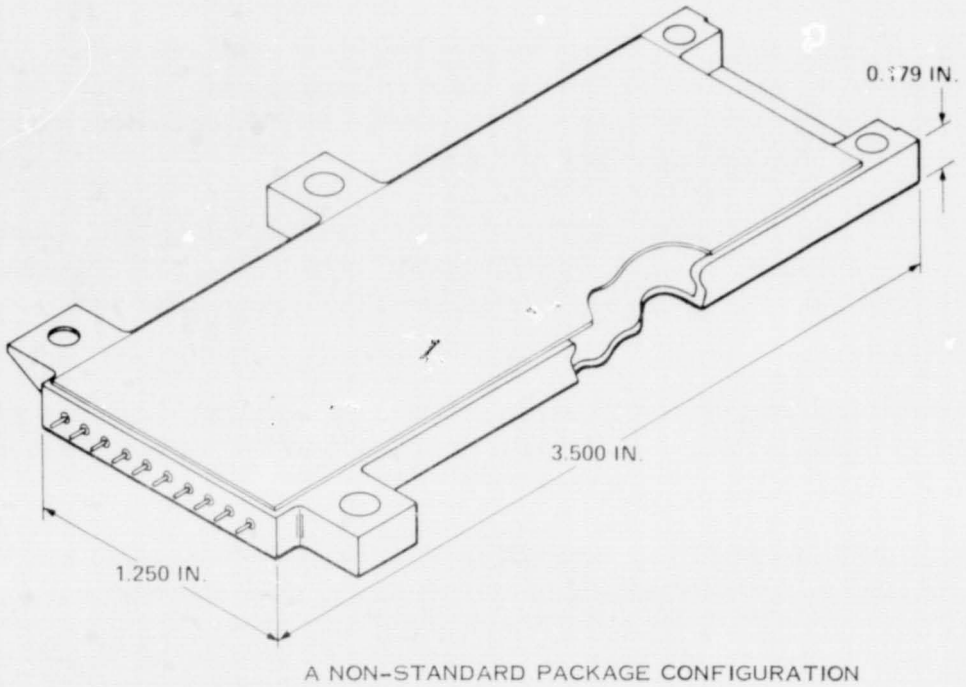


Figure 4. A Non-standard Package Configuration

The close-up view of the welder shown in Figure 5 shows the electrode configuration and package nest used to seal a package with an unusual configuration. The package is 3.5 inches in length and contains mounting lugs and coaxial connections (see Figure 5) that defy sealing with conventional electrode configurations. The electrode rides on top of the seal rim and must track within $\pm$ 0.005 inch along the length of the package.

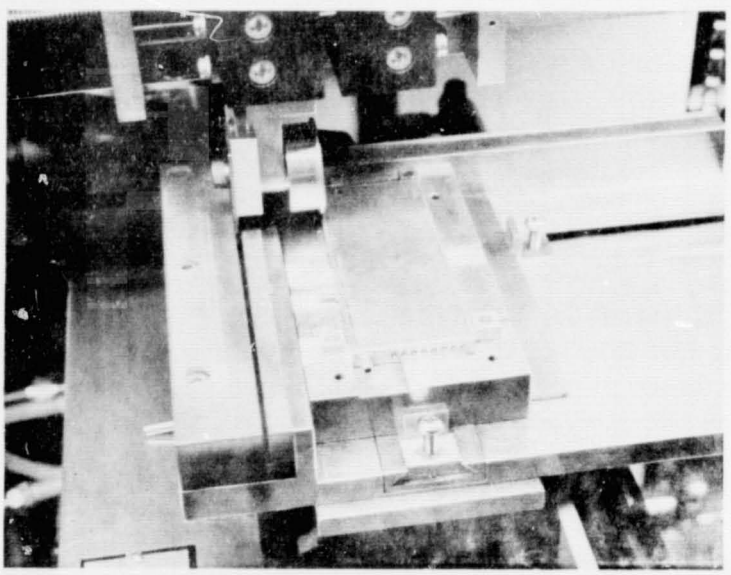


Figure 5. Close-up View of Electrode and Welding Fixture

This is accomplished using a guide attached to the electrode. The guide fits into a groove in the universal mounting fixture. Individual nests are designed to accommodate the package peculiarities. The package to be sealed is placed in the appropriate nest. The nest is then placed on the universal mounting fixture as shown in Figure 5 and secured in place with sliding stops mounted directly into the base of the fixture. The electrode is lowered onto the cover and the welding proceeds.

5.0 PARAMETER DEVELOPMENT AND QUALIFICATION

The objective of this process development effort was to achieve reliable hermetic seals using a 0.010 inch thick lid and package configuration similar to the one shown in Figure 4. After developing the electrode configuration and fixturing to compensate for the package peculiarities as described in Section 4.0, the process parameters shown in Table 2 were varied to establish optimum conditions for sealing.

Table 2. Parameter Settings for Sealing 0.010" Thick Kovar Lids

Weld Parameters	Setting
• Weld Overlap	22 Mils
• Feed Rate	60 per Minute
• Electrode Pressure	8 Pounds
• Weld Energy	120 Watt Seconds

To begin, an arbitrary electrode pressure of 16 pounds was set into the welder and the energy level varied until a strong bond was achieved. The size of the resultant spot weld measured approximately 0.040 inch in diameter and the spot overlap was then set at 22 mils to give about a 50 percent spot overlap producing a continuous seam. The feed rate was varied and 60 welds per minute was determined to be the maximum speed at which complete recovery of the power supply between welds occurred. Having fixed the spot overlap and feed rate, the pressure and energy levels were varied and peel test, temperature measurements and weld deformation were used as measurements to obtain a qualified seal with minimum package distortion and internal temperatures. The result of this development is recorded in Table 2. Cross-sectional photomicrographs were made at the selected parameter settings.

Figure 6 is a photomicrograph of a seal made at the parameter levels considered optimized. Figure 7 represents a comparable optimized laser weld[2]. It is interesting to note the difference in the nugget formation of the two sealing methods. In both cases the strength of the weld exceeded the strength of the parent metal. Figure 8 shows the result of temperature measurements within the package during sealing with both laser[2] and the dc resistance welding techniques. The results show that practically no temperature rise is experienced with the dc resistance welder.

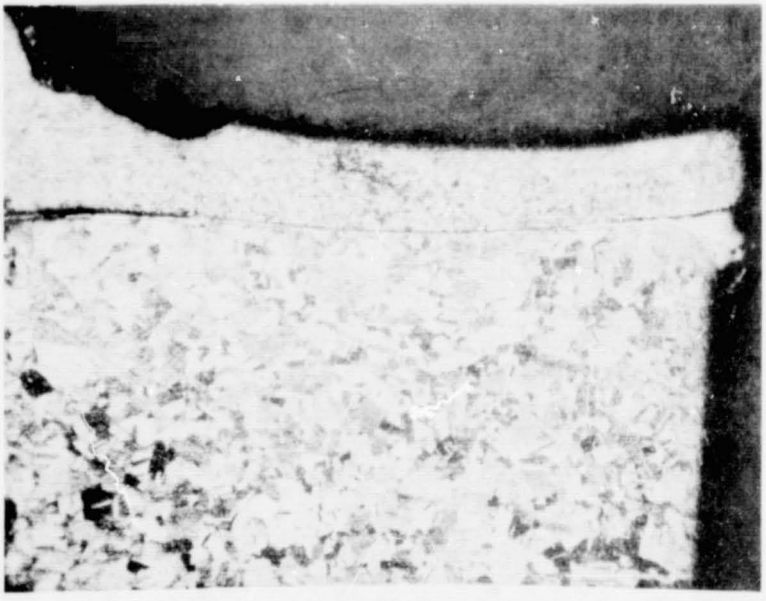


Figure 6. Cross Section of Resistance Weld

Figure 7. Cross Section of Laser Weld

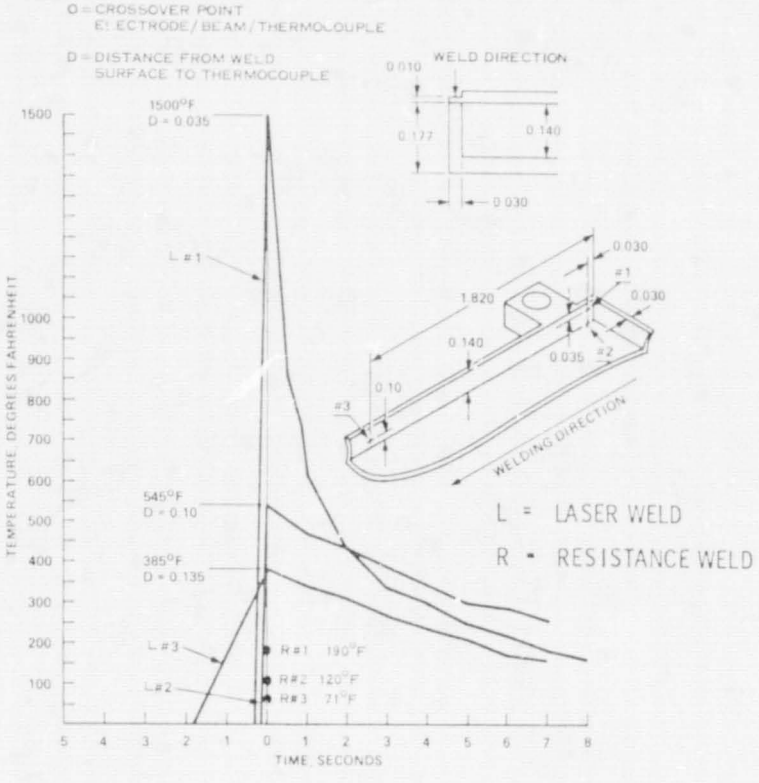


Figure 8. Temperature Measurements for Laser and Resistance Welds

Once the seal parameters were established, two "Prime" packages of each unique shape were sealed and submitted for qualification as follows:

- Map container flatness (Ref. Figure 9)
- Visual inspection of glass beads
- Weld units
- Visual inspection of weld quality
- Visual inspection of glass beads
- Visual inspection of plating and pin damage
- Map container flatness
- X-ray (Ref. Figure 11)
- Seal test per MIL-STD-883A, Method 1014 A2 and C2
- Visual inspection of glass beads
- Acceleration - 5000g's. Y1 axis 1 minute duration using modified fixture and standoffs
- Visual inspection of glass beads
- Map case flatness
- Seal test per MIL-STD-883, Method 1014 A2 and C2
- Visual inspection of glass beads
- Temperature cycle MIL-STD-883, Method 1010; Test Condition A - 30 cycles
- Visual inspection of glass beads
- Seal test per MIL-STD-883, Method 1014 A2 and C2
- Remove lids and perform internal inspection for weld splatter and loose particulate matter.

Qualification status was granted the container sealing process after successful completion of the inspection and test sequence defined above.

6.0 REPAIR PROCEDURE

It was demonstrated that a resistance seam weld which does not produce a hermetic seal can be repaired by making a second pass over the original weld. In fact, this procedure is common practice in the industry. However, if any changes have to be made to the internal electronic circuitry, the cover must be removed and a reseal made. This was accomplished successfully on conformally coated microcircuits as follows:

- The seal edge of the cover was machined to within 0.001 inch of the seal frame using a milling machine such as a Groton Mastermill and an end mill.

- A sharp pointed instrument such as a X-acto knife was then used to penetrate the cover in one corner of the package and peel it off the package.
- A water soluble maskant was then applied to cover the internal circuitry and the remnants removed from the seal frame using a fine grit paper and a Buhler grinder. This also provides a flat surface for resealing.
- The maskant was then removed with water and the hybrid assembly spray rinsed with isopropyl alcohol and dried.
- A new cover was subsequently welded in place.

7.0 POTENTIAL PROBLEMS

7.1 PLATING

Packages constructed with metals, such as Kovar and low carbon steel, require protective coatings to prevent rusting. The most widely used coatings on microelectronic packages are gold and nickel platings. The type and quality of the plating is extremely important. The following plating problems were encountered during process development and caused inability to produce reliable welds:

Problem	Cause	Corrective Action
Weak weld failed during pressure bombing.	Copper under nickel plate-copper not weldable using either laser or resistance welding techniques.	Stripped and replated.
Unable to produce a weld	Contaminants in the plating-organics and other metals in the plating baths.	Stripped and replated. Use fresh plating solutions.
Plating peeled and weld failed during pressure bombing	Poor adhesion of the plating to the base metal due to poor surface preparation.	Stripped and replated.
Brittle welds	Hard electroplated nickel-coating produced a brittle interface which cracked under 30 psi pressure.	Stripped and replated with soft electroless nickel plating and gold plating.

7.2 PACKAGE DISTORTION

Another problem encountered during development of a sealing process for the package shown in Figure 4 was package distortion. The method used to measure this distortion is shown in Figure 9. The fact that many of the packages measure 0.007 to 0.009 inch out of flatness after sealing caused some concern as to the stresses imparted to the ceramic substrates within the package. All attempts at resolving this problem through changes to the sealing process were futile. Some of the changes investigated were:

- Bolting down package during welding
- Changing direction and sequence of welding
- Reduction in lid thickness
- Lowering the electrode pressure.

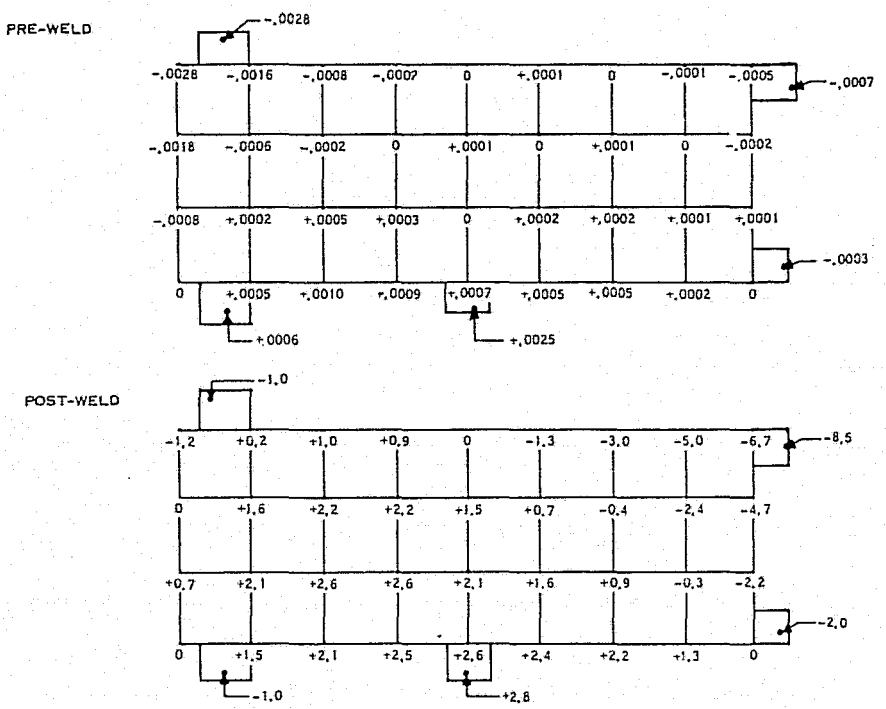


Figure 9. Mapping of Package Flatness Before and After Sealing

Since similar and even greater distortions were also encountered with laser sealed units, it was concluded that the problem was due to structural modification of the Kovar by alloying with the lid and case coatings which caused built in stresses. Figure 10 summarizes this explanation. The design of the package was found to be sensitive to small loads and temperatures. To produce distortions of the order observed it required local point loads of 1 to 2 pounds or a temperature gradient of 23°C to 0°C over the wall depth. The following design changes were made to resolve this problem:

- Increased wall thickness from 0.040 to 0.060 inch
- Added an internal lateral rib to improve the torsional rigidity.

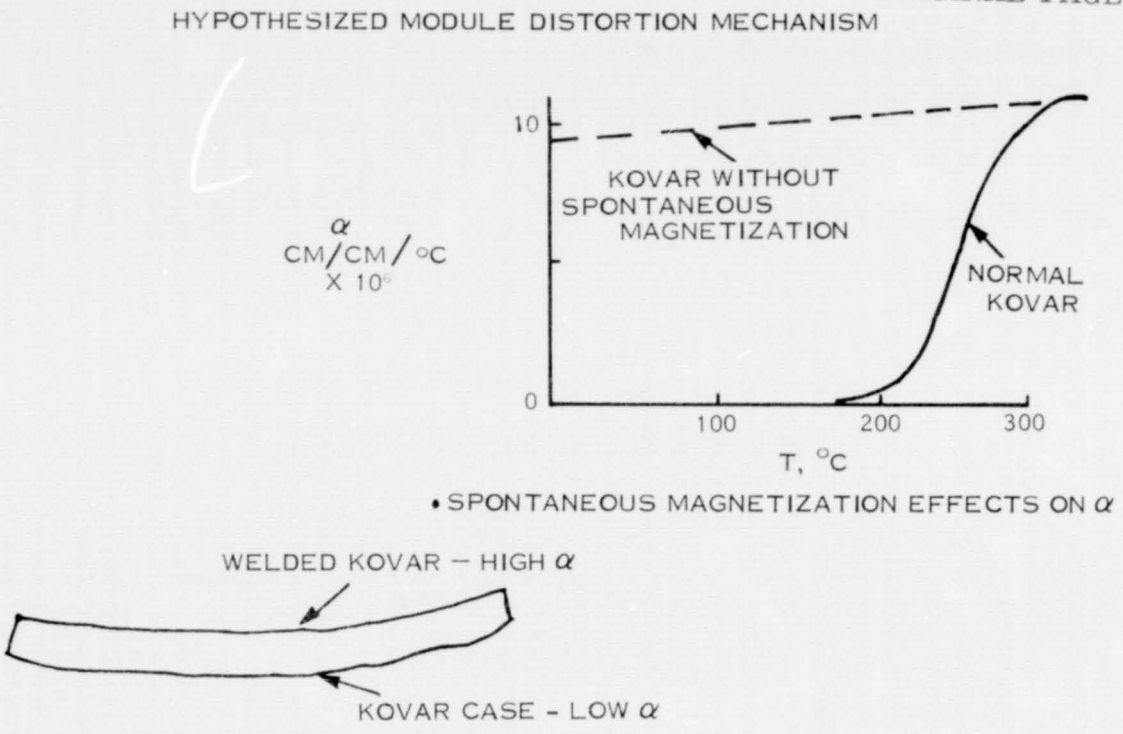


Figure 10. Hypothesized Module Distortion Mechanism Due to Weld Sealing

7.3 WELD SPLATTER

A weld splatter problem occurred on several units. This is shown dramatically in a routine X-ray of a sealed unit, Ref. Figure 11. Opening the package confirmed the splatter as seen in Figure 12. The problem occurred early in the production start up and was determined to be the result of improper electrode alignment and a "hot" weld schedule. The electrode was mistakenly positioned to track along the inner edge of the package wall. Movement of the electrode to the outer edge to allow expulsion to be directed to the outside of the package coupled with a slight decrease in weld energy resolved this problem.

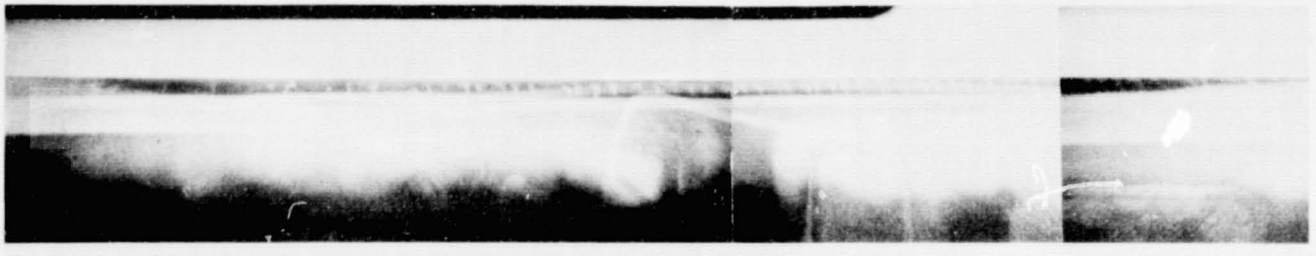


Figure 11. X-ray of Sealed Hybrid Showing Weld Splatter

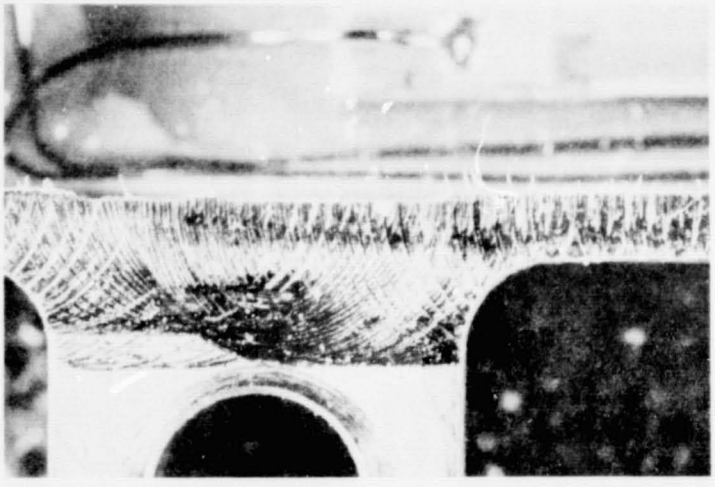


Figure 12. Visual Verification of Weld Splatter After Lid Removal

The following recommendations are made as a result of this experience:

- Seal as close to the outer edge of the package as possible. This is automatically assured in most resistance weld sealing operations.
- Use the minimum pressure and weld energy necessary for a reliable seal.
- Where possible, use stepped lids which act as a barrier to prevent expulsed material from entering the package.
- Use X-ray as a routine tool for spotting weld splatter.
- Provide the Manufacturing Engineer with sufficient material to develop an optimum weld schedule.

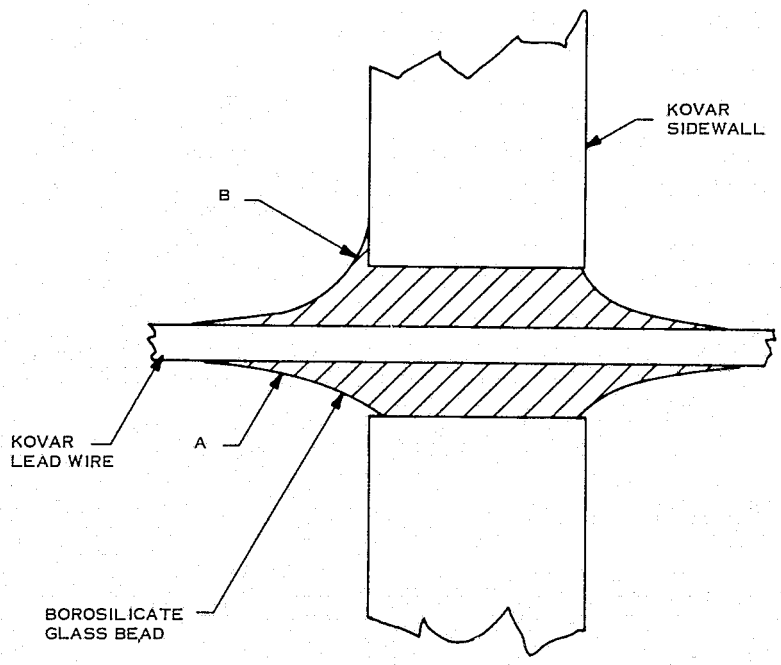
7.4 CRACKED BEADS

Nearly stress-free glass-to-metal seals (< 1000 psi residual tensile stress in the glass) can be produced with annealed Kovar and 7052 borosilicate glass. This stress is sufficiently low to insure freedom from cracking in the bead for a properly designed seal, and it should exhibit long time dependable performance (without crack formation) even under conditions of high humidity and temperature cycling.

Four potential causes of the cracks in the glass beads during package fabrication have been identified. These are (a) too rapid a cooling rate after the bead fusion or sealing operation, (b) extensive flow and meniscusing of the glass along the lead wire, (c) attack on and undercutting of the glass beads by the acids used to prepare the module cases for gold plating, and (d) improper glass bead design (Ref. Figure 13).

A very important metallurgical characteristic for good glass-to-metal sealing is the controlled oxidation of the Kovar surfaces. Bond strength, adherence and the ability to bond without pressure are enhanced by accomplishing the seal through an intermediate "Kovar oxide" which

is primarily a mixture of iron oxides. This oxide is both adherent to the Kovar and soluble in the glass and its expansion coefficient is sufficiently compatible with both. Figure 14 indicates schematically the transition of Kovar to glass in a good seal.



A & B REPRESENT POTENTIAL STRESS POINTS FOR INITIATION OF CRACKS

Figure 13. Schematic Cross-Section of Glass-to-Metal Seal

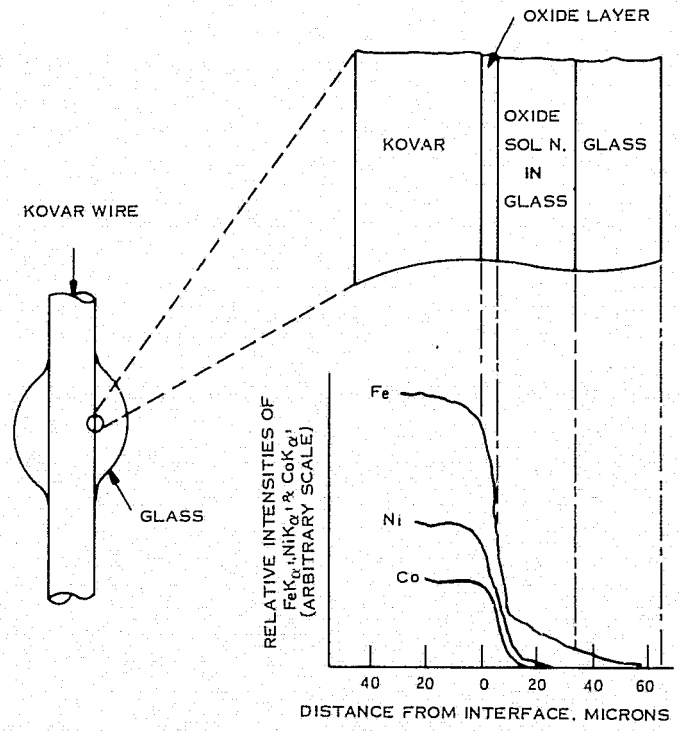


Figure 14. Transition Interface Between Kovar and Glass in Glass-to-Metal Seals

While most of the bead cracking problems were attributed to flaws in the package manufacture, deep weld penetrations, such as laser welds, too close to the beads and excessive distortion of the package walls due to poor package design and/or excessive electrode pressure and weld energy may also result in bead cracking.

It is recommended that a package wall thickness of $\geq$ 0.040 inch and bead location $\geq$ 0.040 inch below the sealing surface be employed in packages to be weld sealed. Bead cracking problems due to the sealing process are easily resolved providing a good package design and properly constructed package are supplied.

8.0 PERFORMANCE

As can be seen from the data summarized in Table 3, the performance of this system to date has been outstanding. With the ability to repair leakers, a 100% yield is achieved.

Table 3. Performance to Date

•	Hybrids Sealed	-	110
•	Seals Passed Environmental Tests	-	104
•	Seals Passed After Touch-Up Seal	-	110
•	Hybrids Delidded and Resealed	-	9
•	Seals Passed After Delid and Reseal	-	9

9.0 SUMMARY AND CONCLUSIONS

- A reliable system for sealing large and irregularly shaped microcircuit enclosures using a dc resistance welder has been demonstrated.
- Yields of 100% for seals that meet the hermeticity requirements of MIL-STD-883 are attainable with minimal reweld.
- Component temperatures remain low ($< 100^{\circ}F$) during the sealing process.
- Reliable delidding and resealing processes for conformally coated hybrids have been developed and demonstrated.

10.0 REFERENCES

1. Operating Manual R1160-Model 160 Automatic Spot Seamwelder, Superior Welder Mfg. Corp., New Bedford, Mass.

2. Micro-circuit Flatpack Sealing by Laser Welding, H. N. Krishnaswamy and V. E. Boccelli, GE/RESD, Phila, Pa. Presented at National Symposium of the Society for the Advancement of Material and Process Engineering, April 26, 1977, San Diego, Calif.

METHODS FOR MEASURING PLATING THICKNESSES ON TAB LEAD FRAMES

by
Michael P. Hagen
Honeywell Avionics Division
St. Petersburg, Florida 33733

ABSTRACT

Plating three layer tape lead frames, used for Tape Automated Bonding (TAB), offers a challenge to the electroplater because of non-uniform topography. Each lead frame contains large (typically .05 x .05 inch) flat test pads located around the perimeter of the frame. These test pads are electrically connected to the bondable lead frame fingers which extend into an area in the center of the frame called the feature hole. The feature hole exposes these fingers to plating on all sides, while the test pads are exposed on only one side. In addition, the fingers are small in cross section (typically .003 x .0015 inches). Recent thickness measurements indicate that plating around the lead frame fingers is nearly twice as thick as that on test pad areas. Procedures and equipment have been developed for measuring the thickness of the deposited material. Discussion is centered on the data obtained using the various measurement techniques and equipment.

INTRODUCTION

A major step toward automated assembly of hybrid microcircuits can be accomplished by Tape Automated Bonding.[1, 2] For several years TAB has been used by I. C. manufacturers to cut production costs, but recently there has been considerable interest in TAB from the standpoint of increased reliability. Thermocompression bonding of I. C. chips to gold plated lead frames on tape may be used to increase bond reliability for military applications.[3, 4] Verification of plating thickness then becomes an important parameter. The thickness of electro-deposited metal is predicted using Faraday's Law which states: "The weight of an element liberated at an electrode is directly proportional to the quantity of electricity passed through the system". Metals, however, do not deposit uniformly over a non-uniform topography. Rather, they tend to deposit at higher rates on peaks due to high local electric fields and lower rates on adjacent larger planar surfaces. The TAB lead frame is an example of non-uniform topography (see Figure 1). Figure 2 contains sections of the lead frame and shows the non-uniformity encountered in electroplating.

Each lead frame contains large (typically .05 x .05 inch) flat test pads located around the perimeter of the frame. These test pads are electrically connected to the bondable lead frame fingers which extend into an area in the center of the frame called the feature hole. The feature hold exposes these fingers to plating on all sides, while the test pads are exposed on only one side. In addition, the fingers are small in cross section (typically .003 x .0015 inches). Since the lead frame fingers are the active parts used in the TAB operation, they are the parts which must be measured for plating thickness. The purpose of this paper is to describe methods and the corresponding results obtained for plated lead frame thickness measurements.

EVALUATION

The plating thicknesses evaluations compared the following conditions:

1. Between lead frame fingers and test pads on a lead frame.
2. Between different lead frames (i.e., frames of different patterns and areas).
3. Between lead frame fingers and test coupons (i.e., rapid process control feedback).
4. Between the theoretically predictable nominal and the actual gold plating thickness.

---

[1]S. M. Stuhlbarg, "Interconnect Metallization for Automated Bonding", AIME Electronics, June 1976

[2]C. Burns, A. Keizer and M. Toner, "Beam Tape Automated Assembly of Dips", Nepcon/West, 1975

[3]R. G. Oswald and W. R. Rodrigues de Miranda, "Application of Tape Chip Carrier Technology to Hybrid Microcircuits", Solid State Tech. 20, 3 (1977)

[4]J. Montante, W. R. Rodrigues de Miranda and R. Oswald, "Wafer Bumping for Tape Automated Bonding", To be Published ISHM 1977, Baltimore Md.

The nominal gold plating thickness selected was to be 100 micro-inches. This thickness was chosen to yield a suitable gold deposit for thermocompression bonding the lead frame to soft gold bumps on the I. C. chip.

SAMPLE PLATING

Samples were first cleaned using methods similar to those used to clean conventional printed circuit boards. This included a 5 minute immersion in Neutraclean 68[5] followed by a 15 second dip in Actane[6] and finally 30 seconds in 25% sulfuric acid. A 3 stage cascade deionized water rinse was done between each of the above cleaning steps. The copper surfaces were then activated with a gold strike from an Aurobond TN[7] plating solution and rinsed. All samples were plated in a Temperex HD[7] gold plating bath. A pH of 4. 25 $\pm$ 0. 25 and specific gravity of 1. 14 $\pm$ 0. 06 was maintained throughout the investigation. The temperature of the bath was 70°C and a plating current density of 4 amps per square foot was used to deposit the softest gold possible. This was done to enhance thermocompression bonding. Finally, the samples were rinsed as above and blown dry with dry nitrogen.

Careful handling of the lead frames becomes an important consideration during the cleaning and plating stages of this process because of their fragile nature.

A lead frame plating fixture was designed that holds three six-frame strips. This fixture provides protection during processing and also flattens the lead frame strips so uniform processing can be achieved. This fixture also made the use of test coupons possible. Test coupons are commonly used in the plating industry to substitute a platable substrate material for production parts. Testing deposited material can then be done without destruction of production hardware.

MEASUREMENT METHODS

Three measurement methods were evaluated, one of which was to be selected as a process control. In addition, the three methods were evaluated to determine which best showed the differences in plating rates associated with topographical variations in the base material.

---

[5]Shipley Co., Newton, Mass. 02162
[6]Enthone Inc., New Haven, Conn. 06508
[7]Oxymetals Ind. Corp. , Nutley, NJ 07110

The three methods were:

1. Microscopic determination of potted and sectioned samples using a metallograph.[8]

2. Physical determination of step height on a masked test coupon using a stylus profilometer.[9]

3. Microscopic determination of a step on a masked lead frame finger.

These methods shall now be described in detail.

SAMPLE PREPARATION

Samples were prepared for measurement on the metallograph. Cleaning and plating was followed by a standard epoxy potting and polishing method. This resulted in transverse and longitudinal sections through the lead frame fingers and longitudinal sections through the test pads.

Another sample was prepared for measurement on a microscope. The tips of the lead frame fingers were masked with platers lacquer[10] then cleaned and plated as above. The lacquer was stripped off the fingers with acetone leaving a visible step from the copper up to the gold.

Three types of test coupons were prepared: copper clad polyimide sheet, alumina sputter coated with gold and glass sputter coated with gold. A portion of each of these samples was masked with 0.1 square inches of tape[11], then cleaned and plated as above. When the tape masking was removed a step in the plating resulted which was measured with a stylus profilometer. In this case, the plating thickness was measured on the test coupons and compared to that on lead frames.

MEASUREMENTS AND RESULTS

This evaluation revealed the average plating thickness around the narrow lead frame fingers was nearly twice as thick as that on the test pads, 128 micro inches versus 86 micro inches. Also, the average plating thickness on the lead frame fingers is about 30% thicker than original calculations indicated, 128 micro inches versus 100 micro inches. (See Figure 4 and Table 1). This can be accounted for by variations in throwing power of the plating solution due to variations in electrical field strengths associated with non-uniform substrate topography.

---

[8]MeF, Riechart, Austria
[9]Dektak, Sloan Technology Corp., Santa Barbara, CA 93103
[10]Microshield, Michigan Chrome and Chem., Detroit, Mich, 48213
[11]Electrical, Scotch Brand. (Red), 3M Co., St. Paul, Minn. 55101

Masking the lead frame fingers with platers lacquer (Figure 3) resulted in a ridge of plated gold at the edge of the microshield which distorted the plated step. The distortion made thickness measurements inaccurate and unusable for this evaluation.

Copper clad polyimide and alumina test coupons were not flat enough for accurate and repeatable determination of plating thickness, with a profilometer, as shown in Figures 5 and 6. The glass slide (Figure 7) was very flat and repeatable measurements could be made. However, very poor coorelation existed between thickness measurements made on test coupons and that made on lead frame fingers. Average plating thickness on test coupons was 55 micro inches compared to an average of 128 micro inches on lead frame fingers. (See Figure 4 and Table 2).

The potting and sectioning approach, while being the most time consuming, was also the most accurate and repeatable compared to the predicted nominal plating thickness and to the test coupon technique (See Table 2 and Figure 4). Table 2 shows good repeatability between the 5 lead frame types.

CONCLUSION

The preferred method of plating thickness measurement on lead frames, as born out by this evaluation, is the sectioning and metallograph approach. The lead frame fingers are the active elements used for thermocompression bonding and must therefore be accurately electroplated. It was shown from the data that significant differences existed in plating thickness measured on the fingers and test pads. Since sectioning the fingers is a destructive test it must be limited to samples on a lot basis for plating process control. In summary, the primary plating process controls are: plating solution temperature, pH, gold content, specific gravity and plating current. The primary process controls when used in conjunction with the preferred method of plating thickness measurement will ultimately result in repeatable Tape Automated Bonded assemblies.

ACKNOWLEDGEMENTS

The author wishes to express his thanks to the TAB team for their cooperation and especially to James M. Montante, Ronald T. Ogan and William R. Rodrigues de Miranda for their help in preparing this paper.

TABLE 1. PLATING THICKNESS SAMPLES

Sample Number	Lead Frame No.	Plating Thickness ($\times 10^{-6}$ inches) Fingers L.S.	Fingers T.S.	Test Pad L.S.
1	8087	122,	115	
2	8090	140,	154	
3	8086	111,	143	
4	8086	125,	107	
5	8087	122,	104	
6	8096	118,	115	97
7	8088	168,	154	75
Average Plating Thickness ($\times 10^{-6}$ Inches)		129	127	86

TABLE 2. PLATING THICKNESS ON VARIOUS BASE MATERIALS

Sample	Base Material	Gold Plating Thickness ($\times 10^{-6}$ Inches)	Average Plating Thickness ($\times 10^{-6}$ Inches)
8	Copper Clad Polymide	60	
9	Gold Sputtered on Aluminum	60	55
10	Gold Sputtered on Glass	46	
1-7	Average Lead Frame		128

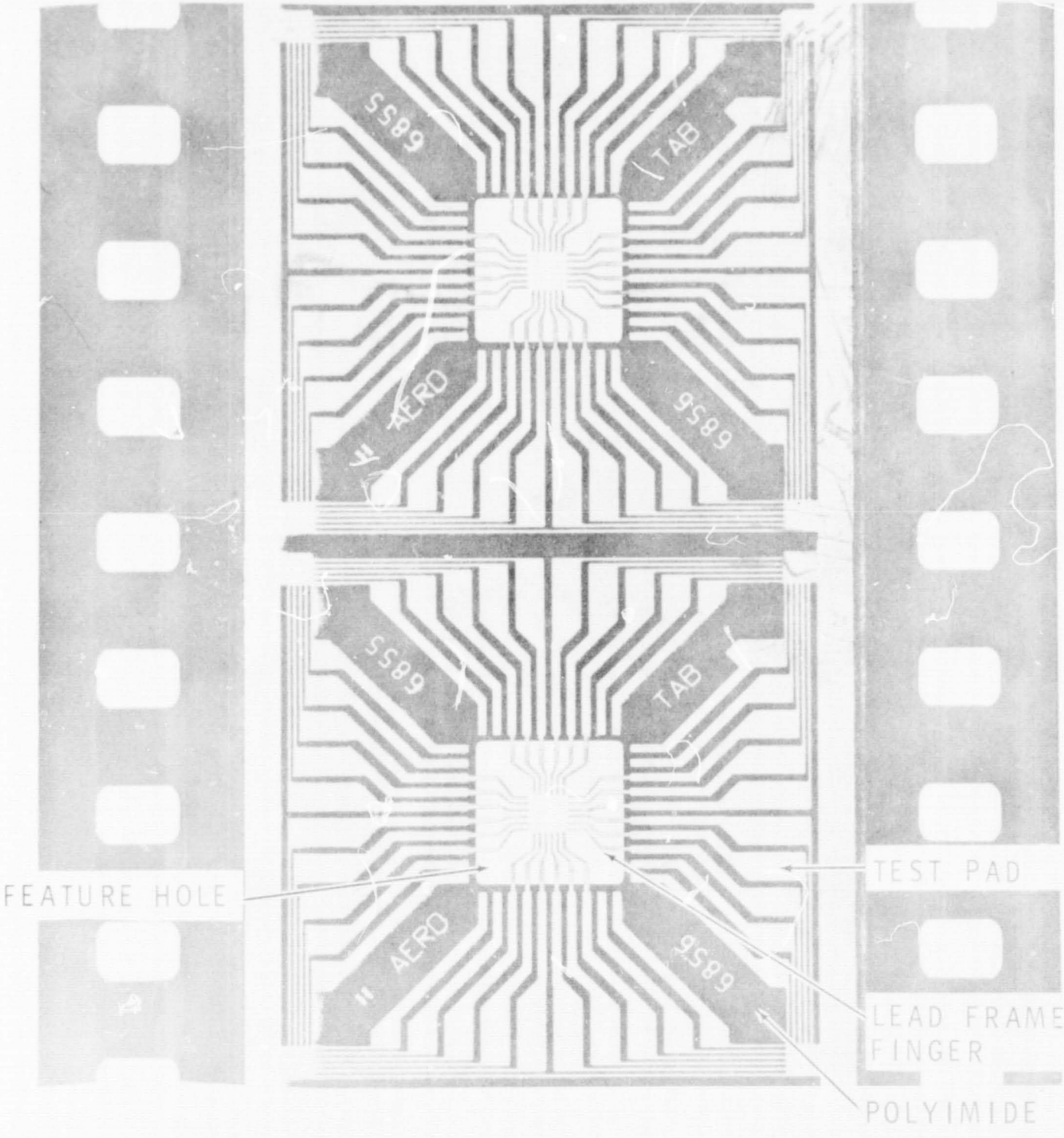
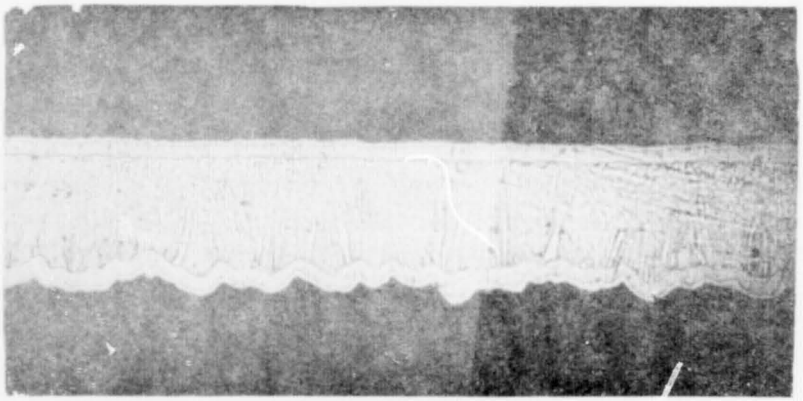
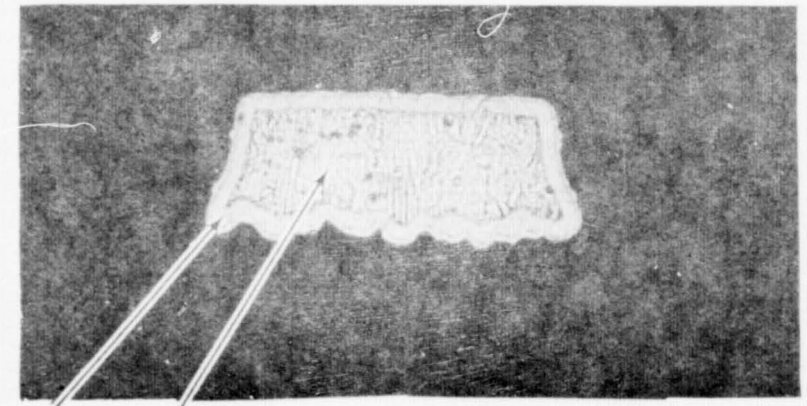


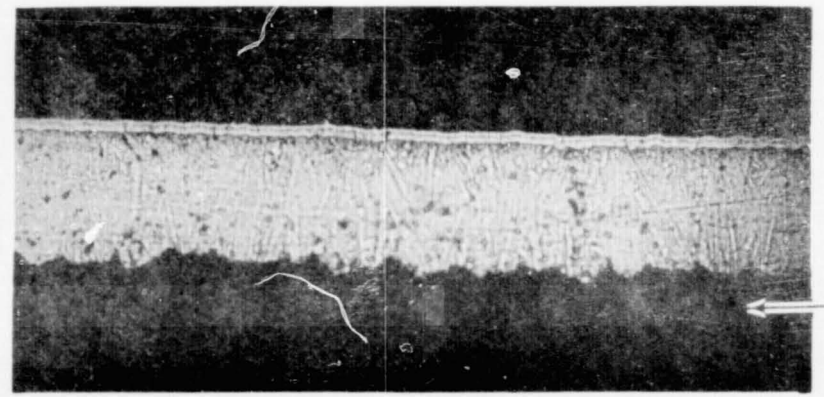
FIGURE 1. LEAD FRAME ON 35mm TAPE



FINGER, LONGITUDINAL SECTION



FINGER, TRANSVERSE SECTION



PAD LONGITUDINAL SECTION

FIGURE 2. DIFFERENCE IN PLATING THICKNESS
BETWEEN TYPICAL LEAD AND PAD

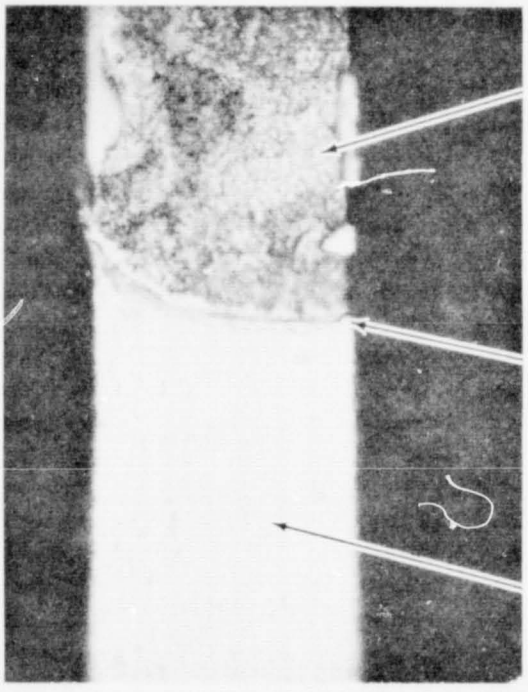


FIGURE 3. LACQUER MASKED LEAD

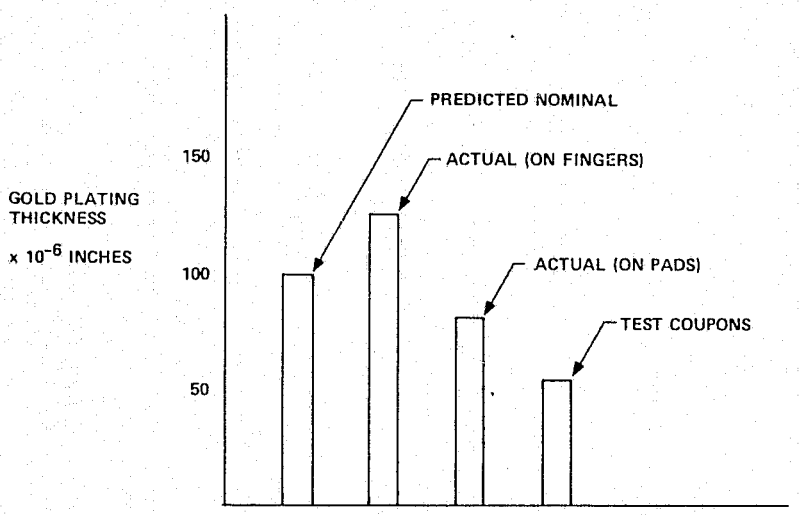
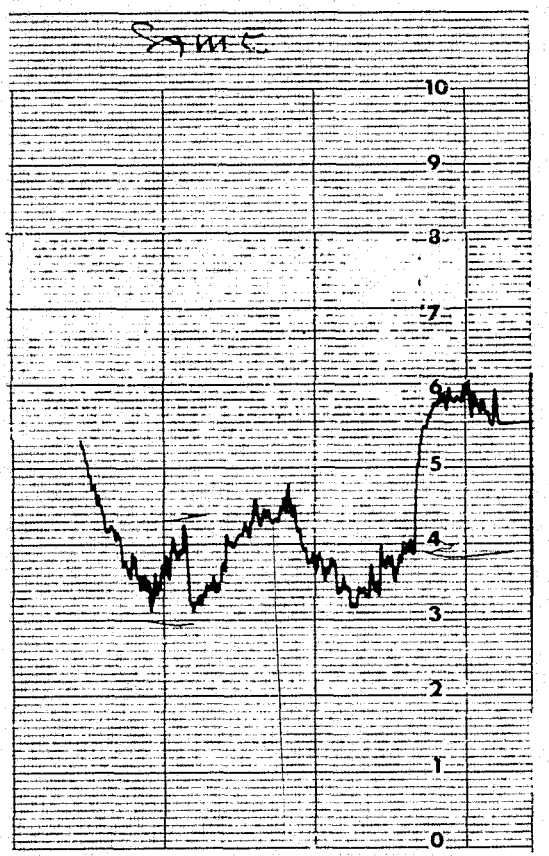


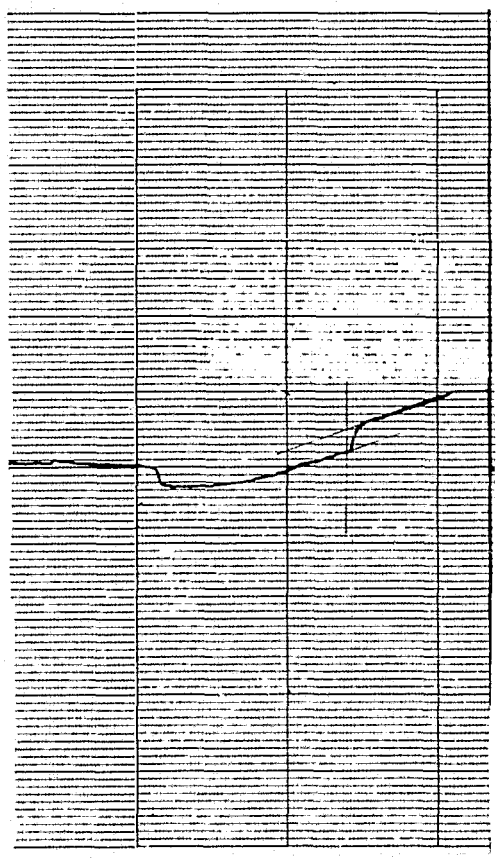
FIGURE 4. COMPARISON OF PLATING THICKNESS ON VARIOUS BASE MATERIALS AND THAT OF PREDICTED NOMINAL

PROFILOMETER CHARTS



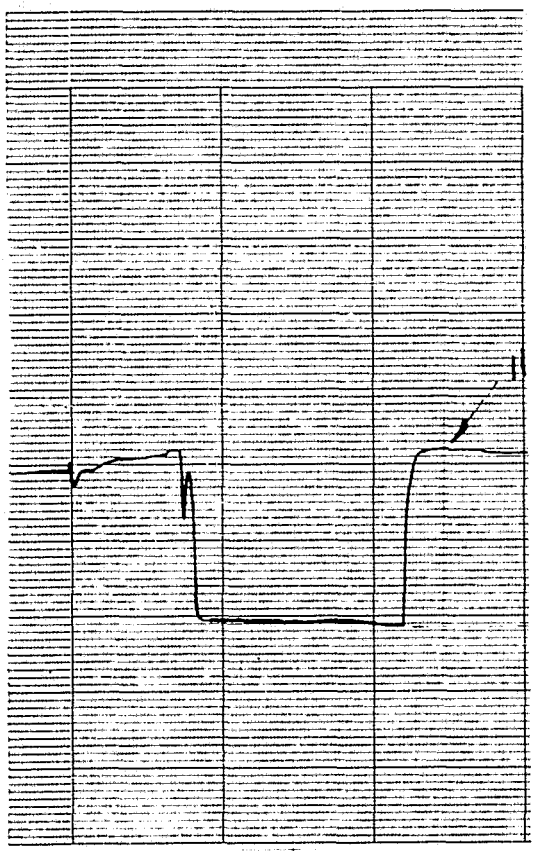
100 KÅ FULL SCALE

FIGURE 5. COPPER CLAD POLYIMIDE



500 KÅ FULL SCALE

FIGURE 6. ALUMINA



50 KÅ FULL SCALE

FIGURE 7. GLASS SLIDE

LASER DRILLING OF VIAS IN DIELECTRIC FOR HIGH DENSITY MULTILAYER LSHI THICK FILM CIRCUITS

T. COCCA

S. DAKESIAN

RAYTHEON COMPANY

WEST ANDOVER, MA. 01810

Introduction

A high density multi-level thick film digital microcircuit, used for large scale integration, is being designed by Raytheon. This circuit employs 4 mil lines, 4 mil spaces and requires 4 mil diameter vias. Present screened and fired thick film technology is limited on a production basis to 16 mil square vias. This paper describes a process whereby 4 mil diameter vias can be fabricated in production using laser technology.

Experimental Objectives

a. General - Provide a process to produce 4 mil diameter vias for conductor patterns which have 4 mil lines and 4 mil spacings.

b. Specific - Determine the feasibility of utilizing laser technology to produce 4 mil diameter vias.

Discussion

A via is an electrically conducting path, used in multi-level circuit fabrication, to connect two conducting levels which would otherwise be electrically isolated by dielectric material.

Conventional vias are produced by printing thick film dielectric pastes, through a screen, over conductor layers. This process, for producing 4 mil diameter vias, is handicapped or limited by the material's properties. In order to print small vias and prevent them from closing during printing or firing, certain thixotropic properties are required for the thick film paste and certain viscosities are required at the firing temperatures. If the paste viscosity satisfies the requirement of maintaining a small via (4 mil diameter), it might also prevent trapped air bubbles from escaping resulting in pin holes. Viscosity at the firing temperatures suffers the same dilemma. Therefore, if the dielectric material could be blanket coated, one could more easily attain a dielectric free of pin holes. The 4 mil vias could be subsequently formed by an etch process (chemical or laser). This approach was investigated at Raytheon and the laser etching technique proved to be more feasible than chemical etchback.

The key to laser etching of vias for multi-level circuits is a process whereby the dielectric material is easily vaporized but the underlying gold is not. The factors controlling this process are the need to:

a. Print as uniform a thickness of dielectric as possible.
b. Provide consistent laser energy for each pulse.
c. Control the level of laser energy such that it is sufficient to vaporize all the dielectric but not enough to vaporize any significant amount of the underlying gold.

The dielectric used is Dupont's 9865 (Black).

The following are some of the material properties of the dielectric:

a. Composition and approximate concentrations

1) Barium and Silicon Oxides - 30% by wt. each

2) Titanium, Aluminum and Zinc Oxides 10% by wt. each

3) The remaining 10% contain Iron, Chromium, Cobalt & Calcium as oxides.

NOTE: The Iron compound provides the black pigment It has a spinal structure. The basic formula is Fe_3O_4 with Co and Cr substituting in the crystal lattice for Fe^{+2} and Fe^{+3} respectively.

b. The absorption of the 1.06 micron wavelength radiation is efficient due to the presence of the black pigment.

c. Thermodynamic Information.

Since the high temperature chemistry of Dupont's 9865 dielectric is not known, a crude estimate of 100,000 cal/mole was used as the heat of vaporization.

The underlying conductor is fritless gold. The following are some of the material properties:

a. Gold is reflective to the YAG laser radiation.

b. Gold has very good thermal conductivity.

c. Thermodynamic Information.[1,2]

Melting Point = $1336^{\circ}K$
Boiling Point = $2933^{\circ}K$
Heat of Fusion = 3,030 cal/mole
Heat of Vaporization = 74,200 cal/mole
Heat Capacity = $5.66 + 1.24 \times 10^{-3}T$ up to $1336^{\circ}K$
Estimated Energy to vaporize one mole of gold = 87,000 cal

(The heat capacity formula, which is valid only up to $1336^{\circ}K$, was used for the temperature of $2933^{\circ}K$).

A Raypak digital microcircuit was used as the experimental vehicle to prove feasibility of laser etching of the dielectric material. The circuit has two conductor levels insulated with a dielectric and has thirty-six vias.

Blanket coats of Dupont's 9865 black dielectric were screen printed on conductor patterns of fritless gold. High quality substrates, lapped flat and parallel, were used to insure uniform thickness. Samples were laser etched such that 1 pulse would create 1 via. This pulse required less than 50 millijoules of energy. The focal point of the laser was .5 mm above the work plane so that the power density diminished as the beam penetrated (Figure 1). The height of the focal point above the work plane was not fully optimized but was satisfactory for the power settings used. Once the laser energy output is adjusted so that each pulse completely etches 1 hole (via), the etching is consistent and uniform for that particular lot of material and dielectric thickness.

[1]American Institute of Physics Handbook - Contributing Editors, McGraw-Hill Book Company, Inc. 1957 - Section Table 4-130 thru 4-159.

[2]Wicks, G.E. & Block, F.E. - Thermodynamic Properties of 65 Elements - Their Oxides, Halides, Carbides, Nitrides - Bureau of Mines Bulletin 605, 1963

A crude calculation of the energy required to remove the volume of a 4 mil diameter via of dielectric material was 5 millijoules. The calculated energy to remove the underlying gold at the via site is 4 millijoules. However, the actual energy generated by the laser beam for producing a via was 42 to 47 millijoules. Energies under 42 millijoules did not remove enough dielectric and energies over 47 millijoules removed too much underlying gold. This energy is measured with a calorimeter, Model No. 100, Thermopile, Harden Company.

These empirical results show that 10 times more energy must be supplied by the laser than is indicated by the calculations. This information implies that the calculations are off by an order of magnitude or that only 10% of the laser energy is absorbed by the material. Further work needs to be done in this area. In the meantime, the laser settings must be arrived at by empirical means.

Description of the Process

The following is a brief description of the process used to prove the feasibility of laser etching as a means of producing 4 mil diameter vias.

a. A blanket coat of fritless gold Electro-Oxide 6980 was screened on a lapped substrate and fired. The thickness of the underlying gold was 5-7 microns approximately one half of the usual thickness to simulate a worst case situation. Thus with the normal 12 to 15 microns of gold there would be at least a 5 micron safety factor during laser etching.

b. The gold conductor was etched using conventional chemical etch back techniques.

c. Dielectric (Dupont No. 9865) was screen printed using special artwork. The artwork provides blanket coating except for very large via areas. Two screen printings were used with separate firing.

d. The vias were then laser etched using a Pulsed YAG laser. A laser with a programmable beam positioner would be used for production.

e. The top conductor gold Dupont 9791 was screen printed and fired.

f. Finally, the collar glass was screen printed and fired.

See Figures 2 and 3.

Units processed were then electrically tested for continuity and isolation; all passed. One substrate was assembled with three (3) beam leaded sixty (60) gate arrays. The assembly passed all electrical tests prescribed for a conventionally processed unit.

A magnified view at the vicinity of the beam lead site is shown in Figure 4 with the standard 16 mil square via holes. Exactly the same area is shown in Figure 5 with the laser etched 4 mil dia via holes. Note that the 4 mil lines at the beam lead site are approximately equal to the diameter of the via holes.

A cross-section was made of a via and shows continuity of the two conducting layers (Figure 6).

A Scanning Electron Micrograph of a via hole was examined and shows melting of the dielectric at the via walls (Figure 7).

Conclusion

It has been proven that laser etching can be used as a powerful manufacturing tool to create vias for high density multi-level circuits. The 4 mil diameter vias produced by laser etching are approximately 1/20 the area of the 16 mil square vias presently in production.

It is recognized that much more work needs to be done to improve the laser energy absorbing characteristics of the dielectric material without compromising it's high quality. Also, a better understanding of laser etching is in order.

NOTE: The "laser etching" process for producing vias in multi-level circuits is patent pending.

Acknowledgements

1. Dr. D. Whitehouse - Raytheon, Waltham, Mass.
2. Failure Analysis/Metallurgical Lab - Raytheon, West Andover, Mass.
3. M. Ohanian - Raytheon, West Andover, Mass.
4. Dr. M. Popowich - Dupont Electronic Material Division, Niagara Falls, New York
5. Dr. L. Hoffman - Dupont Electronic Material Division, Wilmington, Delaware

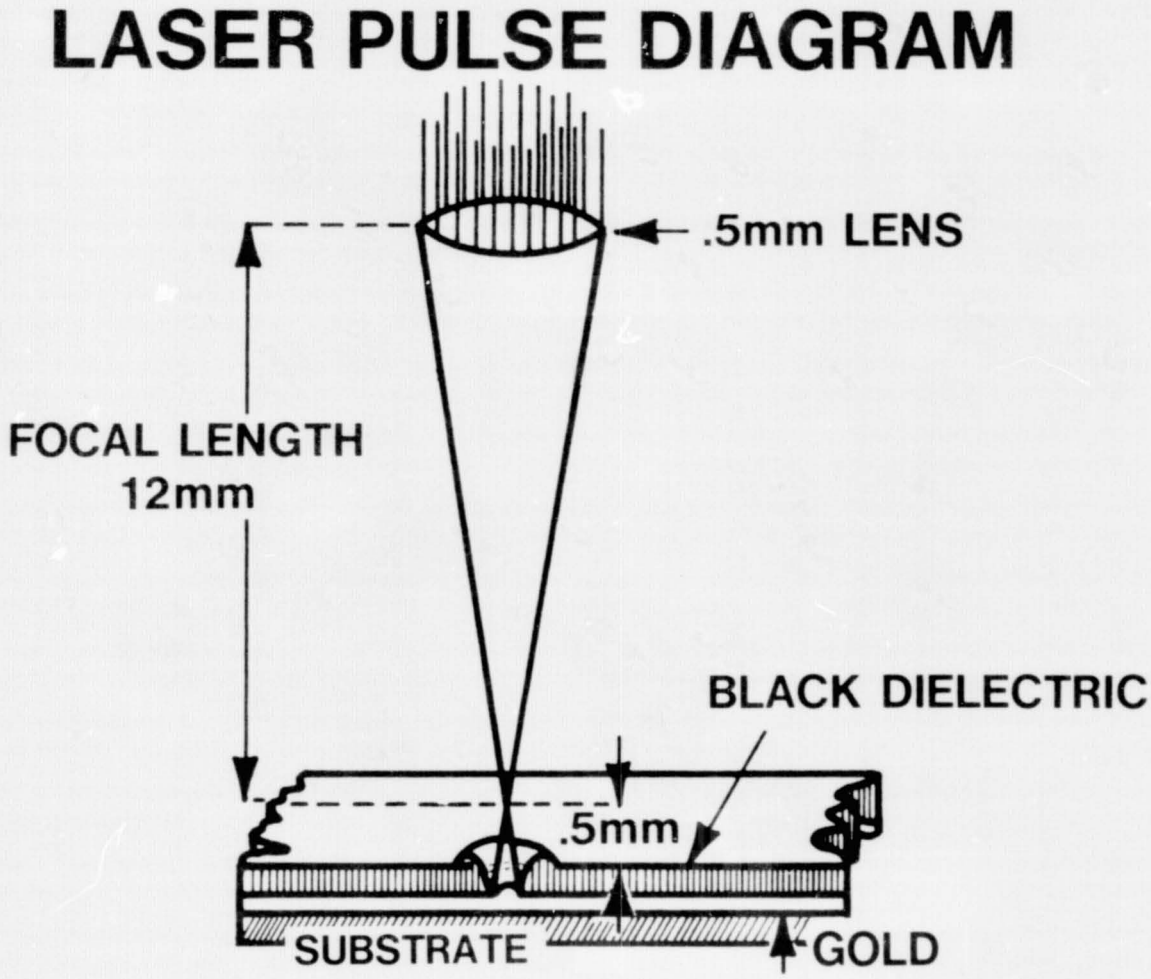

LASER PULSE DIAGRAM
.5mm LENS
FOCAL LENGTH
12mm
BLACK DIELECTRIC
.5mm
SUBSTRATE
GOLD

FIGURE 1

FIGURE 2

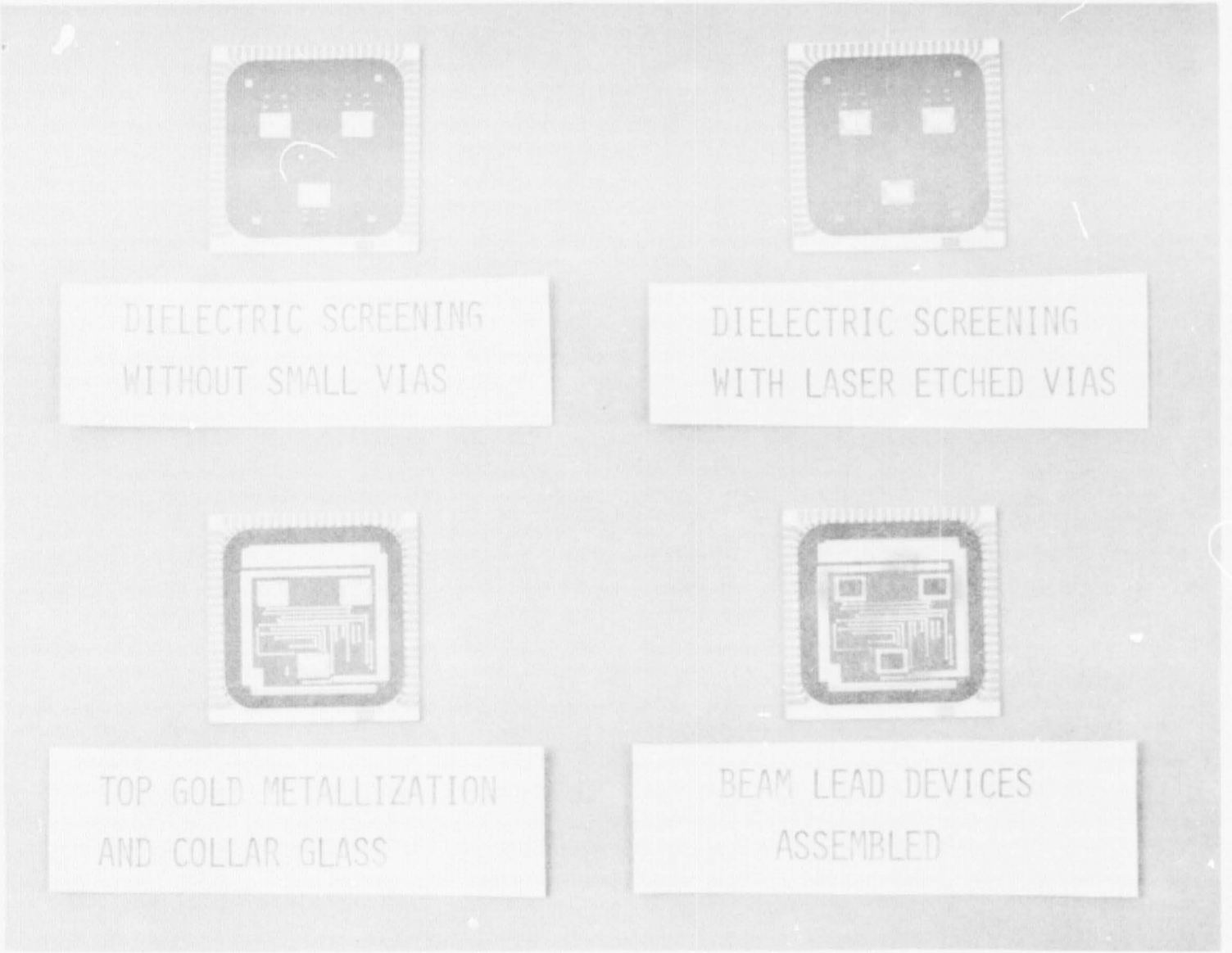

DIELECTRIC SCREENING
WITHOUT SMALL VIAS
DIELECTRIC SCREENING
WITH LASER ETCHED VIAS
TOP GOLD METALLIZATION
AND COLLAR GLASS
BEAM LEAD DEVICES
ASSEMBLED

FIGURE 3

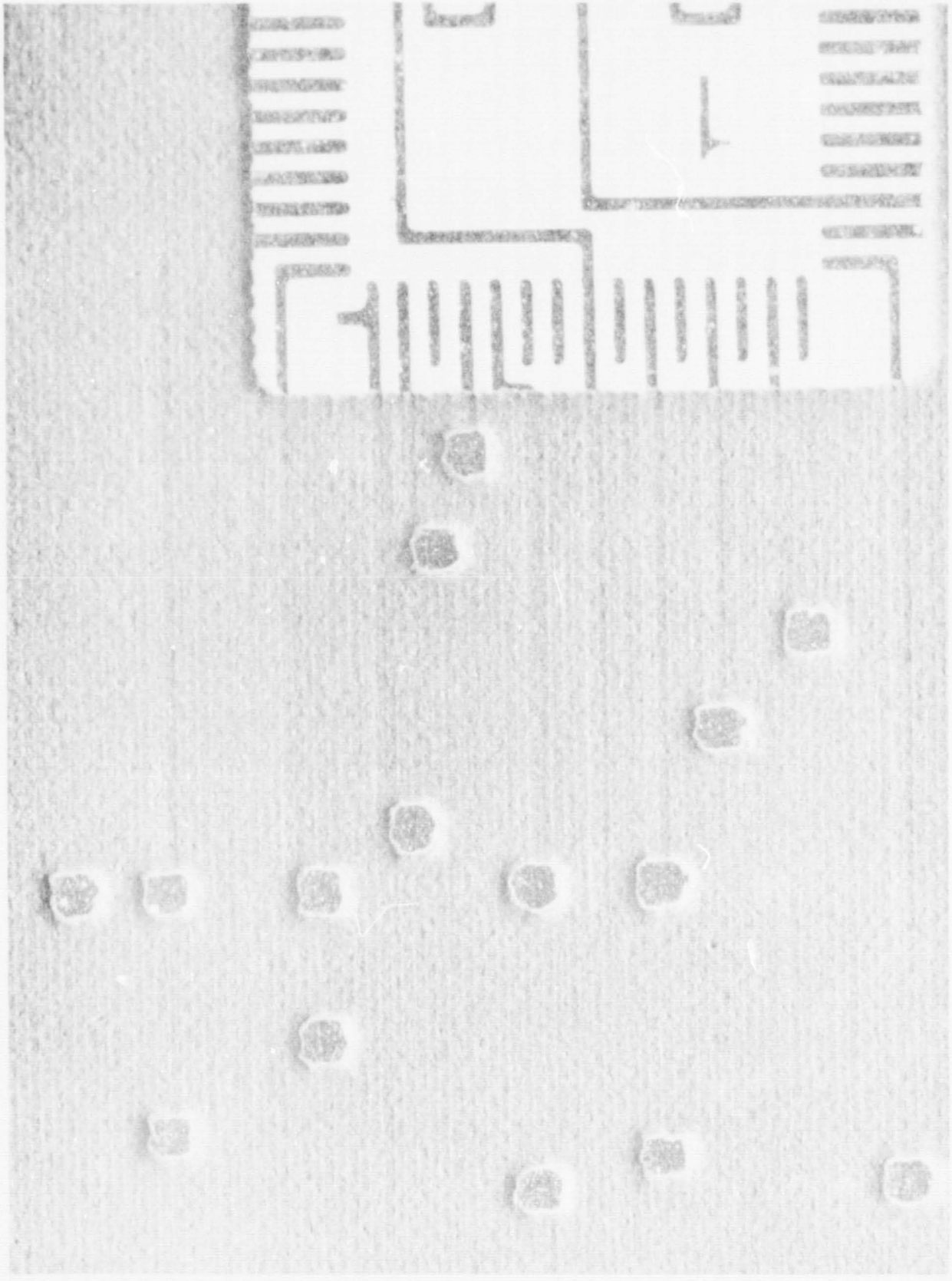
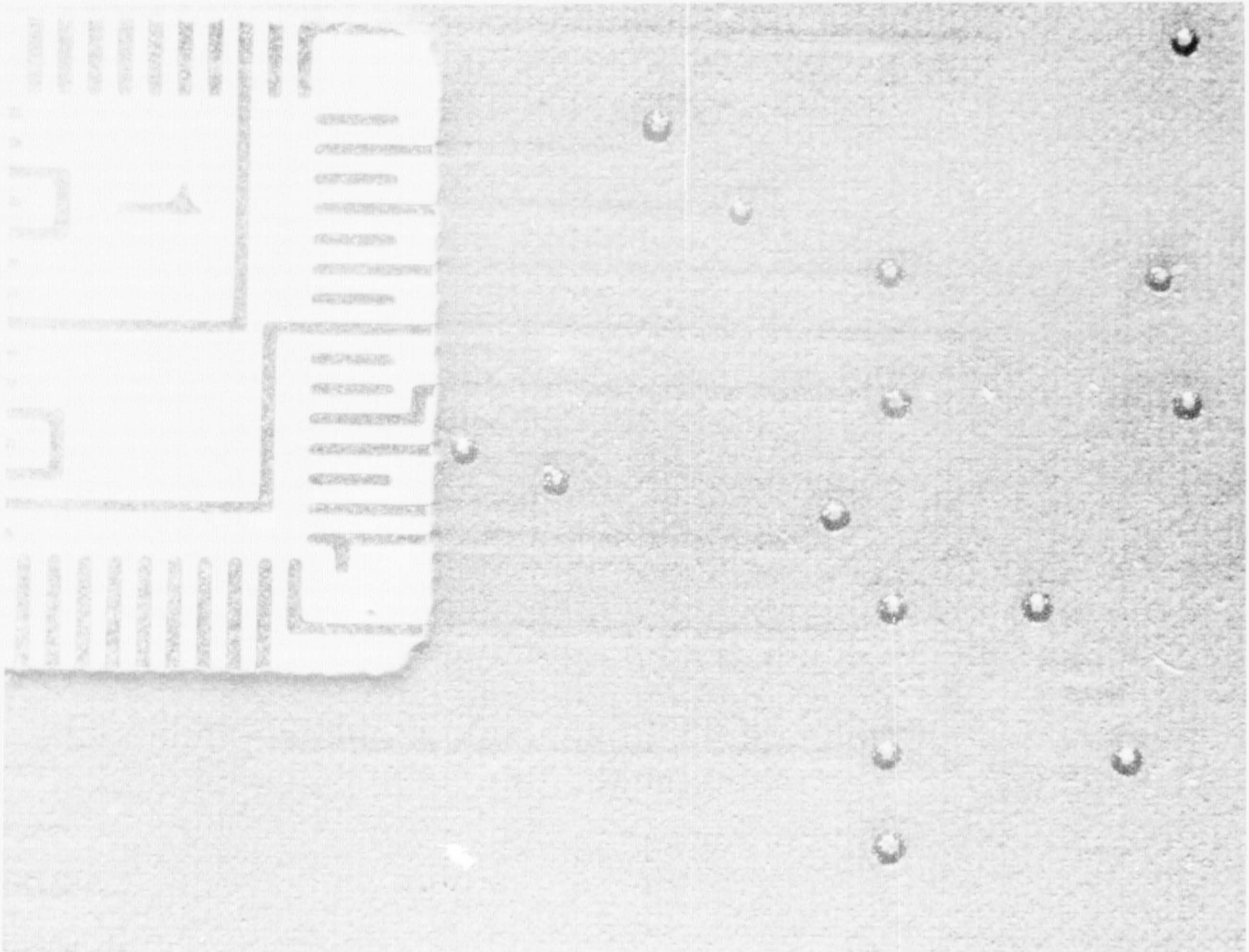


FIGURE 4. Standard Vias



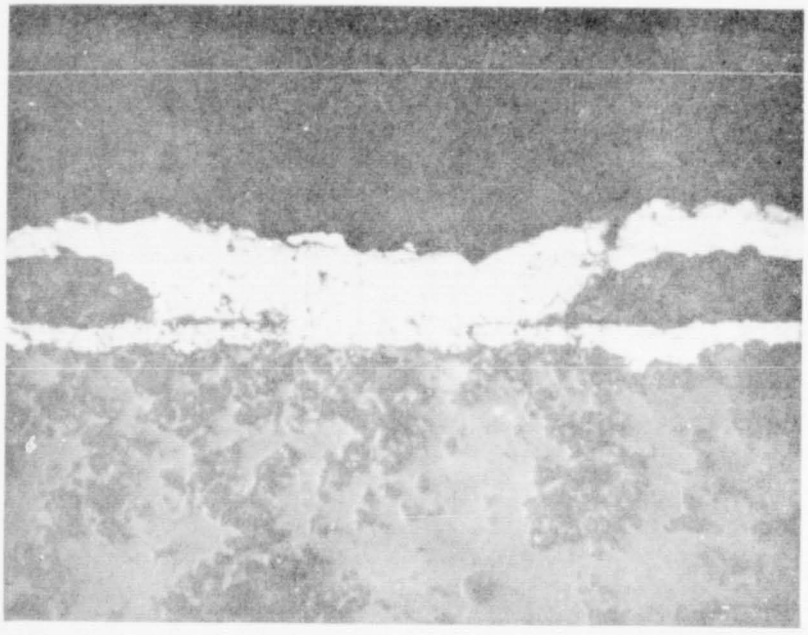


FIGURE 6. Vim Cross-Section

FIGURE 7. Scanning Electro-Micrograph
of Laser Etched Via

391-0711

HUGHES AIRCRAFT COMPANY
CULVER CITY
CALIFORNIA

August 10, 1977

The paper is for presentation and publication at the International Society for Hybrid Microelectronics (ISHM) Conference on Microelectronics for the Nineteen Eighties to be held at Marshall Space Flight Center, AL on September 20, 21, 1977.

SENSITIVITIES OF PARTICLE IMPACT NOISE DETECTION

by

F. Z. Keister
Hughes Aircraft Company
Culver City, CA

S. V. Caruso
National Aeronautics & Space Administration
Marshall Space Flight Center, AL

HUGHES
HUGHES AIRCRAFT COMPANY

INTRODUCTION

This paper describes the results of a study which Hughes Aircraft Company did for NASA/MSFC* on Particle Impact Noise Detection, commonly referred to as PIND testing. The main objective of this program was to determine certain sensitivities of PIND testing as applicable to hybrid microcircuits. Other objectives included: (1) evaluate techniques for removing particles from sealed hybrid packages; and (2) to look into methods for freeing particles which have become trapped or hung up inside the hybrid package and therefore give no PIND test response.

WHY PIND TEST?

Over the past several years, it has been recognized that particulate contamination in the form of loose particles has been responsible for a substantial number of failures in hybrid microcircuits. A recent study at Hughes revealed that loose conductive particles cause about one of every six failures in military hybrid circuits. Most of these failures are due to gold and solder particles resulting from wire bonding, and sealing of packages.

PIND testing has gained widespread acceptance as a method for detecting these loose particles.

Another solution to the particle problem has been to surface coat the microcircuit with an organic, such as Parylene, silicone, or epoxy. Some coatings have disadvantages, such as long-term degradation, purity control, masking, rework, and mechanical stresses on wire bonds. Other particle detection methods include vibration, X-ray, and monitored shock. None of these are as practical or effective as PIND testing.

*NASA Contract No. NAS 8-30876, "The Use of Particle Impact Noise Detection for Contamination Control in Hybrid Microelectronic Modules", (April 1977).

WHAT IS PIND TESTING?

It is a low level vibration technique (usually 30 to 60 Hz at 5 to 20 G) in which loose particles are detected by giving off ultrasonic noise emissions due to particle collisions within a vibrated package. The system consists of a transducer, shaker, driver, a scope for a visual display of particle noise, and an amplifier/speaker so that particle noise can also be heard. See Figure 1.

PACKAGES USED IN STUDY

Figure 2 shows the five hybrid package types and covers used in this study. These were the:

1" x 2" ceramic flatpack
1" x 1" metal butterfly packages with three cover types
1" x 1" metal platform package
5/8" x 5/8" metal butterfly package
TO-8 header

These packages all differ in internal volume, internal height, and weight. During the program, the packages were seeded by carefully placing a small particle of known size and weight inside the package and then hermetically sealing on the cover in a dry nitrogen atmosphere.

There were many types of particles used in this study to seed the packages. The primary particle types were gold balls and wire, aluminum balls and wire solder balls, and silicon chips, since these are the materials normally found in hybrid packages which are known to have caused failures. Ball diameters ranged in size from 1-mil up to 10-mils.

PIND TEST SYSTEMS USED

Three different PIND test systems were used in this study, Figure 3 shows one of these systems consisting of a Dunegan/Endevco Loose Particle Detector (LPD), Loose Particle Shaker (LPS), oscilloscope, mini-shaker, transducer, and a switch for an abrupt shaker turn on and off.

WHICH ATTACHMENT MEDIUM IS BEST FOR MOUNTING PACKAGES ON THE PIN TEST TRANSDUCER?

Two viscous couplants and two double-backed tapes were evaluated. The tapes had better peel strengths and were less messy to use; however, the viscous couplants were superior acoustically. Although the difference is slight, a water-soluble viscous couplant was judged the best.

HUGHES
HUGHES AIRCRAFT COMPANY

CAN WE PIND TEST LARGE HYBRID PACKAGES?

Yes, we can. Two large packages were tested. One was a 2" x 3" package weighing 60 grams. A 4-mil diameter gold ball could be detected at 40Hz/4G. The other package was 3" diameter, weighing 80 grams. A small solder ball was detected at 40 Hz/3G in this package.

HOW SMALL A PARTICLE CAN BE DETECTED BY PIND TESTING?

Particles weighing less than 0.1 microgram were detected. The smallest particle weighed 0.085 microgram. Gold particles slightly less than 1-mil in diameter could also be detected.

However, these size particles were not detected easily nor consistently. Even gold balls as large as 5-mil diameter could not be detected 100 percent of the time because of their tendency to hang up. The larger and heavier the particle, the easier it is to detect.

CAN WE DETECT MULTIPLE PARTICLES IN A SINGLE PACKAGE?

Tests were conducted to see if an operator could tell by PIND testing whether a package contains only one particle or several particles. Identical packages were seeded with from one to four small gold balls. There was a slight difference in the noise response between those packages containing one and four balls. However, the answer to the question is still "no", since a single particle would give as loud a PIND test signal as several smaller particles of equal total mass.

CAN PIND TESTING DISTINGUISH BETWEEN CONDUCTIVE AND NONCONDUCTIVE PARTICLES?

If we knew that the particle inside the package was only nonconductive and harmless, it would not be necessary to reject it. In this study comparisons were made between gold balls and epoxy particles and between solder balls and ceramic chips. Because of the similarities of the oscilloscope noise signals and the similarities of the audible responses, it was not possible to tell the difference between packages containing conductive and non-conductive particles.

IS PIND TESTING SENSITIVE TO PARTICLE SHAPE?

The answer is "yes". Some packages were seeded with balls and some with cylindrical-shaped particles having equal weights and of the same materials (gold and aluminum). It was found that a sphere was more easily detected by PIND testing than a wire of equal mass.

IS PIND TESTING SENSITIVE TO THE PACKAGE COVER MATERIAL?

The answer to this question is "no". Packages were seeded with small gold balls and then sealed by using both Kovar and ceramic covers. There was no significant difference in the PIND test response.

IS PIND TESTING SENSITIVE TO CHIPS AND WIRE BONDS INSIDE THE PACKAGE?

The answer is "no". Different hybrid package types were prepared with assembled substrates inside while other packages were empty. These packages were seeded with different types of particles, sealed, and then PIND tested. Figure 4 shows the appearance of some typical assembled and empty hybrid packages. For all practical purposes, the PIND test responses were identical regardless of whether the package was empty or loaded with chips and wire bonds.

IS PIND TESTING SENSITIVE TO THE PACKAGE SEALING METHOD?

Again the answer to this question is "no". Three different sealing methods were compared. These were soldering, parallel seam welding, and adhesive sealing. For this evaluation, identical packages were each seeded with a small particle and then each was sealed differently. The PIND test results showed no significant difference in loose particle response regardless of the sealing method used.

IS PIND TESTING SENSITIVE TO THE TYPE OF SUBSTRATE METALIZATION?

Thick film and thin film substrates were placed in identical packages. Pairs of these packages were then seeded with particles, sealed, and PIND tested. The same PIND test response was obtained whether the substrate was metallized by thick or thin film techniques or was unmetallized.

IS PIND TESTING SENSITIVE TO DIFFERENT PIND TEST EQUIPMENTS?

To answer this question, three different PIND test equipments were used to test a variety of seeded packages at identical frequencies and G-levels. These were all basically Dunegan systems with different shakers, scopes, and shaker drivers. There was a close correlation between the three PIND test systems in their ability to detect small and large particles. Small particles which were hard to detect on one system were just as hard to detect on another system. However, if the PIND test systems differed substantially in their sensitivities (i.e., signal-to-noise ratio), there was a significant difference in their reject rate. The less sensitive system would consistently pass particle-containing packages because the particle noise was below the system's threshold level.

IS PIND TESTING OPERATOR DEPENDENT?

The answer to this question is "yes". Seeded packages were given to six different operators to PIND test. Their success ranged from 78 percent correct to 100 percent correct. The largest problems that operators have are: (1) detecting trapped particles, and (2) misinterpreting equipment noise for a particle noise burst (thus rejecting a good package). The more experienced an operator becomes, the less likely it is that he will reject good packages or pass bad ones.

IS THERE A PREFERRED PACKAGE ORIENTATION ON THE PIN TEST TRANSDUCER?

Yes, there is. Tests with packages mounted both "lid-up" and "lid-down" on the PIND tester showed that the lid-up position produced the best PIND test response regardless of the package type or particle type. However, the lid-up position is sometimes inconvenient for packages with leads protruding from the bottom and the difference in PIND test response is not that great.

IS PIND TESTING SENSITIVE TO THE PACKAGE TYPE?

Tests with five different package types and seven different particle types showed that PIND testing was sensitive to the package type. Of the five package types evaluated in this study, the best PIND test responses occurred with the 1" x 2" ceramic flatpacks. Particles became more easily trapped in the 5/8" square butterfly package.

IS PIND TESTING SENSITIVE TO THE PARTICLE TYPE?

The answer here is "yes". Seven different particle types were used. PIND testing was found to be sensitive to particle material, weight, and size. The heavier particle will give a more prominant response, even though of the same size as another particle of lesser mass. The smaller and lighter particles gave the faintest responses and also hung up more readily.

REMOVING PARTICLES FROM SEALED PACKAGES

Part of this NASA study was concerned with an evaluation of a method for removing particles from sealed packages once these particles had been detected by the PIND test. It was required that the particle be removed and the package resealed. Removal was done through a hole in the cover.

The best method found for piercing the package cover (as opposed to complete cover removal) was to punch a 40-mil diameter hole in a corner of the cover using an arbor press, as shown in Figure 5. Hole punching must be done carefully to avoid introducing additional particles into the hybrid.

Once the hole is punched, the particle is captured by placing a piece of adhesive-backed tape over the hole and then bouncing the particle through the hole and onto the tape by vibrating the package lid down on the PIND tester for a few seconds. Particle retrieval was shown to be about 99 percent effective.

RESEALING THE HOLE IN THE COVER

Once the particle is retrieved, the hole in the cover must be resealed. The best method found was to use the tip of a soldering iron to wipe solder over

the hole. This is done in dry nitrogen without flux. Figure 6 shows the appearance of two packages with their holes resealed. As with hole punching, resealing must be done carefully to avoid introducing additional particles.

FREEING TRAPPED PARTICLES

Another portion of this program dealt with freeing trapped particles inside hybrid packages. Particles may become trapped before PIND testing or they may hang up after a few milliseconds of vibration. In either case, if the trapped particle goes undetected it may become loose later on and cause a failure.

WHERE DO PARTICLES GET TRAPPED?

By the use of X-rays, seeded packages with glass covers, and by carefully removing covers from seeded packages, it was found that particles could hang up almost any place. A favorite place is between the substrate and the package wall. It is rare that a particle or wire end becomes trapped beneath a chip or wire bond.

WHICH PARTICLES ARE TRAPPED MOST EASILY?

Of the many different particle types tried in this program, the smallest and lightest (in weight) particles would hang up more frequently than others. Aluminum was a particularly bad material. Based on almost 200 tests, 52 percent of the seeded packages contained particles which were initially trapped and failed to give an initial PIND test response unless special shocking methods were used to free the particle.

HOW CAN WE FREE TRAPPED PARTICLES?

During this program, approximately 30 different methods were evaluated for freeing trapped particles. Of these the best methods found were those involving some sort of mechanical impact shock. Two small tools were used during this program to impart low-level shocks to hybrid packages. These are shown in Figure 7.

PRESHOCK TOOL

One of these tools is a preshock tool. It is used to shock the package just prior to PIND testing. As shown in Figure 8, the package is attached to the pendulum arm with double-backed tape and allowed to fall two or three times impacting the edge of the package on the bench top with a G-level from 1500 to 4000 G depending on the package type. By itself, this tool was shown to be 77-87 percent effective in freeing trapped particles.

COSHOCK TOOL

The other tool was a coshock tool and is used to tap the hybrid package while it is vibrating on the PIND tester. Figure 9 shows this tool being used. A free-sliding plunger imparts a shock of from 300 to 2500 G's to the package depending on the plunger material and package type.

For optimum results, both tools must be used - first a preshock if needed and then a coshock, if needed. Together their efficiency was found to be from 90 - 95 percent in freeing trapped particles of all types.

ARE THESE TOOLS SAFE TO USE?

Because of the G-levels involved, tests were conducted to determine if either tool was harmful to wire bonds, die bonds, active and passive chips, and hermetic seals. No degradation was noted.

CONCLUSION

PIND testing has shown itself to be an effective means for controlling particle contamination in hybrids. It is sensitive to package orientation, cover heights, operator subjectivity, package type, and particle type, size, and mass. It is relatively insensitive to package cover material, package sealing method, substrate metallization, and chips and wire bonds inside the package. Particles can be removed from sealed packages through a hole in the cover and this hole can then be resealed. A large percentage of loose particles which "hang up" inside hybrid packages can be freed by applying some type of mechanical impact shock to the package either before or during the PIND test.

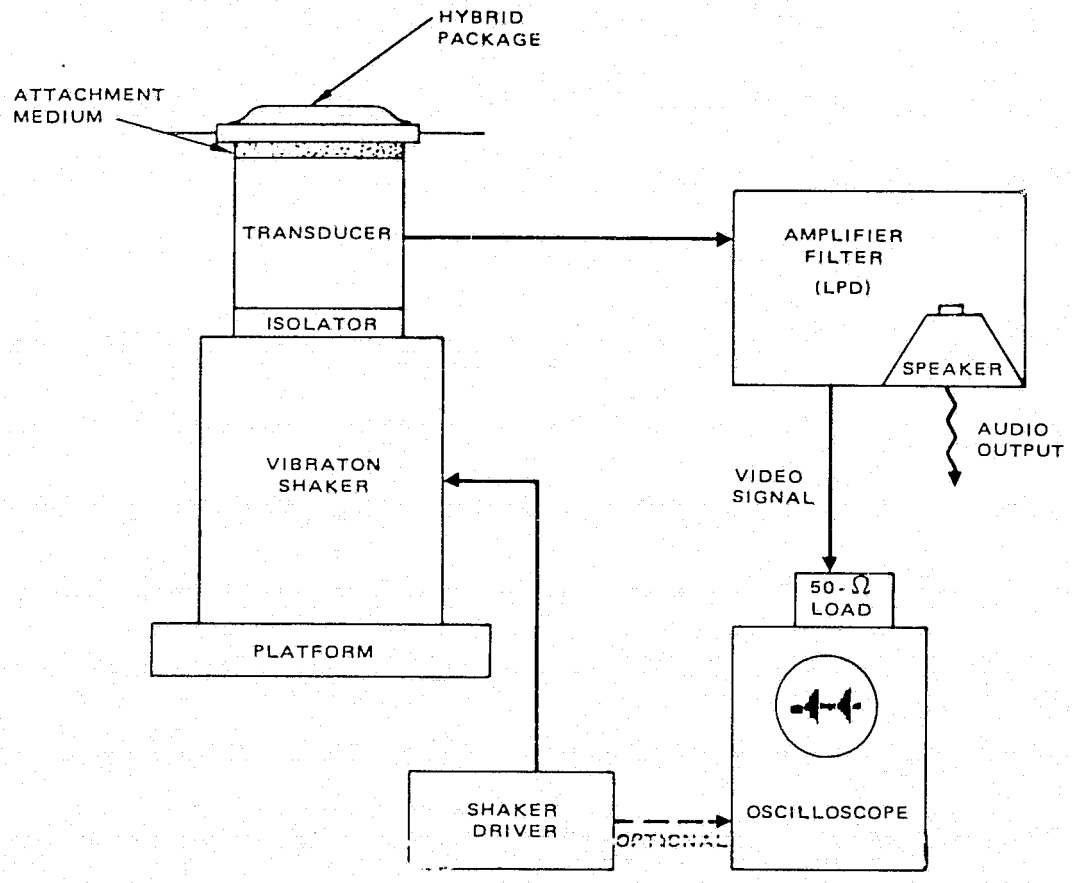


Figure 1. Block diagram of particle impact noise detector.

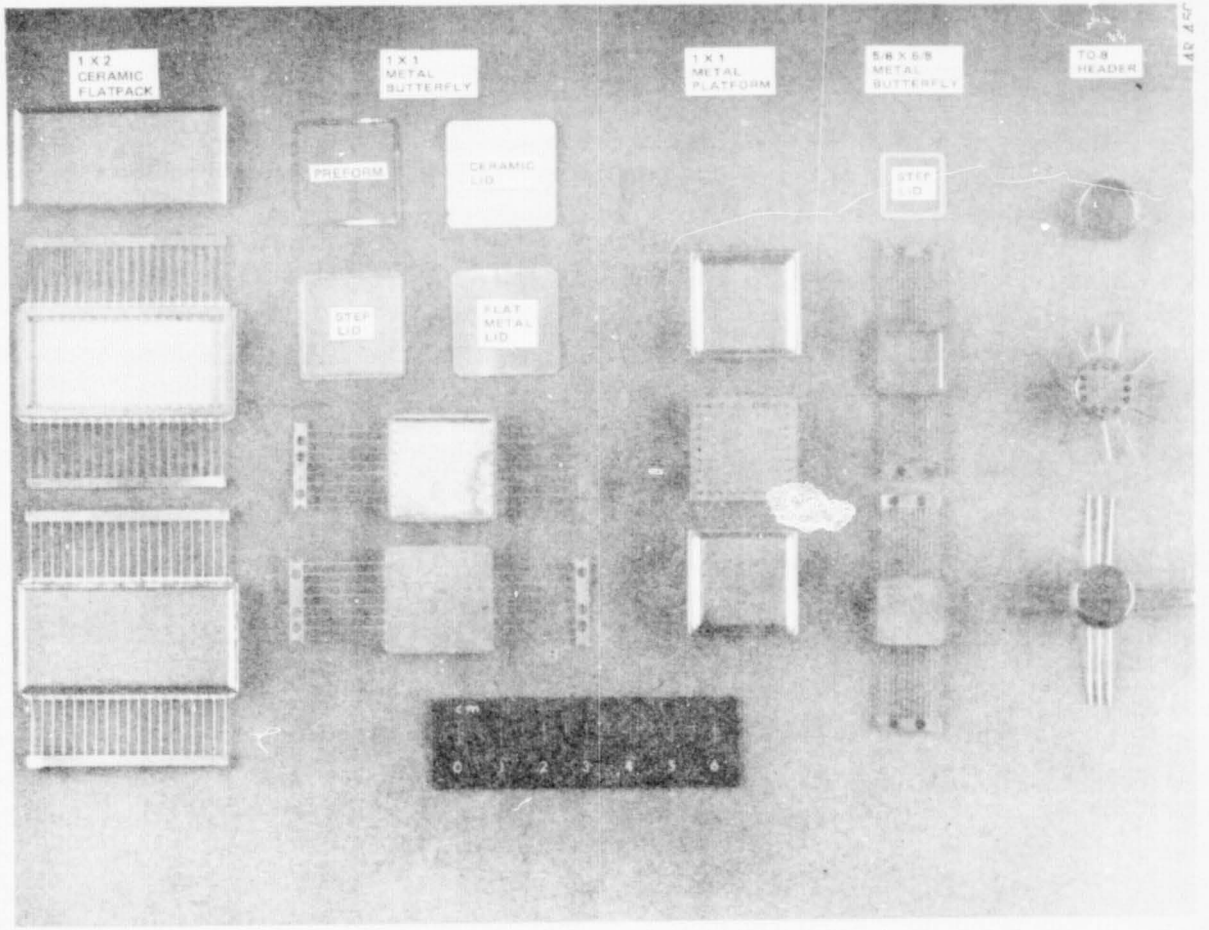


Figure 2. Package types and covers for PIND testing. The packages along the bottom row are lidded.

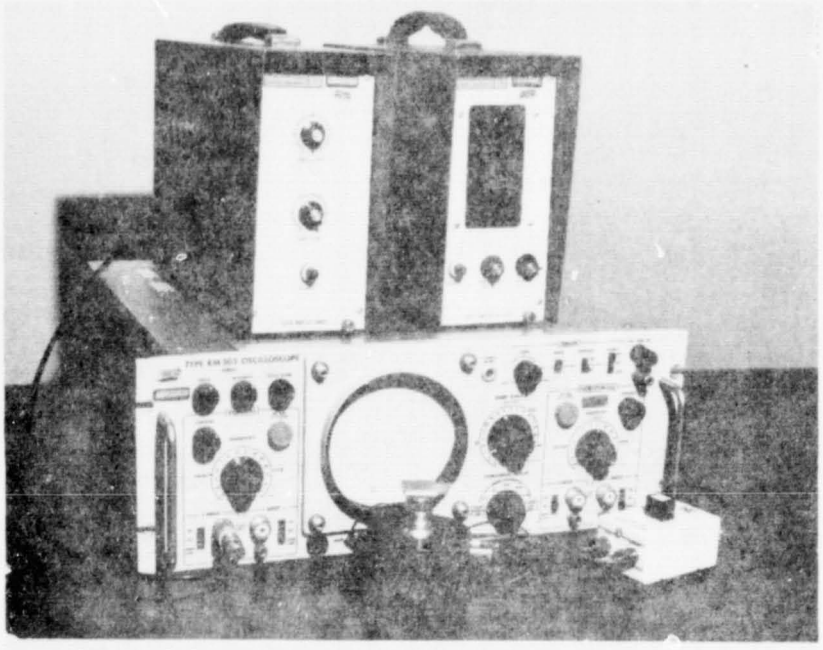


Figure 3. PIND test equipment.

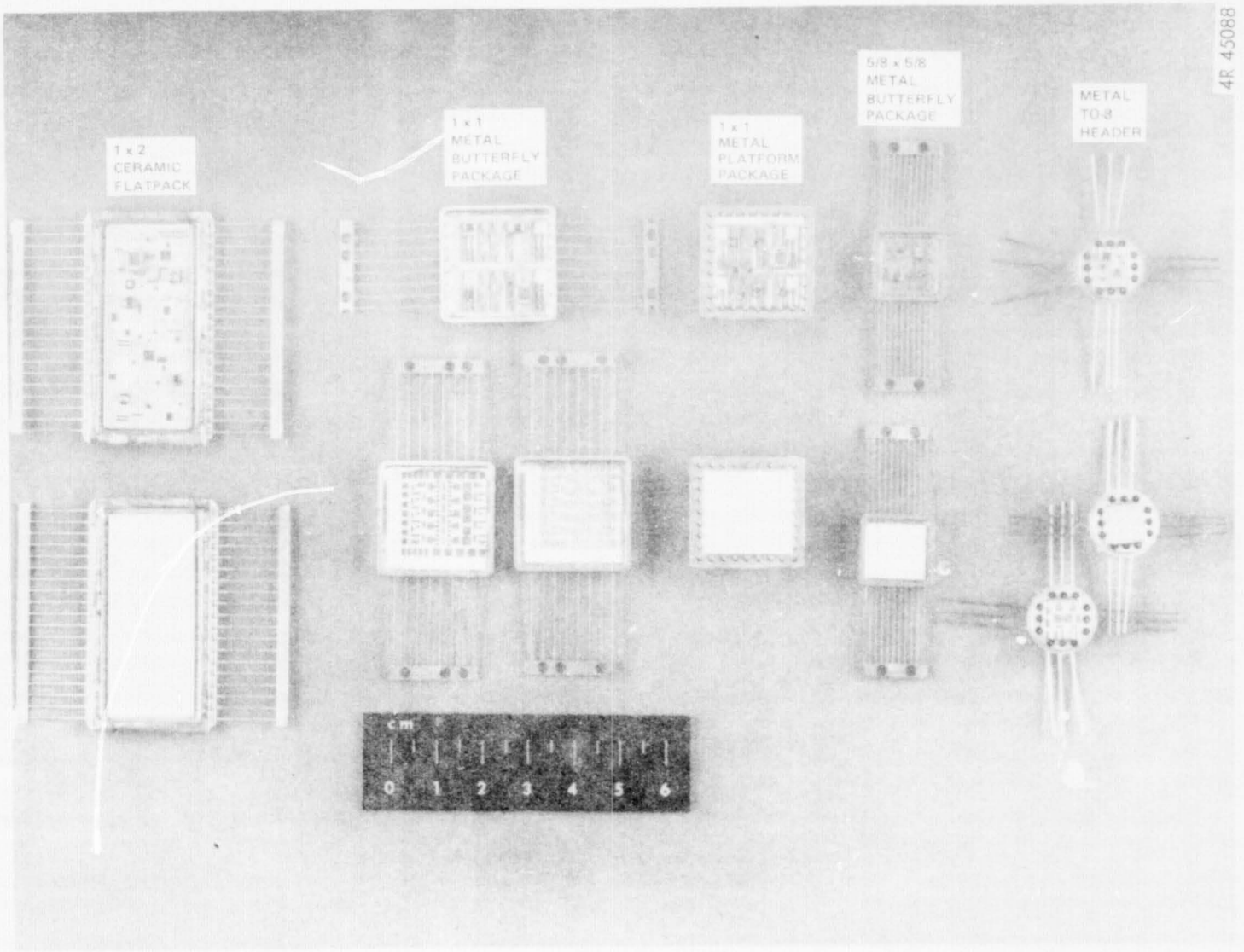


Figure 4. Typical hybrid packages used for PIND sensitivity testing. The packages along the top row have chips and wire bonds inside. Those along the bottom row contain either blank substrates or metalized substrates.

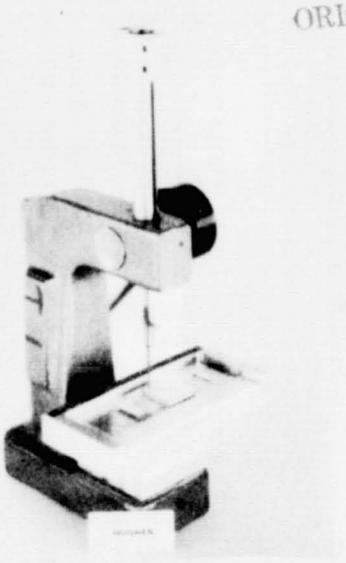


Figure 5. Arbor press used for hole punching.

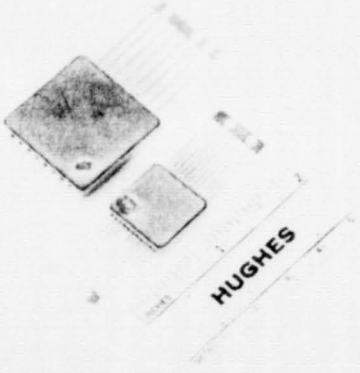


Figure 6. Typical packages which had holes punched in the covers and then had these holes resealed.

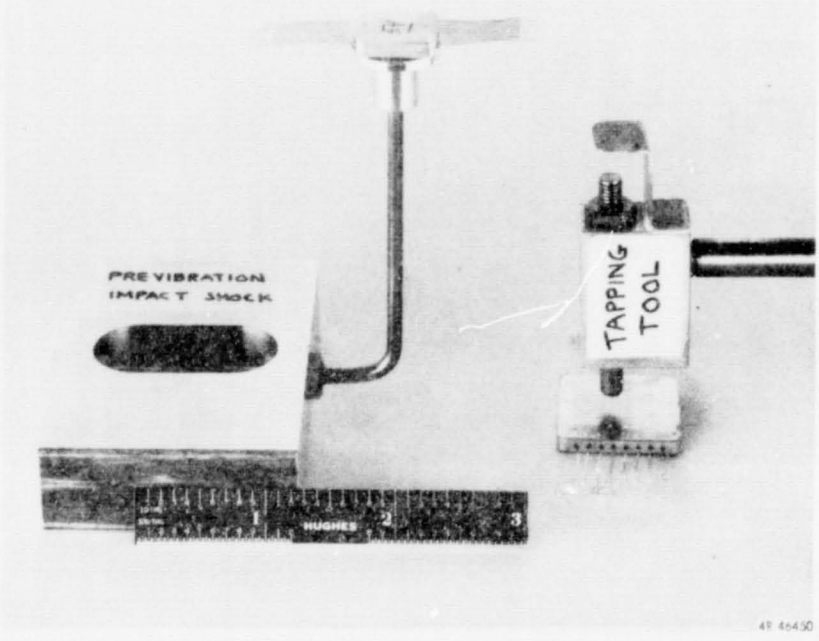


Figure 7. Preshock tool (left) and coshock tool (right).

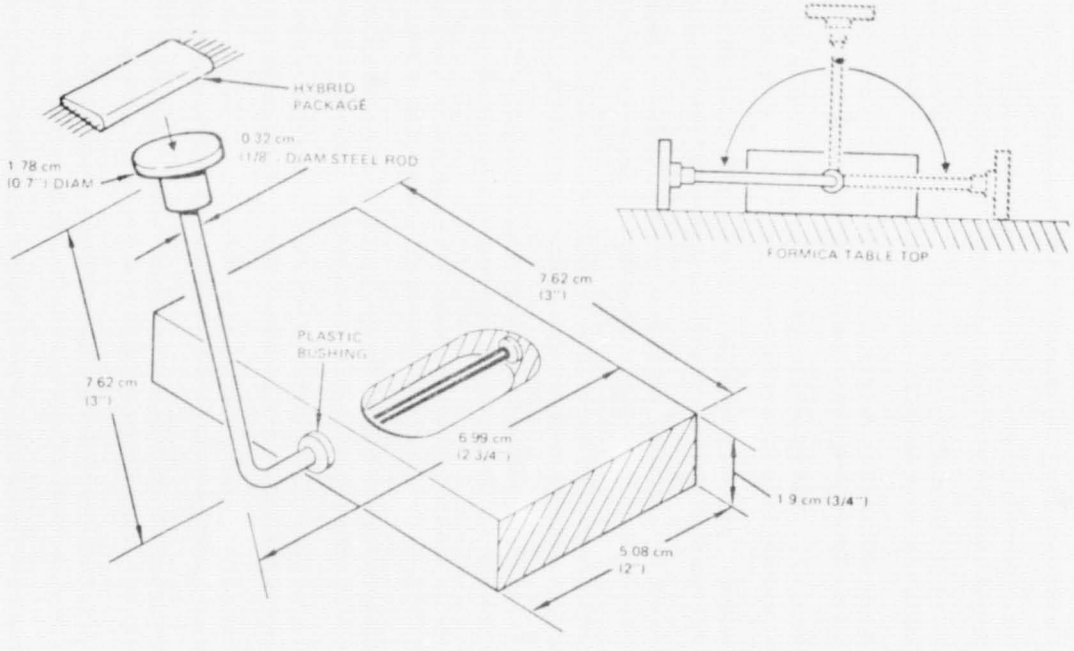


Figure 8. Preshock tool.

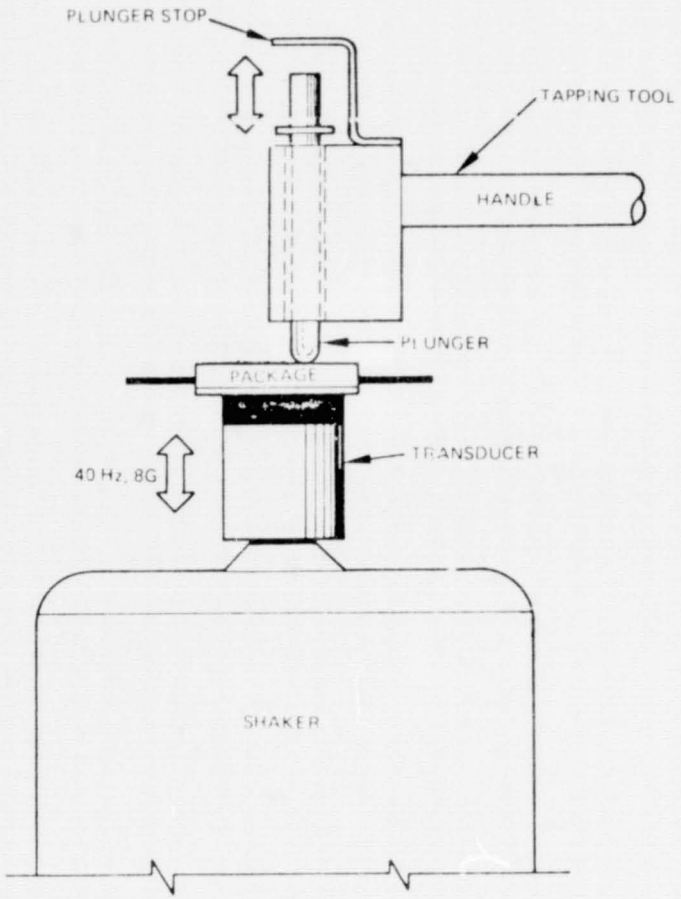


Figure 9. Coshock tool.

N78-16278

FACTORS AFFECTING LASER-TRIM STABILITY OF THICK FILM RESISTORS

R. E. Cote', R. C. Headley

E. I. du Pont de Nemours & Co., Inc.

Photo Products Department, Electronics Materials Division, Niagara Falls, New York

Various factors affecting precision of trim and resistor stability are considered. The influence of machine operating parameters (beam power, pulse frequency and trim speed) on resistor performance are examined and quantified through statistically designed experiments for a Q-switched YAG laser system. Laser kerf quality is examined by scanning electron microscopy and related to kerf isolation resistance measurements. A relatively simple, production oriented, quality control test is proposed for rapid determination of kerf electrical stability. In addition, the effect of cut design and extent of trim on precision and stability are discussed.

MACHINE-RELATED PARAMETERS

A consideration of factors that affect the precision of trim and stability of laser trimmed thick film resistors should begin with an examination of some of the aspects of the laser system itself. Specifically, one should concern himself with those parameters which are generally adjusted when the equipment is set-up and then assumed to remain constant through the laser trimming process. These include beam spot size and sharpness of focus, average beam power, pulse tracking response and measurement bridge settling time. Some of these factors contribute to the quality of the kerf. Others influence the measurement system which can lead to false interpretation of data.

Beam Power

Peak power density, not average power density, removes material. However, peak power density is difficult to measure and average power density is what one normally measures. One of the factors which affects peak power density, in a most critical way, is spot size. When a laser is operated in TEM_{OO} mode (that is, a single spot output from the laser) the distribution of the energy output is nearly Gaussian, as shown in Figure 1A. The beam is then passed through a series of focusing lenses shown diagrammatically in Figure 1B as a single lens. Laser energy in this mode does not focus to an infinitely small spot as does dispersive radiation. At the point of focus, the beam exhibits a minimum waist diameter determined by the lens' focal properties. The beam intensity is then sufficient to vaporize material and cut through the resistor.

It is important to note that peak power varies inversely with the square of beam diameter. If a minimum power required to remove material is defined, we see in Figure 1C that a laser operated in poor focus will direct energy of lower intensity into the walls of the laser kerf. This may cause damage due to thermal shock and may not remove material cleanly. In extreme cases, microcracks and fissures may be produced.

The use of apertures can improve beam focus, particularly with multimode (donut or multispot beam) propagation, by taking a "prime cut" out of the energy distribution. Figure 2 shows this diagrammatically. The aperture blocks most of the divergent radiation of the laser energy output which would otherwise degrade the focus of the beam.

Average beam power is an easily measured machine parameter. It is directly adjustable by panel control of pump lamp current and programmable with most modern computerized systems. When it is varied with other parameters fixed, a relationship between average beam power and post trim resistor stability may be observed for most thick film resistor materials. Figure 3 shows this relationship in generalized form. An optimum level of resistor stability, $\Delta R_O = 1$, is obtained over a limited range of beam power. Extensive inspection of trimmed resistors has shown that below or above this limited range, kerf quality deteriorates in either of two principal ways. These are: incomplete removal of material--(low power) or wider peripheral zones of disturbed material bordering the kerf (high power). In the latter case, the extent of damage is often evidenced by microcracks extending into functional areas of the trimmed resistor. Two other effects to be seen with high beam power are wider kerfs and less well-defined kerf walls.

Pulse Frequency

Ideally, trimming should not result in further resistance change after completion of trim. Laser energy flow into resistor material outside the trim path, or into the substrate should, therefore, be minimized to maintain high integrity of the trimmed configuration. That is, a maximum amount of laser energy should be absorbed in the process of resistor material vaporization. This requires pulsed energy of high peak power and pulses of short duration. These conditions are not independent of pulse frequency, or Q-rate, and stability problems do occur where high pulse frequencies have been used to facilitate high trim speeds. Figure 4 provides a basis as to why this may happen.

The relationship between peak power and pulse duration as the Q-rate is varied was determined experimentally using photocell-oscillographic techniques. Peak power is shown on a relative scale which corresponds to photocell output (volts). Pulse

duration corresponds to the time interval between the pulse half-power points.

Figure 4 shows a noticeable drop-off in peak power as Q-rate increases. At the same time, pulse duration increases. The result is less pulse energy of sufficient magnitude to achieve rapid vaporization and more energy flowing into the resistor body and substrate. The consequences of very high Q-rates are visible as pronounced reflow along kerf walls accompanied by stress induced cracking in the reflowed areas. Inadequate kerf formation also occurs. This study is not complete in that the influence of input pump lamp power has been investigated only up to the level where TEM_{OO} mode propagation predominates.

Trim Speed and Bridge Tracking

Any measurement system requires a finite time to achieve balance and measure resistors. During the trimming operation, resistance values increase by discrete steps the magnitude and frequency of which are determined by the laser pulse conditions, cut mode, resistor size and extent of trim. The bridge tracks the resistance values between laser pulses. If the magnitude and frequency of resistance change does not allow the bridge enough time to reach balance, an accumulating error in measurement will occur as trimming proceeds. The result is overshoot. This is shown in Figure 5 where overshoot is shown to be equal to the measurement lag.

The problem becomes more severe when high value resistors, (in excess of 1 megohm) are trimmed. Measurement lag and overshoot can exceed 1% and predictability can also be lost. In some very high resistance values, the resistor can be trimmed completely open unless sufficiently large cut-offs or adequate delays are programmed into the measurment or provisions are made at the probe ring to speed the measurement. To overcome this problem, it may also be necessary to slow the trimming speed. Tracking response effects can also be minimized by the use of multiple cuts where the final cut requires a maximum 2-3% change. Other factors that influence overshoot are temperature coefficient of resistance and intrinsic stability characteristics of the resistor being trimmed.

Bridge Settling Time

In addition to the bridge tracking response, another factor which affects the accuracy of the measurements is bridge settling time. This factor is present whether or not the resistor is being trimmed. The time interval required to obtain a given measurement accuracy increases as the magnitude of the resistance value becomes larger. A variety of measurements are available with modern laser systems which permit rapid, low precision measurements, or slower, more precise measurements. These "modes", as well as settling time, are usually programmable, and care should

be taken to select the best combination where accurate measurements are required. In Figure 6, the influence of time on measurement accuracy is illustrated by the shaded areas. The figure is intended to provide an indication of the magnitudes involved, and the numbers should not be taken literally.

Probe Station

A final point worth mentioning involves the probe station (Figure 7). Measurement probes are often fragile and subject to vibration and rapid wear. Probe pressure should be of concern for a particular probe style. Long, cantilevered probes are prone to bounce, which can lead to erratic results if the pressure is too low or an adequate delay between probe actuation and measurement time is not maintained. This is most serious in measurements of low resistance values where a significant contribution can result from high contact resistance. Also, stability of the probe placement can be critical to obtaining reproducible results. All thick film resistors exhibit strain effects to a greater or lesser degree. In this respect, excessive, unstable probe pressure, uneven substrates, and poor or dirty nesting can compromise the measured results.

Supporting Data

An experiment was statistically designed to study the relative effects of trim speed, Q-rate and power on precision of trim and resistor stability. The experimental design took the form of a face centered cube illustrated by Figures 8-10. The test matrix included the eight corner points of the cube, the six face points, the center point repeated three separate times and four replicates of the corner points. The experimental design is shown in Table 1. The machine parameters were varied over the following ranges: average power, 0.5 to 1.5 watts; cutting speed, 2.5 to 50 mm/sec. (0.1 to 2.0 inches/sec.); Q-rate, 1 KHz to 5 KHz. Fired films with sheet resistivities of 100 ohms/square, 10K ohms/square and 1 M ohms/square were studied, with each result the average of data points from measurements of 40 resistors. All resistors were 1 mm^2 (0.040" x 0.040") trimmed with a single plunge cut. The spread of resistance values of the as-fired resistors was approximately ±15% around a mean value, and the latter was assumed to be 33% below a hypothetical target value. Thus, on the average, trimming raised the value by a factor of 1.5 with some resistors being "trimmed up" by a factor of 2.

All of the laser trimming and measurement was carried out with a Teradyne Model W311, Q-switched, YAG laser system. Initial deviation from target (precision of trim) and 24-hour and 100-hour percentage resistance drift (referenced to the initial measurement) were measured.

The results of the experiment are shown in Figures 8-10. It can be seen that speed of trim has the largest effect on both precision and drift. This was borne out by a regression analysis which showed speed to be the greatest single contributor but also showed some interdependency of the three variables.

The experiment yielded "volumes" within the experimental cube where combinations of speed, frequency and power produce equivalent results within experimental error. It also indicates that different conditions may be required to achieve satisfactory results with low ohm materials compared to high ohm resistor compositions.

Figure 10 presents data for the 1 megohm/square material. The first cube refers to precision of trim. It is apparent that the trim conditions at the left end, front edge of the cube--the lowest speed and frequency somewhat independent of power--yield the smallest deviation from the target value. The high negative numbers at the left end, back edge of the cube indicate that the material was not trimmed cleanly. This is a case where the speed is too high for the frequency, resulting in a series of unconnected cuts.

Analysis of the cube presenting drift data indicates that optimum trim conditions lie within a diagonal volume running from the bottom left front corner to the top right back corner. The combination of best precision and lowest drift generally is achieved with the lowest speed at the lowest frequency and the lowest power. Drift values generally increase under conditions of high power/high speed/low frequency and low power/high speed/high frequency.

OTHER FACTORS AFFECTING PRECISION AND STABILITY

An effort was made to correlate the data with some physical phenomena. Samples trimmed at the various conditions were cross-sectioned and examined using a scanning electron microscope. An interesting observation was made in a comparison of resistors trimmed at the same average power, but at two different frequencies. Figure 11 shows a cross section of a laser kerf cut at the higher frequency.

Figure 12 shows the same material cut @ a Q-rate of 3 KHz. Penetration of the substrate is obvious in the lower frequency cut. The resistors cut at the higher frequency--no penetration of the substrate--were less stable.

Apparently a kerf must penetrate the substrate (>5μ) to insure adequate isolation resistance, particularly at high resistivities.

In some instances it was found that resistors trimmed with no penetration of the substrate became unstable when subjected to

further elevated temperature hybrid processing. It was found that a quick, production-oriented test which can be run to determine the quality of the laser kerf consists of measuring the insulation resistance (IR) of the kerf of a resistor which has been cut completely through. The resistor is then exposed to 425°C for 10 minutes and the IR is remeasured. The IR of a stable resistor will remain unchanged; the IR of an unstable resistor will decrease by one to two orders of magnitude.

The critical nature of kerf isolation with high resistivity films can be understood by thinking of the kerf as a parallel resistor distributed across the trimmed resistor. Consider a 10 megohm resistor with a kerf (2.5 mm x 25μm) 100 mil long by 1 mil wide. This kerf is equivalent to a .01 square resistor. A marginally clean kerf of this size could easily vary in resistance and over a range of 100 megohm to 10,000 megohm causing up to 10% ΔR of the 10 megohm resistor. The same variation would have virtually no effect on a 10 kilohm resistor. A general rule of thumb is that a trimmed resistor requires a total kerf resistance not less than 10^3 times the trimmed value to maintain stability to 0.1%, all other factors being excluded.

Types of Cuts

The experiment described in the preceding section was carried out with one general type of resistor material. All resistors were trimmed with a single plunge cut which raised the mean value of the resistors by a factor of 1.5. It is possible to improve precision and stability by using multiple plunge cuts or L-cuts and limiting the extent of the cut. Figure 13 illustrates a single plunge cut of a square resistor. If the drift mechanism is defined as the propagation of microcracks from the end of the laser kerf which interrupts the current flow path and causes an increase in resistance, the extent of propagation (ΔX) has a greater effect on resistance when the kerf penetrates to depth X3 than to X1

An attempt was made to correlate the drift observed in the experiment described in the preceding section to the extent of cut. Within the constraints of the experiment (maximum 2X trim), no correlation was seen. However, if the end of the cut is placed parallel to the current flow path (via an L-cut), then one would expect that precision will be improved and drift reduced. This is indeed true and is shown by the histograms in Figure 14.

Another way to improve precision and stability is the use of a double plunge cut with a delay of a few hundred milliseconds between the first and second cut. A method of achieving this in production is to make first cuts in all resistors and then follow with the second cuts.

Figure 15 shows the extent of penetration required to achieve a given resistance change in a square resistor. It is interesting to note that to raise resistance by a factor of two, a 67% penetration of its width is required.

Resistor Intrinsic Properties

To limit the extent of cut, a resistor series which has consistent, reproducible and predictable resistivity is desired. The material should be blendable for both resistivity and TCR. Lot-to-lot reproducibility assures that the values will remain close to the design value and, therefore, that the extent of trim will be consistent from month to month. Achieving a small coefficient of variation within a fired lot is important to insure that the extent of trim does not vary widely. In our experiments, the total spread of resistance values was ±15% around a mean. Had the spread been ±30% (a CV of 10%), some samples would have required the resistance to be raised 3X; i.e., the kerf would have to extend through 80% of the resistor width. Neglecting the effect this has on resistor power handling capability, trimming a resistor to this extent has very dramatic effects on both precision and stability.

The influence of sheet resistivity upon trimmed resistor stability is related to differences in fired print thickness. In general, low resistivity compositions require higher functional phase loading than do high resistivity materials. This results in thicker fired prints. During trimming, the vaporized material is often sufficiently dense, at the point of trim, to attenuate the laser beam intensity and reduce cutting efficiency. (Staining of the kerf floor with condensed material is not uncommon. Although such staining appears to be innocuous, in most cases, it does prevent a reliable inspection of kerf quality by visual methods.) The stability of a thick film resistor can be improved by reducing its fired thickness. Of course, the increase in sheet resistivity must be accounted for in product design.

RECOMMENDATIONS

In summary here are a few key points to remember when laser trimming resistors.

1. The lowest speed consistent with productivity and precision should be selected.

2. Care should be exercised in selecting the proper average beam power.

3. Decreasing the Q-rate can be an effective way of increasing peak power while maintaining a constant average power. This can be used to advantage when trimming lower sheet resistivity materials.

4. The extent of trim should be limited to 2X the fired value.

5. L-cuts or multiple plunge cuts increase the precision and reduce drift.

6. The laser cut should be made with sufficent peak power to penetrate the substrate to a minimum of 5μm.

7. An insulation resistance (IR) test with exposure to 425°C for 10 minutes can be used to assure the integrity of the kerf.

8. Trim stability can be improved by reducing resistor film thickness.

ACKNOWLEDGEMENT

The authors wish to thank Dr. F. J. Anders for his guidance and support. We also wish to thank Mrs. Carolyn Martin for her effort in typing the manuscript. We acknowledge the assistance of Mr. J. T. Herman of Du Pont's Engineering Services Department and Mr. A. Howe of Teradyne who acted as consultants in this project.

D13

N78-16279

RELEVANCE OF MICROELECTRONIC EDUCATION TO INDUSTRIAL NEEDS

J. L. Prince and J. W. Lathrop
Electrical and Computer Engineering Department
Clemson University, Clemson, SC 29631

Every electrical engineering curriculum in the country includes some microelectronics; consequently, every graduate knows something about how microelectronic devices are made and what they can do. However, the teaching of microelectronics varies widely from school to school in both quantity and quality. Some universities have elaborate monolithic facilities where students can design and build devices. Others have hybrid facilities where students are not involved in semiconductor processing, but can still experience the design process. Still others have no fabrication facilities at all and rely entirely on course work to communicate microelectronic concepts to the student. In addition, there are different philosophies on what is required of all students and what is elective. Some schools may teach only a few students a great deal about microelectronics, largely ignoring the rest, while others may teach all their students a fair amount, but offer no chance for greater specialization. By now, as we approach the 20th anniversary of the invention of the integrated circuit, most universities have formulated their policy towards microelectronics education. The initial facilities expansion of the late Sixties and early Seventies is over and both those on the bandwagon and those on the sidelines are attempting to evaluate the effectiveness of their programs. One, but only one, aspect of this evaluation involves how relevant microelectronic education is to industrial needs. The authors do not presume to have reached a specific conclusion concerning this, but they have isolated some points which can serve as the basis of further discussion.

Before the question of relevance to industrial needs can be discussed, it is necessary to decide on what the needs of industry are. Here we are, torn between what industry says they need and what they hire. Industry says they need clever, versatile people, well based in the fundamentals, who are problem solvers - in other words, generalists. Most educators tend to agree with this. On the other hand, the students who are hired the quickest and who get the best job offers are those who know how to do an I^2L layout or who can interface a microprocessor - in other words, specialists. Most educators are skeptical of such an approach because of the spector of obsolescence - today's I^2L was yesterday's T^2L. Because we really can't tell from industry what they want and what they don't want, we will sidestep the question in true academic fashion and tell them what they should want. This is shown in the Ideal EE Profile of Figure 1.

The profile breaks down into four categories: facts and rules (the fundamentals), skills, personality, and deductive-inductive reasoning. Examples of specific items in each category are given to illustrate their meaning, but these items are by no means complete. In this profile we have attempted to indicate which items in each category are strongly impacted (the educator might say reinforced) by microelectronics courses and laboratories.

It can be noted that the major impact of microelectronics courses would appear to be in the "hard" categories of Facts and Rules, and Skills while the major impact of microelectronic laboratories is in the "soft" categories of Personality and Deductive-Inductive Reasoning. The "hard" categories are, of course, the easy ones to teach while the "soft" categories are difficult, if not impossible, to teach - they must be learned. Therefore we can conclude

that microelectronic courses provide the student with the specific type of knowledge which industry likes to hire, while microelectronic laboratories help the student become more of a problem solver, which is the type of person industry says they want. Microelectronics in general, therefore, can only serve to enhance the student in industry's eyes.

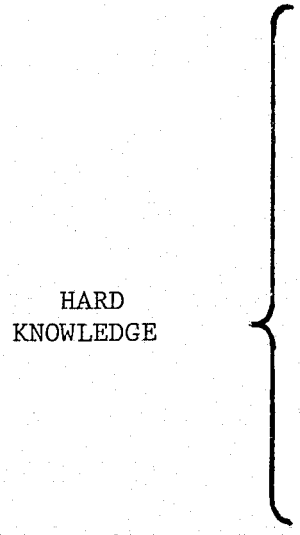
The only controversial part of the argument is why there isn't an "L" by technology; i.e., why doesn't a laboratory course teach technology? The reason is the rapidly changing nature of the technology. Gordon Moore[1] has pointed out that integrated circuits have doubled in complexity every year since their invention in 1959. This has been as a result of both improved technology (photolithography, diffusion, epitaxy, crystal growth, etc.) and greater design cleverness. The "new" technology can be discussed in courses, as can the "new" device structures which result from design cleverness, but with very few exceptions "new" technology is impossible to practice in a university environment. Consequently, the major advantage of laboratory courses is not in familiarizing the student with current technology, but rather in introducing him to the trial and error operation of the real world and allowing him to experience the satisfaction of seeing his design operate (sometimes). If average university laboratory technology (complexity) were correlated with Moore's curve, it would be found to correspond roughly to 1965.

As a final footnote to this discussion of the relevance of microelectronic education to industry needs, it should be pointed out that a microelectronics laboratory is not the only technique for enhancing the deductive-inductive reasoning ability of students. Almost any unstructured laboratory can be made to serve the same purpose. In fact, because of space, equipment, time, and supervision requirements serious questions as to the microelectronic laboratory's

cost effectiveness can be raised. The authors' conclusions, therefore, are that, despite what industry does or says, microelectronics courses are very relevant to their needs, but microelectronic laboratories are only relevant in a general sense.

---

[1] G. E. Moore, "Progress in Digital Integrated Electronics," IEDM, Washington, DC, 1975



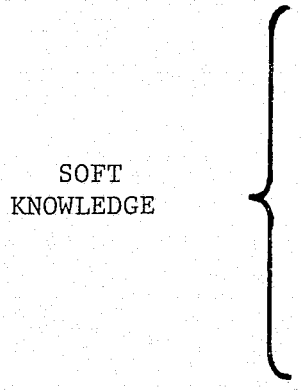
HARD KNOWLEDGE

Facts and Rules

chemistry	
physics	
mathematics	
solid state	C
thermodynamics	
electronics	C
network theory	

Skills

communication	
computer	
technology	C



SOFT KNOWLEDGE

Personality

teamwork	
self reliance	L

Deductive-Inductive Reasoning

engineering judgement	L
design tradeoffs	L/C
ingenuity	L

C = impacted strongly by microelectronics courses
L = impacted strongly by microelectronics laboratories

FIGURE 1. Ideal EE Profile

INNOVATIONS IN MICROELECTRONICS AND SOLID STATE AT N.C. A&T STATE UNIVERSITY*

by Leo Williams, Jr., Professor of Electrical Engineering
Greensboro, North Carolina 27411

ABSTRACT

North Carolina Agricultural and Technical State University at Greensboro, NC is a constitutent institution of the University of North Carolina. This paper describes funded research currently in progress in the following areas:

1. Characterization and Applications of Metallic Oxide Devices supported by National Science Foundation Grant No. SER 76-06793, under the direction of Prof. Leo Williams, Jr. and Dr. D.J. Filatvos, Mechanical Engineering Dept.

2. Electronic Properties and Energy Conversion in Organic Amorphous Semiconductors, supported by National Science Foundation Grant No. SER 76-07560, under the direction of Dr. G.J. Filatvos and Prof. Leo Williams, Jr.

3. Material Growth and Characterization directed toward improving III-V Heterojunction Solar Cells, supported by the Rockwell International Science Center, NASA Grant No. NSG-1390, and National Science Foundation Grant No. NSF DMR 77-19210, under the direction of Dr. Winser Alexander and Dr. E.K. Stefanakos of the Electrical Engineering Department. The first two projects mentioned above involve vastly different kinds of semiconductor materials, viz. oxides and compounds of vanadium and copper in contrast to melanins which are amorphous organic polymers. However, both kinds exhibit similar semiconductor properties such as threshold switching and memory effect. The third project involves III-V compounds and alloys such as gallium arsenide, liquid phase epitaxy techniques to produce solar cells.

*This paper was prepared for presentation at the Tennessee Valley Chapter of the International Society for Hybrid Microelectronics (ISHM) Conference on Microelectronics for the 1980's and for publication in the Conference Proceedings, September 20 & 21, 1977, Morris Auditorium-Marshall Space Flight Center, Huntsville, Alabama 35812

1. Characterization and Applications of Metallic Oxide Devices

The Electrical Engineering Department of NC A&T State University has developed a Microelectronics Laboratory with the capability of processing and evaluating thick film microelectronic components via NASA grants over the past seven years.[1,2] Concurrently with this development, studies and experiments were conducted involving the characterization of metallic oxides, primarily of copper and vanadium, which could have possible applications as switching, sensing and memory elements.[3,4,15] Effects of pressure, temperature, moisture, etc., on bulk resistivity of the oxides in powder, sintered, crystalline and in thick film forms were investigated. Static and dynamic volt-ampere tests as well as temperature-resistance tests were used in the characterization of these materials. More recently, thick film microelectronic fabrication techniques have been employed in conjunction with the semiconductors based on the metallic oxide (MO) materials to realize oscillator and switching devices.[5] Resistance anomalies and conductivity transitions in oxides such as titanium and vanadium have been studied extensively in the past.[10] In recent years, an increasing interst has been manifested in these as well as other transition oxides, and efforts are being made to gain greater insight into the possible causes and mechanisms involved in the insulator-resistor-semiconductor-metal transitions exhibited by them.[6,7,8,9] While the analytical and theoretical studies continue in an effort to explain the switching phenomena in MO materials, the possibilities of utilizing these materils in useful electronic devices has also been in evidence.[11-14] In general, no single theory gives a complete picture of the switching phenomena although they are generally considered to be thermally, and/or electrically and magnetically induced. The following consideration of recent research results on vanadium based compounds and materials which exhibit switching is not an exhaustive list of the materials processed and tested, but is representative of the work done in this area.

Vanadium trichloride, nitride, oxysulphate, trifluoride and tetrafluoride were investigated for switching, in pure form and then each individually with binary mixtures of V_2O_3, and V_2O_4 in various proportions of the oxides (20%, 50%, and 70%). Pure samples were placed in combustion boats and heated at 300 degrees C and at 450 degrees C for 30 minutes at each temperature. Samples of the various combinations (0.2gm each) were placed in plexiglas sample holders and compressed. The combinations were also mixed with both conductive and resistive organic vehicles to form samples in thick film form which were subsequently printed on alumina substrates and dried at 120 to 150 degrees C. Dynamic volt-ampere characteristics and temperature vs resistance tests were made on the various samples. Results of these tests are shown in Figure 1 and Figure 2.

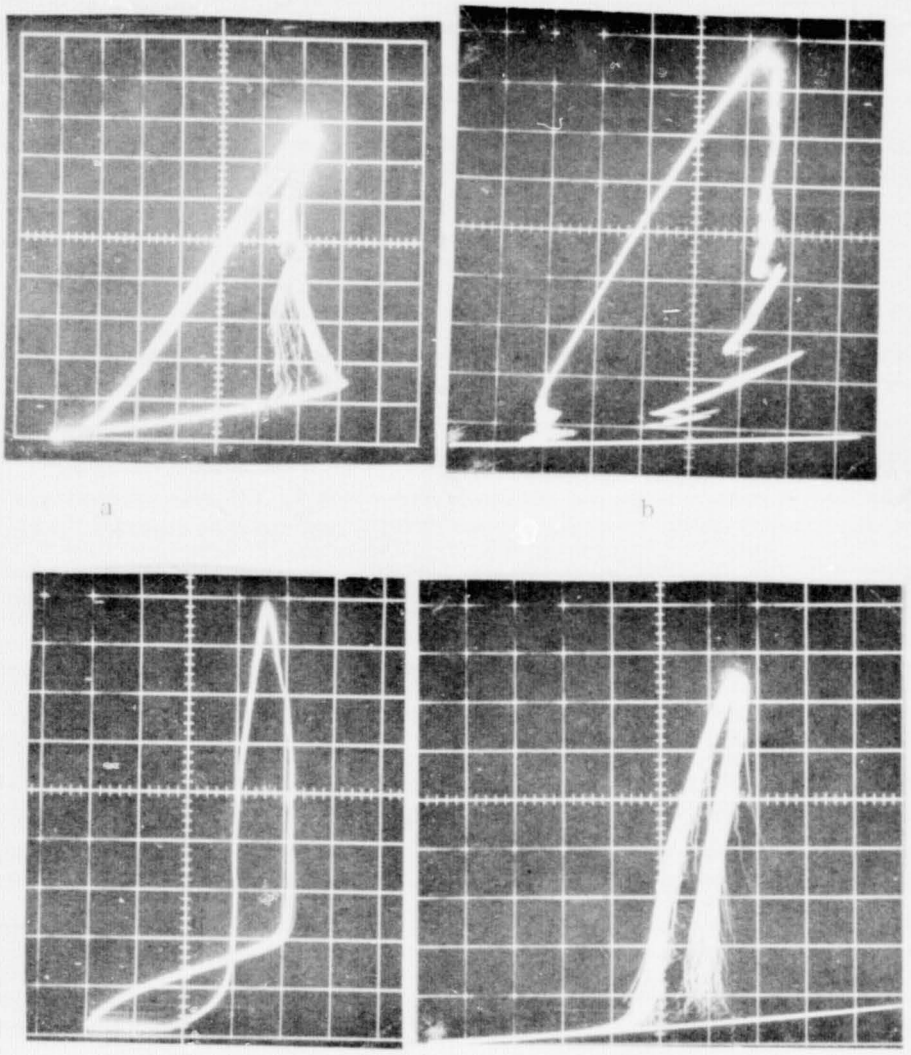


Figure 1. Dynamic volt-ampere curves for vanadium based compounds mixed with vanadium oxides. a) vanadium oxysulphate plus 50% vanadium tetroxide cured at 300° C, 1.0V/div, 1.0 mA/div. b) vanadium nitride plus resistive vehicle printed on alumina substrate, 0.5 V/div, 2.0 mA/div. c) vanadium pentoxide plus 50% phosphorus pentoxide, 2.0V/div, 0.2 mA/div. d) vanadium trifluoride plus 50% vanadium tetroxide, processed at 450° C. 1.0V/div, 50.0mA/div.

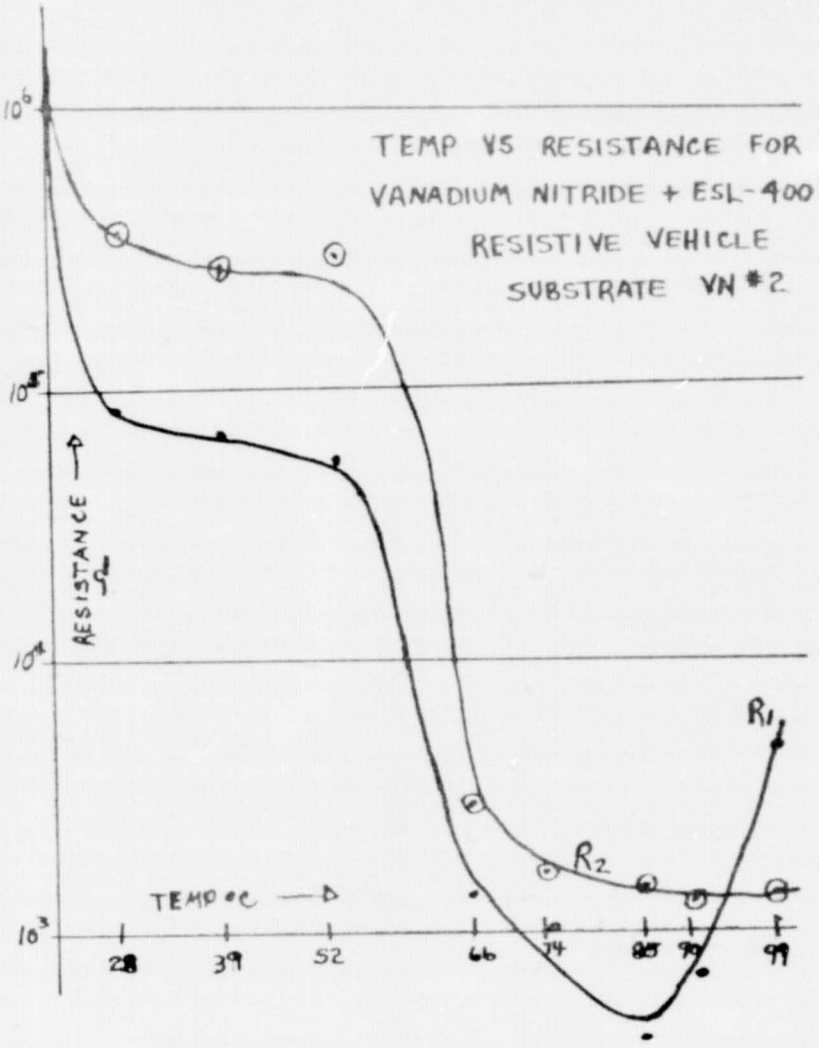


Figure 2. Temperature versus resistance plot of a vanadium compound sample printed on an alumina substrate. R_1 is the same sample as shown in Figure 1 (b)

Pulse tests were used to determine sample switching times as well as the minimum transition energy, W_1, required to initiate the high to low resistance transition. Since the energy supplied to a sample at any time after application of a pulse is given by equation (1), the actual product integration of the instantaneous applied voltage and current with respect to time was obtained from the oscillogram of these wave forms using a two channel oscilloscope and camera.

$$(1)\quad W = \int_0^t vi\,dt$$

Minimum transition energy was obtained by integrating (1) from the time of pulse application to the time, e.g., t_1, at which an abrupt increase in current occurred (indicating the transition from a high to low resistance state). Thus, t_1 read directly from the oscillogram would be maximum turn-on time corresponding to W_1 at a given ambient temperature. Minimum turn-on times would correspond to the time required for the current to increase from its low to high value. Transition energies of a few microjoules were observed, corresponding to minimum turn-on times in the tens of microsecond range for some of the samples. Both high and low dynamic resistances for the various samples could be obtained from pulse tests. Static resistance anomalies as measured by temperature-resistance tests were greater than 10^5 ohms (five decades) for some samples.

Indications are that these materials could have applications as high speed electronic switching, memory, sensing and oscillator devices. Our future research plans are to realize these materials in much smaller sizes and in thin film form with the objective of reducing switching times to the nanosecond range.

2. Research on Amorphous Semiconductors, Melanins

Melanins are amorphous organic polymers which exhibit most of the properpies of amorphous semiconductors, such as photoconductivity, the ability to threshold switch, and a memory effect. It is believed that melanins act as degraders of biologically active quanta, as melanins are found is sites where some form of energy or charge transfer occurs, such as the skin, midbrain, retina, and inner ear. Nature, through evolution, has apparently developed an extremely effective amorphous semiconductor, the study of which may lead to the development of a new class of polymer-based semiconductor devices. In addition, the melanins offer a unique experimental system for the development of a working concept of biological semiconductivity.

In our work at NC A&T State University, we have studied the responses of various melanins to applied electric fields, under various conditions. Melanins in biological systems does not usually occur in a free form, but is polymerized

into a structure, the melanosome, containing lipid and protein. We have used both synthetic and melanosome melanins. The advantage of synthetic melanins is the control of compositional variables, and the addition of controlled amounts of guest (dopant) molecules.

The characteristics which qualify melanins as more sophisticated semiconductors is their ability to threshold switch, and to memory switch. Memory and threshold switches have the common characteristic of switching from a high to a low impedance state on application of a slowly increasing voltage to a threshold voltage V_t, or after a minimum duration pulse of sufficient voltage. The principal difference is that the threshold switch requires a holding current to maintain the conductive state while the memory switch remains conductive after removal of the electric field. In the case of melanins, we believe that threshold switching is another manifestation of memory state.

The figure below summarizes some of our findings.[17] There is a "window" of conditions, with a definite thermal and electrical bias required to activate the memory state. In addition, there is a strong hydration dependance. This on state dependance has been observed in both synthetic and melanosome melanin, with the values of specific switching parameters differing for various melanins. The critical temperature and applied field are used as they are the easiest external variables to control. The current and power are also obviously of interest, and are being studied. However, neither the hydration nor temperature nor current nor applied field, nor power alone is sufficient to assure switching. One must specify the temperature, the hydration and either the applied field, current, or power. In addition, we suspect that there are additional controlling factors such as molecular size, size distribution, and composition, and these are presently under investigation.

In summary, we believe that the study of melanins offers potential into both development of new technological materials, and increased understanding of <u>in vivo</u> semiconduction processes.

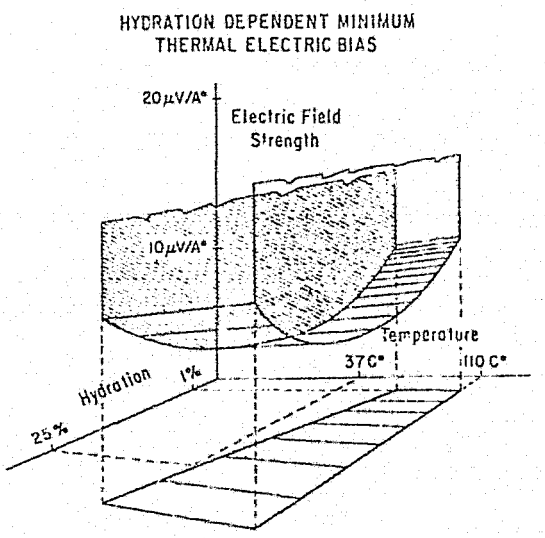


Fig. 3 The minimum temperature and electric field required to produce the on state depend on the hydration as illustrated. The on state can only be produced within the shaded region for a 0.1-sec pulse. Attempts to switch these materials outside the appropriate region for the pulse duration and type of melanin will be unsuccessful. It is essential, therefore, to obtain this type of plot for materials which have not been previously investigated.

3. Solar Cell Research in the Rockwell Solid State Laboratory

The development of the Rockwell Solid State Electronics laboratory started about a year ago. At this time the materials growth and metalization areas are equipped with two complete liquid phase epitaxy (LPE) systems and an E-Beam evaporator. It is expected that a current controlled LPE apparatus will be operational by the end of September. A photolithography room is presently under preparation and expected to be completed by November 1977. Four Master of Science students and four full-time faculty members are presently engaged in research.

The overall objective of the program is to achieve an ongoing capability with facilites for material growth and characterization and device fabrication and testing emphasizing III-V compounds and alloys grown by liquid phase epitaxy and applied to solar cells and other electro-optic devices.

The main objective of the NASA project is to fabricate and test high efficiency solar cells consisting of GaAlAs, GaInAs and GaAs layers. Figure 4 shows a 2 micron epitaxial layer of n-type GaAs grown on p-type GaAs by liquid phase epitaxy (LPE). The layer was grown by cooling the Ga - As saturated melt at 800° C for 30 minutes with a rate of 0.1° C/minute. Figure 5 shows the surface morphology of the GaAs epi-layer of Figure 1. The etch-pits on the surface are probably a result of either thermal etching of the substrate during the time of melt saturation or strong chemical etching of the substrate during substrate preparation. Figure 6 shows the first GaAlAs-GaAs heteroface solar cell fabricated in our laboratories. The power efficiency of the solar cell was about 8% without antireflective coatings.

The main objective of the NSF project is to study the advantages of the so called "Current Controlled Liquid Phase Epitaxy" technique for the growth of III-V compound thin layers. When an electrical d-c current passes across the semiconductor melt interface during normal LPE, the interface is cooled as a result of the peltier effect. This cooling can be used to grow epitaxial layers at constant furnace temperature. Current controlled liquid phase epitaxy was used to grow InP on InP substrates. Figure 7 shows the dependence of layer thickness on current density for a growth period of two hours at a furnace temperature of 650 C. The observed growth rates are at least one order of magnitude larger than the rates anticipated on the basis of the measured Peltier cooling at the interface. Connection and electrotransport of the solute (P) atoms are two possible mechanisms which may contribute to the large growth rates. Growth at constant furnace temperature, growth at temperatures lower than those used with normal LPE, and current modulation of impurities[16] are some of the potential advantages of current controlled LPE.

Figure 4.

Photomicrograph of a cleaved section showing a 2 micron epitaxial layer grown on an N-type GaAs substrate at 750 degrees Centigrade

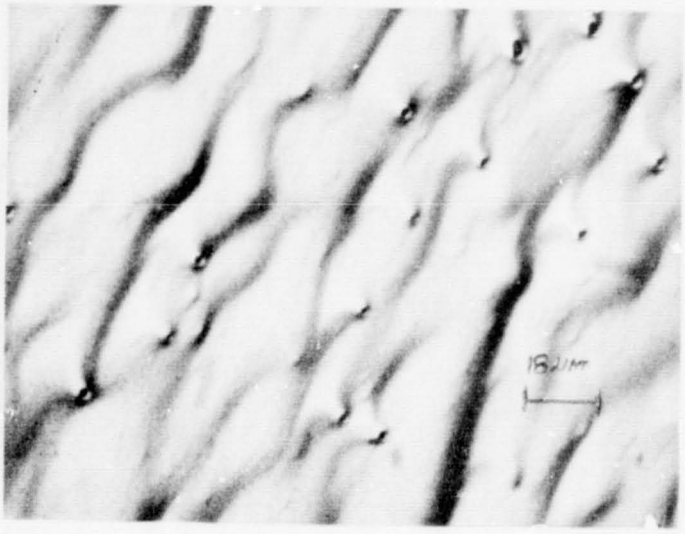


Figure 5.

Photomicrograph of the surface of the grown layer showing etch-pit and surface irregularities

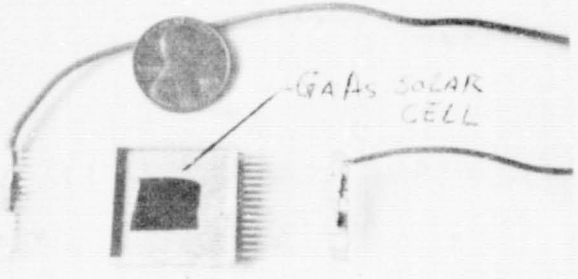


Figure 6.

The first GaAlAs-GaAs heteroface solar cell fabricated in the NCA&TSU Solid State Laboratory

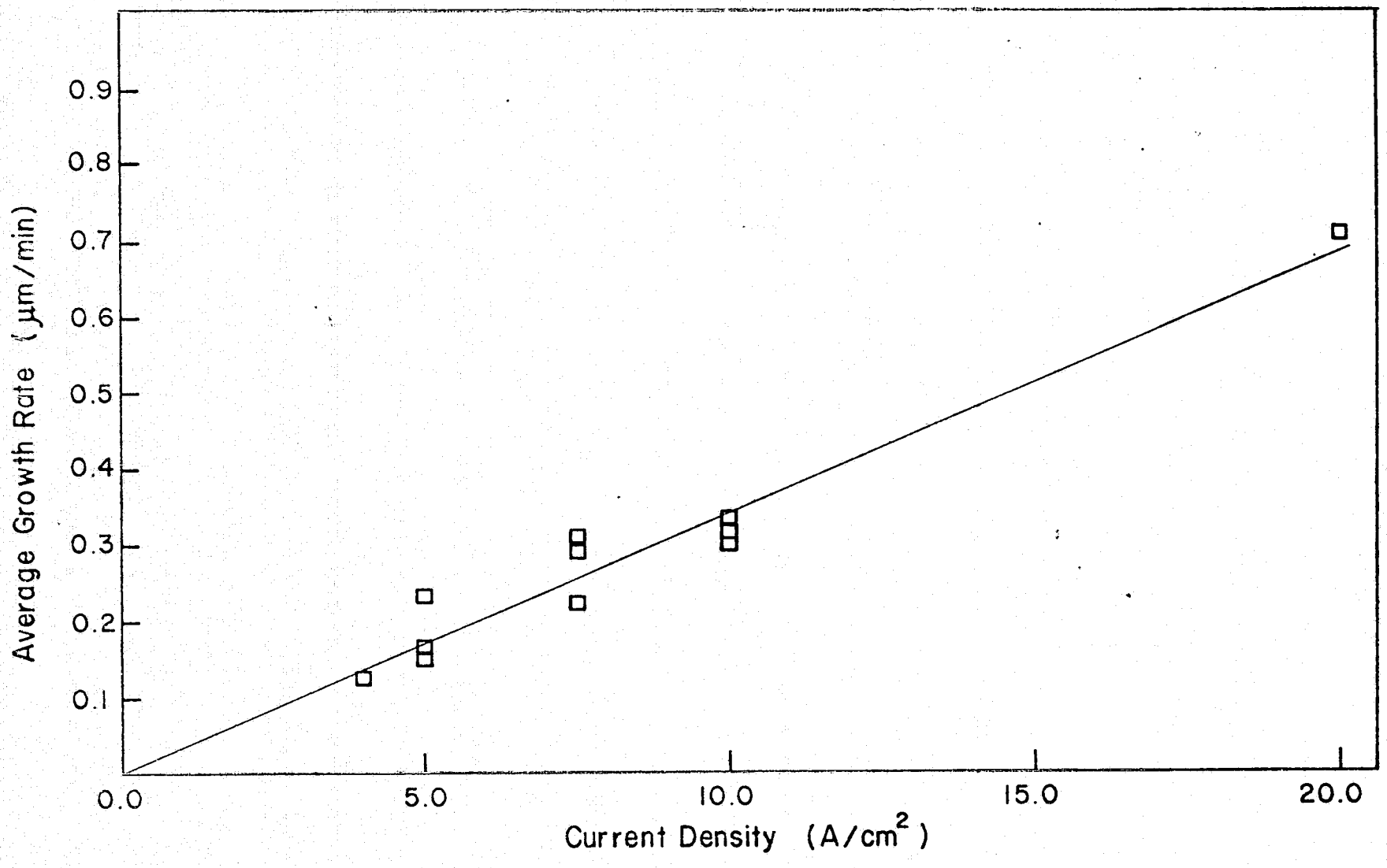


Figure 7. Average growth rate versus current density for current-controlled LPE growth of InP at 650 degrees Centigrade[16]

REFERENCES

1. L. Williams, Jr., "Evaluation tests of NASA thick film resistors over a six year period," American Ceramic Society Bulletin, p. 359, Apr., 1972
2. L. Williams, Jr., "Evaluation tests on commercial thick film resistors," American Ceramic Society Bulletin, p. 606, August, 1974.
3. L. Williams, Jr., "Experimental studies and applications of vanadium oxides," Proc. 1972 Int. Microelectronic Symp., (ISHM), pp. 4A51-4A521, Oct. 1972.
4. D.N. Patel and L. Williams, Jr., "Metallic oxide switches using thick film technology," Proc. 1974 Int. Microelectronic Symp. (ISHM) pp. 477-485, Oct. 1974.
5. L. Williams, Jr., "Oscillator Devices Using Thick-Film Technology," IEEE Vol. PHP-13, March, 1977.
6. C.N. Berglund and N. Klein, "Thermal effects on switching of solids from an insulating to a conductive state," Proc. IEEE, Vol. 59, July 1971.
7. G.J. Hyland, "Semiconductor-Metal Phase Transistions," Journal of Solid State Chemistry 2, p. 318-331 (1970).
8. B.K. Chakraverty, "Insulator-Metal Transitions: Experimental Results," International Symposium, Electronic Properties of Oxides / Applications and Science, Purdue University, May 29 - June 1, 1974.
9. R.A. Bari, "Insulator - Metal Transitions: Theoretical Models,"
10. F.J. Morin, "Oxides Which Show a Metal-to-Insulator Transition at The Neel Temperature," Physical Review Letters, Vol. 3, #1 P. 34-36 (1959)
11. Hisao Futaki, "A New Type Semiconductor (Critical Temperature Resister), Japanese Journal of Applied Physics, Vol. 4, #1 (1965).
12. R.G. Cope and A.W. Penn, "High Speed Solid-state Thermal Switches Based on Vanadium Dioxide, Brit. J. Appl. Phys. (J Phys. D), Ser 2, Vol. 1 (1968), pp. 161-168.
13. Hisao Futaki, "Oscillation Phenomena and Switching Phenomena of V_2O_4 Semiconductors (CTR)," Hitachi Review Vol. 18, No. 11, pp. 440-452, 1969.
14. Y. Taketa, F. Kato, M. Nitta, and M. Haradome, "New thick film oscillation devices," Proc. 1975 Int. Microelectronic Symposium (ISHM), pp. 445-452.
15. L. Williams, Jr., "Experimental studies and applications of copper and vanadium oxides," American Ceramic Society Bulletin, p. 358, Apr. 1972.
16. Abul-Fadl, A., Stefanakos, "Current Controlled Liquid Phase Epitaxial Growth of InP," accepted for publication in J. Crystal Growth, Oct. 1977.
17. J. Filatovs, J. McGinness, P. Corry, "Thermal and Electronic Contributions to Switching in Melanins," Biopolymers, Vol. 15, pp. 2309-2312, 1976.

APPROVAL

Microelectronics for the Nineteen Eighties

Microelectronics Conference held by the Tennessee Valley Chapter of the International Society for Hybrid Microelectronics on September 20 and 21, 1977, at the Marshall Space Flight Center, Huntsville, Alabama.

The information in this report has been reviewed for security classification. The report, in its entirety, has been determined to be unclassified and contains no information concerning Department of Defense or nuclear energy programs or activities.

Harrison Garrett

HARRISON GARRETT
Chief, Electronics Development Division

F. Brooks Moore

F. BROOKS MOORE
Director, Electronics and Control Laboratory