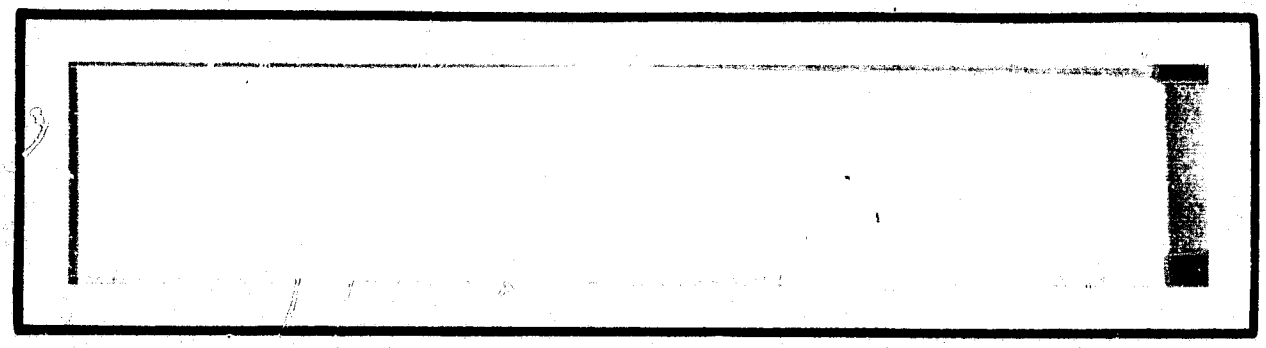

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SHUTTLE ORBITER KU-BAND RADAR/COMMUNICATIONS SYSTEM DESIGN EVALUATION

KU-BAND BENT-PIPE CHANNEL PERFORMANCE EVALUATION

Contract No. NAS 9-15795B

Task #1 Interim Report

(JSC Technical Monitor: E. B. Walters)

Prepared for

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1.0 INTRODUCTION

1.1 Background

This report describes results obtained under Task #1, Exhibit "B", "Ku-Band Bent-Pipe Channel Performance Evaluation." Since Hughes has been experiencing the greatest difficulty with the wideband bent-pipe channel, we have concentrated our efforts in this area. Specifically, the SPA mode 1 channel 3 input port has a bit detector which is the subject of considerable redesign effort by Hughes. This port accepts high data rate NRZ data (2 - 50 Mbps) and clock. The SPA input bit detector attempts to sample the data at mid-bit in order to preclude sampling during a transition. The inherent problem is the wide variability of data rate and input waveform parameters.

The original bit detector circuit consisted of a derived two-phase clock and a coincidence circuit. Proximity of data/clock transitions would trigger sampling on the alternate clock phase. This circuit proved to be unstable under worst-case conditions of data asymmetry and rise time. A relatively simple modification, that of providing a four-phase clock, also proved unsuitable at the higher data rates. As a result, Hughes has had to design a new bit synchronizer.

1.2 Summary

This report describes the two principal designs considered by Hughes as well as our analysis of these designs. During the progress of this work, it became evident that the input waveform parameters had not been adequately characterized and specified. In particular, distortion due to cable effects, in terms of frequency-dependent attenuation and rise time, had not been accounted for. In Appendix A, we discuss the model used to calculate the effects of cable attenuation and rise time degradation. Results of this analysis were subsequently incorporated in the Rockwell specification. Discussions of the two prime candidate designs for a bit synchronizer are contained in Appendices B and C.

The first synchronizer, which was proposed by Pat Conway, is shown on page 2 of Appendix B. Since a detailed description is given in Appendix B, we will summarize by stating that this loop utilizes a phase-frequency detector to frequency track the received data clock

frequency and a mid-bit and transition point sample detector to generate a bit timing error (phase error) signal to control the relative phase between the local clock and the local data stream.

It was determined that the basic design was adequate with symmetric bits but could lock up with a large timing error and be quasi-stable (timing will not change unless the clock or bit sequence drifts). This will result in incorrectly detecting some bits.

In particular, for the case of 25% asymmetry at 50 Mbps, the following is true:

(1) With timing errors up to ±2.5 ns (±12.5%), no timing change is performed by the loop and no bit errors will be made.

(2) With timing errors between ±2.5 ns and ±7.5 ns (±37.5%), the loop error control will reduce the timing error and no bit errors will occur.

(3) With timing errors between ±7.5 ns and ±10 ns (±50%), the loop will not adjust the timing error, but bit errors will occur.

A second bit synchronizer was analyzed and is treated in detail in Appendix C. This synchronizer also utilizes a phase-frequency detector as the first one did, but has a different and rather complex bit timing error detector to adjust the phase between the received and local bit epochs. Whereas the Conway synchronizer tracked transitions, this synchronizer tracks rising edges of the bit stream only. It was determined (Appendix C) that this new bit synchronizer will successfully track the rising edges of the received data bits with 25% asymmetry and up to a 90° phase shift between the received clock and the data bit timing. Furthermore, the data bits will be sampled correctly under these conditions. In both synchronizers, it is advisable to zero the digital-to-analog converter loop filter voltage in order to avoid the possibility of false lock.

2.0 CONCLUSIONS

Hughes has elected to implement the modified Pat Conway bit synchronizer as described in Appendix C. With input data and clock parameters within the specified limits, the bit synchronizer should track and bit detect correctly.

APPENDIX A

HIGH DATA RATE CHANNEL CABLE AND CONNECTOR LOSS EFFECTS

By

James G. Dodds

1.0 INTRODUCTION

During the redesign effort of the mode 1 channel 3 bit synchronizer, it became obvious that the current input specifications were inadequate. The specifications did not account for data-dependent losses, e.g., losses incurred due to cable attenuation of the higher frequencies, whereas this effect had been noted in cable measurements. In addition, rise time effects had not been adequately modeled. Since the new bit synchronizer is going to incorporate a variable threshold to adaptively set decision levels, it has become mandatory to more accurately predict the input waveform parameters.

2.0 DATA-DEPENDENT LOSS EFFECTS

The concept of data-dependent loss is depicted in Figure 1. A long run of 1's or 0's will allow the cable output voltage to reach MAX "1" or MIN "0", respectively, whereas a single pulse preceded and followed by data of the opposite sense will attain only MIN "1" or MAX "0."

The analysis techniques involved modeling the frequency-dependent loss of the cable and connectors, calculating the Fourier transform of a single pulse, attenuating the Fourier coefficients, and taking the inverse transform to ascertain the loss. In actual fact, since the calculations were performed on a computer, the most simple approach was to approximate the single pulse with a very low duty cycle rectangular pulse train. Thus, the Fourier series was used.

Worst-case conditions assume 92 ft of cable with seven connector pairs. From [1], we find that the cable attenuation of RG142 can be modeled as $1.92 \times 10^{-4} f^{0.538}$ dB per 100 ft. This is derived from the table on page 194 of [1] by using a linear regression of the tabular data. The resultant correlation coefficient is 0.9997, indicating that the log of attenuation versus the log of frequency can be accurately approximated by a straight line in the range of interest. Assuming SMA connectors, the connector loss is given as $0.03 \sqrt{f_{GHz}}$ dB per connector.

The resultant data-dependent loss is calculated to be 11.4%. That is, a single pulse will be 88.6% of the steady-state voltage difference. This can be written as:

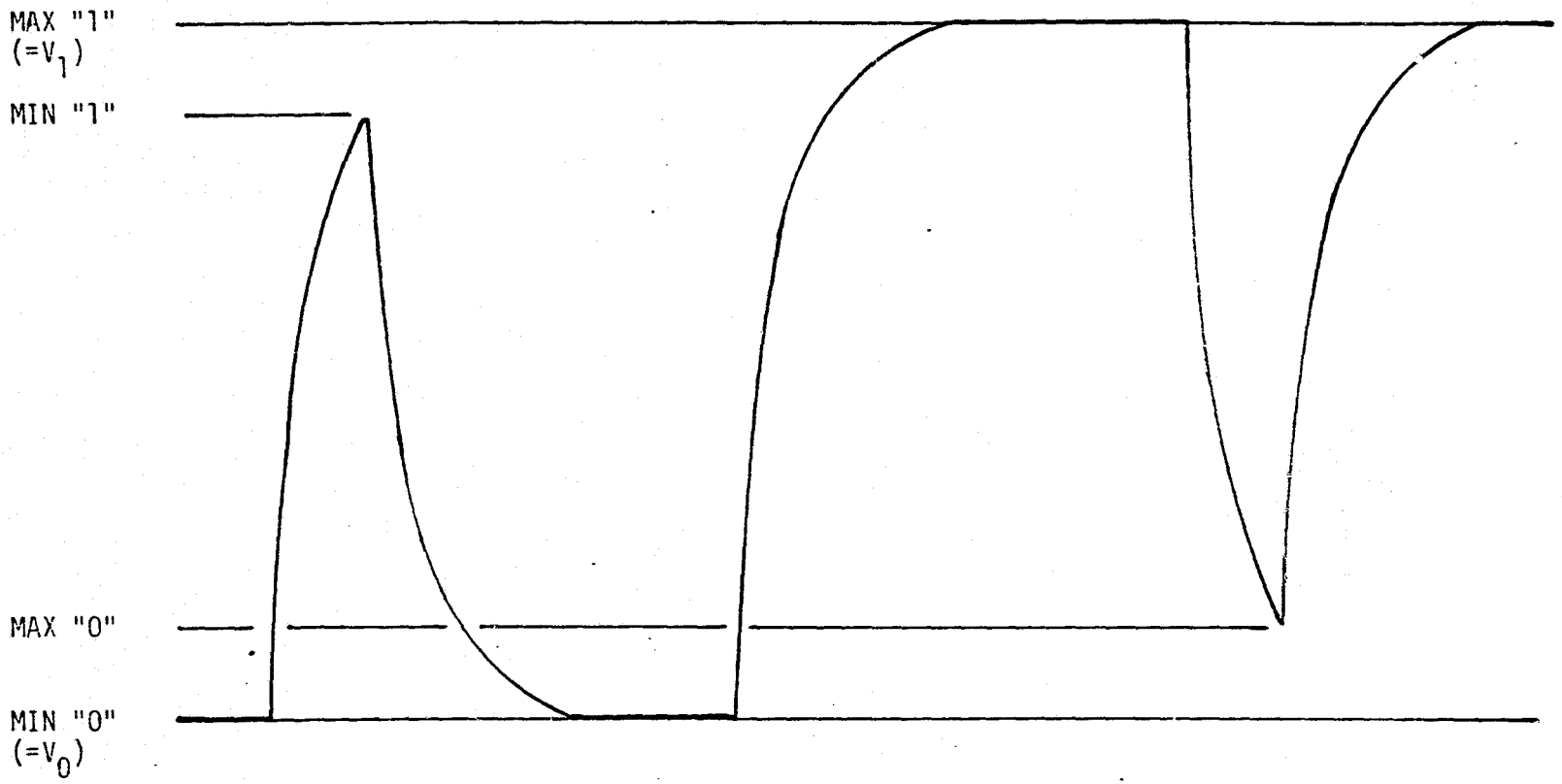

Figure 1. Worst-Case Short-Term Variation Single Pulse After Steady State

$$\text{MIN "1"} = V_0 + 0.886\,(V_1 - V_0)\ ,$$

$$\text{MAX "0"} = V_1 - 0.886\,(V_1 - V_0)\ .$$

3.0 CABLE RISE TIME EFFECTS

The response of a cable to fast rise time inputs cannot be modeled as a simple filter. Cable measurements indicate a very rapid initial rise, followed by a slow tapering off to the final value. From [2] and [3], we find that the response to a unit step (1/S) input can be given as:

$$V[t] = 1 - \text{erf}\left(\frac{\ell\, K}{4R_0\sqrt{t}}\right)\ ,$$

with ℓ the cable length, K the cable attenuation constant in ohms per unit length per square root hertz, and R_0 the characteristic impedance. This expression is obtained by multiplying the Laplace transform of the cable transfer function by 1/S, then taking the inverse transform.

The parameter K is not necessarily readily available for all cables. Cable specifications are normally supplied as dB attenuation per 100 ft at a specific frequency.

We can determine K/R_0 as a function of attenuation, as follows:

$$\frac{E_0}{E_i} = e^{-\left(\frac{K}{R_0}\right)\frac{\sqrt{S}}{2}\ell}\ , \text{ the cable transfer function.}$$

With $s = j\omega$ and $\sqrt{j} = \frac{1+j}{\sqrt{2}}$,

$$\frac{E_0}{E_i} = e^{-\frac{K}{R_0}\ \frac{\sqrt{f}\ \sqrt{2\pi}}{2}\ \frac{(1+j)\ell}{\sqrt{2}}}\ ,$$

A, attenuation per 100 ft, is

$$A = \left|\frac{E_0}{E_i}\right| = e^{-\left(\frac{K}{R_0}\right)\sqrt{f}\ \frac{100}{2}\ \sqrt{\pi}}$$

and

$$A\left(\frac{dB}{100\ ft}\right) = 20 \log \left[e^{\left(\frac{K}{R_0}\right)\sqrt{\pi}\ \sqrt{f}\ 50}\right]$$

$$= 10^3 \left(\frac{K}{R_0}\right) \sqrt{\pi f} \log e$$

Thus,

$$K/R_0 = \frac{A}{\sqrt{f}}\left(\frac{1}{\log e\ \sqrt{\pi} \times 10^3}\right),$$

which can be substituted into the step response to give

$$V(t) = \text{erfc}\left(\frac{3.25 \times 10^{-4}\ \ell A}{\sqrt{t}\ \sqrt{f}}\right).$$

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2. Dreher, Thad, "Cabling Fast Pulses? Don't Trip On The Steps," The Electronic Engineer, August 1969.

3. Botos, Bob, "Nanosecond Pulse Handling Techniques in I/C Interconnections," Motorola Applications Note #AN-270.

APPENDIX B

CRITIQUE OF A HUGHES SHUTTLE KU-BAND DATA SAMPLER / BIT SYNCHRONIZER

By

Jack K. Holmes

1.0 SUMMARY AND CONCLUSIONS

A bit synchronizer proposed by P. H. Conway of Hughes Aircraft is analyzed in a noise-free environment. This task is accomplished by considering the basic operation of the loop via timing diagrams and by linearizing the bit synchronizer as an equivalent, continuous, phased-lock loop (PLL).

It was determined that the basic approach was a good design which, with proper implementation of the accumulator, up/down counter and logic should provide accurate mid-bit sampling with symmetric bits.

However, when bit asymmetry occurs, the bit synchronizer can lock up with a large timing error, yet be quasi-stable (timing will not change unless the clock and bit sequence drift). This will result in incorrectly detecting some bits. The apriori probability of falling into this quasi-stable region is equal to the asymmetry (defined in Section 6.0) expressed as a fraction. This assumes a uniform distribution over T sec. Thus, except for the case of no asymmetry, there is always some possibility of remaining in lock but incorrectly detecting some bits.

As a final comment, if the timing difference between the bit stream and the clock can be held to less than $\pm \frac{1-ASY}{2}$ T sec (T is the undistorted bit duration), the bit synchronizer loop will never get into the third zone, where bit errors are made but the loop holds lock.

2.0 INTRODUCTION AND DESCRIPTION OF THE NEW BIT SYNCHRONIZER

The purpose of this report is to discuss one "fix" to the operation of a Shuttle Ku-band bit synchronizer which utilizes both clock and data inputs. The present bit synchronizer has a jitter problem and, consequently, occasionally will sample the same bit twice and skip the following bit.

An alternative bit synchronizer suggested by P. H. Conway of Hughes Aircraft [1] is shown in Figure 1. The loop is composed of a Motorola high-frequency phase-frequency detector (ϕ-DET) [2-4] which is capable of detecting both phase and frequency errors and is used to track the clock, and a bit transition detector which attempts to track the transitions of the data bits.

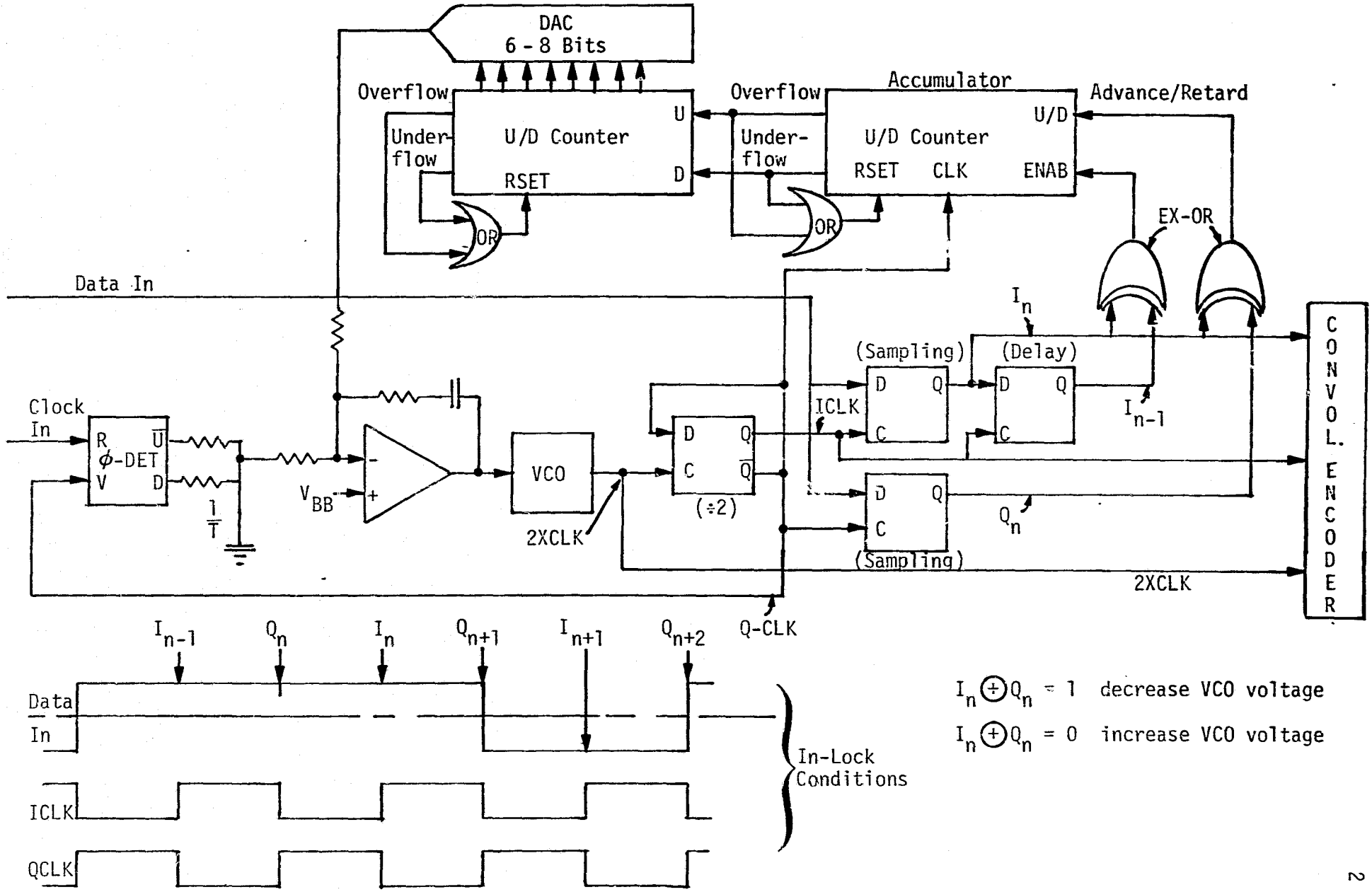


Figure 1. Ku-Band Data Sampler With PLL Clock Tracking

The Q clock signal shown in Figure 1 is compared with the received clock (clock in) which, by virtue of the phase/frequency detector, produces a signal which has a dc component proportional to the frequency error (if there is one). Then, when in frequency lock, it produces a signal which has a dc component proportional to the phase error between the input clock and the VCO output.

Now, if the digital-to-analog converter (DAC) output was not hooked up to the loop filter, the bit synchronizer would track the received clock with negigible phase error. However, since the received clock and data are at the same frequency but are not phase coherent, it is necessary to bump the clock phase so that data samples are taken at mid-bit. The function of the DAC is to provide samples of the data at the mid-bit point. The VCO clock runs at twice the rate of the received clock and is divided down to the clock rate by the D flip-flop following the VCO. Actually, this flip-flop provides both an I and a Q clock which are phased one-half a bit apart, as shown in the lower left corner of Figure 1.

The I and Q clocks are used to sample the data one-half of a bit apart, when synchronized. This sampling is effected by the two D flip-flops following the divide by 2 flip-flop. By using the "exclusive-OR" of two successive data samples, a transition detector is created, thereby producing a binary one with a transition and a binary zero when there is no transition. This control enables or disables the up/down counter to count either up or down. By comparing the I and Q data samples (I_n and Q_n in Figure 1), an estimate of the error in the actual transition sample (Q_n) and the data transition location is obtained. It is to be noted that the exclusive-OR output yields only the algebraic sign of the error, not the magnitude. This error, assuming a data transition, will be accumulated in the up/down (U/D) counter until it either underflows or overflows. The accumulator actually has two functions. The first is to reduce the speed to the DAC; the second is to control the quantization of the loop phase error control. The second up/down counter feeds into a DAC which converts the accumulated count into an analog voltage, which drives the bit synchronizer loop filter. In effect, the up/down counter acts upon the bit timing error signal the same way

an integrator would. This integration is precisely what is needed to force the mid-bit data sampler into the mid-bit position! This fact will be made clearer in Section 5.0.

In conclusion, the bit synchronizer shown in Figure 1 is designed to track the clock and sample the data sequence at the mid-bit point. We now consider the phase/frequency detector and the bit detector in more detail in the following sections.

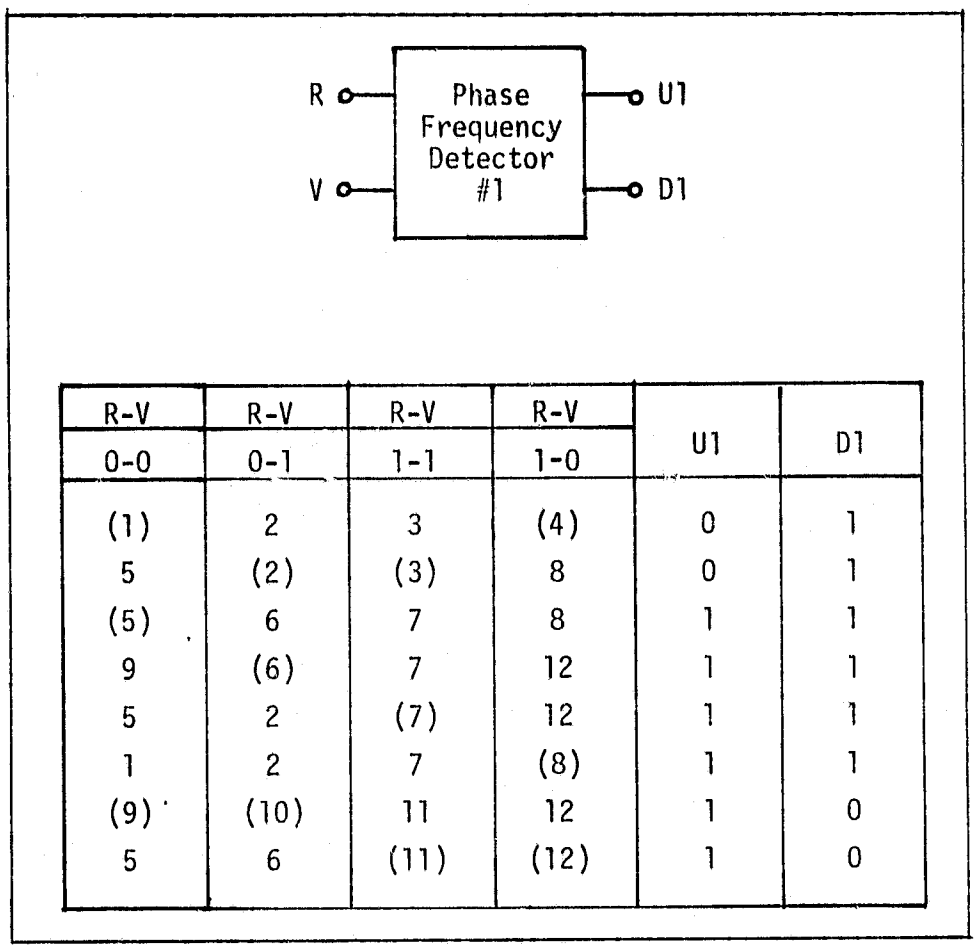
3.0 DESCRIPTION OF THE MOTOROLA PHASE/FREQUENCY DETECTOR

Both the MC4344/MC4044 [3] and MC12040 [4] Motorola phase/frequency detectors can be used in a broad range of phased-lock loop applications. Both sets of detectors are functionally equivalent, however, the MC12040 is capable of operating at higher clock speeds. Because of the functional equivalence, we shall confine our discussion to the MC4344/MC4044 unit.

The Motorola MC4344/MC4044 phase/frequency detector is composed of a phase/frequency detector, a quadrature phase detector, a charge pump and an amplifier. It is the function of the charge pump to convert the pulses out of the phase/frequency detector to a DC value which is essentially proportional to either the phase or frequency error.

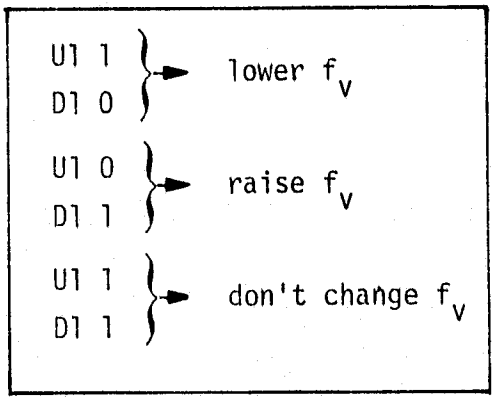
In Figure 2, the phase/frequency flow table for the phase/frequency detector is given, along with the charge pump/amplifier frequency control.

In order to understand the usage of Figure 2, we shall consider an example. Assume that the received clock (R input to the ϕ-frequency detector) lags the local reference (V input to the ϕ-frequency detector) by one-twelfth of a square wave clock cycle, as shown in Case I of Figure 3. Starting at state 8 in Figure 3 which corresponds to the R,V pair being in state 1,0, we go to Figure 2a and note that state (8) (with the parentheses) produces an output U1 = 1 and D1 = 1. Now, in the time interval denoted by (7), we note that R,V = 1,1. Moving horizontally in the same row to the left, one column (under R-V = 1,1), we find a seven. Therefore, we look vertically in the column for (7) which we find one row higher, with a corresponding output of U1 = 1 and D1 = 1. The next input is R = 0, V = 1. Moving horizontally in the fifth row, we find a 2. Moving vertically to the second row, we find the (2), which has a



R-V 0-0	R-V 0-1	R-V 1-1	R-V 1-0	U1	D1
(1)	2	3	(4)	0	1
5	(2)	(3)	8	0	1
(5)	6	7	8	1	1
9	(6)	7	12	1	1
5	2	(7)	12	1	1
1	2	7	(8)	1	1
(9)	(10)	11	12	1	0
5	6	(11)	(12)	1	0

(a) Phase Frequency Detector Flow Table



(b) Charge Pump-Amplifier Control

Figure 2. Phase/Frequency Detector Flow Table and the Charge Pump-Amplifier Frequency Control

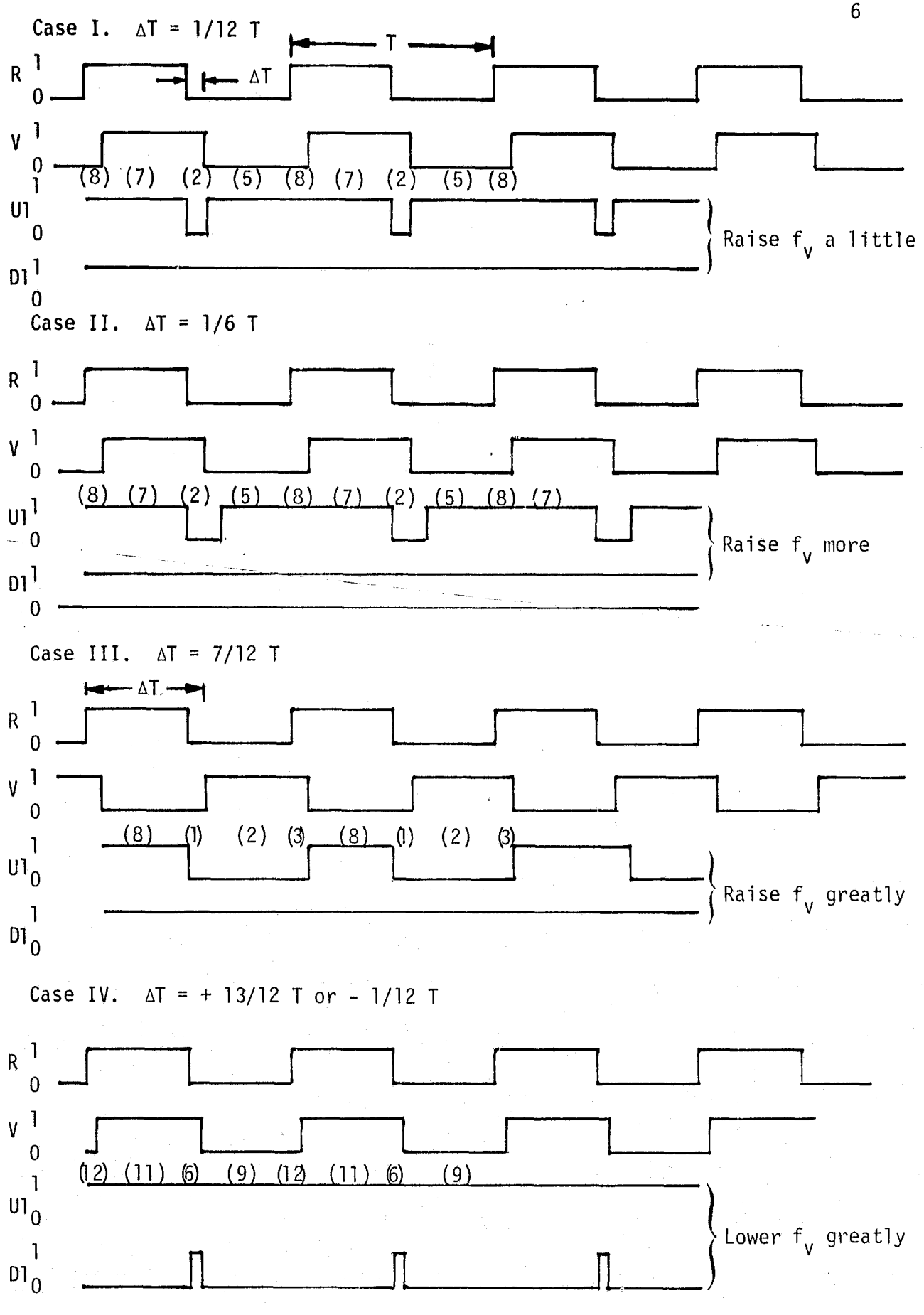


Figure 3. Performance of the Phase/Frequency Detector for Various Phase Errors

corresponding output of U1 = 0, D1 = 1. Hence, at this point, the U1 output drops to zero while the V1 remains at one, as shown in Figure 3. Continuing in this manner, we find that the phase/frequency detector goes through the states (5), (8), (7), (2), (5), (8), etc., generating the waveforms U1 and D1 shown in Case I, Figure 3. Now, by considering Figure 2b, we see that, when U1,D1 = 0,1, the DC voltage out of the charge pump/amplifier is increased and, when U1,D1 = 1,1, the DC voltage does not change. As a consequence, the DC voltage applied to the loop filter-amplifier increases to the VCO input, causing the local reference to catch up to the received clock.

By viewing Figure 3 cases II and III, it is seen that a large timing or phase error produces a larger DC voltage out of the charge pump. By virtue of the way the charge pump works, the error control signal, when properly smoothed, is proportional to the timing error over the region $\pm T$, where T is the clock or bit period. In viewing the error to be phase rather than timing, we find the error signal to be linear over $\pm 2\pi$.

In case IV of Figure 3, the situation when the timing error is increased to $\frac{13}{12}$ T $\left(\text{or} - \frac{1}{12} \text{T}\right)$ is shown. Even though the error is equivalent to case I of Figure 3, the error signal derived from the flow table of Figure 2 yields a different error control voltage. The reason for this difference is obvious when one considers the S-curve of Figure 4.

Because of the memory in the phase/frequency detector, there are two error control signals for each error position, or phase error, ϕ. The arrows in Figure 4 indicate how the the loop behaves as the phase increases, first to 2π and then to 4π on a different branch, then returns to zero on the new branch. The original stable point was 0 rad on the first branch but the second branch is stable at 2π rad (T sec).

The above discussions were concerned with phase or timing errors. We now consider frequency errors. Using the flow table of Figure 2a, we can establish that, when $f_R/f_V = 10$ or when $f_V/f_R = 10$, error control amplitude is monotonically increasing with increasing frequency error (it is not linear). The results are plotted in Figure 5 for the case of 10:1 frequency error and Figure 6 for 3:1 errors.

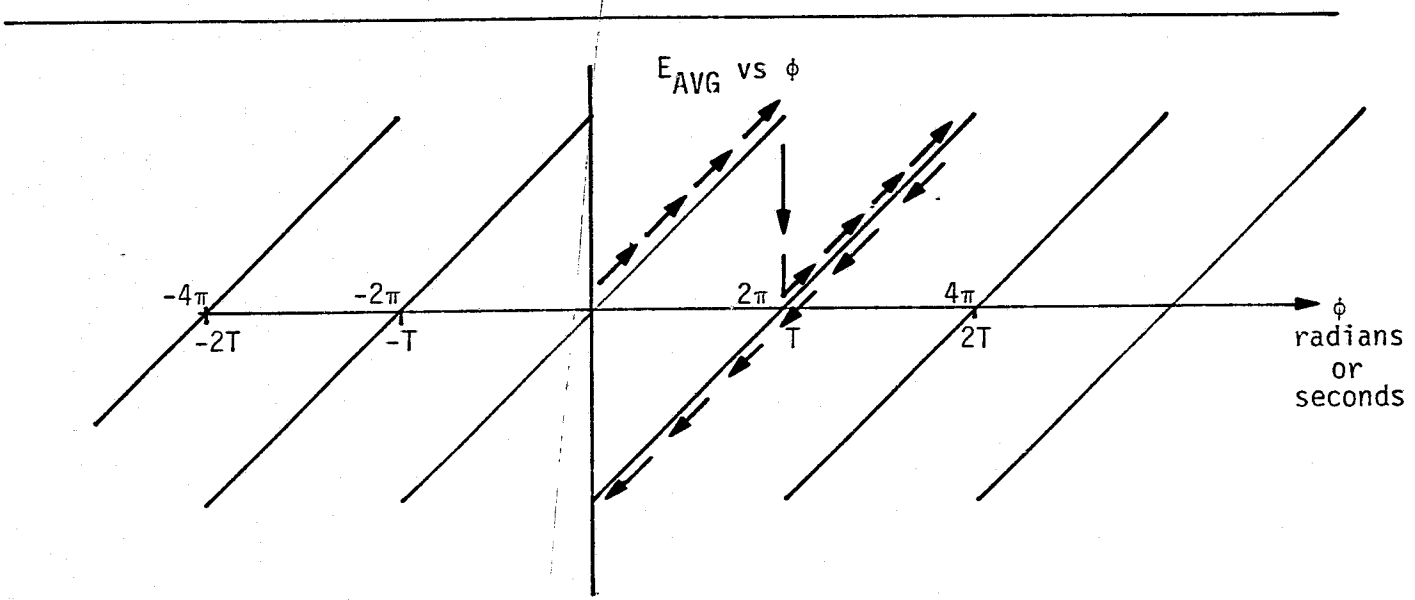


Figure 4. S-Curve of the Phase/Frequency Detector (Frequency Locked)

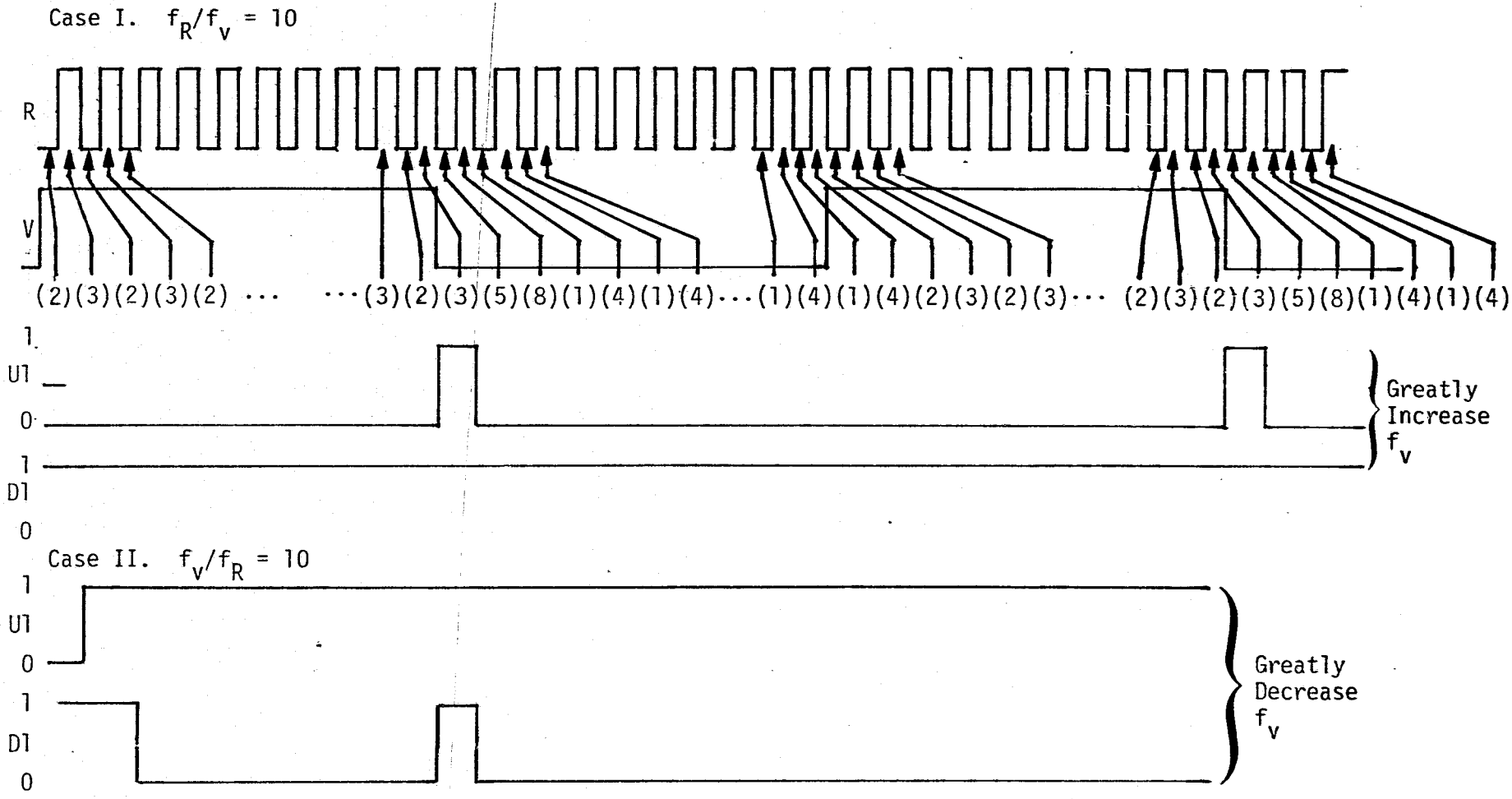


Figure 5. Phase/Frequency Detector When a Large Frequency Error Exists

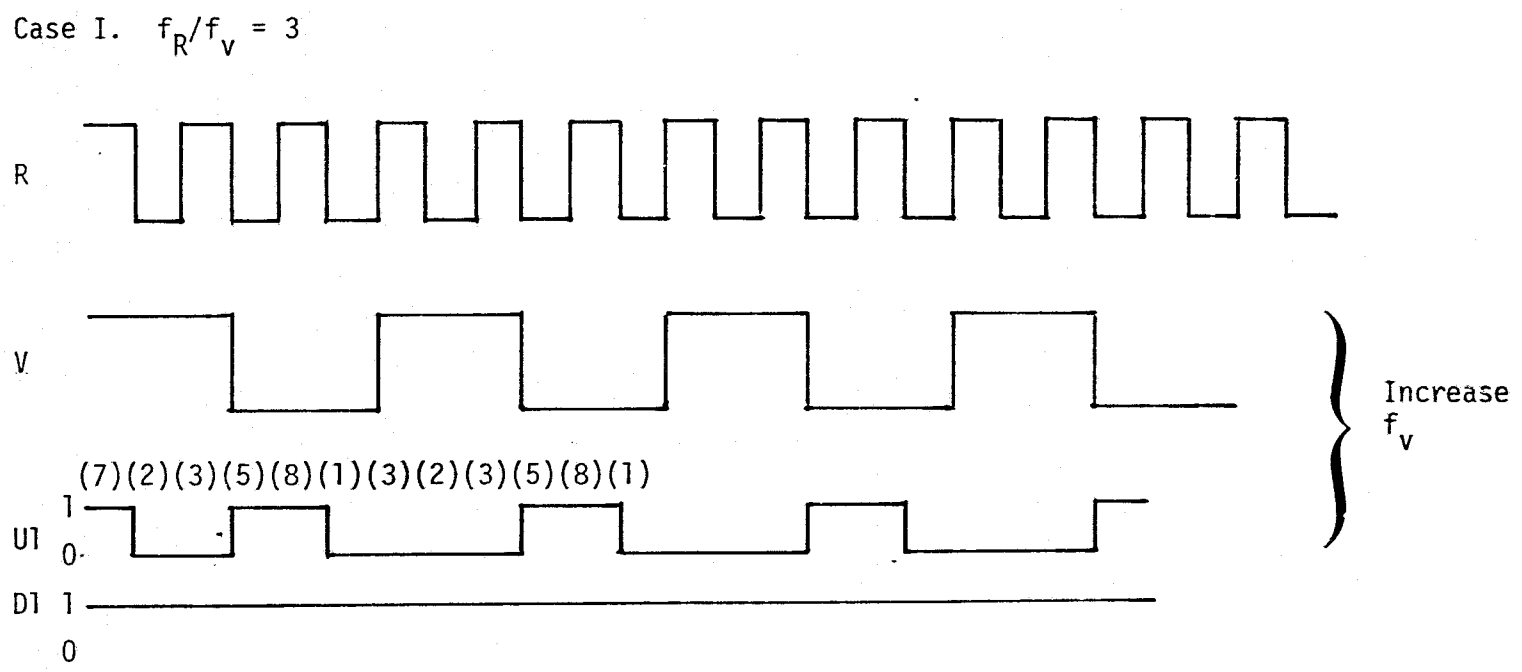


Figure 6. Phase/Frequency Detector for a 3:1 Frequency Error

4.0 DECRIPTION OF THE DATA DETECTOR

As was mentioned previously, the phase/frequency detector provides an error signal to track the clock while the data detector provides a perturbation error signal to force the data sampling to be mid-bit. The divide-by-two D flip-flop of Figure 1 produces both the I and Q samples which are one-half a bit apart in time when the loop is in frequency lock. The in-phase samples are delayed one bit in the second D flip-flop, labeled "delay" in Figure 1. Using an exclusive-OR gate, the present data bit is modulo-two added with the previous data bit. When the past and present data bits are of the same algebraic sign, obviously no transition could have occurred; hence, sampling the transition point could yield no useful timing information so that the accumulator is not enabled. On the other hand, when a transition occurs, the previous and past data bits do not agree and useful information can be obtained from a transition sample. The exclusive-OR gate enables the accumulator only when a transition occurs.

Data bit timing error information is obtained by comparing the present I and Q samples via an exclusive-OR gate. As shown in Figure 7, when the clock timing samples are either late or early, the modulo-two sum of I_n and Q_n is either 0 or 1, respectively. Therefore, $I_n \oplus Q_n$, where $\oplus$ denotes modulo-two addition, determines in which direction the loop timing should be adjusted in order that the Q samples lie very near the transition of the bits. Therefore, the I samples will be in the mid-point of the data bits, which is the result desired to avoid missing bit samples.

By using an accumulator with overflow, an up/down counter can be used to reduce the speed of the up/down counter driving the DAC. Furthermore, the accumulator sets the quantization error in the bit time tracking accuracy. The DAC converts the up/down counter output to an analog voltage which, in turn, adds with the phase/frequency detector to produce the loop filter input signal.

When the bit synchronizer is not frequency locked, it produces no useful information. Although it is not necessary, inhibiting the bit detector DAC output during acquisition would improve acquisition time.

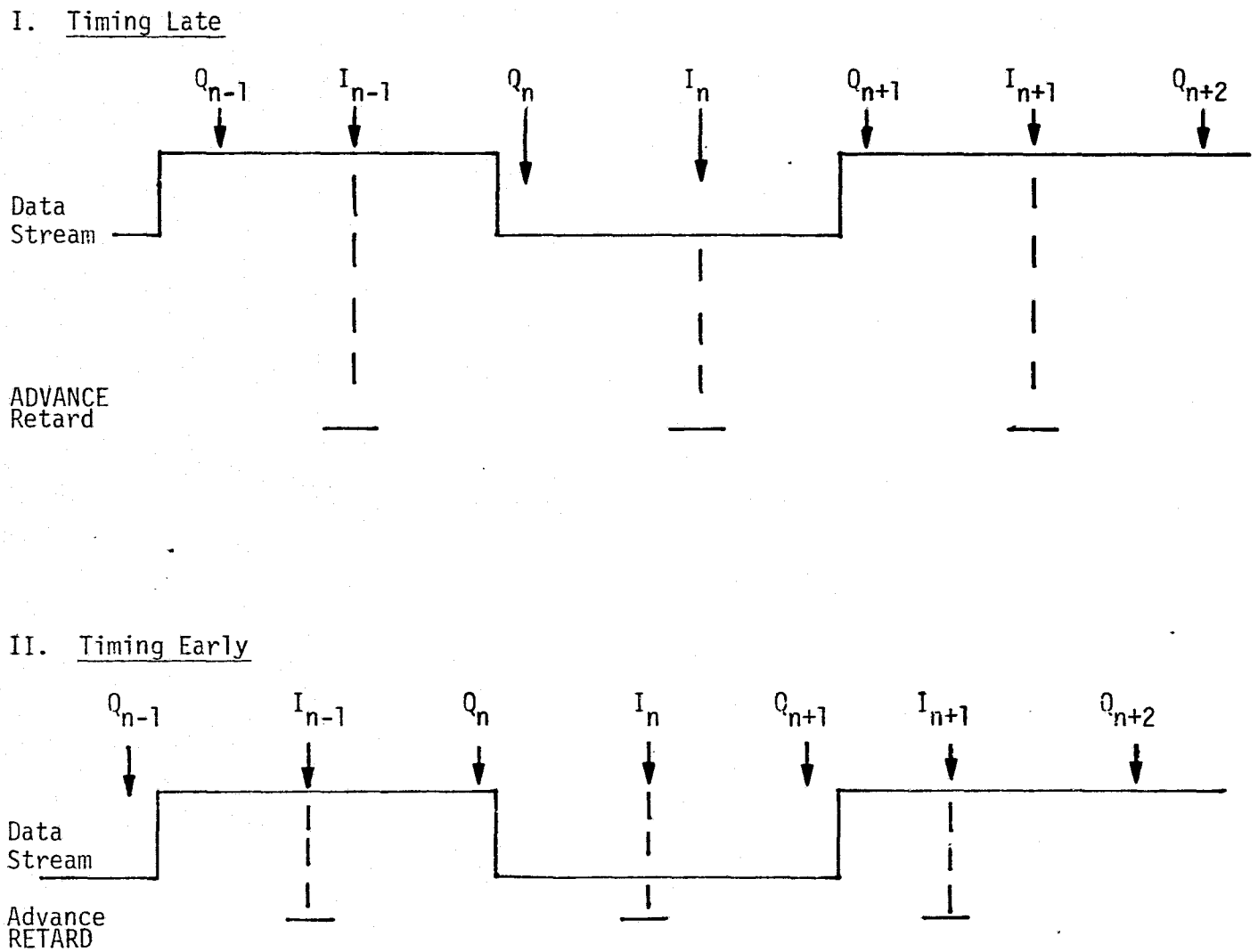


Figure 7. I-Q Relationship for Bit Sampling Showing Bit Timing Control

5.0 LINEARIZED ANALOG EQUIVALENT LOOP ANALYSIS

In this section, we model the loop of Figure 1 in a simplified, linearized, loop structure shown in Figure 8. First we replace the phase/frequency detector with a phase detector (multiplier). Next, we replace the data detector with a phase detector (multiplier). Finally, the accumulator and up/down counter are replaced with an integrator since, in effect, that is the function they perform.

In order to utilize this model, the clock and the data must be replaced with sinusoidal signals, as shown in Figure 8. We have assumed that the phase of the data is arbitrary with respect to the clock which is indicated by the phase angle ψ.

The phase error is defined to be the error between the data clock and the VCO reference, r(t). thus,

$$\phi(t) = \theta + \psi - \hat{\theta}(t) \tag{1}$$

We shall now show that, for any value of ψ, $\phi(t) \to 0$ as $t \to \infty$. Note that $\phi(t)$ is proportional to $\varepsilon_4(t)$. Now,

$$\varepsilon_1(t) = CLK(t)\cdot r(t) = \sqrt{2}A \sin\left(\omega_0 t+\theta\right) \sqrt{2}B \sin\left(\omega_0 t +\hat{\theta}\right) \tag{2}$$

or

$$\varepsilon_1(t) = AB \sin (\theta-\hat{\theta}) \tag{3}$$

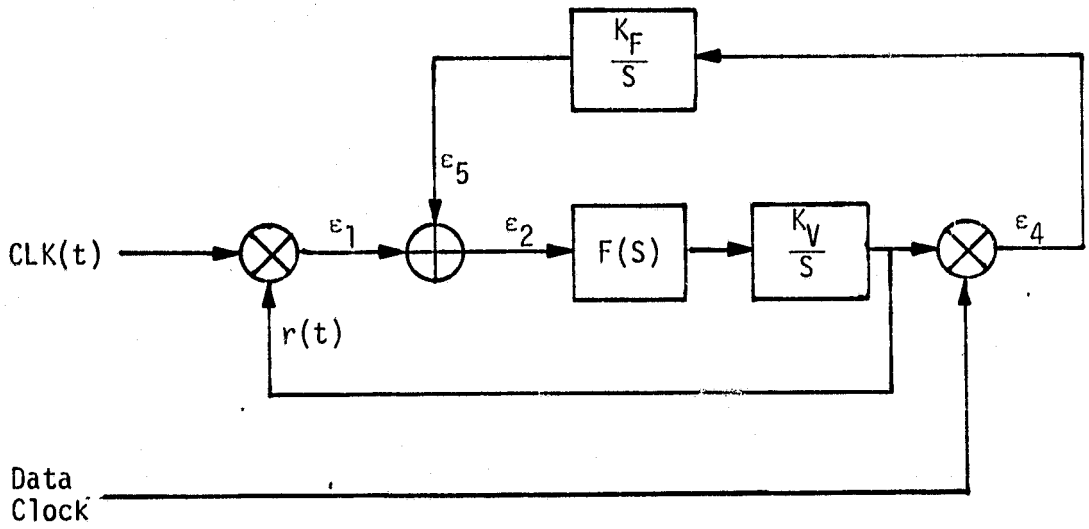
where we have neglected the $2\omega_0$ term which will be filtered out by the loop filter and VCO. Now,

$$\varepsilon_2(t) = AB \sin(\theta-\hat{\theta}) + \frac{K_F}{S} \varepsilon_4(t) \tag{4}$$

where

$$\frac{1}{S} \varepsilon_4(t) = \int_{-\infty}^{t} \varepsilon_4(u)\, du \tag{5}$$

with S being the Heaviside operator. We use the Heaviside operator notation in what follows. Now we have



$$CLK(t) = \sqrt{2}\, A \sin(\omega_0 t + \theta)$$

$$r(t) = \sqrt{2}\, B \cos(\omega_0 t + \hat{\theta})$$

$$DCLK(t) = \sqrt{2}\, A \sin(\omega_0 t + \theta + \psi)$$

Figure 8. Simplified, Linearized Model of the Bit Synchronizer

$$\varepsilon_4(t) = r(t)\cdot DCLK(t) = \sqrt{2}B\cos(\omega_0 t+\hat{\theta})\ \sqrt{2}A\sin(\omega_0 t+\theta+\psi) \quad (6)$$

or

$$\varepsilon_4(t) = AB\sin(\theta+\psi-\hat{\theta}) = AB\sin\phi \quad (7)$$

If we linearize (3) and (7), we obtain

$$\varepsilon_1(t) = AB(\theta-\hat{\theta}) \quad (8)$$

$$\varepsilon_4(t) = AB(\theta-\hat{\theta}+\psi) = \varepsilon_1(t) + AB\psi \quad (9)$$

Now we can also linearize (4) to yield

$$\varepsilon_2(t) = AB(\theta-\hat{\theta}) + \frac{K_F}{S}AB\phi \quad (10)$$

The phase estimate out of the VCO, $\hat{\theta}(t)$, in Heaviside operator notation is given by

$$\hat{\theta} = F(S)\frac{K_V}{S}\varepsilon_2 = F(S)\frac{K_V}{S}\left\{AB(\theta-\hat{\theta}) + \frac{K_V}{S}AB\phi\right\} \quad (11)$$

where F(S) is the loop filter represented as a function of the LaPlace variable S. Now, $\hat{\theta}$ also satisfies, from (1),

$$\hat{\theta} = \theta + \psi - \phi \quad (12)$$

so that

$$\theta + \psi - \phi = F(S)\frac{K_V}{S}\left\{AB(\theta-\psi) + \frac{K_F}{S}AB\phi\right\} \quad (13)$$

Since θ is unimportant in our analysis, we can let it be zero, producing from (13)

$$\Phi(S) = \frac{\left(1 + \frac{ABK_VF(S)}{S}\right)\Psi(S)}{\left[\frac{ABK_VF(S)}{S} + \frac{ABK_VK_FF(S)}{S^2} + 1\right]} \quad (14)$$

where $\Psi(S)$ is the LaPlace transform of $\psi(t)$, i.e.,

$$\Psi(S) = \mathcal{L}\{\psi(t)\} \tag{15}$$

and $\Phi(S)$ is the LaPlace transform

$$\Phi(S) = \mathcal{L}\{\phi(t)\} \tag{16}$$

In order to evaluate how well the loop samples the midpoint of the bit, we must consider the phase error, $\phi(t)$, as time increases without bound. Letting the $\Psi(S)$ be modeled as a phase step in time so that

$$\Psi(S) = \frac{\psi_0}{S} \quad , \tag{17}$$

where ψ_0 is a uniform random variable taking on values in the range $(-\pi, \pi)$ and using the final value theorem of LaPlace transforms, we have

$$\lim_{t\to\infty} \phi(t) = \lim_{S\to 0} [S\Phi(S)] \tag{18}$$

Hence, using (17) and (18) produces

$$\lim_{t\to\infty} \phi(t) = \lim_{S\to 0} \left[\frac{\left(1 + \frac{ABK_V F(S)}{S}\right) \psi_0}{\frac{ABK_V F(S)}{S} + \frac{ABK_V K_F F(S)}{S^2} + 1} \right] \tag{19}$$

Assuming a second-order loop requires that the loop filter be of the form

$$F(S) = \frac{1 + \tau_2 S}{\tau_1 S} \tag{20}$$

so that (19) can be evaluated as

$$\lim_{t\to\infty} \phi(t) = 0 \quad , \quad |K_F| > 0 \tag{21}$$

which means that, in our simplified and unquantized model, the data samples are always taken midbit, as desired, irrespective of the phase relationship between the clock and the data. It should be noted that, if θ were not zero, the result of (21) would still hold. It is interesting to consider the tracking error, $\phi(t)$, when the feedback integrator is removed, corresponding to $K_F = 0$. In this case, we find that

$$\lim_{t\to\infty} \phi(t) = \lim_{S\to 0} \left[\frac{\psi_0 \left[S^2 + ABK \frac{(1+\tau_2 S)}{\tau_1} \right]}{\frac{ABK_V}{\tau_1}(1+\tau_2 S) + S^2} \right] = \psi_0 \tag{22}$$

Therefore, without the integrator (or accumulator up/down counter), the bit synchronizer is incapable of controlling the location of the data bit samples. This fact satifies one's intuition.

We now establish that, while $\varepsilon_2(t)\to 0$ as $t\to\infty$, neither $\varepsilon_5(t)$ nor $\varepsilon_1(t)$ approach zero as $t\to\infty$. From Figure 8, it is obvious that

$$\varepsilon_5(t) = \frac{K_F}{S}\varepsilon_4(t) \cong \frac{K_F}{S} AB(\theta+\psi-\hat{\theta}) \tag{23}$$

Also, the oscillator output phase estimate is given by [using (11) and (23)]

$$\hat{\theta} = F(S)\frac{K_V}{S}\left\{AB(\theta-\hat{\theta}) + \varepsilon_5\right\} \tag{24}$$

Rearranging, we obtain

$$\hat{\theta} + \frac{ABK_V F(S)}{S}\hat{\theta} = AB\frac{K_V}{S}F(S)\theta + \frac{K_V}{S}F(S)\,\varepsilon_5 \tag{25}$$

Solving (25) for $\hat{\theta}$, we obtain

$$\hat{\theta} = \frac{\frac{AK_V}{S} F(S)\ \theta(S) + \frac{K_V}{S} F(S)\ \varepsilon_5(S)}{\left[1 + \frac{ABK_V F(S)}{S}\right]} \tag{26}$$

Rearranging (23) produces

$$\varepsilon_5 = \frac{ABK_F}{S} (\theta(S) + \Psi(S)) - \frac{ABK_F}{S} \hat{\theta} \tag{27}$$

Using (27) in (26) produces, after some algebra, the result (again letting $\theta = 0$)

$$\varepsilon_5(S) = \frac{\frac{ABK_F}{S} \Psi(S)}{\left[1 + \frac{ABK_F K_V F(S)/S^2}{1 + ABK_V F(S)/S}\right]} \tag{28}$$

Again using the final value theorem, we obtain

$$\lim_{t\to\infty} \varepsilon_5(t) = \lim_{S\to 0} \left[S\varepsilon_5(S)\right] \tag{29}$$

so that, assuming $\psi(t)$ is a step in phase of ψ_0 rad, we have, using (28) and the fact that $\Psi(S) = \psi_0/S$, that

$$\lim_{t\to\infty} \varepsilon_5(t) = AB\psi_0 \tag{30}$$

It can be shown that (30) also holds for a first-order loop (where $F(S)=1$) and it also holds for a step in phase of θ.

Now consider the steady-state value of $\varepsilon_1(t)$. We use linearized equations in the following. From (8), we have

$$\varepsilon_1 = AB(\theta - \hat{\theta}) \tag{31}$$

and from (10) we have

$$\varepsilon_2 = AB(\theta-\hat{\theta}) + \frac{K_F}{S}\varepsilon_4 \tag{32}$$

Also from (9), we have

$$\varepsilon_4 = \varepsilon_1 + AB\psi \tag{33}$$

Now, since

$$\hat{\theta} = \frac{K_V}{S}F(S)\,\varepsilon_2 = F(S)\,\frac{K_V}{S}\left[\varepsilon_1 + \frac{K_F}{S}\varepsilon_4\right] \tag{34}$$

we can use (33) in (34) to yield

$$\hat{\theta} = F(S)\,\frac{K_V}{S}\left[\varepsilon_1 + \frac{K_F}{S}(\varepsilon_1 + AB\psi)\right] \tag{35}$$

From (31), we have

$$\hat{\theta} = \theta - \frac{\varepsilon_1}{AB} \tag{36}$$

Now equating (36) and (35) produces (letting $\theta = 0$)

$$\varepsilon_1(S) = \frac{-\frac{ABK_VK_F}{S^2}\,\Psi(S)}{\left[\frac{K_VF(S)}{S} + \frac{K_VK_F}{S^2} + \frac{1}{AB}\right]} \tag{37}$$

Again assuming a step in the phase term $\psi(t)$ yields

$$\varepsilon_1(S) = \frac{-\frac{ABK_VK_F}{S^2}\frac{\psi_0}{S}}{\left[\frac{K_VF(S)}{S} + \frac{K_VK_F}{S^2} + \frac{1}{AB}\right]} \tag{38}$$

using

$$\lim_{t\to\infty} \varepsilon_1(t) = \lim_{S\to 0} S\varepsilon(S) \tag{39}$$

produces

$$\lim_{t\to\infty} \varepsilon_1(t) = -AB\psi_0 \tag{40}$$

From (30) and (40) and Figure 8, we deduce that $\varepsilon_2(t)\to 0$. Therefore, when tracking, the bit synchronizer operates in such a manner that $\varepsilon_2(t) \cong 0$ and $\varepsilon_1(t) \cong -\varepsilon_5(t)$. Without the feedback, of course, the loop would drive $\varepsilon_1(t) \cong 0$.

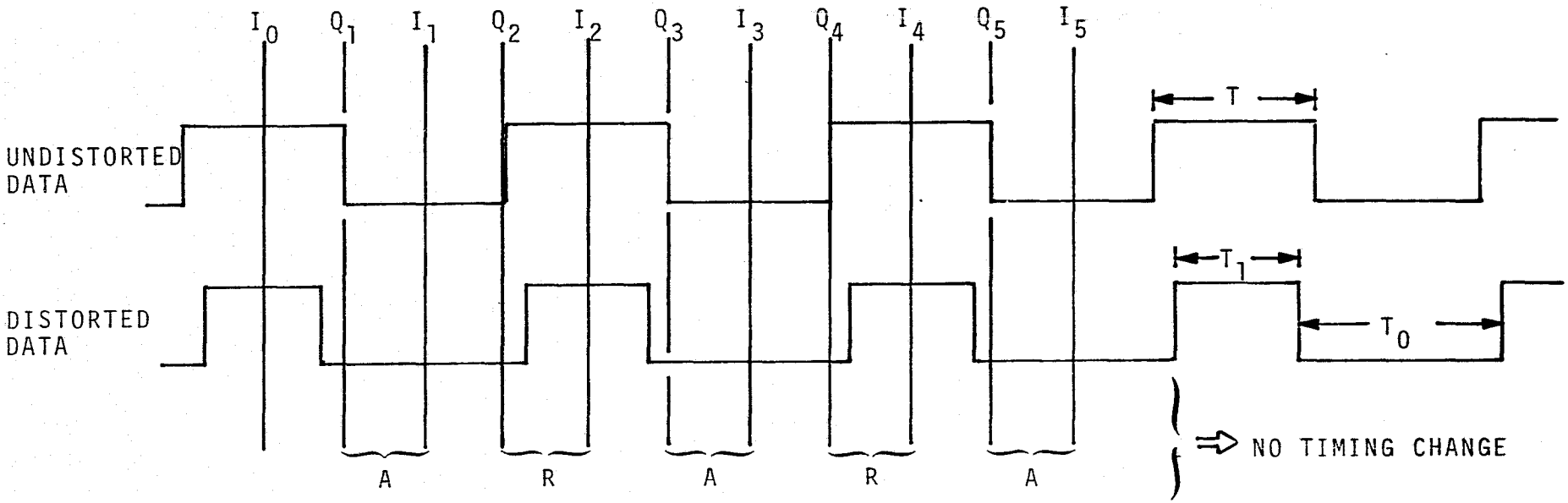
6.0 THE EFFECTS OF ASYMMETRY ON BIT DETECTION

In this section, we address the problem of bit asymmetry on both synchronization and bit demodulation. Bit asymmetry percentage is defined by

$$ASY = \frac{|T_1 - T_0|}{T_1 + T_0} \times 100\% \tag{41}$$

where T_1 is the bit duration of a "one" when preceded and followed by a zero, and T_0 is the bit duration of a "zero" when preceded and followed by a one. It is predicted that the total asymmetry due to rise time and transmitted asymmetry will be in the region of 25-35% when the bit rate is at 50 Mbps.

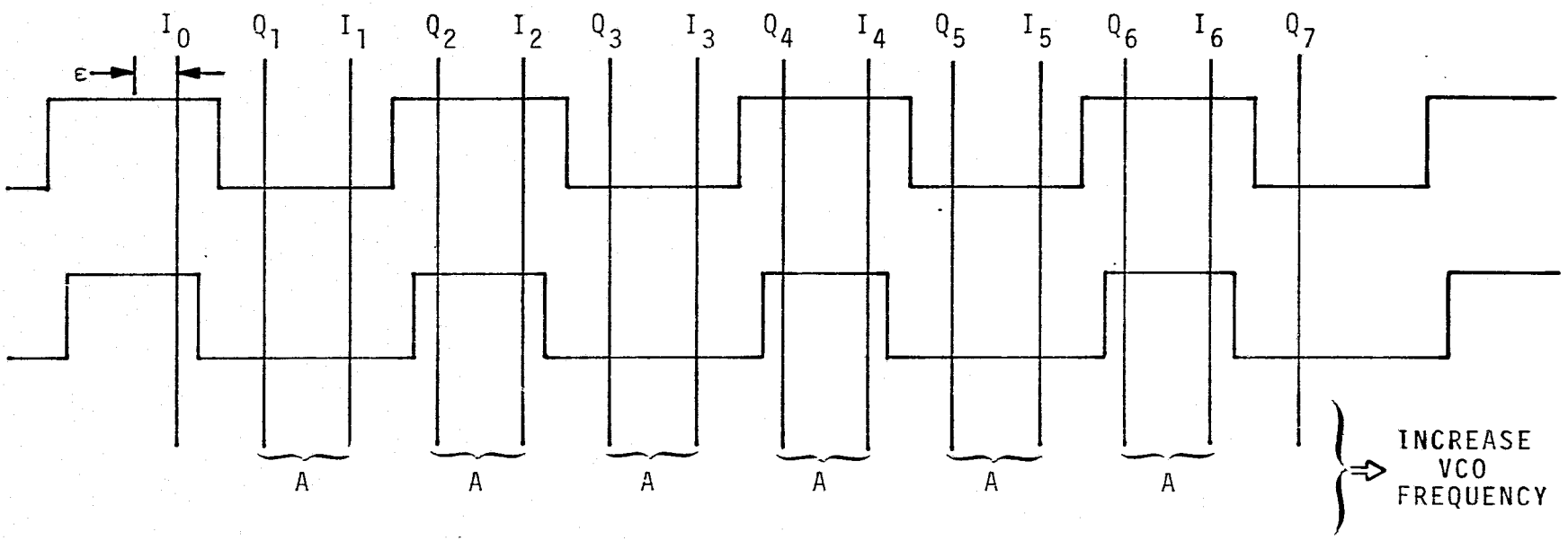
In Figures 9a-c, the case of 25% asymmetry is shown for an alternating one/zero sequence, running at 50 Mbps, with three distinct timing error regions. Since T_1 = 15 ns and T_0 = 25 ns, we see that, in



- Bit Synchronizer Timing Error Circuit Legend:
  - A = advance timing (increase VCO frequency)
  - R = retard timing (lower VCO frequency)
  - INH = inhibit accumulator (don't change VCO frequency)
  - R_b = 50 Mbps

CONCLUSION: With timing errors up to ±2.5 ns, no timing change, and bits are correctly detected.

Figure 9a. One/Zero Bit Sequence with 25% Asymmetry and 0 to ±2.5 ns Timing Error



Bit Synchronizer Timing Error Circuit Legend:

A = advance timing (increase VCO frequency)

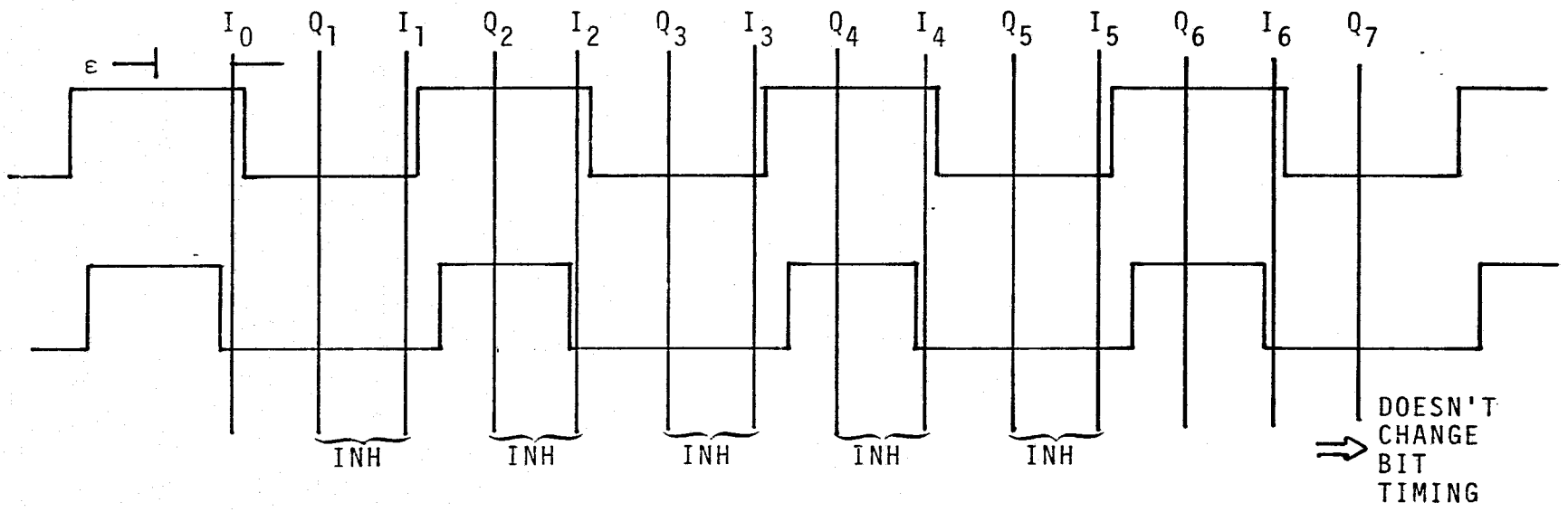
R = retard timing (lower VCO frequency)

INH = inhibit accumulator (don't change VCO frequency)

R_b = 50 Mbps

CONCLUSION: With timing errors in the region ±2.5 ns to ±7.5 ns, the loop reduces the timing error and correctly detects the bits.

Figure 9b. One/Zero Bit Sequence with 25% Asymmetry and ±2.5 to ±7.5 ns Timing Error



INH = INHIBIT

Bit Synchronizer Timing Error Circuit Legend:

A = advance timing (increase VCO frequency)
R = retard timing (lower VCO frequency)
INH = inhibit accumulator (don't change VCO frequency)
R_b = 50 Mbps

CONCLUSION: With timing errors in the region ±7.5 ns to ±10 ns, the loop does not change its timing but it does incorrectly detect some bits (50% error rate for the square-wave data sequence).

Figure 9c. One/Zero Bit Sequence with 25% Asymmetry and ±7.5 to ±10 ns Timing Error

fact, ASY=25%. For the vertical lines, the Q_i, I_i pairs determine which way to adjust the phase of the VCO according to $I_n + Q_n = 0 \rightarrow$ ADVANCE (INCREASE VCO VOLTAGE) and $I_n + Q_n = 1 \rightarrow$ RETARD (DECREASE VCO VOLTAGE) when $I_n + I_{n-1} = 1$, and no bit timing change when $I_n + I_{n1} = 0$. For example, in Figure 9a, region I errors are illustrated. For this timing relationship, the input to the accumulator up/down counter would be the sequence advance (A), retard (R), advance (A), etc. or, equivalently, ones and minus ones to the accumulator which would not change the sample points relative to the bit stream. In Figure 9b, the error is ±5 ns, which produces a sequence of advances. In this region (±2.5-±7.5 ns), the loop would pull in to the ±2.5 ns region and correctly decode the data bits. When a shift of 8 ns (7.5-10 ns) is considered in Figure 9c, we find that there would be a sequence of A's and R's which would not reduce the error but would cause bit errors to be made in the bit sampling process. For the case of alternating one/zero shown, the detected bits are all zeros, resulting in errors on every other bit. By carefully considering Figures 9a-c, it can be concluded that, with 25% asymmetry, the following is true (timing error is defined as timing difference between sampling at the center of the bits and the actual sampling point):

1. With timing errors up to ±2.5 ns, no timing change is effected by the loop and no bit errors are made.

2. With timing errors between ±2.5 ns and ±7.5 ns, loop error control will reduce timing error and no bit errors will occur.

3. With timing errors between ±7.5 ns and ±10 ns, the loop will not adjust the timing, <u>but bit errors will occur</u>.

The case of 35% bit asymmetry is illustrated in Figure 10 for an alternating one-zero sequence. After careful study, we conclude that the following is true:

1. With timing errors up to ±3.5 ns, no timing change is effected by the loop and no bit errors are made.

2. With timing errors between ±3.5 ns and ±6.5 ns, loop error control will reduce the timing error and no bit errors will occur.

3. With timing errors between ±6.5 ns and ±10 ns, the loop will not adjust timing, however, <u>bit errors will occur</u>.

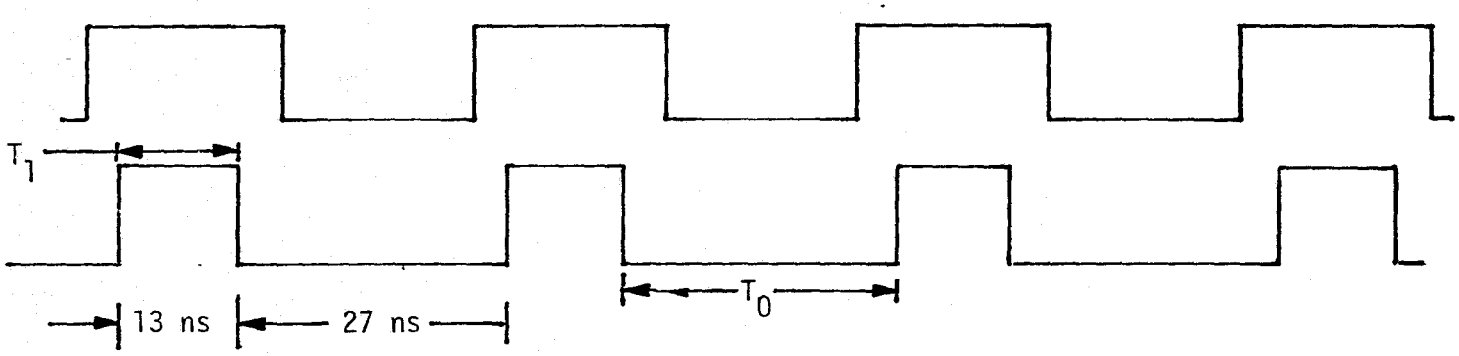


Figure 10. One/Zero Sequence With 35% Asymmetry

Sequences other than the one-zero alternating sequence were considered and the result was basically the same for any level of asymmetry.

In conclusion, we see that three "zones" or timing error regions will apply. The first region is a dead zone in the sense that the no-error control signal is generated in the accumulator because the error signals alternate back and forth in algebraic sign. This region extends in magnitude from zero timing error to $\frac{ASY \cdot T}{2}$ seconds, where T is the undistorted bit symbol duration. The bits are correctly detected in this region.

The second region extends from $\frac{ASY \cdot T}{2}$ seconds to $\left(\frac{1-ASY}{2}\right)T$ seconds. In this region, the loop provides an error control signal from the bit timing error detector which reduces the error to the outer edge of zone 1. The bits are correctly detected in this region.

In the third zone, the error ranges from $\left(\frac{1-ASY}{2}\right)T$ seconds to T/2 seconds. This region causes the bit timing error detector to produce a sequence of alternating ones and minus ones which will therefore not exceed the accumulator threshold and, consequently, not update the loop (i.e., a quasistable lock point). Bit errors will occur in this region. When the one-zero sequence is considered, only zeros or all ones will be detected depending on whether the one bits or the zero bits are of greater duration due to asymmetry. For arbitrary sequences of ones and zeros, errors will occur although not at a 50% rate.

As a final comment, if we assume that the a priori probability of the initial timing just after acquistion is uniformly distributed, the probability of locking in the third region, where bit errors occur, is given by

$$P_{FL} = \frac{\frac{T}{2} - \left(1 - ASY\right)\frac{T}{2}}{\frac{T}{2}} = ASY$$

and therefore, only with zero asymmetry does this problem disappear. If the timing error between clock and bit stream could be held to be less than $\left(\frac{1-ASY}{2}\right)T$ seconds in magnitude, it is possible to avoid the troublesome third region.

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3. Motorola MC4344-MC4044 Phase Frequency Detector Specifications and Operating Characteristics, Issue A, 1972.

4. Motorola MC12040 Phase Frequency Detector Specifications Contained in Motorola Semiconductor Library, Vol. IV, MECL Integrated Circuits, Series A, 1974.

1.0 SUMMARY AND CONCLUSIONS

A bit synchronizer proposed by Hughes Aircraft (Culver City) is analyzed via timing diagrams in a noise-free environment. This synchronizer is, in part, a substantial revision of the bit synchronizer proposed by P. H. Conway [1] of Hughes Aircraft Company (HAC).

Based on a review of a HAC note [2] and the timing diagrams of Figures 2 through 9, it is believed that this new bit synchronizer will track the rising edge of the data bits with 25% asymmetry and up to a 90° phase shift between the received clock and data bit timing. In addition, the data bits will be demodulated correctly.

It is not true that phase shifts larger than 90° will necessarily be corrected by this bit synchronizer, as evidenced by Figures 8 and 9. However, the specifications currently require the loop to operate over only a ±75° phase shift between the received data stream leading edges and the bit synchronizer leading edges; consequently, there should be no problem.

2.0 INTRODUCTION AND DESCRIPTION OF THE LEADING EDGE BIT SYNCHRONIZER

The purpose of the bit synchronizer, shown in Figure 1, is to track the leading edge of the incoming bit stream with the aid of the received clock and, from this, to regenerate a symmetric bit stream to be processed by the convolutional encoder. In addition, the synchronizer provides a clock at the data rate as well as twice the data rate.

In Figure 1, two additional subsystems are shown; the first is an adaptive threshold device that attempts to restore symmetry to the bit stream, and the second is a false frequency lock detector. Since the asymmetry corrector will be the subject of another report, we will now discuss the false frequency lock detector.

The purpose of the false frequency lock detector is to ascertain whether the bit synchronizer is in true lock or false frequency lock. This is accomplished by counting both the received clock and the synchronizer-generated clock in two separate 8-bit counters. After either one counts to its maximum count of 256, the other counter is inhibited from further counting. At this point, the count of the unfilled counter is compared to 256. If the error is small enough, true lock is accepted;

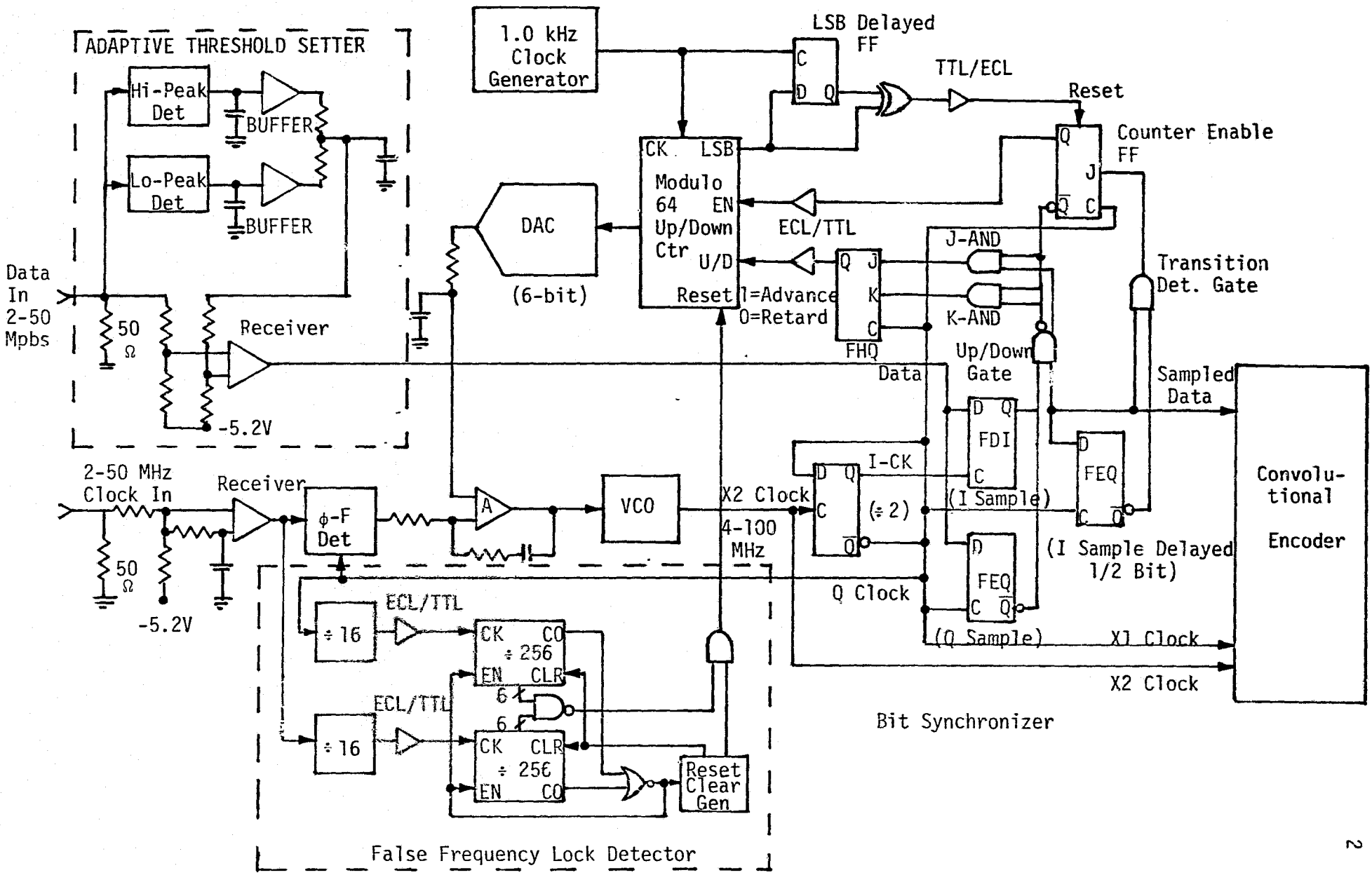

Figure 1. Hughes Culver City Ku-Band Bit Synchronizer Block Diagram

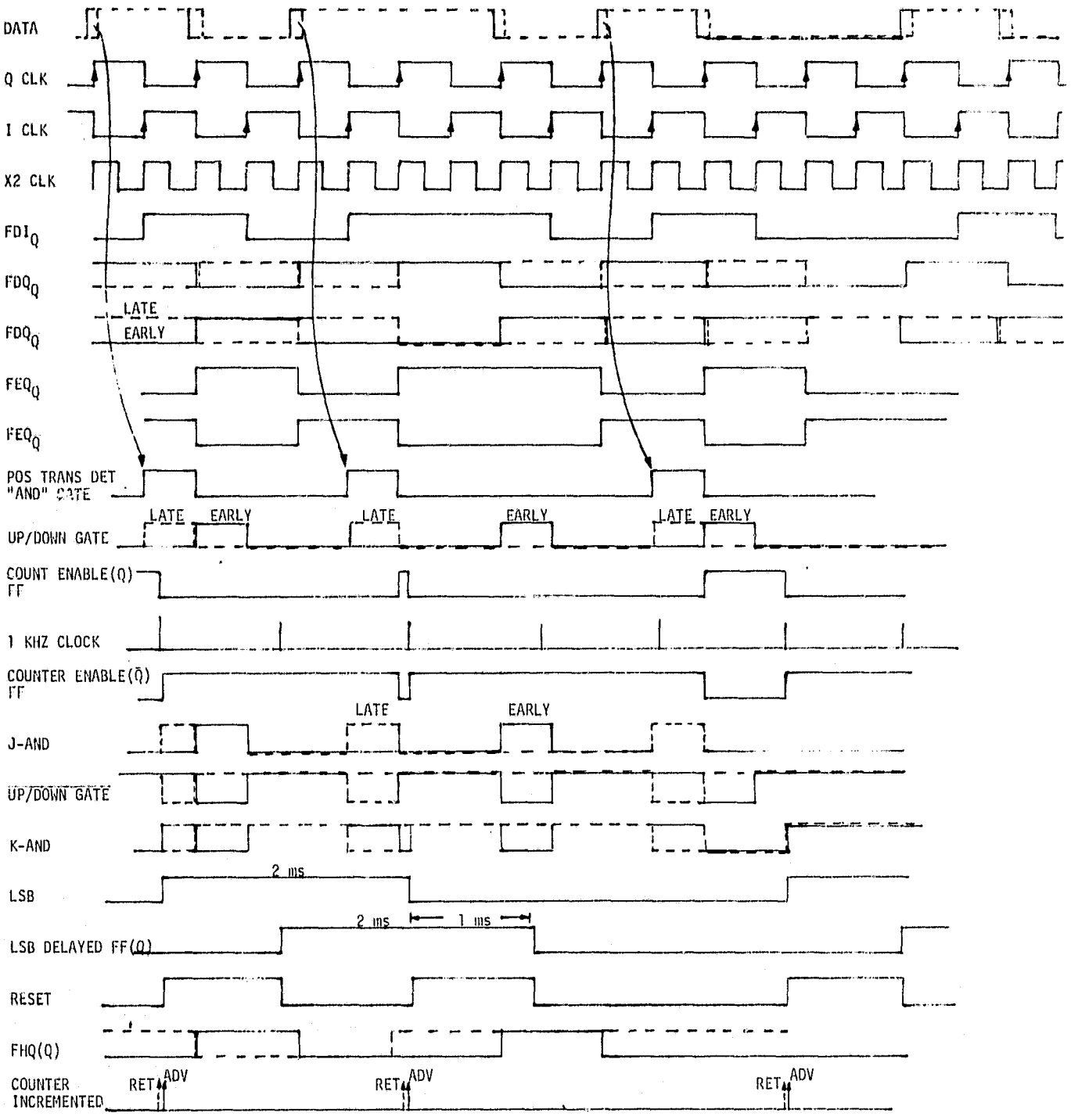

Figure 2. Timing Diagram of the Bit Synchronizer Illustrating An Early and Late Bit Sequence For the Culver City Ku-Band Bit Synchronizer

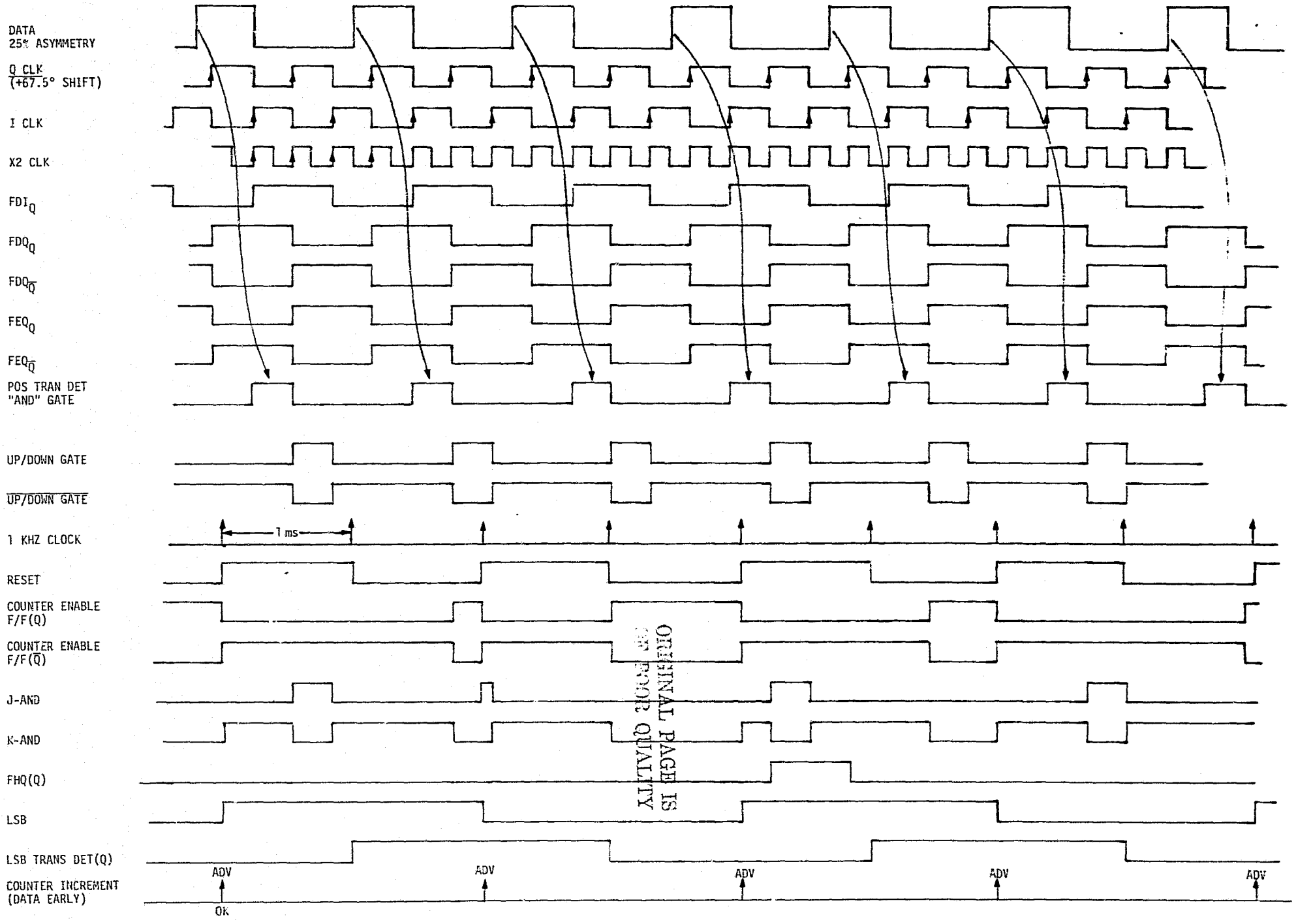

Figure 3. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25 Asymmetry and the Data Leading the Q-Sampler by 67.5° (Results Hold Up To 90)

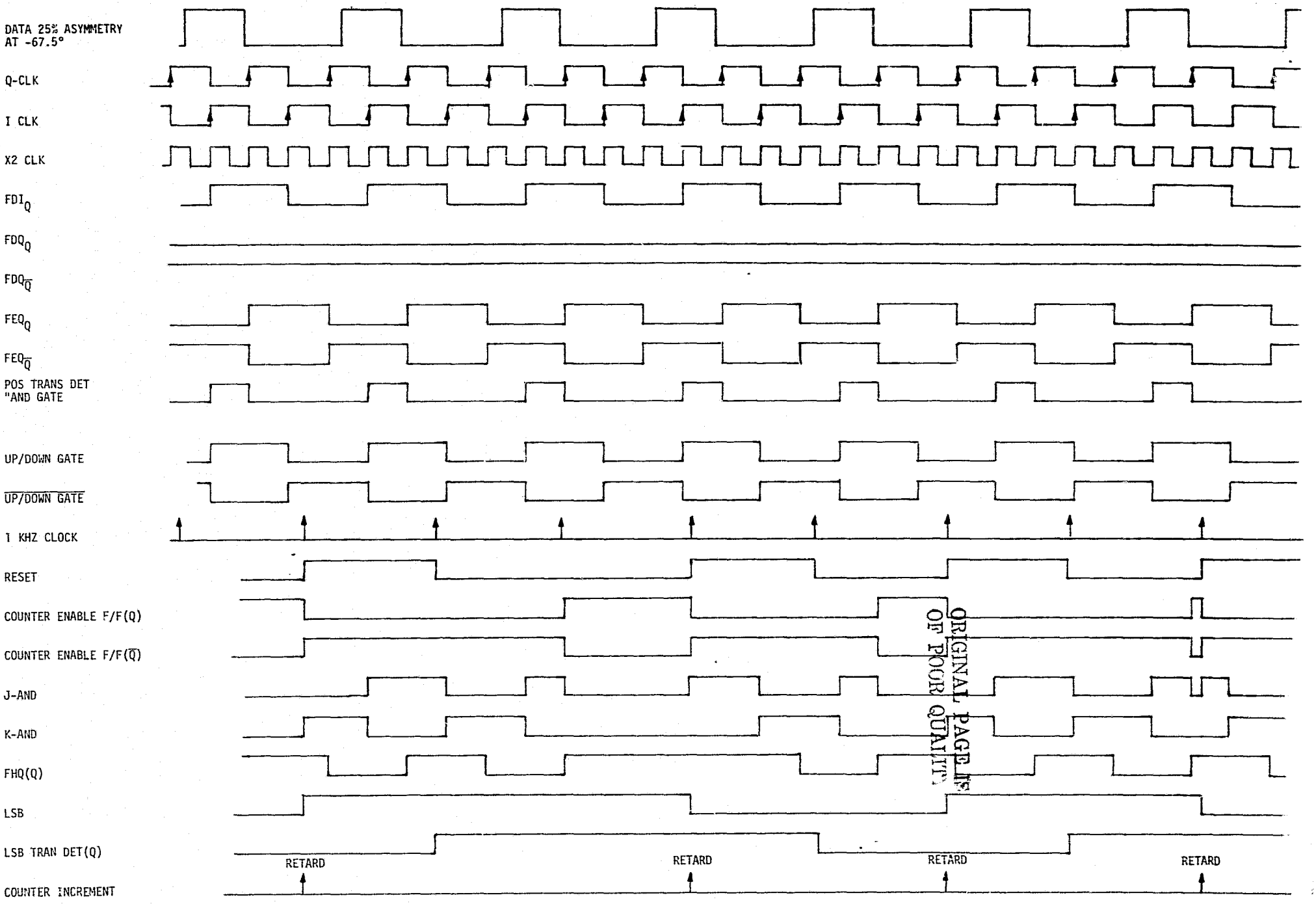

Figure 4. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Lagging the Q-Samples by 67.5° (Results Hold Up to 90°)

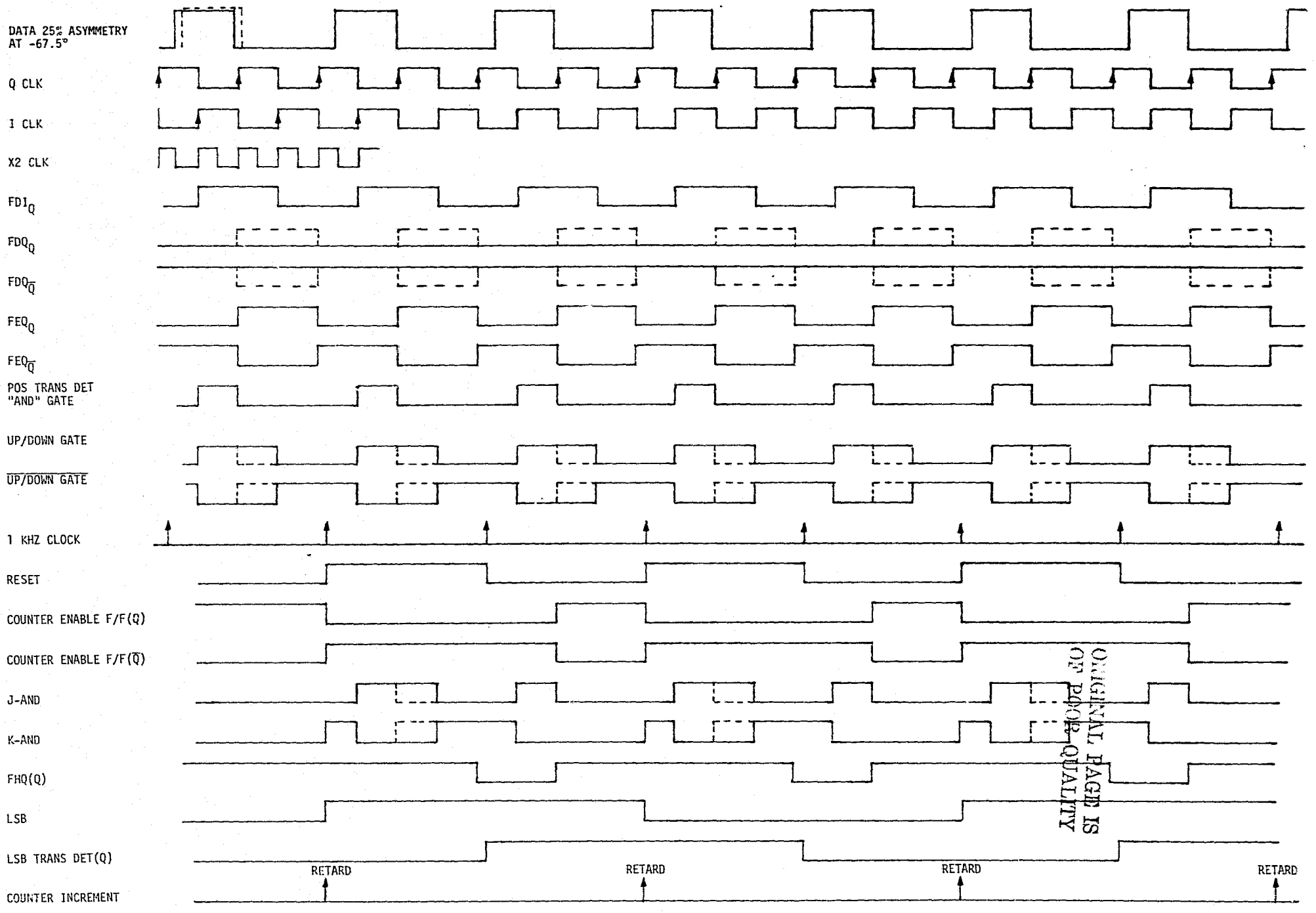

Figure 5. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Lagging the Q-Samples by 67.5° (Different 1 kHz Clock Phase Than That of Figure 4)

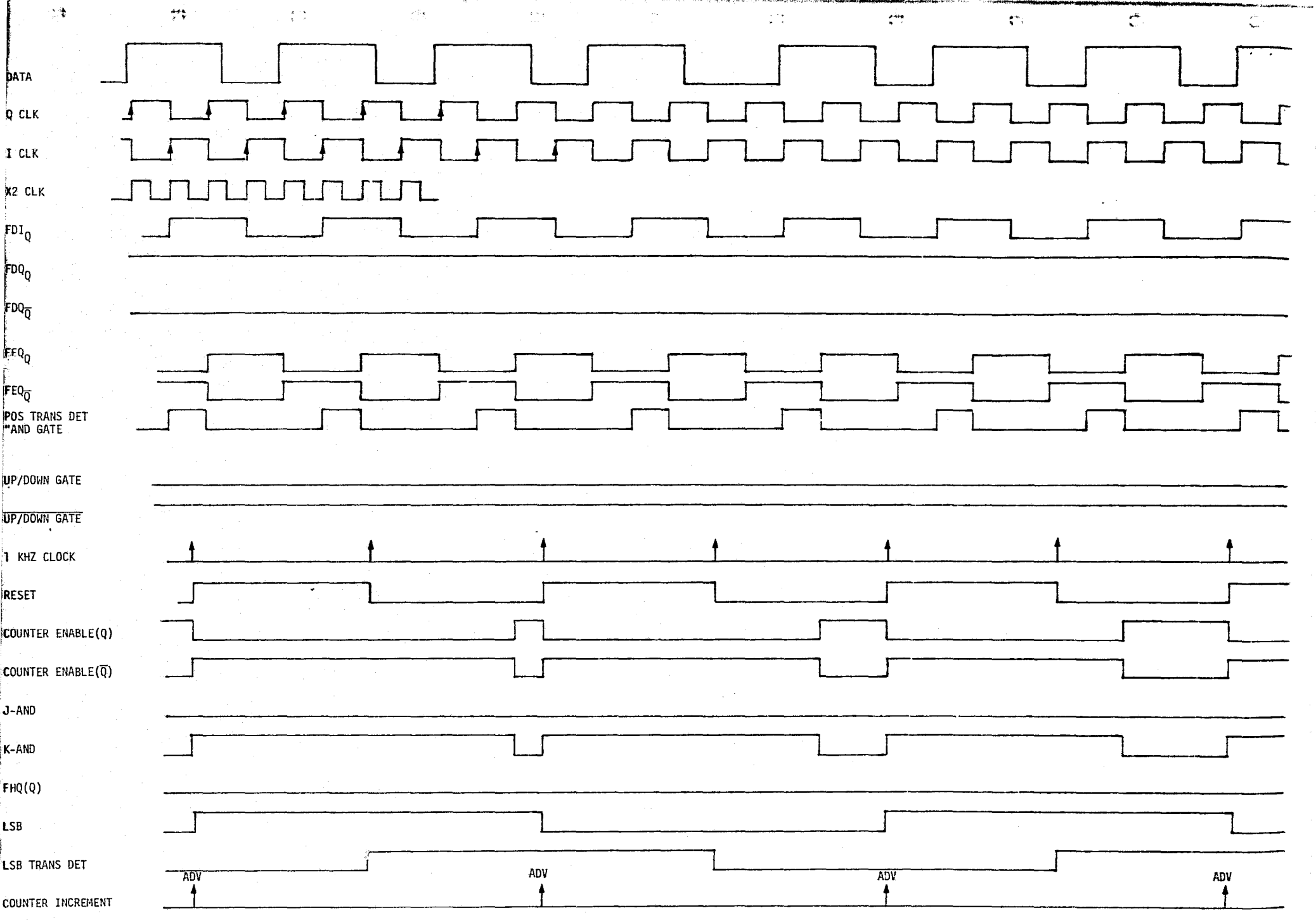

Figure 6. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Leading the Q-Samples by 22.5°

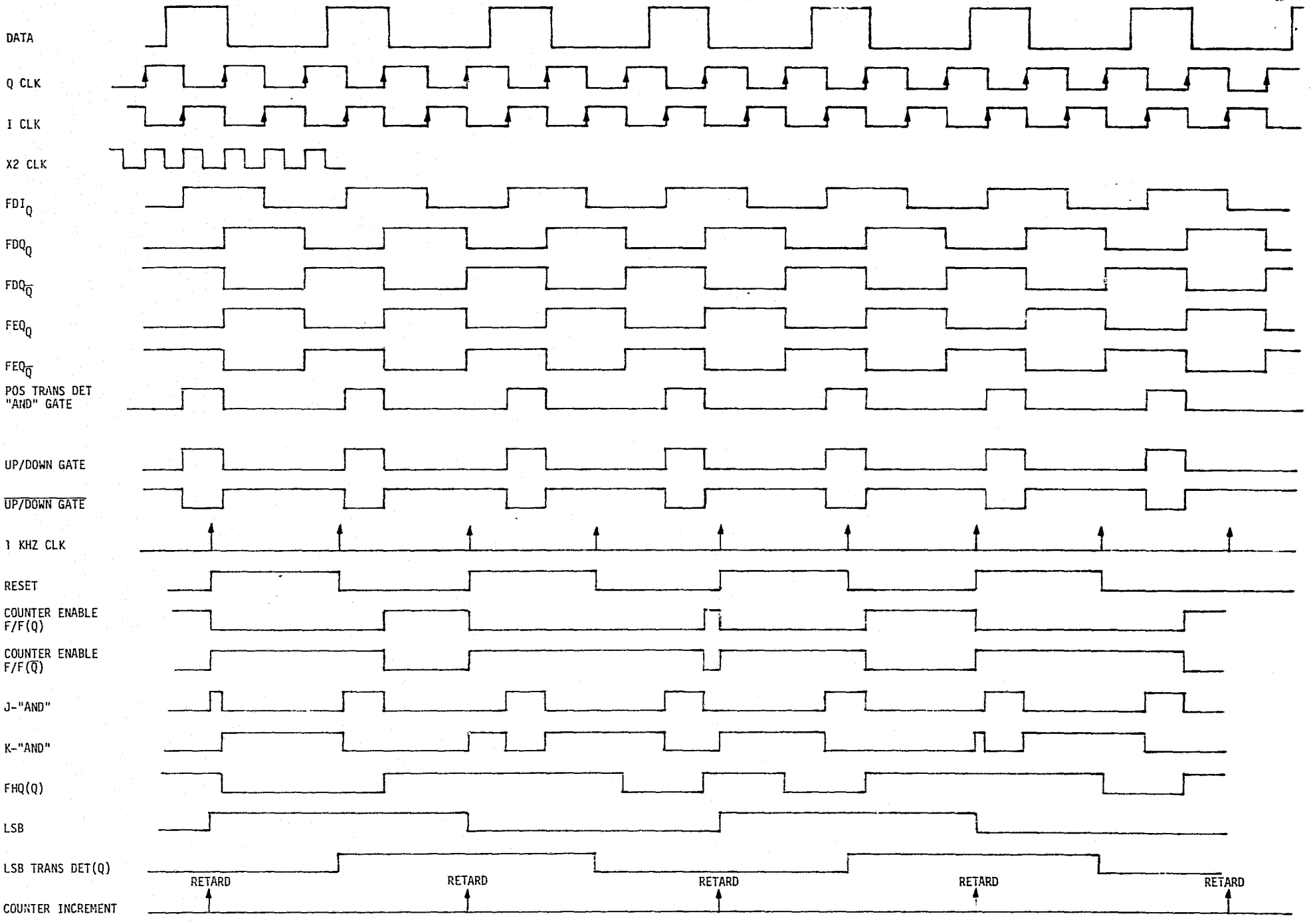

Figure 7. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25% Asymmetry and the Data Lagging the Q-Samples by 100°

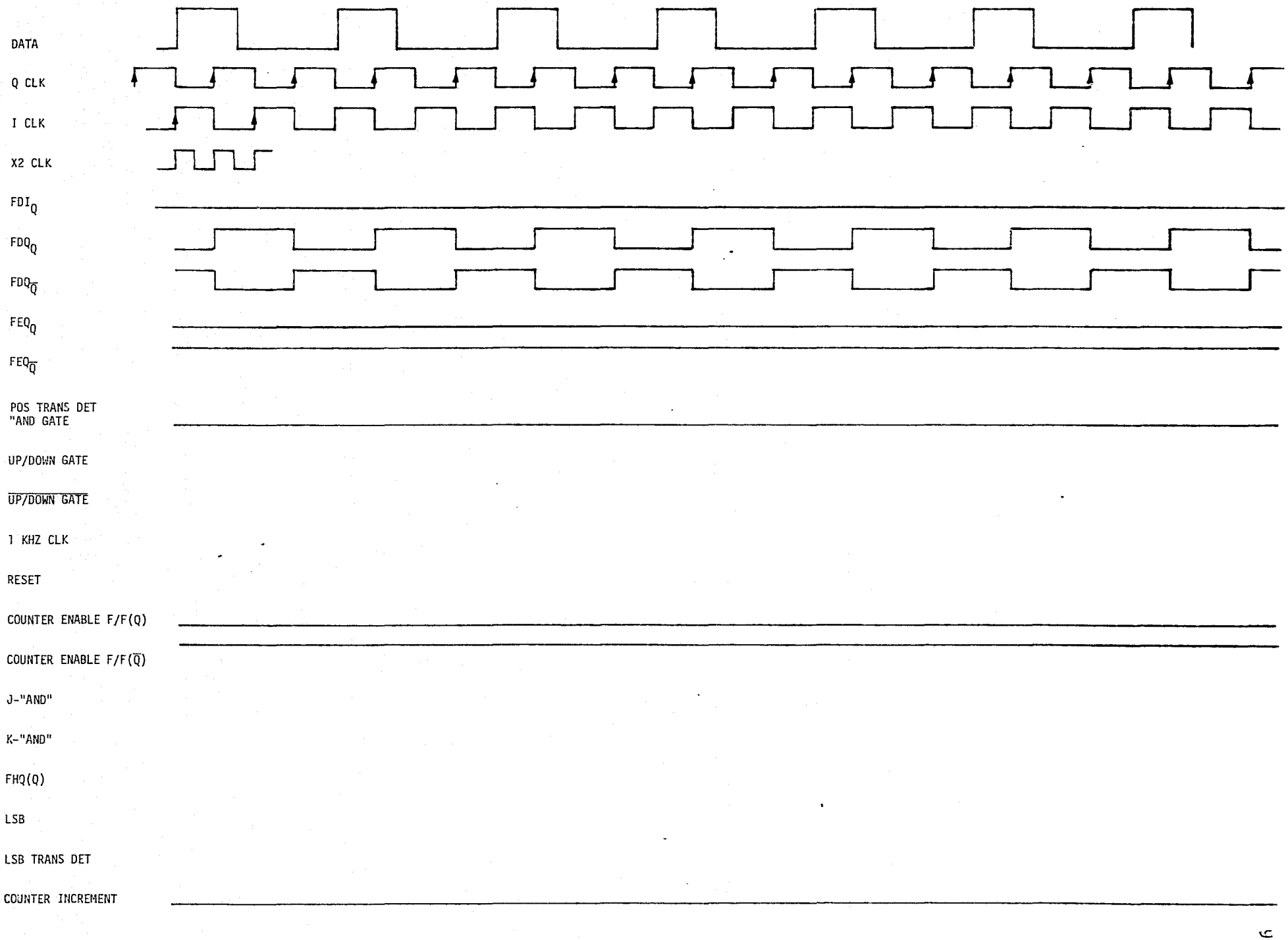

Figure 8. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25. Asymmetry with the Data Lagging the Q-Samples by 190°

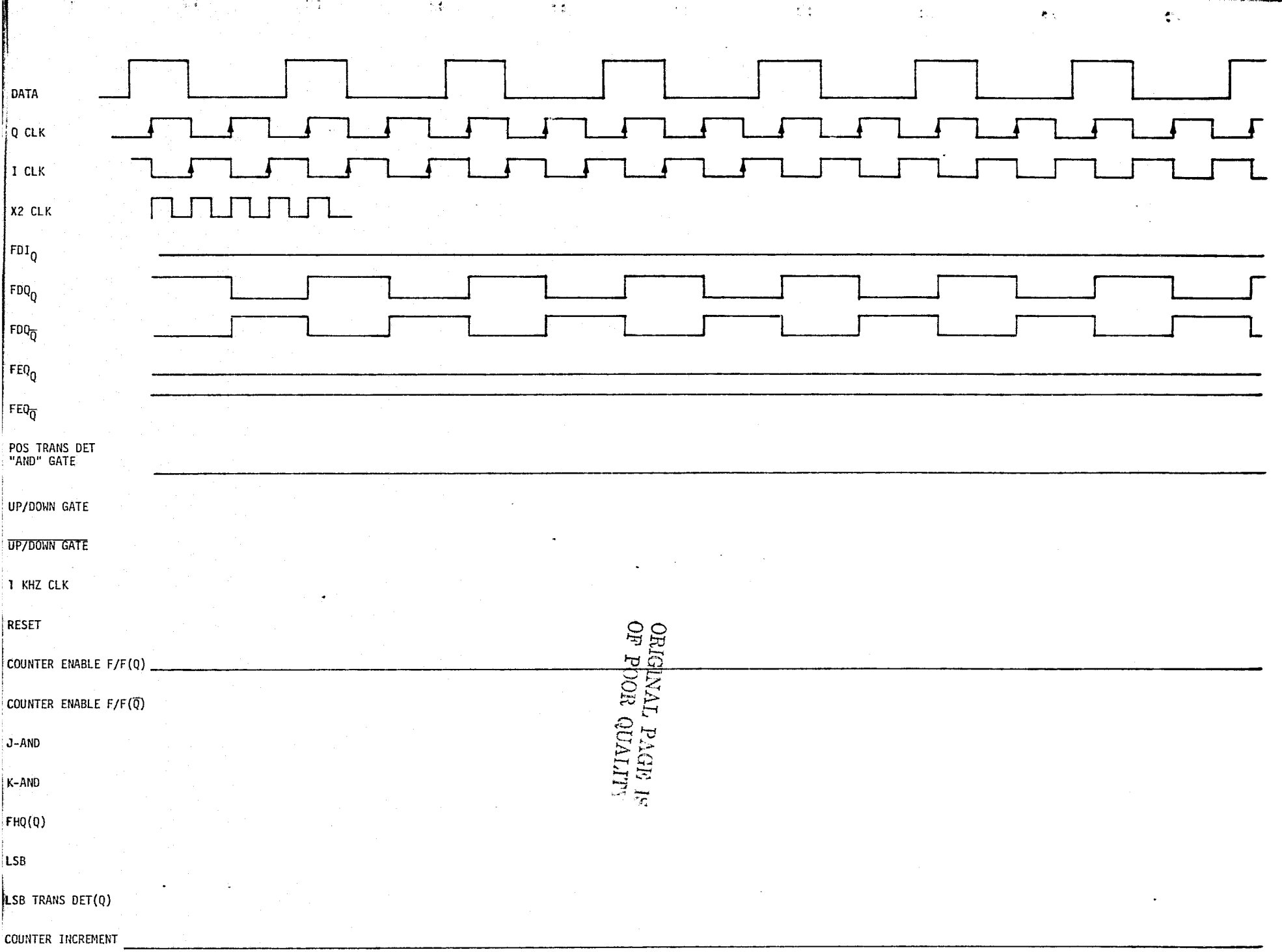

Figure 9. Timing Diagram of the Bit Synchronizer Illustrating the Case of 25° Asymmetry and the Data Leading the Q-Clock Leading Edge by 100°

otherwise, false lock is assumed. If false lock is detected, the digital-to-analog converter (DAC) voltage is set to provide 0 DC bias into the loop filter, which allows the loop to reacquire in true lock.

The bit synchronizer loop is composed of a Motorola high-frequency phase-frequency detector (ϕ-F) [3-4] which is capable of detecting both phase and frequency errors and is used to track the received clock, as well as a bit timing detector, based on positive data transitions.

The phase-frequency detector has been discussed in some detail in [1] and will not be discussed here except to say that its function is to act as a discriminator in a frequency lock loop during frequency acquisition and as a phase detector during tracking.

In effect, the ϕ-F detector removes the frequency error between the VCO and the received clock, then removes the phase error. The function of the flip-flops, least significant bit detector, and counter-DAC unit is to position the clock-generated bit timing so that the Q-clock straddles the leading edge of each bit.

The VCO is run at 4-100 MHz and divided by 2 by the D flip-flop (F/F) following the VCO. From the $\overline{Q}$ output, the Q-clock is generated and, from the Q output, the I-clock is generated. Flip-flop FDI then provides samples of the I sample (mid-bit samples) whereas FDQ outputs the Q samples (or transition samples). The function of FEQ is to delay the I sample by one-half of one bit so that the positive data detector gate will go high when a positive transition occurs. The up/down gate, along with the J-AND and K-AND gates, set the JK flip-flop so as to increase or decrease the counter count and, therefore, the DAC voltage. This voltage is subtracted in the loop filter amplifier, thereby adjusting the loop VCO phase relative to the received clock phase. Both the Q-clock and the X2 clock, plus the resynchronized data, are sent to the convolutional decoder. The function of the least significant bit transition detector is to provide a settling time of 2 ms before a new update can be processed.

Now consider Figure 2, which illustrates how the loop provides corrections so as to align the leading edge of the Q-clock with the leading edge of the bit stream. The top row illustrates an early data stream in the solid line and a late data stream in the dashed line. The next three rows illustrate the I, Q and X2 clocks.

In the 5th row, the FDI D-type flip-flop samples the data stream at the rising edge of the I-clock (CLK), whereas FDQ_Q outputs the Q-CLK sample of the data in row 6. The 7th row indicates that the $FDQ_{\overline{Q}}$ output is simply the complement of FDQ_Q. Notice that both FDQ_Q and $FDQ_{\overline{Q}}$ are dependent on the data timing relative to the Q-CLK timing.

Row 8 illustrates the output of FEQ_Q which is a one-half-bit delay of the I samples. $FEQ_{\overline{Q}}$ is the complement of FEQ_Q. In the 10th row, the positive transition detector output AND-gate is shown. Notice that a pulse occurs one-half a bit after the occurrence of the leading edge of each bit.

The 11th row illustrates the up/down gate output for both late and early data streams. In the 12th row, the count enable flip-flip is indicated. In order for the count enable to be high, the reset input must be at the 0 state and the transition detector must be high when the Q-clock arrives. When the Q-output is high, the up/down counter is free to accept a unit change in its count.

In the 13th row, the 1 kHz clock tick marks are shown, for convenience, at a much higher rate than 1 kHz. The counter enable ($\overline{Q}$) output of the flip-flop of row 14 is the inverse of the 12th row output.

Row 15 depicts the output of the J-AND gate, illustrating the difference for early and late data streams. In the same manner, row 17 illustrates the output of the K-AND gate. In row 16, the inverse of the up/down gate is illustrated.

Row 18 illustrates the least significant bit output of the up/down counter which feeds the LSB delayed flip-flop. This control stays high for 2 ms rather than 1 ms since the up/down counter is enabled just after the next 1 ms clock occurs, which therefore requires 2 ms to change the LSB.

In row 19, the least significant bit detector flip-flop output stays high for 2 ms, as can be seen from the sketch. The reason for the 2 ms duration is the same as for the LSB 2 ms duration. The reset control for the counter enable F/F is just the modulo 2 sum of the LSB and the LSB-delayed F/F, which is shown in row 20.

In the 21st row, the JK F/F called FHQ(Q) provides the advance or retard signal which, when clocked into the up/down counter and converted via the DAC, provides the timing error reduction. This advance or retard

is relative to the Q-clock epoch times. Finally, the last row illustrates the times when the counter is updated to correct the loop timing. Notice that the correction will be an advance of the VCO-generated clock when the leading edge of the bit stream leads the clock and a retard if the data leading edge is retarded from the clock.

3.0 TIMING DIAGRAMS UNDER IMPERFECT DATA STREAMS

In this section, timing diagrams are presented which consider data asymmetry of 25% and various timing errors. In Figure 3, the case of 25% asymmetry is illustrated via a timing diagram. Asymmetry is defined as

$$ASY = \frac{|T_1 - T_0|}{T_1 + T_0} \times 100\% \qquad (1)$$

where T_1 is the bit duration of a "one" when preceded and followed by a zero, and T_0 is the bit duration of a "zero" when preceded and followed by a one. It is currently expected that the total asymmetry due to rise time and transmitted asymmetry will be no more than 25% at 50 Mbps, and less at low bit rates.

In the last row of Figure 3, it is seem that the updating is in the correct direction; that is, the Q-clock is advancing. We conclude from Figure 3 that errors up to 90° (data leading edge of the Q-clock) are acceptable to the bit synchronizer when the data "ones" are larger than the data "zeros" with 25% asymmetry.

In Figure 4, the same case as in Figure 3 is illustrated, except that the data lags the Q samples leading edge by 67.5°. As can be seen in row 6, the Q samples are all zero; however, the last row of the timing diagram indicates that the error correction signal retards the timir which is the proper action for the loop to take. We conclude from .g- ure 4 that, with errors up to 90° (data lagging the leading edge of the Q-clock) and 25% asymmetry, the bit synchronizer works properly so as to decrease the timing error.

Figure 5 illustrates the same case as Figure 4 except that the phase of the 1 kHz clock has been changed to verify that the loop operates properly, which it does.

In Figure 6, the case when the data leads the Q-clock by 22.5° is illustrated. This figure has the "ones" larger than the "zeros" but, again, the bit synchronizer provides the correct correction so as to reduce the tracking error.

Figure 7 illustrates the case where data lags the Q samples by 100° and has 25% asymmetry with the "zeros" wider than the "ones." As can be seen from the last row, the loop still corrects in the proper direction so as to reduce the timing error.

The point of Figure 8 is to illustrate the fact that the bit synchronizer has limitations as to how large a timing error can be tolerated. With the data lagging the leading edge of the Q sample by 190°, it is seen that the loop has no response; that is, no loop correction occurs since the counter enable is always at 0 or, equivalently, the counter is disabled.

Finally, Figure 9 illustrates the case when, with 25% asymmetry, and the data leading the Q-clock by 100°, the loop is incapable of providing updates to reduce the timing error.

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