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PREFACE

J. Byron McCormick, Conference Chairman
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Major impetus for the development of high temperature electronic materials, devices, circuits and systems can probably be credited to the energy crisis which appeared dramatically in 1974. At that time it was acknowledged that the necessary discovery and exploitation of national energy resources would require a long-term commitment to research and development, and federal funds were made available for this purpose. In 1975, a workshop was held to set directions for work in geothermal exploration,[1] and a number of contracts were subsequently negotiated. As work continued, interest broadened beyond the geothermal area. In 1978, Dr. A. F. Veneruso, of Sandia Laboratories, organized a session on High Temperature Electronics at Midcon 1978 in Dallas, Texas.[2] This session included a paper on aircraft engine controls, as well as papers on integrated circuits directed at the high-temperature needs of the well-logging industry. In 1979, interest broadened still further, as evidenced by the High Temperature Electronics and Instrumentation Seminar organized in Houston, Texas by Dr. Veneruso.[3] Most recently, a session of the 1980 Electro-Professional Program was devoted to The Frontiers of High Temperature Electronics.[4]

More than five years have passed since the first workshop was held, and in that time much progress has been made. Interest in the field has continued to grow and the diversity of requirements has rapidly increased. It therefore seems important at this time to re-evaluate the status of and directions for high temperature electronics research and development. This conference has been organized for that purpose. Specifically, the conference has three major objectives: to identify common needs among those in the user community; to put in perspective the directions for future work by focusing on the status of current research and development programs; and to address the problem of bringing to practical fruition the results of these efforts. While the importance of the technical content of the papers is not to be underestimated, the Program Committee felt that because of the diversity of interests represented in the audience, the identification of common problems and the need for perspective with regard to the implications, both technical and commercial, of these problems were perhaps as important as the high-temperature technologies themselves. Accordingly, special attention was given to the program in two ways.

First, considerable care was taken to put together a session on Users Requirements which included papers from as broad a spectrum as possible, and this session was scheduled as the first of the conference. Second, the need for perspective was recognized to be part of the broader problem of determining what results of research and development have long-range potential for commercialization, and how these can be reduced to practice. To meet this need we are introducing what we believe to be an innovation in conferences of this type: the final session, A Conference Perspective, by Dr. Robert Pry, Vice-President for Research and Development, Gould, Inc. During the conference, Dr. Pry will talk with as many as possible of the conference attendees. Combining the results of these encounters with what he learns of the status of the various high-temperature technologies from the conference papers, he will develop a commentary of his views of the conference in general, and technology transfer and commercialization in particular. I would, therefore, encourage everyone who has special needs in high-temperature electronics, or opinions about the field, to talk with Dr. Pry at some time during the conference. I also hope that everyone will plan to stay for this final and possibly most important session.

It is worth noting that more than half the papers in the conference deal with materials and devices, rather than circuits and systems. While this is due in part to the conference emphasis on research and development, it is in larger measure a reflection of the lack of maturity of the field. Circuits and systems are the last in the development chain of which materials form the beginning. The evolution to a mature technology base is unfortunately impeded by the relatively small size of the market for high temperature electronics when compared with, for example, the market commanded by integrated circuits. This small size is not, however, indicative of its importance when viewed in the context of national energy and space programs. It is, therefore, the goal of this conference to expedite the development of high temperature electronics for these most important applications.

No conference such as this can be successfully organized without the hard work of a number of cooperative individuals; I would like to thank all those who served on the Program Committee for their efforts. Special acknowledgements are due Dr. John C. Rowley and Dr. Jan A. Narud, both of Los Alamos National Laboratory, for their outstanding and tireless efforts to establish a program of the highest quality. Special acknowledgements are also due Dr. C. R. Hausenbauer and his staff in Special Professional Education at The University of Arizona, for handling all the conference arrangements.

Finally, I would like to express our gratitude to those agencies which have contributed financially to the success of the conference: The National Aeronautics and Space Administration; The Department of Energy, Division of Engineering, Mathematical and Geosciences; The Nuclear Regulatory Commission, Division of Reactor Saftey Research; and The National Science Foundation.

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SESSION I

USERS REQUIREMENTS

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HIGH TEMPERATURE ELECTRONICS APPLICATIONS IN SPACE EXPLORATIONS *

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Electronic instruments and systems used for space exploration have not generally been exposed directly to harsh environments of outer space or the dense atmospheres of several of our planets. Instead, protective enclosures, insulation, shielding, and small heating systems are provided to control the environment. Also the design of spacecraft systems and instruments are carried out with fairly conservative design rules, because the cost of a mission is high, and failure is easy to achieve. The design of electronic instruments for use within the wide range of the earth's environment is difficult enough, and extension of our electronic technology to operate at very high or low temperatures or great pressures is no small challenge.

Operation of electronic systems in environments having temperatures or pressures beyond the capability of the electronics requires systems to protect or insulate the electronics from the environment. The maintenance of the protection requires energy, and the energy source itself may require protection. In vacuous space, the energy transfer to the spacecraft is entirely dependent upon radiative transfer, and temperatures can be controlled by varying the reflectivity of the spacecraft surfaces. This form of control may require little energy since it often can be accomplished with little more than the rotation of the spacecraft or the reorientation of reflective panels. Pressure differences are seldom larger than the difference between that of the earth and vacuum. In these respects, the exploration of space is considerably less difficult than the exploration of the earth's inner space where temperatures and pressures are high.

The exploration of the planets having large atmospheres is entirely a different matter. In the case of Venus, for example, the surface temperature is near 730°K and the atmospheric pressure 90 bars. The atmospheric profiles of the large outer planets are relatively unknown, but one thing is sure, both the pressure and temperature will increase well beyond our technical capability to design instruments before any surface is likely to be found. The depth to which these atmospheres can be studied depends on one of two things, 1. our ability to design probes that can withstand the great temperatures and pressures, 2. the ability to transmit the information through the dense absorbing atmospheres.

The problem of protecting electronic systems from the great temperatures and pressures of these atmospheres is a very different problem from that of outer space. Here the thermal energy transfer is caused primarily by conduction to the atmosphere. The atmospheric pressures may be hundreds of times greater than those of the earth's atmosphere, so our spacecraft may look more like a craft designed for deep ocean exploration. We have two choices as to the design of our craft, either we design our systems to withstand the high temperatures and pressures, or we maintain temperature and pressure differences within the craft. The maintenance of temperature and pressure differences requires energy, and energy is always a very expensive and a scarce commodity on any space probe. Therefore it is very important that we minimize or eliminate the need to maintain such differences. The extension of range of operating temperatures of electronic components and systems is a start in that direction.

Missions

The exploration of the atmosphere of Venus will probably be the first example of the use of high temperature electronic systems in space applications. Studies of the Venusian atmosphere could be accomplished by the use of balloon borne instruments. The simplest sort of experiment might be one that determines only the circulation properties of the atmosphere at various altitudes. All that is required here is a beacon of sufficient power to be tracked by either orbiting spacecrafts or from ground-based radio telescopes. A more advanced probe might contain a radar transponder. The localization of the balloon, for example, could be accomplished by VLBI, Doppler tracking, range tracking in the case of a transponder, and all combinations of these. Two missions are presently being studied. The first carries only a simple beacon transmitter and flys at 18 km altitude where the temperature at about 325°C. Electronic breadboard designs for operation at this temperature are presently being constructed and tested at JPL. The second flys between 40 and 48 km where the temperature does not exceed 150°C. Here, more advanced instrument packages are presently within the available technology. Possible instruments include pressure, temperature, differential temperatures, light fluxes, lightning detectors, and sound pressure levels. Balloon missions are likely to last no longer than a few days to a few weeks, therefore only short term studies can be carried out (These are much longer, however, than the present Venera and Pioneer-Venus probes). Longer missions are desirable and would most likely have to be carried out from the surface.

If a landing probe could sit on the highest part of Terra Ishtar (about 10 km above the mean surface level) the temperature would be about 380°C. A number of interesting experiments could be accomplished from this remarkable peak including all the traditional weather measurements, atmospheric turbulance, light scattering from dust particles, and so on. Equally as interesting are measurements related to planetary and solar systems dynamics. For example, very accurate measurements of the rotation rate, direction of the spin axis, and orbital motion could be made. These measurements could easily establish whether the rotation is in synchronous lock with the earth or if some form of precession exists. As the planet rotates, two occultations could be observed per revolution as viewed from the earth. An orbiting spacecraft could observe several occultations per day. Such measurements not only aid in establishing the variation of the atmosphere but give a measure of the turbulance which establishes the ultimate "seeing" capability through the Venusian atmosphere at microwave frequencies.

Going to our outer planets, there is much work to be done. The first direct measurements of the Jovian atmosphere will be made by the Galileo space probes. These probes, like the PV probes, will last a short time until they are either crushed or their signal extinguished by the absorption in the atmosphere. The data

they return will ultimately determine if other methods of exploration are possible. Among the most exiciting might be a hot air balloon mission to explore the circulation below the visible cloud regions. Though it is too early to know what might be possible, high temperature electronics will most likely be required.

Going towards the inner part of our solar system we find Mercury and the Sun. The Mariner 10 spacecraft measured surface temperatures on Mercury ranging from 90 to 460°K. Radiative transfer models indicate that temperatures as high as 650°K (377°C) exist when Mercury is closest to the sun. The precession of the perihelion of Mercury has been used to test the general theory of relativity, however, this rate of precession is also partly caused by the solar oblateness which distorts the gravity field of the sun. Further tests of the general relativity theory could be facilitated by placing a transponder on the surface of Mercury or by placing a close orbiter around the sun. The solar orbiter could map the gravity field, measure the oblateness, and carry out other measurements of fields and particles. Measurement of the perihelion precession of orbiter could give an even better verification of the general relativity theory.

Electronic Hardware

Most conventional military electronics will operate to 100°C. Therefore, at 100°C it is simpler to ask what won't work than what will. Even though many components will still function to 150°C, very few electronic systems will function properly. Therefore, electronic systems must be designed specifically to reach this temperature. As we go beyond 200°C, many standard components and packaging techniques begin to fail. By 300°C, very few silicon semiconductor devices continue to operate. As we go beyond 150°C it is especially important to consider what is really needed for space exploration, as every good designer would like to have everything, and everything could be much too expensive.

There are on our list of components and systems many of the same things that are required for well-logging instumentation, so to the degree that instrumentation requirements are more or less identical, operation to 300°C should be possible using hybrid circuit techniques developed for well-logging. A fairly good summary of the limits of electronic components was given by Veneruso (1979). Much work has been reported by Palmer (1977), Palmer and Heckman (1978), Palmer (1979), and Prince et. al. (1980) describing tests, design rules, and fabrication of electronic circuits suitable for many instrumentation systems. However, our list contains some items not essential to the well-logging industry. These are:

1. High temperature power sources
2. Ultra stable oscillators and clocks
3. VHF, UHF, and Microwave transmitters
4. Antennas
5. Electromechanical actuators, motors, and guidence systems
6. Special deployment components and systems

The power source is so important that it is placed first in the list. An effective way to evaluate power sources for space applications is by figures of watt hours per kilogram, watt hours per cubic centimeter, and watt hours per dollar. The last measure is often the most difficult to obtain as most high temperature

Table I. High Temperature Energy Sources

Energy Device	Type	Manufacturer	Temperature Range	Wh/kg	Wh/cc	Max Watts	Efficiency	
Lithium/Carbon	Primary	Power Conversion Inc.	-50° to 60°C	270	0.41	0.90	NA	D-size tested available
Lithium/Carbon	Primary	Electrochem Industries	-30° to 150°C	515	0.98	9.60	NA	D-size tested available
Sodium/$NiPS_3$	Secondary	EIC	130°	-	-	-	-	Experimental
Sodium/Sulfur	Secondary Fused Salt	General Electric	280° to 350°C	150	-	-	-	Experimental
LiSi/FeS	Secondary Fused Salt	Rockwell International	400° to 450°C	79	-	-	-	Experimental
Sodium/Sulfur	Secondary Fused Salt	Marcoussis	280° to 350°C	200	-	10.0	80%	Experimental
Photovoltaic	Silicon	Many	< 150°C	NA	NA	NA	~12% @ 20°C	Available in many sizes
Photovoltaic	GaAs	Rockwell International	< 300°C	NA	NA	NA	~14% @ 20°C	Experimental .25cm x .25cm
Thermal Electric Gen.	Pyro-technique	Aerospatiale	-40° to 50°C	< 20	< 0.07	-	-	Available in many sizes
Radio Isotope Thermionic Generator	Pt 238	General Electric	< 500°C	> 0.5×10^6	-	~4w/kg @ 300°K	0.25%	Requires Custom Design

power sources are not commercially available. Table I summarizes some of the power sources that are either available or are known to operate at extended temperature ranges. Certain special mechanical and electromechanical storage systems have not been included. For example steam engines, compressed gas, internal combustion engines, and windmills. The use of such systems should not be discounted, as a few of these may be entirely practical. For example, the atmosphere of Jupiter is mostly hydrogen. The operation of a internal combustion engine fueled on hydrogen is quite practical if an oxidizer is carried on the probe. Table I, then, concentrates on direct electrical power systems not requiring the conversion from mechanical to electrical energy.

The primary batteries listed in Table I have very high energy densities compared to most primary or secondary cells. They also have good storage capability, which is essential since many missions require six months to several years to arrive at their intended target. The present temperatures limit for commercially available primary batteries is about 150°C. The fused-salt batteries listed do not begin to operate until the materials fuse. These batteries can be stored in the charged state indefinitely below the temperature of fusion. Since the lowest temperature battery is the sodium-sulfur type which begins to operate near 280°C, there is a range between 150° and 280°C for which no batteries are presently available. Fused salt batteries can operate to 500°C, so they are ideal for Venus landers. Although a large number of experiments on various fused salt cells have been run, only two types of cells have received sufficient study to be manufactured. The work on Sodium-Sulfur cells has been reported by Mitoff, Breiter, and Chatterji (1977) and Chatterji, Mittoff, and Breiter (1977). Work on the Lithium-Silicon/Iron Sulfide batteries has been reported by Sudar, Heredy, Hall, and McCoy (1977). Most work since then has been directed at manufacturing large cells for industrial load leveling and for electric vehicles, therefore, a wide range of sizes are not available.

Energy sources that could support longer missions than possible with batteries are: 1. photovoltaic cells, and 2. thermionic cells. Photovoltaic cells may be usable if the power requirements are not too large. High light intensities are generally not available deep in the atmosphere of Venus and at the outer planets, thus the solar cell array sizes would have to be fairly large to provide even 20 to 30 watts. Silicon cells are not useful above 200°C, although work is being done to extend the temperature range for use with large concentrators. GaAs cells show the greatest promise for operation above 200°C, although their efficiency will decrease. Tests of a few samples of GaAs cells supplied by Rockwell International showed a near linear decrease in terminal voltage with increased temperature. Although these cells survived the 350°C testing, their efficiency at this temperature went to zero.

Thermionic cells or generators operate by establishing a temperature difference on two junctions formed of dissimilar metals. Two types of thermionic generators are listed in Table I. The pyrotechnique generators suffer from a low energy to weight ratio, but could potentially operate to a higher temperature than the primary cells. Commercially available cells are rated only to 65°C. These generators operate only for a short time following ignition (30 seconds to a few hours). During this time the energy must be used or it is lost. The Radioisotope Thermionic Generator (RTG's) suffer from many of the same problems, but their energy/weight ratio is much greater than any other power source. The life-time of these generators is controlled by the half-life of Pu 238 which is the most common heat source (86 years). A typical power source, such as the ones used on the Voyager spacecraft, generate about 150 watts over a ten-year period and weigh about 40 kg. The efficiency of thermionic generator is proportional to some fixed percentage of the Carnot efficiency, thus the efficiency decreases linearily with increased temperature on the cold side of the junction. Typical high-side temperatures are near 1280° K. If the high-side temperature remains fixed, the Carnot efficiency would be about 2.5 times poorer on the surface of Venus than on earth. Higher efficiencies, of course, are possible if the high-side junction temperature can be raised. This requires either higher powered radioactive materials or ways to reduce the heat transfer through the thermionic converter. Higher powered radioisotopes probably imply shorter half-lives, so the total energy may not change greatly. In spite of this, the future for RTG's looks good when long missions are to be considered, as no other power source is presently available.

Ultra Stable Oscillators

Ultra stable oscillators (USO's) are used to control the frequency and timing of all signals in the space probe. Microwave signals are generated by multiplying the basic oscillator or some lower frequency derivative of it by a series of simple multiplier stages. As a result, any phase jitter or frequency variation of the USO is multiplied by the same ratio. Thus, the purity of the final signal is controlled by the USO. Lower frequencies are usually generated by counting the USO frequency down with digital counters. The short term stability is most important for the transmission of information, while the long term stability is most important for maintaining timing of sequences of operations and for guidance and tracking. High quality USO's maintain long term stabilities of a few parts in 10^{10} and short term stabilities several orders of magnitude better. Relatively little is presently known about the stability at temperatures above 100°C. In order to determine what might be possible, several experimental oscillators are being designed at JPL for operation at 325°C. These units use special crystals cut to have a zero temperature coefficient at that temperature. The oscillator electronics is being fabricated with the standard hybrid circuit techniques. Experimental oscillators have already been tested at 280°C with off-the-shelf crystals. This circuit operated without failure during the two-week test period. The stability of crystal oscillators at high temperatures depends not only upon the stability of crystal and its Q, but on the drifts in the other electronic components. Clearly, components will age faster at high temperatures, and stabilities are sure to be poorer than obtained at room temperature or with the best oven controlled crystal oscillators. Just how much poorer is a question that remains to be answered.

Transmitters

The measurements of scientific data in a high temperature environment is of little use unless the information can be sent out of the environment. In the case of planetary exploration, the only feasible communications channel is via radio. The choice of wavelengths is dictated by the transparency of the atmosphere, the feasibility of the antenna structures, the availability of receiving equipment, and the background noise level. In the case of Venus, the atmosphere becomes opaque in the cm range, and a one-way transmission loss of 5 dB is encountered for 4 cm waves. Since Venus has no appreciable ionosphere, longer wavelengths pass freely. The physical size of antennas for wavelengths longer than a few meters probably restricts the low frequency range to 100 MHz. The radio background noise is contributed by the thermal radiation from the planet and the radiation from free space. The

free space background radiation becomes smaller as the wavelength is shortened, so shorter wavelengths are generally preferred. Therefore, any transmitter technology that can operate in the frequency range from 100 MHz to 3 GHz is a potential candidate for our purposes. If we restrict our study to devices that could operate above 150°C, we find only vacuum tube and GaAs semiconductor devices. In the case of vacuum tubes, there is no reason to believe that a wide variety of devices would not work if special precautions were taken in fabrication. Included as possibilities would be Klystrons, TWT's, and standard ceramic vacuum tubes. Of these only the ceramic triode vacuum tubes have been tested to temperatures of 450°C and found usable. A small pulsed oscillator is being designed and fabricated by General Electric for testing at JPL. This oscillator could be used as a beacon, a simple telemetering device, or possibly a radar altimeter. Vacuum tube devices have the potential or operating at either continuous low power or high peak pulse power, thus they are ideal for pulsed radar and beacon applications.

GaAs transistors are available and provide the possibility of higher efficiencies than vacuum tubes, since no heater power is required. GaAs transistors supplied by Microwave Semiconductor Corporation have been tested at JPL to temperatures as high as 210°C for a period of 10 days with no noticeable deterioration of the S-band performance. Operation of these devices to higher temperatures is likely to be possible with reduced efficiency.

Antennas

Given that a suitable transmitter can be designed and fabricated, the power must be radiated to the observer. Antennas are passive devices constructed of metal and insulators. They must be structurally solid enough that the deformations are small compared to the scale size of the wavelength. In general, the more directive the antenna is, the more important is the structural integrity. Also important is the resistivity of the metal surfaces at high frequencies, that is, the losses in the antenna are contributed by the currents flowing near the surface of the metal, therefore, since the resistivity increases with temperature, the losses will be larger at high temperatures. Exposed antenna surfaces will most likely have to be gold plated to insure that active gasses in the atmosphere will not react with the metal raising the resistivity and increasing the losses. Some antenna components employ ferrite devices for switching, isolation, hybrid combiners, and so forth. Many ferrites reach their Curie point at fairly low temperatures, and devices dependent upon high frequency magnetic materials may not be available to the designer. Otherwise, the antenna system is not considered to be a serious problem, but systems to point it are likely to be a greater problem.

Electromechanical Devices

Electromechanical devices include such things as motors, solenoids, relays, resolvers, synchros, and so forth. Transformers are also usually included as simple machines even though they do not employ mechanical motion. Both adequate magnetic materials and magnet wire exist for fabrication of transformers for operation to 500°C. Transformers have been built for even higher temperatures, however, commercial suppliers are scarce. Recently, transformers have been built by General Magnetics for testing at JPL for temperatures to 350°C. These transformers have operated for several hundred hours at temperatures between 200°C to 300°C. As a result, we believe that electromagnetic devices of all types can be designed. Presently under testing are several transformers and reed switches. High temperature motors were demonstrated by General Electric in the 1950's, but apparently this technology has been lost. At the present time, few high temperature electromechanical devices can be found, but modifications of standard designs should be possible simply by substituting high temperature materials for the standard materials.

Deployment Devices

Spacecraft designers have a number of favorite devices for deploying spacecraft systems. Among these are various pyrotechnique devices such as exploding bolts. All pyrotechnique materials become increasingly unstable as the temperature increases, and the use of such devices at high temperatures seems out of the question unless insulation or cooling is provided. A number of other deployment techniques seem applicable. For example, since the temperature increases as we enter the planetary atmospheres, various fusable pins and plugs can be used to initiate deployment. Pressure sensitive devices may also be practical.

Conclusions

There are many applications requiring high temperature electronics for space exploration. Presently, there seems to be no applications requiring systems operating above 500°C, where very few electronic components continue to operate. A number of important missions can be carried out with 300°C electronics, most interesting would be the low altitude balloon studies of the Venus. Even more extraordinary would be a low altitude airplane imaging system flying only a few hundred meters above the surface. Although it may be several years before such missions could be considered seriously, a balloon system to study the Venusian atmosphere at an altitude of 40 km is being designed by the French Space Agency and initial studies of 300°C electronics are being carried out at JPL for a possible balloon mission near an altitude of 18 km.

Electronic systems that are required include instruments, modulators, ultra stable oscillators, transmitters, power supplies, and power sources. Many of these systems would benefit from further work in high temperature semiconductors. Especially lacking are high temperature diode rectifiers and microwave transistors. New developments in GaAs and GaP devices would greatly aid in simplifying the design of high temperature systems. The ultimate 500°C applications will require new technology. Further work on SiC semiconductors seem appropriate. The integrated thermionic circuits being developed by McCormick (1978) at Los Alamos Scientific Laboratory coupled with ceramic triode transmitters by General Electric could provide the basic building blocks for the first entry into the area of 500°C exploration.

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NEEDS FOR HIGH TEMPERATURE ELECTRONICS IN FOSSIL ENERGY PLANTS

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The purpose of this paper is to present needs for high temperature electronics in fossil energy plants by first discussing several case histories on applications and second by discussing the measurement methods. This will present some of the typical operating conditions encountered in addition to temperature as well as the electronic requirements of high temperature transducers. Emphasis will be placed on unmet measurement needs as identified in a State-of-the-Art Survey.[1]

Process temperatures in synfuels plants have wide ranges which may be grouped as follows:

1. Ambient (-40°C to + 125°C) (solar plus self heat in enclosures);

2. 800°F (426°C) limit for carbon steel piping;

3. 1500-1700°F (800-925°C) in combustor effluents;

4. 2500-3200°F, in oxygen fed combustors and magneto hydrodynamic channels.

   Oil and gas well logging tools encounter operating temperatures of 100°-200°C. Under sodium viewing and signalling in fast breeder reactors can be done at 400°F (200°C) during loading or shutdown conditions.

Measurement methods include:

1. Ultrasonic, velocity by time difference and by Doppler effect (using piezoelectric transducers) as well as noise vibration, erosion and safety related measurements;

2. Electromagnetic induction, pressure gauges and flowmeters;

3. Capacitive, velocity by cross-correlation and present-by-weight solids in two phase (slurry) flows.

All of these, especially the piezoelectric and capacitive transducers, may benefit substantially by placement of preamplifiers or pulser/receivers near the transducers to transmit high level, low impedance analog signals or, in the future, fully digitized signals.

Future fossil energy plants will require automated control for efficiency, safety and environmental acceptability. Electronics and transducers capable of operating at and withstanding temporary high temperatures will be needed.

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HIGH TEMPERATURE ELECTRONICS UTILIZATION FOR PRESENT AND FUTURE NUCLEAR INSTRUMENTATION

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Electronics used in nuclear instrumentation is compromised by restrictions relative to the environment (temperature, radiation, pressure, etc.). Electronics, by necessity, must be located at considerable distances from the measuring point.

There will inevitably be many improvements made in instrumentation and controls because of the three-mile-island incident. Improved electronics capability will complement this surge for safer controls.

Other areas, such as diagnostics, will advance rapidly as ability to withstand harsh environments becomes reality. The remoteness of temperature measurement electronics significantly reduces time response. Minimum response time in the infant controlled fusion plasma diagnostics and control is vital.

Fluid density measurements would benefit from electronics mounted close to a gamma densitometer detector. This would improve response time and stability.

In conventional nuclear reactor instrument applications, a continuing engineering problem is the large number of pressure boundary penetrations necessary. With electronics capable of withstanding severe environments, the number of penetrations could be greatly reduced.

Fiber optics and electronics together capable of resisting temperature and radiation, in the nuclear reactor realm, would greatly enhance measurement capability along with reducing mechanical cabling and penetration requirements.

HIGH TEMPERATURE ELECTRONIC REQUIREMENTS IN AEROPROPULSION SYSTEMS

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Summary

This paper discusses the needs for high temperature electronic and electro-optic devices as they would be used on aircraft engines in either research and development applications, or operational applications. The conclusion reached is that the temperature at which the devices must be able to function is in the neighborhood of 500° to 600° C either for R&D or for operational applications. In R&D applications the devices must function in this temperature range when in the engine but only for a moderate period of time. On an operational engine, the reliability requirements dictate that the devices be able to be burned-in at temperatures significantly higher than those at which they will function on the engine. The major point made is that semiconductor technology must be pushed well beyond the level at which silicon will be able to function.

Introduction

The purpose of this paper is to describe the needs for high temperature electronics in the aircraft engine field. The viewpoint expressed is as seen from the Lewis Research Center of NASA in light of the fact that a major element of the Center's mission is to perform basic research and development aimed at improving aeropropulsion systems. This view is also based on discussions of the topic with many other groups involved in aeropropulsion both in government and industry.

The major areas of research and development in the aircraft engine field today are: (1) higher fuel efficiency, (2) greater durability, and (3) reduced emissions, both gaseous and acoustic. There is a fourth major area of work which is not tied so directly with laboratory research and development but with flying operational engines. This area is the reduction of direct operating cost via reductions in the cost of mainterance and improvements in control systems. This may well be the most significant motivator of all when one gets to the bottom line.

In this paper we will endeavor to show that all these areas of work, separately and together, provide strong motivation for development of high temperature electronic and electro-optic devices.

Requirements for Ground Testing of Engines

In this section we will discuss the need for high temperature electronics for operation on the hot rotating turbine disks of engines used for research and advanced development. One urgent requirement is for a multiplexer operating at 500° to 600° C.

The development of a new aircraft engine is a very long and expensive process. The process can take as long as 10 years from start on the drawing board to first engine certified to fly. During this process many prototypes are built for testing and development purposes. These prototypes, as well as individual engine components, are operated repeatedly in ground test facilities. For each of these test runs the engine or component is instrumented with the maximum number of sensors possible so that as much of the desired information as possible is obtained from each facility run. Even after an engine is certified for flight, problems arise in its operation on aircraft, or ways of improving its operational characteristics become apparent so that this testing process continues well into the useful life of an engine model. An example of this is the REFAN program conducted by NASA to modify engines like those on the DC9 and the Boeing 727 to reduce the acoustic noise. This model engine had been in service for many years but new pressures generated by environmental concerns made it desirable to go back and redesign parts of it for reduced noise emission. This program, by the way, led to the improved engine now on the new stretched DC9.

The net result of all this is that engine and engine components receive a lot of testing and this is a very expensive process. An individual new engine can cost a few million dollars per copy. It can take the order of twenty of these to come up with the first certifiable copy. The cost to tear down an engine, put in new sensors and wiring, and rebuild for another test run is frequently upward of a quarter million dollars. On top of all this is the fact that the cost of performing the test run itself is skyrocketing because of the rising cost of engine fuel and test facility operating power. A typical engine test stand capable of altitude flight simulation uses upwards of 50 megawatts.

These testing costs provide a tremendous impetus toward getting as many sensors on an engine at one time as possible in order to reduce the number of rebuilds and test runs. This is accentuated by the fact that every rebuild generates a possible assembly error which on rare occasion can result in catastrophic failure causing loss of engine and/or part of the facility itself.

What currently limits the number of sensors which can be installed and utilized for one test? To answer this one must look at the current reasons for engine R&D. As was mentioned in the Introduction, two of the main motives for R&D are reduced fuel consumption, and greater durability. In this area of work, detailed measurements on the hot rotating turbine are required. The example we will discuss is the need for data from this turbine. Here is where the need for high temperature electronics arises.

A fundamental law of thermodynamics, the Carnot theorem, says that greater efficiency results from higher turbine inlet temperature. Another fundamental law (related to that of Murphy) says that hotter rotating machinery is either less durable or weighs more. Part of the process, then, of producing more efficient and durable engines is one of obtaining information about the temperatures and stresses within the turbine to a level of detail never before attempted. The level of detail needed in a particular section of the engine is, in fact, proportional to the severity of conditions in that section because the margin for error is less in those sections where the temperatures and stresses are the greatest. This leads to the need for far more data than ever before from the turbine disks and blades. This is the hottest part of the engine other than the combustor itself. In the turbine the temperatures are not only

very high but they are also very non-uniform due to cooling flow through small bleed holes within the blades.

These very same conditions that make full instrumentation of the turbine mandatory also make reliable instrumentation most difficult. In a turbine test of this type, it is necessary to obtain data from the order of one hundred sensors, like thermocouples and strain gages, mounted on the rotating blades and disks. All these sensors can be mounted but routing the leadwork becomes impossible. One is faced with routing a few hundred wires down from the blades and/or disk to the shaft. From here they must be routed through a hole in the hollow shaft out to some transmission device such as a slip ring assembly or telemetry device to get the data from the rotating shaft to the stationary data handling equipment. The problem is that the hole is too small and/or the wires are too thick. If the hole is made bigger, the shaft has too little strength and its mechanical resonant frequencies begin to lie in dangerous regions. If the wires are made too thin, they break either in installation and/or in operation. Compounding this problem, in full scale engine testing, is the fact that there is no telemetry system available today which is capable of handling all these channels of data simultaneously in the severe environment where it must be located.

The current practice is to bring all the wires to the disk but connect only as many as can be brought through the shaft. After testing is complete with this configuration, the engine is torn down solely to allow connecting another batch of the wires. This process is repeated maybe three to five times until all the data is obtained. Not only is this a terribly expensive process but by the time you get to the third or fourth reassembly of the engine, many of the sensors and/or wires have failed from either the rigors of testing or those of disassembly and assembly. This whole situation is obviously not very good.

What is needed is electronics which can function in the environment in the region of the turbine disk. Here the temperatures are in the neighborhood of 500° to 600° C and the centripetal accelerations are tens of thousands of G's. What is needed most urgently is a multiplexer so that all the sensors can be read out during a single test run. Given the technology to build the multiplexer, the next item of interest may be some form of analog to digital converter capable of handling the millivolt level signals from thermocouples. Additionally, a high temperature telemetry system to send the signals from the rotating shaft to a stationary receiver would be highly desirable. The ideal would be one that requires no cooling because getting cooling air flow to these regions is not only complex and expensive but also the cooling air flow itself upsets the conditions in the engine to some extent. It should be noted that the capability for telemetry, multiplexing, and analog to digital conversion in this environment, except for the high temperature, has already been demonstrated.

What we have described here is the need for rugged electronics to be used at sink temperatures of about 500° or 600° C. It is most important that these devices work reliably for the order of 50 to 100 hours at test conditions. This is not continuous operation, though, because typical test runs last from 2 to 10 hours. More will be said about reliability in the next section when we deal with the problems encountered on engines that are on operational aircraft.

Requirements for Operational Engines

In this section we will develop the needs for high temperature electronics on operational engines. Even though we will arrive at the same temperature level requirement of 500° to 600° C, it will be for a different reason. The functioning temperature level of the electronics on an operating engine will be about 300° C but reliability will dictate a much higher burn-in temperature.

The most significant problem with operational aircraft engines today is that their direct operating costs are too high and getting higher. Certainly the rising cost of fuel is a major contributor to this problem. It is the root reason for the R&D aimed at reduced fuel consumption. However, fuel costs are not the only major constituent of direct operating cost. Another major factor is engine maintenance. As the engines become more sophisticated and complex in the interest of reduced fuel consumption and lower weight, they also become more difficult and costly to maintain. This has led to emphasis on greater durability and to modularization of engine designs.

Because we seem to be hammering away at costs so hard here, the reader may get the impression that these problems apply primarily to the civilian fleet. Not so. The military is also acutely concerned with these cost problems both because of their budget constraints and because they are flying the latest, most sophisticated engines which have not yet developed the maturity and refinement of design that usually leads to reduced maintenance costs.

How does one know when to pull an engine from service and tear it down for maintenance? The most common criterion is that a particular component of the engine has operated for a predetermined number of hours or cycles. Another common criterion which is used to determine when to remove an engine is that the required thrust cannot be achieved without exhaust gas temperature exceeding a permissible level. This temperature is monitored for just this purpose. If this temperature gets too high the turbine life is drastically reduced. There are other criteria used for removing an engine such as the belching of strange looking flames or smoke from the tail pipe or the emission of atypically cacophonous sounds and vibrations. Though these will not be considered significant for the purposes of this paper, they are usually considered urgent in the extreme by those aboard the aircraft.

The approaches to maintenance described above are not necessarily cost effective. The fact that an engine has operated for a given number of hours or cycles says nothing of the conditions under which it operated. In the interest of safety, these intervals are usually set shorter than really necessary so that maintenance is frequently performed on an engine that really does not need it. Exhaust gas temperature is only a very gross indicator of health so that the engine may be in sore need of maintenance before this criterion demands it. An alternative approach, which has been tried with some instances of success, is an engine monitoring system. The ideal monitoring system would be on the engine. It should collect data on selected engine parameters and process this data to a form that indicates whether the engine needs maintenance, points to the component needing the maintenance, and, perhaps, specifies what maintenance is needed. Such a system, coupled with the modularity of modern engines, will allow rapid access to the parts needing repair or replacement based on actual performance data. However, the modularity requirement dictates that at least some of the electronics required for engine monitoring be located on the engine.[1]

The need for such an engine condition monitoring system leads rather directly to the need for high

temperature electronics. The devices needed here are for sensor signal conditioning, signal transmission, and a monitoring computer. Compared with the requirement discussed in the previous section on ground testing needs, the device requirements dictated by this monitoring system at first appear to be quite benign. There are far fewer sensors needed. They are probably not in the rotating environment. The signal conditioning, transmission, and computing equipment will not be located right in the very hottest parts of the engine but on the outside casing somewhere where the temperatures are lower. Careful consideration of this system, though, leads to the conclusion that the requirements may well be as difficult to satisfy.

The operating temperature requirements for this monitoring system usually come out to be about 300° C for high performance military aircraft or the possible future supersonic transport.[2] This temperature is set by the fact that the coldest air available at maximum speed and altitude is at what is called ram air temperature or total temperature at these flight conditions. Every other available fluid temperature, except that of the fuel, is higher. Fuel cooling of the electronics is now being used in some cases but it is very undesirable from the standpoint of complexity, weight, and leak potential. Thus 300° to 400° C seems a reasonable target for flight engine monitoring devices. This level does not seem very severe until one considers the problem of reliability.

Whereas, in the previous section we came up with operating time requirements of about 100 hours, in the flight monitoring system we need thousands of hours of absolutely trouble free operation. The primary reason for this is that you will not reduce maintenance cost if your monitoring system fails. Failure of the monitoring system will result in either premature engine repair or in monitoring system repair or, far worse than these, the indication that the engine is healthy when it is not. This leads to the inescapable conclusion that very high reliability is needed.

Common practice for achieving high system reliability for a given functional temperature is to use components that have been burned-in at a significantly higher temperature in order to weed out potential failures. The higher the burn-in temperature, the shorter the burn-in must be to weed out the bad parts. An acceptable burn-in temperature would be about the same as the temperature required for ground test applications discussed earlier.

A further requirement on operational engines arises from the need for more sophisticated engine control systems. This is being pursued by going to all electronic controls. These controls are required in order to achieve peak performance with high efficiency, long life, and safety. Requirements for modularity, flight safety, and combat survivability dictate that this control system be located on the engine.[2] This puts it also in an environment like that discussed for the monitoring system. Indeed the control computer may also be the monitoring computer. Thus, engine control requirements result in about the same environmental and reliability needs for electronic devices as do those of the monitoring system.

We should point out here that there is also a need for optic and electro-optic devices to operate on the engine. This need arises primarily in military aircraft. Fiber-optic, rather than electronic cable, transmission of data from place to place on the aircraft brings the significant advantages of enhanced freedom from electromagnetic interference and the ability to send data over multiple paths without incurring the weight penalties of multiple electronic cables. Since much of the data originates on the engine, at least some of the electro-optic devices and fiber optic bundles will reside on the engine and therefore have to operate reliably in the same thermal environment as the monitoring and control electronics.

To summarize this section, the needs of operational aircraft engine monitoring and control dictate electronic and electro-optic devices capable of very high reliability while operating at temperatures not too much higher than 300° C. This reliability requirement, we believe, will require burn-in at the 500° to 600° C temperature level.

Concluding Remarks

In this paper we have discussed the needs for high temperature electronics and electro-optics as they would be used on aircraft engines in research, development, and operation. The conclusion reached is that the temperature at which the devices must be able to function is about the same either for R&D or for operational applications though the reasons for arriving at this estimated temperature are quite different. In R&D applications the devices must function at this temperature when in the engine but only for a moderate period of time. On an operational engine, the reliability requirements dictate that the devices be able to be burned-in at temperatures significantly higher than those at which they will function on the engine.

We have been purposely vague in defining the temperature goal as being around 500° to 600° C because there are arguments for a goal a hundred degrees above and below this temperature range. The major point to be made is that we must push well beyond the level at which silicon will be able to function.

As a final thought, we would like to say that all of this constitutes the justification needed to get support for a program aimed at high temperature electronics. It probably has little to do with the most significant future applications of these devices. They are presently unknown. Consider the original justifications for developing integrated circuits. They were to enable small, low power circuitry for spacecraft applications. As it has turned out, they were indeed useful for these purposes but these uses have proved to be of trivial impact on society relative to the other, more mundane uses to which they are now being applied. At Lewis we had a high temperature electronics program going in the late 60's and early 70's aimed at the needs of nuclear power systems for spacecraft. When that was no longer supported the electronics program went down the tubes with it. Now we are starting up essentially the same program for completely different reasons. We cannot help but feel that high temperature electronics will indeed have wide application not only to the areas discussed at this conference but also to far more important areas which we just do not have the vision to predict.

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PRESENT AND FUTURE NEEDS IN HIGH TEMPERATURE ELECTRONICS FOR THE WELL LOGGING INDUSTRY

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Introduction

The economic and political conditions which have increased the cost of fossil fuels along with changes in government regulations which have provided the incentive to produce hydrocarbons from depths greater than 15,000 feet, has encouraged the oil exploration industry to drill to depths not previously considered economically producible. This increased drilling activity has placed more demands upon the well logging service companies to provide a wide range of logging and completion services for wells with bottom hole temperatures greater than 200°C and pressures in excess of 20,000 psi. An example of this type of activity is along the U.S. Gulf Coast, which has a high geothermal gradient that can produce temperatures as high as 250°C at depths of only 16,000 feet.

Standard downhole tools for well logging measurements are typically rated for an environment of 175°C ambient temperature and pressure of 20,000 psi[1]. The ability to log the higher temperature wells has generally been limited to engineering developmental tools or tools in which the electronics section is housed in insulating dewar flasks with heat sink compound capable of maintaining component temperatures below 150°C. The limitation in power available from portable power units has limited the use of thermoelectric units for cooling.

The Challenge

Deep wells with temperatures and pressures above the limits of the standard tools have been considered as curiosities and very limited in number; thus, the use of special tools prepared and operated by engineering personnel, although expensive, was acceptable. However, as deep pays have been proven and the economic incentive to produce these wells has increased, the amount of deep exploration activity has significantly increased. The logging service companies have found it necessary to develop tools that can be accurately run by field personnel and which give reliable performance for several hundred hours at temperatures greater than 200°C.

Not only has the deep well put more severe temperature requirements on the tools, but the need to reduce expensive drilling rig downtown has dictated that a number of different tools be run in combination on a single logging run. This need has increased the complexity of the tools by requiring extensive analog signal conditioning, as well as the addition of a digital communications system to transmit the large amounts of sensor data to the surface over the limited number of lines available in the logging cable.

Increased complexity in the tool electronics would normally mean an increase in the tool length since drilled hole limitations restrict the maximum tool diameter. However, to reduce tool string length and weight, emphasis is placed on elimination of flasks and the miniaturization of electronics through the use of medium and large scale integrated circuits and the combination of ICs and discrete components into hybrid microcircuits.

It is this requirement that forces the well logging tool designer to design for reliable operation at high temperature and to put as much circuitry as possible into the small space available. To meet this need the designer must have a wide range of semiconductors, passive electronic components, and dielectric materials commercially available. The key point here is "commercial availability" such that tools can be designed and then manufactured in sufficient quantities to support the expanding field requirements.

A successful high temperature logging tool is a combination of various mechanical and electronic components with special consideration required in the application of metals, elastomers, cables, pressure seals, feed thrus, as well as electronic components. The following limited discussion addresses only a segment of this - the electronic components.

The Components

Functional Blocks

The preferred component for a downhole logging tool is actually a functional block, either monolithic or hybrid, which integrates a complete schematic block into a single package characterized and tested for high temperature operation. This allows maximum utilization of available space in the pressure sealed housing and gives added assurance that the system will function properly after assembly. The other major contribution of the functional block integration is the improved reliability obtained with component prescreening and reduced number of packages with the resulting fewer interconnects.

Some types of electronic functions which are utilized and needed for downhole tools include the following:

1. Voltage Regulators - linear and switching
2. Precision Voltage Reference
3. Instrumentation Amplifier with 100dB CMRR
4. D to A and A to D, 12 Bit Converters
5. Wide Bandwidth Operational Amplifier with temperature stable bandwidth and offset
6. Precision Comparator
7. High Current, Wide Band Linear Driver
8. Phase Sensitive Detector
9. FET Switch and Driver with low leakage and ON resistance
10. Sample and Hold
11. Logic family
12. Crystal Controlled Oscillator
13. V to F Converter

Preferred specifications at 200°C for the functions listed would be the same as for better parts presently available at 125°C. Operation with some specification degradation to 250°C would be acceptable.

Relays

Relays in downhole tools are kept to a minimum, but if made more reliable, would be used. A holding relay which dissipates power only when actuated is desirable. At least a DPDT, crystal can size relay with self-wiping contacts for dry circuit to one amp loads is needed. More poles and smaller size (TO-5) would be a bonus.

Thyristor

SCRs capable of switching up to 35 amps of current and blocking 800 volts with less than 2.5 milliamps leakage at 250°C are needed for power control and control of capacitor discharge.

Diodes

With many of the radiation logging tools requiring high voltages, there is a particular need for rectifiers with reverse breakdown voltages greater than 3000 volts at leakage currents less than 25 microamps at 250°C. It is expected that GaP devices might fill this requirement, but they have remained as laboratory specimens rather than commercial catalog items.

Capacitors

Capacitors with the low dissipation factor of Teflon (0.5%) over temperature, the TC of NPO Ceramic (± 30 ppm/°C) and a high volumetric efficiency are needed. Capacitors with these characteristics are needed particularly for applications such as active filters and sample and hold circuits. Although Ruby Mica offers the low dissipation factor and high temperature operation, its TC exceeds the desired ±30 ppm.

Resistors

Fixed resistors using metal films have operated satisfactorily up to 250°C and beyond, but a trimmer potentiometer is needed that will maintain its setting over this same range of temperature. Since thick film resistive elements on ceramic are suitable for high temperature, the major factor in obtaining such a device is in the mechanical design of the contact and drive mechanism to maintain the precise setting over such a wide temperature range.

Although selection of fixed resistors to compensate for circuit variations is an obvious alternative, it gives considerable difficulty in field calibration and alignment.

Magnetics

Inductor and transformer design with existing materials has allowed for operation up to 200°C for some time. Operation above this temperature for extended periods awaits the development of more stable magnetic materials and higher temperature wire insulation. Although the designer can remove transformers from most small signal circuitry, the need for power transformers for low loss conversion of downhole supply power is still important.

Dielectric Materials

In several types of logging tools, there is a need to fabricate portions of the tool from a dielectric material to permit the transmission of electric fields or to isolate an electrode from an adjacent conductive housing. For temperatures up to 200°C this has been accomplished by use of epoxy/polyimide glass laminate because of its mechanical strength and its ability to be machined to precise dimension in any shape. The epoxies presently used begin to deteriorate rapidly with storage at temperatures above 200°C so new materials are needed to extend this capability.

Conclusion

New developments and increased vendor interest in high temperature electronics have definitely improved the availability of components for hostile environment equipment. This paper has attempted to show that the market continues to expand and opportunities exist for the continued growth of commercial products in well logging services.

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SESSION II

DEVICES

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PASSIVE COMPONENTS FOR HIGH TEMPERATURE OPERATION

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Thin film technology has been well-established as a viable and necessary part of modern microelectronics. Extending the technology of thin films for use at high temperatures has required the development of new materials and processes in order to meet the required electrical specifications at elevated temperatures. By developing thin film components for high temperature applications such as geothermal well-logging, aircraft engine instrumentation, and nuclear reactor monitoring, it will be possible to provide high circuit density and improved reliability.

One of the major objectives in developing thin film materials and processes has been to ensure that they would be fully compatible with standard silicon integrated circuit technology. This would lead to the ability to adapt one or more of the processes into existing processing lines with minimum disturbance. The passive components must also be compatible with hybrid circuit fabrication and, if possible, Integrated Thermionic Circuits.

Research and development work at The University of Arizona has been directed toward resistors, capacitors, and interconnect metalizations. The use of Low Pressure Chemical Vapor Deposition (LPCVD) has been used in material development and component fabrication. This is a major departure from the standard thin film deposition method of sputtering and thermal evaporation. LPCVD by its very nature is a process which allows the passive components to be fabricated at temperatures higher than their highest required operating temperature.

The deposition of thin films by LPCVD is accomplished by reacting one or more gases on the surface of a heated substrate. The major components of an LPDVD reactor are illustrated in Figure 1.

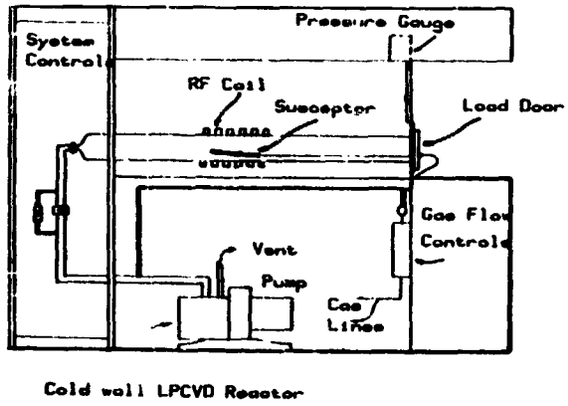

Figure 1. Pictoral representation of the major internal components of the LPCVD reactor.

The substrates to be coated are placed on the graphite susceptor and then loaded into the center of the quartz reaction tube. RF power is applied to the coil on the outside of the reaction tube which in turn is coupled into the graphite susceptor causing it to heat. Temperature of the susceptor is measured with a type-K thermocouple.

The vacuum pump is a special chemical-grade roughing pump designed to withstand the pumping of corrosive gases. Prior to the application of RF power, the atmospheric pressure is reduced to the pressure limit of the pump; the carrier gas is turned on, and the pressure _____set. Pressures of several torr or less are typical, with carrier-flow rates of 0.1 to 2.0 liters/min. Nitrogen, hydrogen and helium are typical carrier gases. These are controlled with mass flow controllers and the pressure is continuously monitored with a capacitive manometer.

Material selection is of primary importance in designing high temperature passive components. All of the materials must have the desired electrical properties, and they must also have compatible mechanical properties including coefficient of expansion, stress, and adherence. Without the required mechanical properties, the components would not survive long enough to test. A group of materials that can be deposited by LPCVD and which also are electrically, chemically, and mechanically well-matched are:

(1) Tungsten
(2) Tungsten-silicon
(3) Silicon nitride

Substrate materials are equally important for the same reasons; the two substrates recommended are:

(1) Oxidized silicon wafers
(2) Sapphire.

The reactions to form the materials are:

$$WF_6 + 3H_2 \rightarrow W + 6HF$$

$$WF_6 + SiH_4 + H_2 \rightarrow W - Si + HF$$

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

Not only must the materials be compatible, but so also must the deposition reactions at elevated temperatures so that the deposition of one material does not destroy the previously deposited thin film layers.

Delineation of the materials is accomplished with standard equipment and processes used in silicon IC fabrication. The thin films can be etched by wet chemical etches, or by plasma etching. Negative photoresist has been used since the developers for positive photoresists are basic and therefore tend to etch the tungsten.

Specifications for thin film resistors required stable operation to 500° C. with temperature coefficients of resistance (TCR) less than 50 ppm/°C. over the entire temperature range. The material selected for the resistors was tungsten-silicon deposited by LPCVD. The characteristics of the tungsten-silicon can be adjusted to meet the requirements of high temperature operation, stability, and low TCR.

Tungsten-silicon is grown from the reaction of tungsten hexafluoride, silicone, and hydrogen:

$$WF_6 + SiH_4 + H_2 \rightarrow W - Si + HF + H_2$$

The ratio of tungsten to silicon can be varied. The TCR can be made both positive or negative depending on

the process parameters used. Figure 2 is a resistance vs. temperature curve for a W-Si resistor. Typical resistivity of the tungsten-silicon used for the resistors is 2,500 μΩ.cm. Sheet resistors range from 50 to 1000 Ω/□ and TCR values from -50 to 50 ppm/°C. The process is compatible with silicon IC fabrication and thin film capacitor processes.

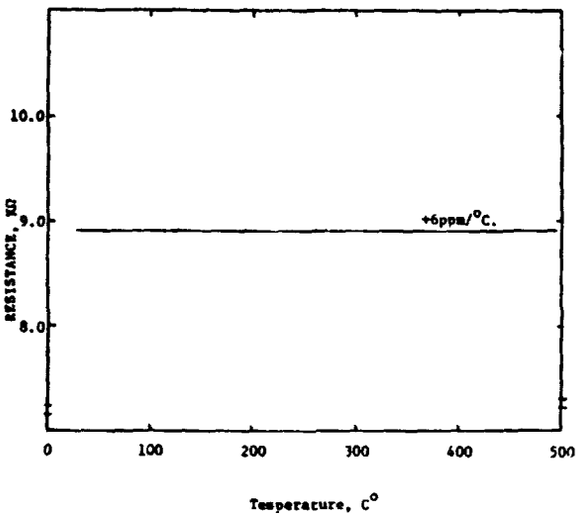

Figure 2: Resistance versus temperature curve for a W-Si thin film resistor TCR = +6 ppm/°C.

The thin film capacitors are designed to operate from room temperature to 350° C. and to fill the need for high temperature capacitor with capacitance up to 0.1 μF. Work voltage is specified at two points:

(1) 50 WVDC at 25° C,

(2) 20 WVDC at 350° C.

With a 20-volt bias applied across a capacitor at 350° C., the DC resistance must be greater than 1×10^7 Ω.

Dissipation factor is required to be less than 0.010 at 1 KHz. over the above temperature range.

Capacitors are parallel plate structures using oxidized silicon wafers as substrates; however, sapphire could be used. A cross-section is illustrated in Figure 3.

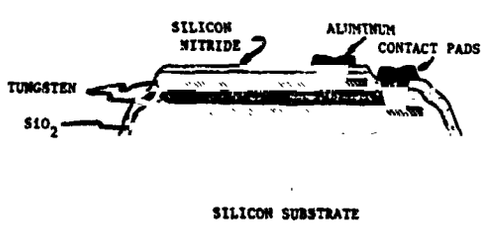

Figure 3: Cross-section of thin film capacitor. Tungsten is used for the parallel plate electrodes, and silicon nitride is used for the dielectric layer and the passivation. All materials with the exception of the aluminum bonding pads are deposited by LPCVD.

The electrodes are tungsten and the dielectric layer and passivation are silicon nitride. Bonding pads are thermally evaporated aluminum.

With LPCVD deposition of the layers, pinhole problems in the nitride have not been encountered, and it has therefore been possible to fabricate capacitors with several square centimeters area. Typical capacitance is 0.02 μF/cm.^{2}; areas as large as 4 cm. have been used.

The relative dielectric constant of the silicon nitride is 8.6 and the dissipation factor due solely to the silicon nitride is 0.0002. For large value capacitors, the series resistance term becomes the dominant factor in increasing the dissipation factor. The total dissipation factor is generally less than 0.003 at 350° C. and 2.0 KHz.

In order to meet the DC resistance requirements, it is necessary that the silicon nitride have very low conductivity. The conductivity is a function of both the temperature and the applied electric field so both must be considered when designing a capacitor. Capacitors which were fabricated exhibited a temperature coefficient of capacitance of approximately +70 ppm/°C.; a typical capacitance-temperature relationship is shown in Figure 4.

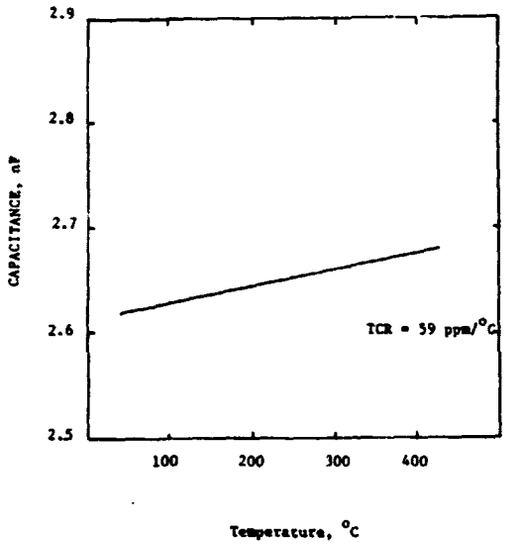

Figure 4: Capacitance as a function of temperature for a thin film capacitor.

The processing needed to form high temperature capacitors with areas up to 4.0 cm.^{2} and capacitance values to 0.1 μF has been developed to the point where it can be transferred to commercial production. Table I shows the salient features of the process.

By extending the use of the LPCVD tungsten, interconnects between passive components can be formed. If the tungsten is deposited directly over the surface of a silicon wafer that has been processed to the point where it is ready for the metallization, tungsten can be substituted for the normal aluminum interconnect metallization.

Aluminum as an interconnect metal on silicon integrated circuits has a number of problems when high current densities and high operating temperatures are present. Under these conditions, electromigration

of the aluminum can occur, causing the physical transport of silicon out of the contact regions of the silicon.

TABLE I

HIGH TEMPERATURE CAPACITOR MANUFACTURING PROCESS

1. LPCVD TUNGSTEN - 2,000 A.
2. PHOTOLITHOGRAPHY - BOTTOM ELECTRODE
3. LPCVD - Si_3N_4 (3500 A) FOLLOWED BY LPCVD TUNGSTEN (2000 A, TOP ELECTRODE)
4. PHOTOLITHOGRAPHY - TOP ELECTRODE
5. LPCVD - Si_3N_4 (1,000 A, PASSIVATION) AND LPCVD TUNGSTEN (2,000 A, USED AS ETCH MASK)
6. PHOTOLITHOGRAPHY - CONTACT WINDOWS IN TUNGSTEN ETCH MASK.
7. ETCH Si_3N_4
8. PHOTOLITHOGRAPHY - REMOVE ETCH MASK
9. ALUMINUM CONTACT EVAPORATION
10. PHOTOLITHOGRAPHY - ALUMINUM CONTACTS.
11. TEST.

Failure of the interconnect then occurs; the failure rate is accelerated as the temperature is increased. Failure can also occur because of poor step coverage of the aluminum used in silicon IC. Tapered regions in the interconnects often form in the bottom of the steps during the deposition process.

Tungsten was investigated as a possible material for use with high temperature silicon IC to avoid the problem of premature failure of the metallization at elevated temperatures.

The contact regions between the tungsten interconnect and the silicon must form ohmic contacts. This was investigated as a function of silicon doping, process parameters in the tungsten deposition and temperature. Ohmic contacts were formed in both n- and p- type silicon for phosphorus doping levels of 4 x 10^{18} cm.$^{-3}$ to 5 x 10^{20} cm.$^{-3}$ and boron levels of 2 x 10^{17} cm.$^{-3}$ to 1.0 x 10^{20} cm.$^{-3}$. The ohmic characteristic of the contact is seen in the linear I-V relationship for a 10 μm x 10 μm contact shown in Figure 5.

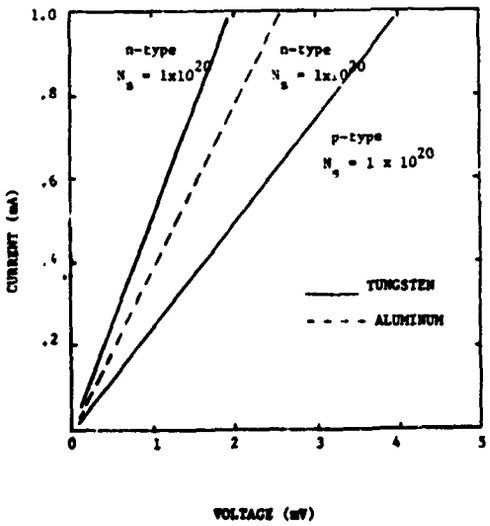

Figure 5: I-V curves for ohmic contacts to n- and p-type silicon. The solid line represents tungsten metallization, and for the comparison, the dashed line is for an aluminum/silicon contact to n-type material.

Tests for electromigration were made using two metallization strips; each strip was 10 μm wide and 0.5 μm thick. They were designed so that the current could be injected into or brought out of the tungsten through a silicon contact or through the tungsten alone. One strip was designed to traverse .5 μm of oxide strips. The contact resistance between the silicon and tungsten could also be monitored separately.

No evidence of electromigration was seen in the tungsten at current densities of 4 x 10^6 A/cm.^{2} for 72 hours. Tests were run at substrate temperature from 25° C. to 300° C. The actual temperature of the interconnect was somewhat higher due to the power dissipated by the test current.

Critical current densities (current density at point of interconnect failure) were 4.5 x 10^6 A/cm.^{2} for Si_3N_4 passivated tungsten, and 5.7 x 10^6 A/cm.^{2} for hydrogen-annealed tungsten.

SEM microphotographs of the tungsten over oxide steps indicated excellent step coverage. No failures due to exceeding the critical current densities occurred in the step regions.

Schottky diodes were also formed between the tungsten and the silicon wafer; however, they were leaky. It is now felt that the leakage current was the result of improper diode design rather than an inherent problem in forming good Schottky diodes between silicon and LPCVD tungsten.

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DEVELOPMENT OF AN 1100°F CAPACITOR*

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SUMMARY

The feasibility of developing a high temperature capacitor for 1100°F operation which is as small and light as conventional capacitors for normal operating temperatures is discussed in this paper.

Pyrolyic boron nitride (PBN) was selected for the dielectric after evaluating three other candidate materials at temperatures up to 1100°F. PBN capacitors were made by slicing and lapping material from thick blocks and then sputtering thin film electrodes. These capacitors had breakdown strengths of 7,000 volts per mil and a dissipation factor of less than 0.001 at 1100°F.

Additional processing improvements were made after testing a multi-layer or stacked PBN capacitor for 1,000 hours at 1100°F. Sputter etching the wafers before depositing electrodes resulted in a 2-3 fold reduction in dissipation factor. A sputtered boron nitride film applied to the outer electrode surfaces produced a more stable capacitor. This data will be presented together with a design for a 0.1 μF capacitor and a summary of PBN wafer fabrication costs.

INTRODUCTION

Capacitors were one of the electrical components that limited the operating temperatures in the advanced electric power systems being developed for spacecraft in the 1960s. As electric power requirements in spacecraft increase, the amount of power lost as heat also increases. This heat must be removed to keep temperatures from building up beyond the operating limits of the electrical components. Specially designed mica capacitors were available for 750°F operation but these devices were larger and heavier than standard units. In order to build a higher temperature-lightweight capacitor, a better dielectric was needed.

MATERIAL SELECTION

At least ten different dielectric materials were considered initially as candidates for a high temperature capacitor. From published data, four likely materials were selected for test: single crystal Al_2O_3, polycrystalline Al_2O_3, hot pressed BeO and pyrolytic boron nitride (Pyrolytic boron nitride, formed by a chemical deposition process at 3600°F, is a denser and purer material than compressed and sintered boron nitride). Wafers were sliced from blocks or pieces of the candidate materials and then lapped and polished. Since capacitance varies inversely as the thickness of the dielectric material, the wafers were made as thin as practicable. The thinnest wafers were produced from pyrolytic boron nitride (PBN). This material is soft (Moh's scale-2) and less brittle. It was found that PBN could be lapped into flexible, pin-hole free wafers as thin as 0.0004 inches from thick blocks of starting material (1).

After careful cleaning, thin film electrodes of platinum - 20% rhodium were applied by DC triode sputtering. Glass masks were used for pattern definition. A small test furnace was built to fit inside an 18-inch glass bell jar that was pumped to the test pressure of 1-4 x 10-7 Torr with a liquid nitrogen trapped diffusion pump. Electrical tests of the single wafer capacitors in vacuum at temperatures up to 1100°F showed that pyrolyic boron nitride was by far the best material. The dissipation factor of PBN capacitors was less than 0.001, 10 to 100 times better than that of capacitors made from the other candidate materials as shown in Figure 1.

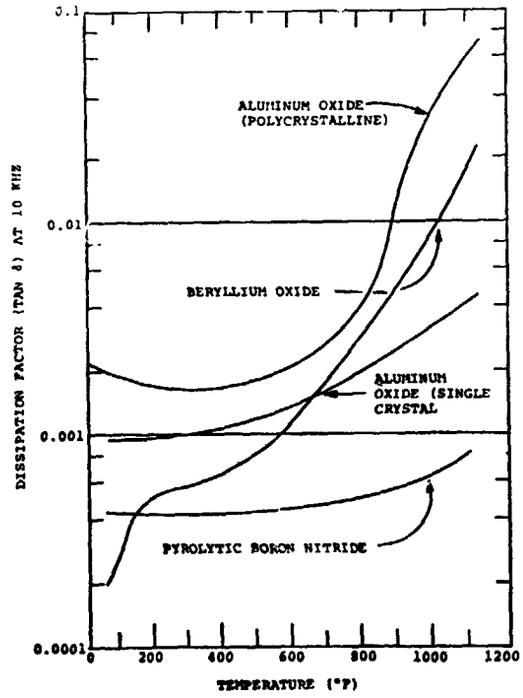

Figure 1. Comparison of Dissipation Factor Versus Temperature for Candidate Purity Materials.

Figure 2 shows that the change in capacitance from room temperature to 1100°F was minus 1.7 percent compared with plus 10 percent for single crystal Al_2O_3. The measured DC breakdown voltage was 7,000 volts per mil for a 0.001 inch PBN capacitor at 1100°F, compared to 1800 volts per mil for the closest competing material (single crystal Al_2O_3).

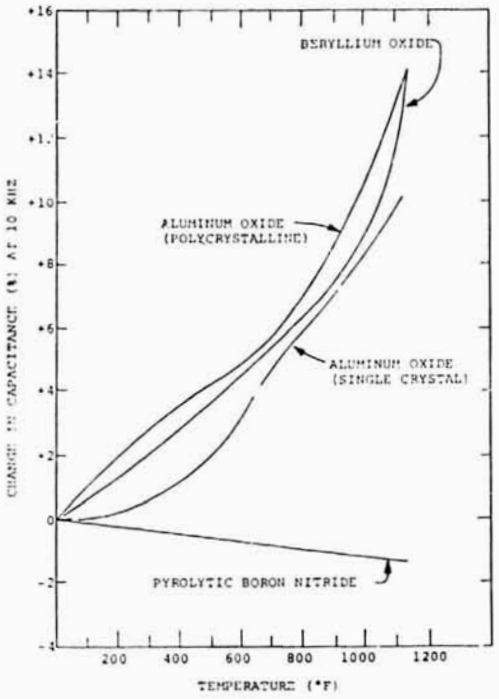

Figure 2. Change in Capacitance From Room Temperature to 1100°F for Candidate Materials.

PYROLYTIC BORON NITRIDE CAPACITORS

To obtain higher capacitance units, individual PBN capacitor wafers were shaped, electroded with sputtered platinum and stacked. Actual capacitor wafers (rectangular and round with tabs) are shown in Figure 3.

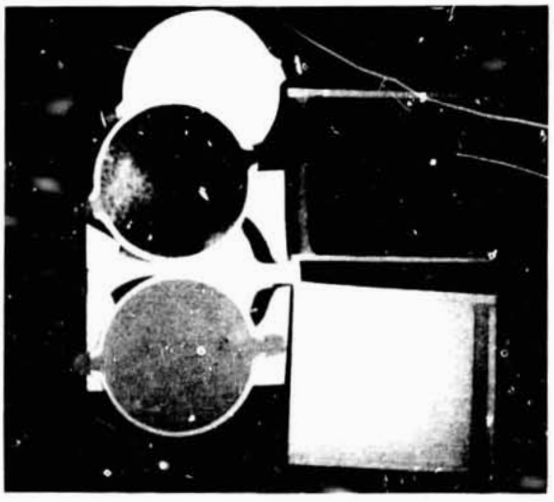

Figure 3. Photograph of Rectangular PBN Capacitor Wafers and tabbed 0.750-inch diameter wafers.

The platinum sputtering targets were positioned on opposite sides of a wafer. The wafer was clamped between two glass masks as shown in Figure 4 so that both surfaces of

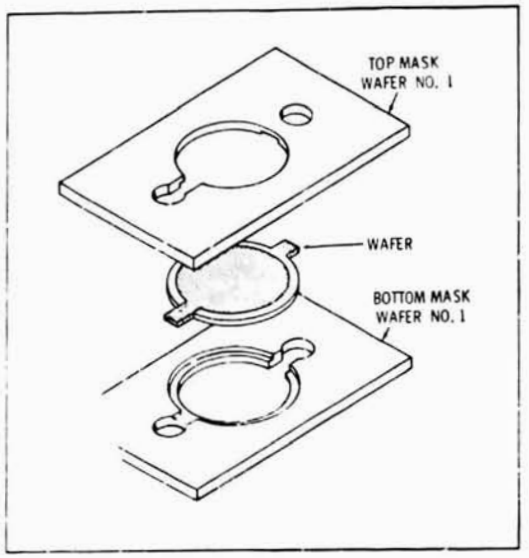

Figure 4. Glass masks used for sputtering electrodes on tabbed wafers.

the wafer were coated at the same time including the conducting path around each tab. By properly orienting the tabbed wafers, alternate electrodes are connected together as shown in Figure 5. The total measured capacitance of each stack is then the sum of the capacitances of all wafers.

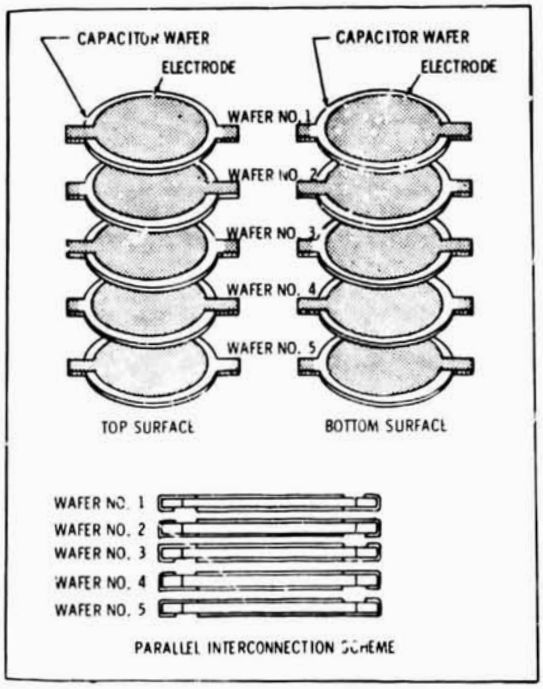

Figure 5. A Five-Layer Stacked Capacitor Showing Tabbed Wafers and Electrode Geometries and Electrode Orientation Necessary for Parallel Electrical Interconnection.

TABLE 1

Pyrolytic Boron Nitride Capacitor Compared with Lower-Temperature Capacitors*

Capacitor Type	DC Working Voltage	Maximum Operating Temp. (^{o}F)	Capacitance per Unit Volume (μF/in.^{3})	Volumetric Efficiency (μF-V/in.^{3})	Capacitance Change from Room Temp. to	Dissipation Factor At 1 kHz
Metallized Polycarbonate	600	200	0.54	320	200^{o}F,+1%	0.002 at 200^{o}F
Teflon, Foil Electrodes	200	400	0.64	127	400^{o}F,-4%	0.001 at 400^{o}F
Mica (Commercial)	150	750	0.13	19	750^{o}F,-4%	0.02 at 750^{o}F
Mica (experimental)	250	900	0.03	8	900^{o}F,-25%	0.10 at 900^{o}F
Pyrolytic Boron Nitride (5-wafer stack)	500 to 1000	1100	0.8 to 1.74 (uncased)	400 to 1740 (uncased)	400^{o}F,-05% 1100^{o}F,-1.%	0.001 at 400^{o}F 0.003 at 1100^{o}F

*Values are typical for the general types of dielectric systems indicated.

Electrode thickness is negligible (about 0.00001 inch) making the total stack height essentially the sum of the thicknesses of the PBN wafers. This construction produces higher capacitance per unit volume than that of other capacitor types, and also considerably higher volumetric efficiency. These and other qualities are compared in Table 1 for a PBN capacitor and several commercial capacitors.

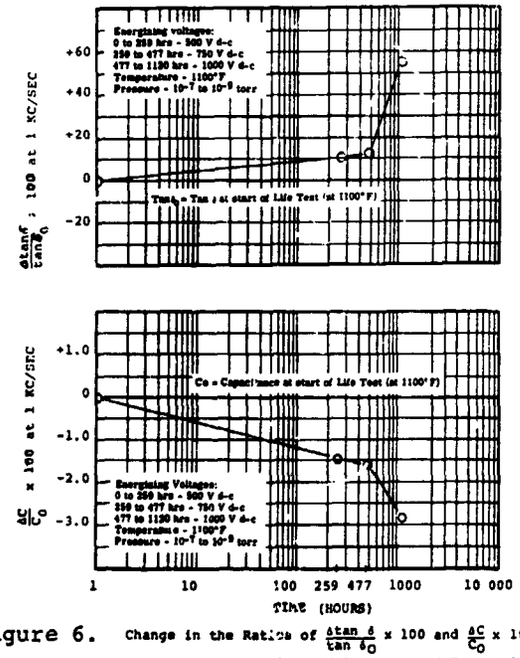

Figure 6. Change in the Ratios of $\frac{\Delta \tan \delta}{\tan \delta_0} \times 100$ and $\frac{\Delta C}{C_0} \times 100$ as a Function of Time and Increased DC Energizing Voltages for a Five-Wafer Multi-Layer Pyrolytic Boron Nitride Capacitor with Sputtered Platinum Electrodes in Vacuum at 1100° F

A 5 wafer PBN capacitor was life tested at 1100^{o}F in vacuum for a total of 1120 hours at a DC voltage stress up to 1,000 volts per mil. Figure 6 shows the change in dissipation factor and capacitance as functions of time and increasing voltage. Note, however, that a more rapid change in capacitance occurred at 477 hours which corresponds to an increase in energizing voltage from 750 to 1,000 volts per mil. Subsequent analysis showed that these changes were probably due to a slight separation of electrodes from the wafer surfaces in the stacked capacitor.

FABRICATION IMPROVEMENTS

Two methods were developed to improve the electrode adherence on PBN wafers in a stacked capacitor. The first method was to RF sputter etch (texturize, both surfaces of a PBN wafer just prior to depositing electrodes. This treatment produced an ultra clean surface and electrode adhearance values greater than 1,000 psi. A 2-3 fold reduction in dissipation factor was an unexpected bonus compared to capacitors made without etching. The reduction in dissipation factor is attributed to the removal of mechanically disturbed surface layers produced during final lapping. About 3,000 angstroms was removed from each surface of a PBN wafer by sputter etching. Removal of additional material had a negligible affect on dissipation factor.

The second improvement was to deposit a diffusion barrier layer over the outer surfaces of each electrode to prevent interelectrode bonding in a stacked capacitor. Boron nitride was RF sputtered from a PBN target using a glass mask to protect the contact tabs. About 500 angstroms of boron nitride was deposited on each electrode at 70 angstroms per minute.

A three wafer capacitor was tested that incorporated these improvements (sputter etching and BN barrier layers). Figure 7 compares the rate of change in capacitance

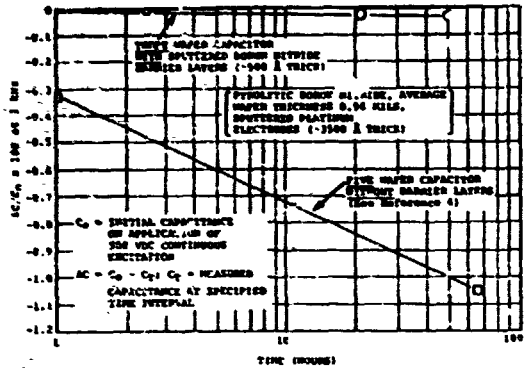

Figure 7. Comparison of the Change in Capacitance Versus Time at 500 V dc/Mil in Vacuum at 1100° F for Pyrolytic Boron Nitride Multi-Layer Capacitors With and Without Sputtered Boron Nitride Barrier Layers.

versus time for the improved 3 wafer capacitor and the original 5 wafer capacitor. The 3 wafer capacitor shows a negligible change in capacitance for the duration of the test (75 hours at 1100°F).

LARGER PBN CAPACITORS AND COST ANALYSIS

The specially designed ceramic package shown in Figure 8 was fabricated to provide the necessary compressive forces, orient and hold PBN capacitor wafers and provide a hermetic enclosure. More than 40 defect free PBN capacitors were made with sputter etched surfaces and boron nitride barrier layers for this package. The package has sufficient internal volume to hold more than 300 capacitor wafers which would be equivalent to a 0.1 uF capacitor. In 1976 a cost analysis was made based on yield data from previous laboratory experience with this process. A 16 percent overall yield assumption was made (from raw material to final test). The cost to fabricate 572 finished wafers (equivalent to 0.16 uF) was about $51,000. Half of this cost was for purchased raw materials (PBN) in the form of 1 x 1 x 1/8 inch blocks.

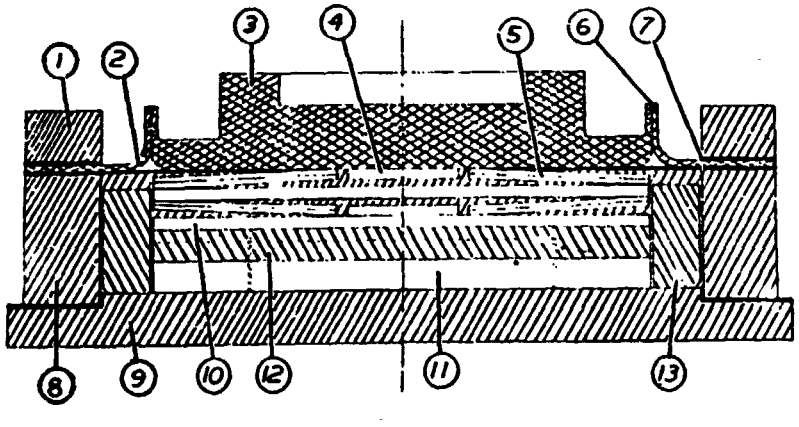

Figure 8. PBN Capacitor Hermetic Package - Volume 0.87 In^3 (to 0.1uF)

CONCLUSIONS

Pyrolyic boron nitride capacitors offer the promise of high stability and reliability over long periods in a wide range of environments and operating conditions. These new capacitors should find use in many demanding applications. The cost to make these capacitors by slicing and lapping thick blocks of material is a deterrent to commercialization. A study of methods of producing low defect thin films of PBN would provide the basis for a more cost effective high temperature capacitor technology.

ACKNOWLEDGMENTS*

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The author would like to thank A. C. Beiler and R. A. Lindberg for their support and guidance and S. D. Burkholder, H. Banks and R. Schumate for capacitor fabrication and testing.

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(1) R. E. Stapleton, NASA-CR-1213 (1968) and NASA-CR-1799 (1971). These reports contain a full discussion of PBN wafer slicing, lapping, cleaning, electrode deposition and testing.

LEGEND (Figure 8)

1. Al_2O_3 Cylindrical Ring (1.5 inch O.D.)
2. Top Ring, Cb-1%Zr
3. Top Plug, Cb-1%Zr
4. Spring Alignment disk, Mo
5. Bellville Spring, Ta(T-111)
6. Electron Beam Weld
7. Braze Alloy, 60Zr-25V-15Cb
8. Al_2O_3 Cylinder
9. Metallized BeO Disk, Sputtered Mo
10. Spring Support Plate, Mo
11. PBN Capacitor Stack, 0.78 inch dia.
12. Pressure Plate, PBN
13. Alignment Bushing, PBN

HIGH-TEMPERATURE MEASUREMENTS OF Q-FACTOR IN ROTATED X-CUT QUARTZ RESONATORS*

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The Q-factors of piezoelectric resonators fabricated from natural and synthetic quartz with a 34° rotated X-cut orientation have been measured at temperatures up to 325°C. The synthetic material, which was purified by electrolysis, retains a high enough Q to be suitable for high-temperature pressure-transducer applications, whereas the natural quartz is excessively lossy above ∿ 200°C for this application. The present results are compared to results obtained previously on AT-cut resonators.

Introduction

Quartz-resonator pressure transducers are being developed at Sandia National Laboratories for high-temperature (≈ 300°C) applications in geotechnology areas.[1] Areas of particular interest include surveying of geothermal and deep oil and gas resources. In order for a crystal resonator to be used as a pressure gauge, the effect of temperature changes on the resonator frequency must be minimized compared to the pressure-induced frequency shift. Thus it is desirable to use a resonator design that is temperature-compensated to as high a degree as possible over the temperature range of interest. Plate resonators operating in the thickness shear mode are generally utilized in temperature-compensated applications, as they have turnover points in their frequency vs temperature characteristics. This means that the derivative df/dT (f = frequency, T = temperature) is zero at some appropriate temperature. For applications around 200-300°C, a rotated X-cut orientation of the resonator plate has been shown to be more suitable than other temperature-compensated orientations because it exhibits a lower curvature of f(T) at the turnover point.[2] The geometry of the rotated X-cut plate is shown in Fig. 1. Here a rotation angle of $\theta = 34^\circ$ is shown, as this is the angle that provides compensation in the temperature range of interest.

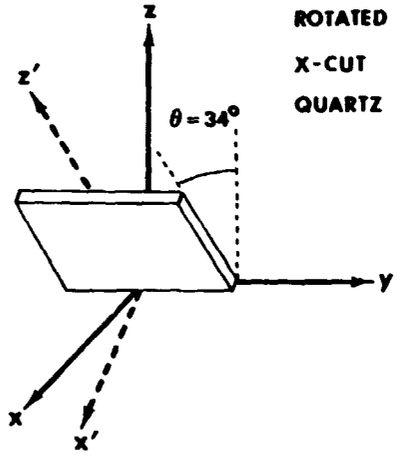

Fig. 1. Illustration of the 34° rotated X-cut orientation used for temperature-compensated pressure gauge applications.

A more detailed description of the pressure gauge being developed can be found in Ref. 1.

Although the rotated X-cut orientation has been found to be optimum from the viewpoint of its frequency vs temperature and pressure characteristics, there are no data in the literature on the Q-factor of resonators with this orientation. For stable and reliable gauge operation it is necessary to have a Q of over ∿ 10^5 for all operating temperatures.[1] It is known from previous work on quartz that the Q depends on a number of factors including crystalline orientation, growth conditions (natural or synthetic), sample preparation, and the number and type of defects present. The present work was undertaken to characterize the temperature dependent Q-factor of rotated X-cut quartz resonators fabricated both from natural and synthetic (electrolyzed) material.

Experiments

Four samples were studied in the present investigation: two natural quartz samples from Hoffman and two synthetic quartz samples from Sawyer. The Sawyer material was electrically swept (electrolyzed) at Sandia. Plano-convex resonators with deposited Au electrodes were fabricated and then mounted in hermetically sealed cans. The samples were heated in a tube furnace, and care was taken to stabilize the temperature before taking each Q measurement.

The simple apparatus used for the Q measurements is shown in Fig. 2.

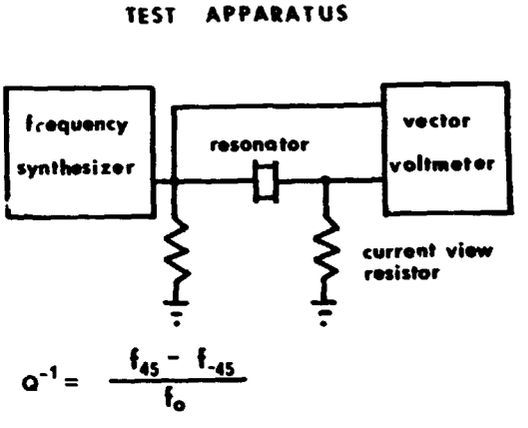

Fig. 2 Apparatus used for Q measurements

The output of a frequency sythesizer is used to excite the resonator and is simultaneously applied to the reference terminal of a vector voltmeter. Current flow through the resonator is monitored via a current viewing resistor, the voltage across which is applied to the signal input of the voltmeter. To ensure that the resonator is excited by a low impedance source, the output of the synthesizer is shunted by the resistor shown to the left of the resonator in the drawing. With this arrangement the voltmeter measures the complex admittance of the resonator. Provided that the resonance is sufficiently strong, the width (at the half power points) of the resonance is the difference of the frequencies f_{45} and f_{-45} where the current and voltage are $\pm 45^\circ$ out of phase.[3] For the resonators used in the present work, the resonances were somewhat weaker than expected under ideal conditions. Because of this, it proved impractical to measure Q values below about 5×10^4 readily, as doing so would have required a

point-by-point tracing out of the resonance circle in the complex admittance plane.[3]

All the data presented in this paper were obtained at the third overtone (f≈3 MHz) of the resonators. Resonator data are typically obtained at the fifth harmonic, but for the present devices the third harmonic exhibited a higher Q and a stronger resonance than did the fifth.

Results

Typical data showing the temperature-induced shift in resonance frequency for a θ = 34.0° rotated X-cut resonator at atmospheric pressure are shown in Fig. 3.

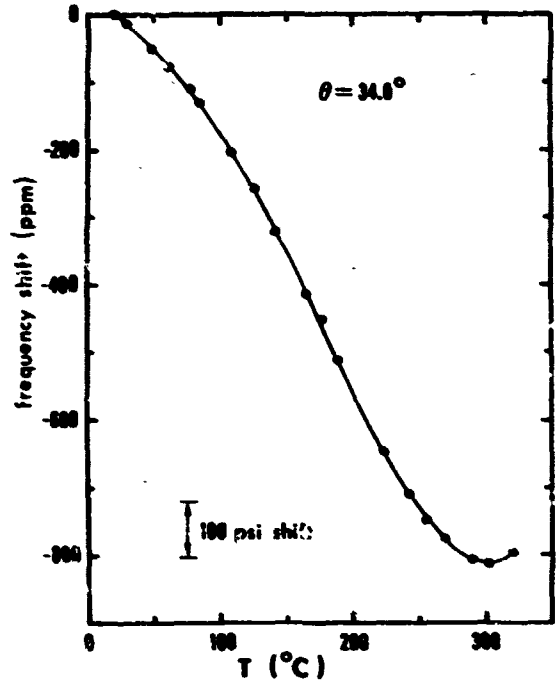

Fig. 3. Fractional change in resonant frequency vs. temperature for a (contoured) rotated X-cut resonator.

Also shown in this figure is the magnitude of the frequency shift produced by a pressure increase of 100 psi for an actual pressure gauge at 275°C.[1] For the resonator measured, the turnover point is at 300°C, compared to the value of 220°C expected from the data in Ref. 2. The shift in turnover point is believed due to the resonators in the present work being slightly contoured whereas the previous work pertains to flat plates.

Typical data for Q as a function of temperature are shown in Fig. 4. The quantity actually plotted is the loss Q^{-1} (on a logarithmic scale), as is conventional. The upper curve is for the natural (unswept) material. For this sample there is a loss peak at ∿ 70°C and a rapid increase of loss with temperature above 200°C. As mentioned above, it was not convenient with the simple apparatus utilized to measure values of Q much lower than 5 x 10^4. However it was observed that the loss did continue to increase with increasing temperature up to 300°C.

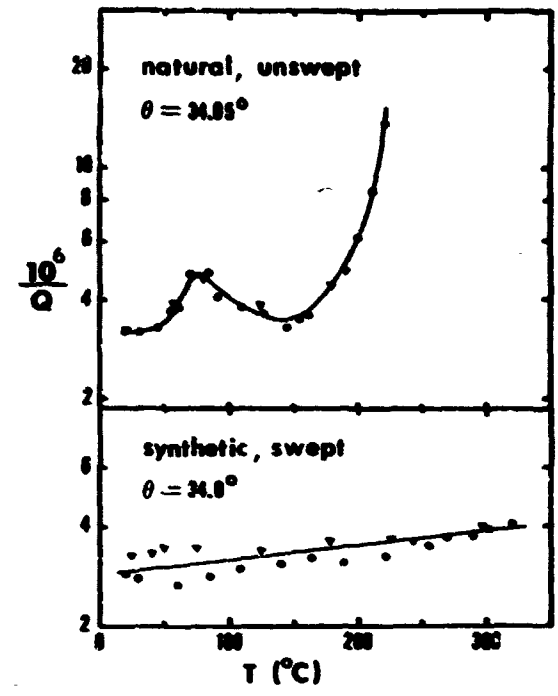

Fig. 4. Typical data for acoustic loss Q^{-1} up to 325°C. Data were taken at 3 MHz (3d harmonic).

Data obtained for a sample of synthetic swept quartz are shown in the bottom part of Fig. 4. The dramatic improvement due to the electrolytic purification is immediately apparent. Since the Q is more than 2.5 x 10^5 over the entire range of temperature, it appears that synthetic swept quartz is suitable for pressure gauge applications. Data obtained on the other sample of swept synthetic material are similar t those shown in Fig. 4. An important point to mention with regard to the present data is that the actual intrinsic Q of the swept synthetic material may be higher than the data indicate. This is because the resonators were plated and the resulting stresses may dominate the loss for high quality quartz. Previous workers have noticed this effect,[4] and for reliable measurements of Q ≥ 10^6 it is advisable to drive the resonator by capacitive coupling across a gap.

Discussion

It is of interest to compare the present results with those obtained in previous studies of resonator loss as a function of temperature. Most of the previous work in this area has been done on AT-cut thickness shear resonators. The extensive early work that was done has been reviewed by Fraser,[4] who discusses in detail the effects of impurities, radiation, and electrical sweeping on the temperature dependent acoustic loss. Nowick and Stanley[5] have given a group-theoretical analysis of dielectric and acoustic relaxation in quartz and have used the results to interpret data in the literature.

From symmetry considerations, Nowick and Stanley have argued that all pure shear mode deformations will couple to relaxational normal modes transforming according to the doubly degenerate E representation of the crystalline point group (D_3). Since the AT-cut thickness shear mode involves a pure shear deformation, and since the rotated X-cut thickness shear mode is very nearly a pure shear mode,[2] one would expect similar anelastic behavior for the two different orientations. Of course, the magnitudes of the anelastic

relaxations cannot be deduced from symmetry arguments. Nonetheless, it is not particularly surprizing that the data of Fig. 4 are somewhat similar to previously published data on AT-cut resonators fabricated from natural and swept-synthetic quartz.

The previous work[4,5] on anelastic loss in quartz resonators has led to a partial understanding of the relation between various impurities in the samples and the various loss peaks observed. Unfortunately, the behavior at low temperature is better understood than at high temperature. All quartz, natural or synthetic, contains a significant number ($\geq$ 5 ppm) of aluminum (Al^{3+}) impurities which substitute for silicon in the lattice. These defects are charge-compensated by alkali ions (Na^+, Li^+ or K^+) at interstitial positions adjacent to the Al. Compensation by protons is also possible. The motion of the interstitial ion among equivalent positions in response to the acoustic stress is an important mechanism for producing acoustic loss. Careful electrolytic sweeping can remove the alkali impurities, and it is believed that protons or, in certain cases, holes provide charge compensation of the Al^{3+}. Water may also be incorporated into the quartz lattice (eg during growth) by replacing a Si-O-Si bridge with two Si-O-H structures.

For natural quartz the rapid rise in loss above 200°C as seen in Fig. 4 is believed due to alkali diffusion in response to the applied stress. Removal of alkalis by electrolysis is necessary to reduce this source of loss. The loss peak shown at $\sim$ 70°C in Fig. 4 may be of the same origin as a similar peak observed in natural Brazilian opaline quartz and in fast Z-growth synthetic quartz.[4] It appears to be associated with OH bonds.

The data for synthetic quartz in Fig. 4 do not show any evidence of acoustic loss peaks. The previous work on AT-cut resonators has shown that loss peaks usually are observed, but that they are quite weak. It appears that the background loss due to electroding and mounting may have obscured any small loss peaks in the present measurements.

Conclusions

Two main conclusions may be drawn from the present work. The first is that the acoustical loss properties of rotated X-cut resonators appear similar to those of the widely studied AT-cut. Thus most past experience on AT-cut resonators may provide a valuable guide in designing devices using the rotated X-cut. The second conclusion is that electrolytically swept synthetic quartz appears to have sufficiently high Q for pressure gauge applications, whereas natural quartz is unsuitable for temperatures above $\sim$ 200°C.

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†A U. S. Department of Energy facility.

ASSESSMENT OF HIGH TEMPERATURE METALLIZATIONS FOR I^2L AND CMOS TECHNOLOGIES

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Introduction

As part of the Navy's high temperature electronics program, high temperature barrier metallizations were assessed and tested for I^2L and CMOS applications. Life tests were accelerated to 375°C in view of the -55°C to +300°C temperature range established for engine-located electronics without fuel cooling.

The gold-refractory metallizations evaluated were Au-TiW-PtSi, Au-TiW/TiO_2/TiW-PtSi and Au-TiW(N)-PtSi. These metallization systems were thermally annealed to at least 375°C for up to 250 hours. The critical requirement for stable diffusion barrier is the TiW grain size. Small grain (250Å-500Å) films were observed to be stable up to 375°C. Deposition to TiW diffusion barrier in the presence of oxygen and nitrogen also results in an effective diffusion barrier. Life tests at 340°C up to 100 hours have been completed.

AES profiles of the PtSi indicates some penetration by the TiW. In the case of PtSi/TiW interface, the redistribution of oxygen further passivates the system by forming a TiO_2 layer at the interface. Characterization of I^2L devices subjected to 340°C anneals will also be presented.

High Temperature Metallizations

The Au-TiW System

Previous investigations[1-3] on the interdiffusion and reliability of Au-refractory films used in devices have neglected "substrate" effects. It is recognized that the substrate can be a very active member of diffusion couples which may in many cases accelerate degradation observed in the gold conductor and refractory barrier.

In assessing the high temperature reliability of Au-Ti(W) films for high temperature applications, we compare the role that 3 different intervening layers on silicon substrates play in the stability of these metallizations. These layers are PtSi, SiO_2 and Si_3N_4. Each of the layers have, on occasion, been incorporated in MPTS. The Si_3N_4 is used for passivation and the PtSi layer is used as the ohmic contact.

Table I summarizes the deposition conditions, giving film thickness, sputter target, substrate temperature and film characteristics.

TABLE I

Deposition Conditions for Small Grain Size TiW Diffusion Barriers

Film Thickness	1200Å - 1800Å
RF Sputtered	$Ti_{0.3}W_{0.7}$ Target
Substrate Temperature	120°C
Resistivity of TiW	77 μ Ω-cm
Grain Size	250 - 750Å

The differences in the Ti(W) reaction with Si, SiO_2 and PtSi are shown in Figur 1. At 375°C there is no enhancement of the diffusion between Si and Ti(W). This

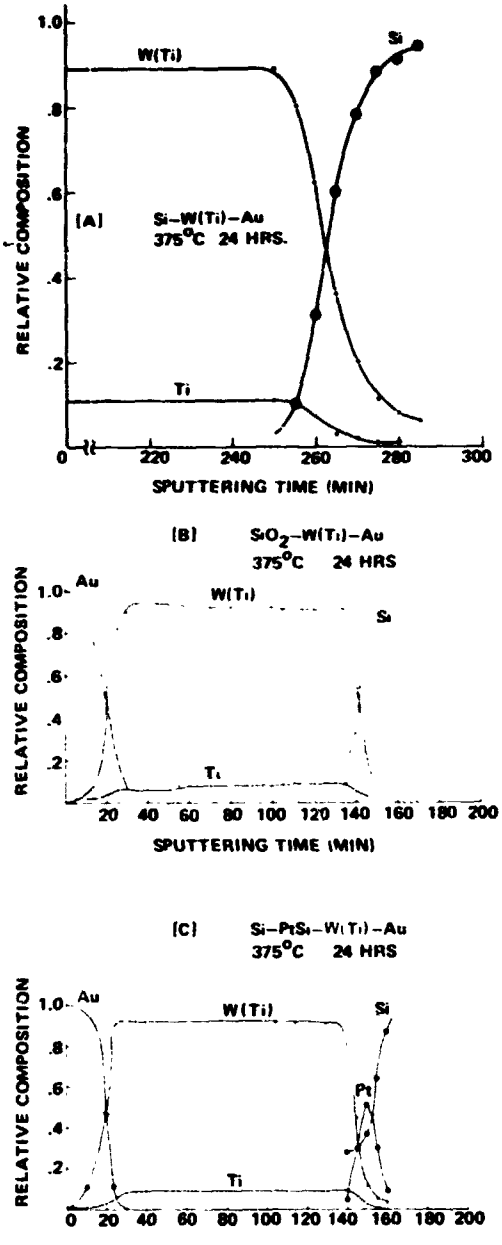

Figure 1. Diffusion profilesof the TiW diffusion barrier. (A) Silicon substrate, (B) SiO_2/Si substrate, (C) PtSi/Si

is as expected from the diffusivities of these systems which is of the order of 10^{-20} cm/sec. Likewise, the interdiffusion effects are minimal between SiO_2 and Ti(W) at this temperature. However, when the layer is PtSi, it acts as a source and sink for Silicon atoms resulting in the outdiffusion of Si into the refractory film. The amount of Si detected in the Ti(W) film is not satisfactorily explained from a solid solubility

argument. These results agree with our previous work with Ta on Si and PtSi and with Sinha's work with WSi_2 formation on PtSi-Si substrates. The excess silicon in the TiW will result in a refractory silicide formation at higher temperatures. Our conclusion, to date, is that the Au-TiW system with small grain TiW is stable up to 375°C.

The Oxide/Nitride Assisted Diffusion Barriers

The deposition of TiW in the presence of oxygen overpressure or nitrogen has been determined to improve the overall thermal stability of the TiW diffusion barrier. An overpressure of 10^{-3} Torr of oxygen or nitrogen was used in each case resulting in Titanium nitride passivation of the TiW grain boundaries.[4,5] Since the primary diffusion mechanism at temperatures below 500°C is grain boundary diffusion, the formation of TiN at the TiW grain boundaries inhibits significant grain boundaries up to 450°C. The Au-TiW(TiN)-PtSi system was found to be stable up to 450°C as shown in Table II, where the at. % Si and Au detected in the bulk of the TiW by energy dispersive x-ray analysis i summarized.

TABLE II

Evaluation of the TiW(TiN) Diffusion Barrier up to 450°C

Anneal Temperature (100 hrs)	at. % Si Detected in TiW(TiN)	at. % Au Detected in TiW(TiN)
300°C	ND	ND
340°C	1.1	1.0
350°C	1.8	2.0
400°C	2.5	3.0
450°C	4.2	6.5

However, at 450°C, the significant observation is that Silicon was not observed in the Au overlayer thus showing the overall stability of TiW(TiN) as a diffusion barrier.

I^2L Test Elements With Au-TiW Metallizations

As part of the Navy's High Temperature Electronics a custom I^2L metallization test mask set has been processed using the Au-TiW-PtSi system. The test mask includes a number of different test elements which are aimed at determining design constraints on ohmic contacts, metal width and spacing. Also included are symmetrical cell I^2L logic gates and ring oscillators. The initial test results look promising in that 2 of 6 (8%) of the oscillators failed within 275 hours. A total of six oscillators have now reached 580 hours with no failures. These tests are continuing and additional refinements to the metallization will be incorporated in the I^2L devices to be processed in the future.

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AMORPHOUS METALLIZATIONS FOR HIGH-TEMPERATURE SEMICONDUCTOR DEVICE APPLICATIONS

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Abstract - In this paper we present the initial results of work on a new class of semiconductor metallizations which appear to hold great promise as primary metallizations and diffusion barriers for high-temperature device applications. These metallizations consist of sputter-deposited films of high-T_g amorphous-metal alloys which (primarily because of the absence of grain boundaries) exhibit exceptionally good corrosion-resistance and low diffusion coefficients. Amorphous films of the alloys Ni-Nb, Ni-Mo, W-Si, and Mo-Si have been deposited on Si, GaAs, GaP, and various insulating substrates. The films adhere extremely well to the substrates and remain amorphous during thermal cycling to at least 500°C. Rutherford Backscattering (RBS) and Auger Electron Spectroscopy (AES) measurements indicate atomic diffussivities in the 10^{-19} cm^2/S range at 450°C.

INTRODUCTION

One of the most difficult problems associated with the design of semiconductor devices intended for high-temperature operation is that of finding a suitable metallization system for providing contacts to the semiconductor. Typical difficulties which limit the lifetime of semiconductor devices at high temperature include: (1) altered electrical behavior caused by interdiffusion of metal and semiconductor; (2) dimensional changes or embrittlement caused by compound formation, or grain-growth; and (3) catastrophic metallization failure due to electromigration. These must be considered as *intrinsic* failure modes in the sense that, while they may vary in absolute and relative importance from one system to another, they must always be present to some extent. Furthermore, all of these failure modes involve diffusive transport within and/or among the metal and semiconductor layers, and increase roughly exponentially with increasing temperature. The design of high-temperature metallizations, therefore, necessarily involves a search for means to impede atomic diffusion within the metal-semiconductor system. The most common approach to the problem of limiting diffusion between dissimilar materials involves the use of intervening metallization layers which are intended to act as diffusion barriers. A well-known example is provided by the Ti-Pt-Au metallization which is used in the "Beam-Lead" technology [1,2]. This metallization (on Si) has survived brief stress-tests at over 400°C, but degrades rapidly at all temperatures above 350°C [2]. Similar results are obtained with many other diffusion barriers [3]. The reason for the failure of conventional passive diffusion barriers is simple, but has only recently become well-recognized: Diffusive transport in polycrystalline thin-films is dominated by diffusion along grain boundaries and dislocations at all realistic operating temperatures [4]. The barrier layer cannot be fully effective if it is, itself, a thin, polycrystalline film. Nicolet has recently given a comprehensive review of thin-film diffusion barriers [3], in which the importance of grain-boundary diffusion is highlighted. In addition to reviewing the shortcomings of traditional diffusion barriers, Nicolet discusses more sophisticated concepts including "stuffed barriers" (in which the grain boundary paths are blocked by suitable impurities) and "thermodynamically stable" barriers (which utilize stoichiometric compound barriers such as transition metal nitrides or borides). In the present paper, we present an alternative approach to the design of high-temperature metallizations. We propose the use of sputtered *amorphous* metal films, either as primary metallizations, or as thin diffusion-barrier layers between conventional polycrystalline films.

Amorphous metallizations are easily produced by sputtering from various transition-metal and transition-metal/metalloid alloys. As noted above, most of the inherent reliability problems of conventional metallizations are associated with polycrystallinity and atomic motion. In amorphous metals, there are no grain boundaries or dislocations, and diffusive transport is thus determined by bulk diffusion coefficients [5,6]. As a consequence, diffusive transport in amorphous metal films can be orders of magnitude slower than in polycrystalline films of comparable composition. It is primarily for this reason that we believe amorphous metal films constitute an interesting new class of materials for semiconductor metallization applications.

EXPERIMENTAL

Materials Selection

If amorphous films are to be useful in the proposed applications, it is necessary that they remain amorphous at the desired operating temperatures. Typically, the time constant for crystallization is of the order of $\leq$ 1 hour at the glass transition temperature, T_g, and extrapolates to several years at $T \leq 0.85\ T_g$ [5,6]. We have therefore focused on alloys having known or predicted T_g values of $\geq$ 500°C. Donald and Davies [7] have discussed various factors which promote glass-forming ability and high T_g values, and have published several useful tables of known glass-forming compositions. After consideration of the factors discussed by these authors, we selected the Ni-Nb, Ni-Mo, Mo-Si, and W-Si systems for investigation. A full discussion of our selection criteria has been given elsewhere [8].

The substrate requirements for successful vapor deposition of amorphous metals are easily satisfied by almost any crystalline or amorphous solid. The main requirement is that the substrate surface remain at a temperature well below T_g during deposition. This, in turn, requires that the substrate have a thermal conductivity adequate for rapid transfer of the heat-of-condensation to a heat sink. The fact that amorphous metals have been deposited successfully on such notably poor thermal conductors as pyrex (σ ~ 0.01 watts/cm°K) leaves little doubt that all common semiconductors ($\sigma \geq$ 0.1 watts/cm°K) will provide adequate heat-sinking and be useable as substrates. Most of the work reported here was done using single-crystal Si substrates, although fully amorphous films have also been obtained on GaAs, GaP, Al_2O_3, glass, mica, Cu, and Al substrates.

Film Preparation

Amorphous metal films were deposited by RF sputtering using a Varian 980 diffusion-pumped sputtering system. This system uses a split circular cathode, 9" in diameter, with a 3 1/2" cathode-to-substrate spacing. In order to sputter alloys of uniform composition, 1/4" thick base cathodes of either Ni or Si were partially covered by 10 mil foil masks of Nb, Mo, or W, having uniform distributions of holes to expose an appropriate fraction of the base cathode. In initial work, the exposed areas of base-cathode and foil were approximately equal. For each of the four alloy-systems studied, the area ratios were subsequently ad-

justed to achieve the desired film composition using feedback from annealing studies and electron-beam microprobe measurements.

Sputtering was done using $\geq 2 \times 10^{-4}$ Torr Ar pressure at a total RF power of $\leq$1kW. Under these conditions the deposition rate was typically $\approx$ 300°A/min. In order to provide a deposit which was sufficiently thick for X-Ray diffraction and electron microprobe measurements, a standard sputtering time of 30.0 min. was used. Thus, most of our films were approximately 1 μm thick. Compositional uniformity was found to be typically ±0.5 At% over a 1/4" × 3/4" sample area.

Routine Characterization

The as-deposited films were routinely characterized as to adhesion, film-thickness (stylus measurements), composition (electron beam microprobe measurements), structural order (X-Ray diffraction measurements) and electrical resistivity (4-point probe measurements). For semiconductor metallization applications, the adhesion and resistivity results are of particular interest: We find that the films adhere extremely well to the semiconductor substrates and are very resistant to scratching. No flaking or wrinkling was observed on any of these films in the as-deposited state, nor after thermal cycling between -200 and +500°C. SEM examination shows the surfaces to be smooth and featureless. Typical room-temperature resistivity values obtained for the as-deposited films are as follows:

Alloy	Composition	ρ(μΩcm)	R_s (Ω/□)
Ni-Nb	55-60 At%Ni	200-230	2.0-2.3
Ni-Mo	55 At% Ni	110-130	1.1-1.3
Mo-Si	60 At% Mo	160-200	1.6-2.0
W-Si	90 At% W	140-150	1.4-1.5

The sheet resistance values given in Col. 4 are scaled to a film thickness of 1μ. As expected, the resistivities of the amorphous films are somewhat higher than the resistivities of corresponding polycrystalline films (typically a factor of ~5 higher), but sheet resistances of the order of 1 Ω/□ are perfectly acceptable for many device applications. For those applications in which these resistivities are excessive, it may be possible to overcoat the amorphous metal with a layer of Au or Cu to provide a lower-resistance metallization.

Annealing and Crystallization

As the crystallization of amorphous metals is controlled by kinetic factors, any experimental value of the crystallization temperature, T_c, depends on the time-scale of the experiment. Fortunately, the characteristic time for crystallization is an extremely strong function of temperature, so that reasonable estimates of the maximum "operating temperatures" of amorphous metallizations can be obtained using relatively brief anneals. The results reported here were obtained by annealing the samples for one hour in evacuated quartz ampoules which also contained a small slug of Ti for gettering.

In order to determine the one-hour crystallization temperature of a given alloy composition, the following sequence was followed: The first anneal was performed at 400°C, after which the sample was removed from its ampoule for examination by X-Ray Diffraction (XRD). If there was evidence of crystallinity, the sputter-mask was altered to achieve a different alloy composition. (Crystallization temperatures below 400°C are of no interest at the present time). If there was no evidence of crystallization, the same sample was resealed in an ampoule and annealed at 500°C for 1 hour. This procedure was repeated at 100° increments until crystallization was detected. A new sample from the same batch was then annealed at the penultimate temperature, measured for crystallinity, and reannealed at successively higher temperatures using 50°C increments. Finally, a third sample was used to find T_c to within 25°C.

Figure 1 shows a sequence of typical XRD scans for initially amorphous Ni-Mo films (~65% Ni). It is somewhat difficult to judge whether or not small features on the amorphous peak correspond to the early stages of crystallization. Massive crystallization, however, is unmistakably evidenced by the appearance of numerous sharp diffraction peaks. These comments are illustrated in Fig. 1 by the 600°C and 650°C traces: After annealing at 600°C, small bumps are seen at $2\theta \approx 39°$ and 45°. These features are reproducible, and apparently indicate a small volume-fraction of crystallites in an amorphous matrix. After the 650°C anneal, the 39° peak is quite strong, but the 45° peak is either missing or

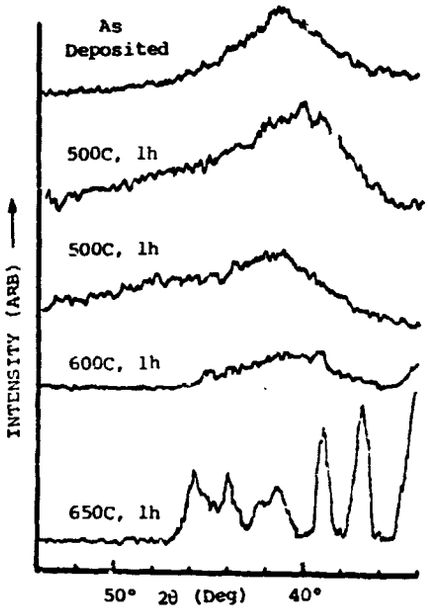

Figure 1. X-Ray Diffractometer scans of an initially amorphous film of Ni-Mo after 1h anneals at successively higher temperatures.

split into several peaks. It appears likely that the path of crystallization in the Ni-Mo system is complex, involving intermediate phases. Similar effects are seen in the other alloys as well. TEM investigations are planned for exploration of the crystallization mechanisms.

The results of the annealing studies to date are as follows:

Alloy	Composition	T_0 (°C)	T_1 (°C)
1) Ni-Nb	55 At% Ni	500	550
2) Ni-Nb	57 At% Ni	575	600
3) Ni-Mo	55 At% Ni	525	550
4) Ni-Mo	65 At% Ni	550	600
5) Mo-Si	60 At% Mo	550	600
6) W-Si	90 At% W	(Partially crystalline as deposited)	

The temperature T_0 is the highest 1-hour annealing temperature at which no evidence of crystallinity has been observed. T_1 is the lowest 1-hour annealing temperature at which some evidence of crystallinity has been observed. The W-Si alloys deposited to date have contained a small volume-fraction of microcrystalline phase in a predominantly amorphous matrix. Further re-

finement of the composition is required. Nevertheless as will be shown in the next section, the largely amorphous W-Si films still function as effective diffusion barriers.

Diffusion

The diffusion of Au in amorphous metal films is of great practical interest because Au is widely used in multilayer metallizations and bonding wires for semiconductor devices. Au is also a prime candidate for use as an overlayer to reduce metallization resistances.

Au was ion-implanted into an amorphous Ni-Nb film which was subsequently annealed and measured by Rutherford Backscattering (RBS) to monitor any Au diffusion [9]. The amorphous film was deposited on a single-crystal Si substrate to a thickness of 1μ, and was composed of 56.5 At% Ni, 43.5 At% Nb. The implanted Au profile was Gaussian, with a peak concentration of 3.3 × 10^{20} cm^{-3} occurring ~400Å below the surface, and a "full width at half maximum" of 300Å. Since a Gaussian profile remains Gaussian during diffusion, it is straightforward to deduce diffusion coefficients from the half-widths of fitted Gaussian curves. Figure 2 shows a comparison of the Au profiles after 0.5 hours

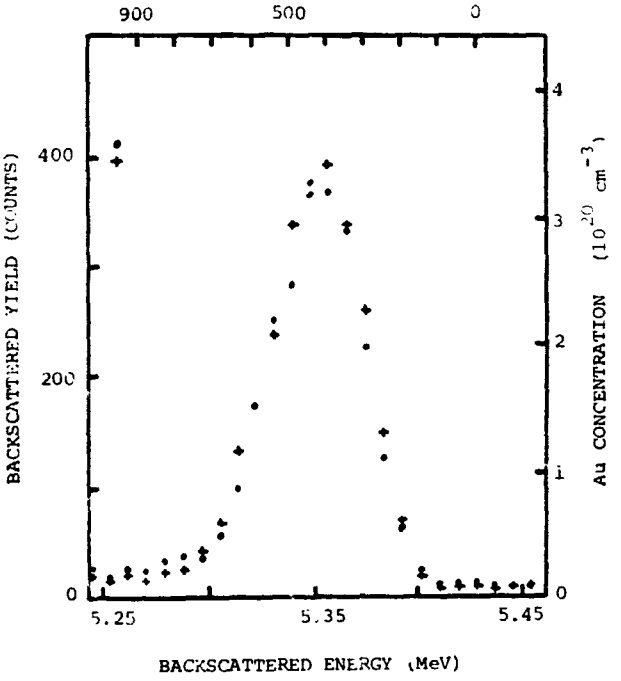

Figure 2. Comparison of the ion-implanted Au profiles after anneals of 30 minutes and 35 hours at 450°C, illustrating the extremely low rate of diffusion of Au in amorphous Ni-Nb at this temperature. The profile change can only be discerned by fitting Gaussian curves to the data.

and 35 hours of annealing at 450°C. Analysis of these and similar profiles obtained for longer annealing times gives a diffussivity of D ≈ 8 $10^{-19}$$cm^2$/sec for Au in this alloy at 450°C. Note that: (1) D ≤ 10^{-18} cm^2/s implies that an Au atom would require roughly 300 years to diffuse a distance of 1μ; and (2) the annealing temperature of 450°C is very near the estimated glass-transition temperature for this film: The one-hour crystallization temperature for films of this composition is in the neighborhood of T_c ≈ 550°C, and T_g must be ≤ T_c. Thus, our anneal temperature of 450°C is ≥.88 T_g. Rutherford Backscattering studies of interdiffusion between amorphous metal films and overlayers of Cu or Au, and between amorphous metal films and semiconducting substrates are currently underway, and no quantitative results can be reported at this time.

In addition to the RBS measurements, we have used Auger Electron Spectroscopy (AES), together with Ar-ion sputtering to study interdiffusion. Figure 3 shows a series of AES profiles for an amorphous Ni-Nb film on which a ~750Å Cu layer was deposited. After 10 hours of annealing at 500°C, there was a slight broadening of the Cu/Ni-Nb interface, but no large-scale interdiffusion. After one hour at 600°C, however, the Cu,Ni, and Nb have thoroughly interdiffused, and the "interface" has moved very deeply (≥ 2000Å) into the Ni-Nb film. Other Ni-Nb films of the same composition were found to crystallize in one hour at 575°C. It is therefore clear that crystallization is responsible for the sudden, massive motion of Cu into the Ni-Nb (probably along grain boundaries). Similar results have been obtained with Au overlayers and with other amorphous alloys. It is interesting to note that we found essentially no interdiffusion between Au and amorphous W-Si despite the fact that the W-Si contained a detectable (but small) volume-fraction of microcrystalline phase. Thus, we believe that partially crystalline films can still function as effective diffusion barriers as long as the crystallites are well-separated by an amorphous matrix.

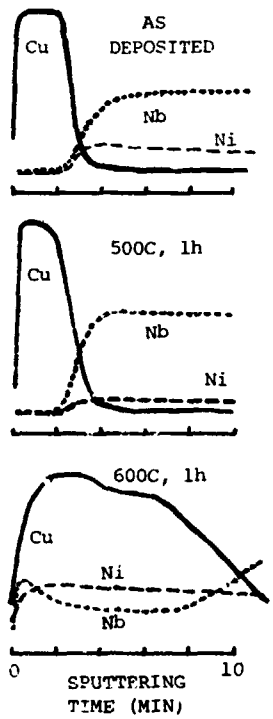

Figure 3. AES depth-profiles of Cu, Ni, and Nb. The top trace shows the as-deposited structure: A Cu layer on amorphous Ni-Nb. The middle trace shows that there was very little interdiffusion after 10 hours of annealing at 500°C. The bottom trace shows considerable interdiffusion after only 1 hour at 600°C. The rapid interdiffusion at 600°C is a consequence of crystallization.

CONCLUSIONS

Amorphous metal films of appropriate compositions can be deposited on semiconducting and insulating substrates, and remain amorphous after one-hour anneals at temperatures in excess of 500°C. It is very important to note that the annealing temperatures used in this

study were specifically chosen to find the temperature ranges in which the alloys under investigation would crystallize on a time-scale of one hour ($T \geq 0.9T_g$). At slightly lower temperatures, crystallization will not be observable on any reasonable laboratory time-scale. Our results also show that, as long as the films remain amorphous, they exhibit exceptionally low diffusivities. Indeed, the W-Si results show that films containing a small volume-fraction of microcrystallinity can still function as effective diffusion barriers. This observation is consistent with our basic working hypothesis that the advantages of amorphous metallizations stem from the absence of grain boundaries: As long as the volume-fraction of microcrystallinity is small, the crystallites will be separated by an amorphous matrix, preventing an interconnected network of grain boundaries. At some critical volume-fraction (which can be estimated from percolation-theory to be about 0.3 [10]), the crystallites will merge, and an essentially polycrystalline film will result. Based on the work reported here, we conclude that films of high-T_g amorphous metal alloys are indeed viable candidates for use as high-temperature metallizations for semiconductor devices. We anticipate that this new class of semiconductor metallizations will find important applications as primary metallizations, interlayer diffusion barriers, and corrosion-resistant overlayers.

ACKNOWLEDGEMENTS

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OHMIC CONTACTS TO GaAs FOR HIGH-TEMPERATURE DEVICE APPLICATIONS

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Summary

Ohmic contacts to n-type GaAs have been developed for high-temperature device applications up to 300°C. Refractory metallizations were used with epitaxial Ge layers to form the contacts: TiW/Ge/GaAs, Ta/Ge/GaAs, Mo/Ge/GaAs, and Ni/Ge/GaAs. Contacts with high dose Si or Se ion implantation (10^{12} to 10^{14}/cm^2) of the Ge/GaAs interface were also investigated. The purpose of this work was to develop refractory ohmic contacts with low specific contact resistance (~10^{-6} Ω-cm^2 on $1x10^{17}$/cm^3 GaAs) which are free of imperfections, resulting in a uniform N^+ doping layer.

The contacts were fabricated on epitaxial GaAs layers (n=$2x10^{16}$ to $2x10^{17}$/cm^3, grown on N^+ ($2x10^{18}$/cm^3) or semi-insulating GaAs substrates. Ohmic contact was formed by both thermal annealing (at temperatures up to 700°C) and laser annealing (pulsed Ruby). Examination of the Ge/GaAs interface revealed Ge migration into GaAs to form an N^+ doping layer.

Under optimum laser anneal conditions, the specific contact resistance was in the range 1-5x10^{-6} Ω-cm^2 (on $2x10^{17}$/cm^3 GaAs). This is an order of magnitude improvement over thermally annealed Ag/Si[1] or Ni/Ge[2] contacts. Thermally annealed TiW/Ge had a contact resistivity of 1x10^{-6} Ωcm^2 on $1x10^{17}$/cm^3 GaAs under optimum anneal conditions. The contacts also showed improved thermal stability over conventional Ni/AuGe contacts at temperatures above 300°C. The contact resistivity of thermally annealed TiW/Ge does not increase appreciably with a 350°C, 190 hr anneal, while that of Ni/AuGe degrades appreciably between 25-35 hrs at 350°C. Under bias conditions (6V, 15 mA) the contact resistance of these contacts did not increase appreciably at 300°C after 160 hr. Preliminary results with the laser annealed contacts showed no measurable increase in resistance after 6 hr at 350°C.

Introduction

Low specific contact resistance ohmic contacts to n-type GaAs using epitaxial Ge films have been reported using molecular beam epitaxy[3] and vacuum epitaxy.[2,4] The epitaxial Ge film allows (in theory) the formation of contacts with a uniform N^+ layer, in the highly doped Ge film itself[3] or, from Ge doping of the GaAs.[2,4] These contacts should be more nearly free of imperfections compared to polycrystalline Ge or AuGe eutectic films in which rapid impurity diffusion occurs at grain boundaries. Both thermal annealing and laser annealing have been used to form ohmic contact. Laser annealing was used to form these contacts[5] because when a refractory metal overlayer is desired it was found[2,4] that oven anneal temperatures in the range 500-750°C were required. Subjecting the entire substrate to these high temperatures can have deleterious effects on the active and semi-insulating GaAs layers and to other metallizations previously deposited on the chip, e.g., for the purpose of fabricating integrated circuits. This problem can be obviated by selective contact annealing with a laser beam. Pulsed laser annealing may also be important in obtaining enhanced activation of implanted dopants and in obtaining certain doping profiles when rapid heating and cooling are important.

In this paper we report on TiW (88 wt. % W, 12 wt. % Ti)/Ge, Ta/Ge, Mo/Ge, and Ni/Ge ohmic contacts to n-type GaAs which have two possible areas of applications: 1) to devices which are designed to operate for extended periods of time in a high temperature ambient (above 150°C)[1], and 2) to improve the reliability of devices which experience high channel or contact temperatures, such as power field-effect transistors (FET) and transferred-electron devices (TED).[6] In both cases, local melting at imperfections in the contacts can result in device failure. Formation of an N^+ layer at the GaAs-contact interface by Ge doping can also result in significant performance gains in power FETs and TEDs through reduction in contact resistance and increased voltage levels.

Experimental Method and Results

Fabrication of the ohmic contacts was similar to that described previously.[2] A number of different types of contacts were investigated: TiW/Ge, Ta/Ge, Mo/Ge, and Ni/Ge, both with and without a high dose of Si or Se ion implanted (I^2) at the Ge/GaAs interface. Ohmic contacts were fabricated on n-type epitaxial GaAs layers with carrier a concentration of $2x10^{17}$/cm^3 grown on N^+ (100) oriented GaAs substrates doped to $2x10^{18}$/cm^3 or on GaAs epitaxial layers (n=$1x10^{17}$/cm^3, 2000Å thick) grown on semi-insulating (SI) GaAs substrates. To prepare the GaAs surface for growth of the epitaxial Ge layer, the surface was cleaned in organic solvents, etched in a solution (10 mℓ HCℓ, 10 mℓ HF, 40 mℓ H_2O, 6 drops of H_2O_2) to remove carbon and oxygen, and placed immediately into a high vacuum system. Oxides were desorbed by heating the substrate to 575°C for 15 min in a vacuum of $2x10^{-7}$ Torr. Oxide desorption was carried out at 575°C because it was found[4] by Auger electron spectroscopy (AES) that the oxide concentration was at a minimum at this temperature without greatly changing the GaAs stoichiometry. An epitaxial Ge layer was then grown in the same vacuum at 425°C to thicknesses between 200 to 2000Å by electron beam evaporation from pure Ge source. For contacts on N^+ substrates, circular Ge contact patterns (30 to 250 μm in diameter) were formed by etching and the metal overlayers were deposited to thicknesses between 1000 to 2000Å (by electron beam evaporation in the case of Ta, Mo, and Ni; and by sputtering in the case of TiW). Isolated circular contact patterns were defined using photoresist and lifting or by performing the deposition through a metal mask. Ohmic contact to the N^+ backside was made with AuGe/Ni, alloyed at 450°C for 15 sec prior to fabrication of the frontside contacts. Typical contacts are shown in Fig. 1. In the case of TiW/Ge/I^2 Si contacts to the GaAs epitaxial layer on SI substrates, transmission line model (TLM) contacts were formed by etching the mesa, TiW, and Ge in three separate etching steps.

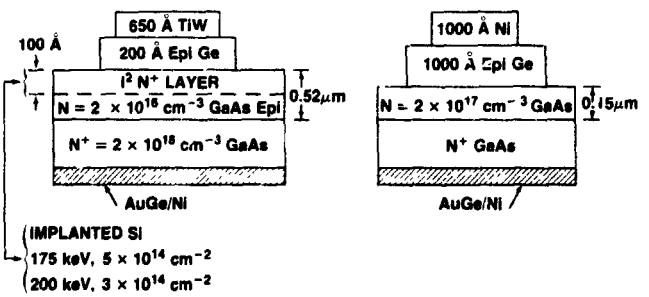

Fig. 1. Schematic cross sections of typical refractory metal/Ge ohmic contacts to GaAs.

Thermal annealing of the TiW/Ge/I^2Si contacts (1500Å TiW/400Å Ge/I^2Si at 60keV, $2x10^{14}/cm^2$) was carried out in forming gas at 700°C. Near optimum annealing conditions of 25 min, the specific contact resistance was $1x10^{-6}\ \Omega cm^2$ as measured by the TLM method.[8] Auger electron spectroscopy (AES) sputter profiles, as deposited and after sintering in vacuum, are shown in Fig. 2. After sintering, Ge migration into GaAs was observed indicating an N^+ doping layer at the GaAs surface. This condition is necessary for a low specific contact resistance.[9] The Si implant may also have been partially activated resulting in a further increase in the concentration of the N^+ doping layer. After 25 min at 700°C, Ga outdiffusion was also observed, allowing vacant sites for Ge or Si doping atoms.

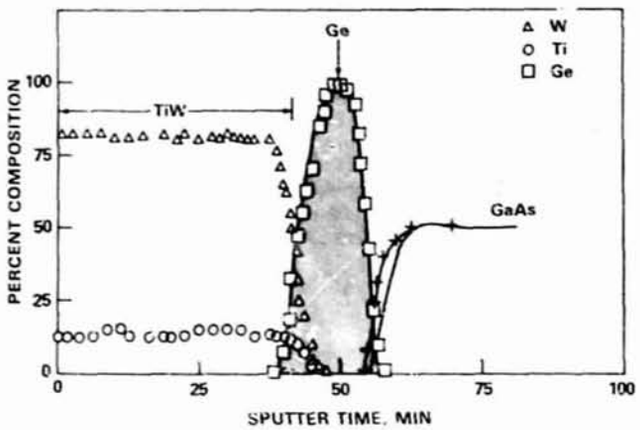

Fig. 2. AES sputter profile of TiW/Ge/GaAs contact, (a) as deposited and (b) after ohmic contact formation at 700°C for 15 min at 10^{-9} Torr.

Laser annealing was performed with a ruby laser which emitted a one joule, 22 ns pulse obtained by Q-switching the cavity with a Pockel's cell. Experiments were performed both in single TEM_{00} mode and in multimode operation. The single mode was used for the small diameter ohmic contact experiments while the multimode was employed for large area AES analyses. For the TEM_{00} mode case, a 0.8 mm circular aperture was placed in the optical cavity. The output beam was then focused to form a 260 μm diameter spot at the sample. A 30 to 50 μm diameter spot, which contained only the center of the Gaussian beam, was obtained by use of a metal mask. Ohmic contacts were obtained at energy densities between 0.09 to 5 J/cm^2, depending on the type of contact. For the multimode case, the full one joule output was homogenized by a method similar to that described by Cullis, et al.[7] by sending it through a 1.2 cm diameter fused quartz optical wave guide which was bent and tapered to obtain a spot diameter at the sample of 0.7 cm. Although this "light guide diffuser" was effective in homogenization of the multimode structure of the beam and reducing speckle patterns, "hot spots" were still observd at the output (particularly apparent on GaAs surfaces). A detailed analysis of the appearance of hot spots will be published later.

Current/voltage (I/V) characteristics of a typical Ni/Ge contact before and after laser annealing are shown in Fig. 3 as displayed on a curve tracer. Before laser annealing the contacts were reasonably well behaved Schottky barriers; the upper curve shows a reverse breakdown voltage of about 5 volts on $2x10^{17}/cm^3$ doped GaAs. After a pulse of 0.04 J/cm^2 the rectification softens, indicating some very limited melting, perhaps associated with preferentially absorbing imperfections on the top surface. At 0.14 J/cm^2 the contact was ohmic and the photomicrograph of this contact, shown in Fig. 3, indicated very shallow, uniform melting had occurred. Similar results were found with TiW/Ge, Mo/Ge, and Ta/Ge contacts

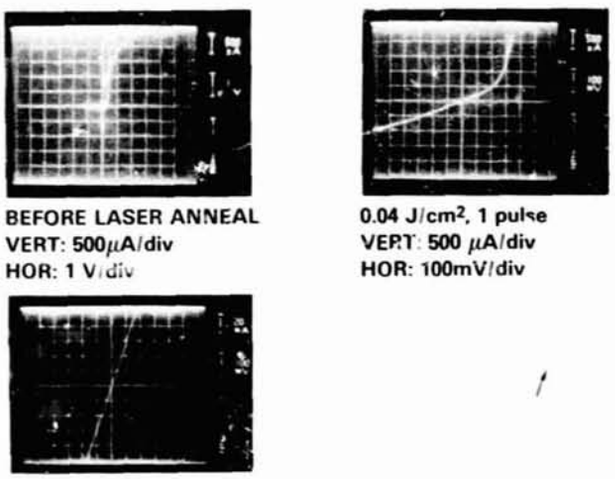

Fig. 3. Curve tracer I/V curves of Ni/Ge/GaAs contacts before laser annealing and after laser annealing at 0.04 J/cm^2 (soft Schottky barrier) and 0.14 J/cm^2 (sufficient energy density to form ohmic contact). Photomicrograph of ohmic contact after 0.14 J/cm^2.

Experimental curves of the specific contact resistance versus laser energy density are shown in Fig. 4. Measurements were made with a method similar to that of Cox and Strack.[10] These results were obtained using the TEM_{00} mode with a 30 to 50 μm diameter metal mask over (typically) 250 μm diameter isolated contacts. Approximate melting points for each of the contact types are shown at the top, as determined from photomicrographs of the irradiated surfaces. However, the melting points could not be determined precisely from the photomicrographs and very shallow melting probably occurred below these points. It was found that the contact resistivity was at a minimum near the melting point for Ni/Ge and Ta/Ge contacts. Similar TiW/Ge ohmic contacts formed on $n=2x10^{16}/cm^3$ GaAs epitaxial layers resulted in a specific contact resistance of $1x10^{-5}\ \Omega cm^2$. The higher value of specific contact resistance evidently resulted from the lower doping in the GaAs. Similarly, contact resistivity values for Ta/Ge, Mo/Ge, and Ni/Ge were approximately an order of magnitude higher on $2x10^{16}/cm^3$ as compared to $2x10^{17}/cm^3$ GaAs.

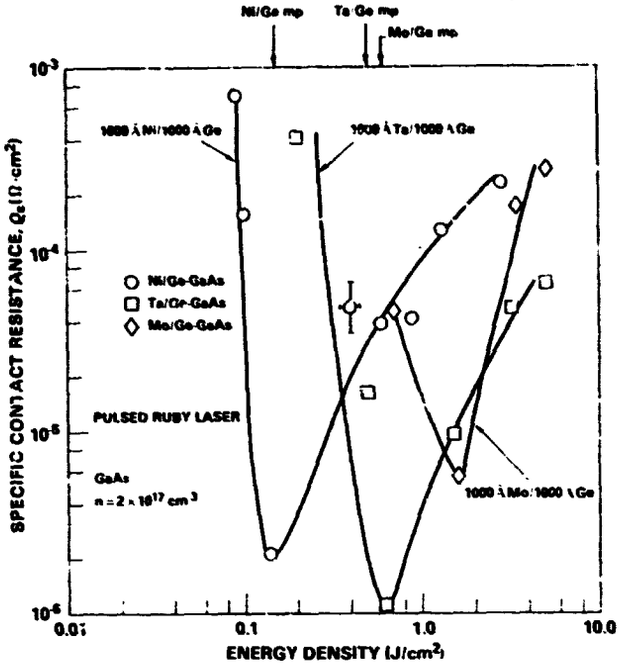

Fig. 4. Experimental values of specific contact resistance as a function pulsed ruby laser energy density; mp indicates approximate melting points as determined from surface photomicrographs.

The interfaces before and after laser annealing were investigated using AES sputter profiling techniques. Figure 5 shows AES sputter profiles of a Ni/Ge contact before laser annealing and after laser annealing at an energy density just high enough to form ohmic contact. A multimode 7 mm diameter beam was used to irradiate a GaAs sample approximately 10 mm x 10 mm containing 2000Å Ni and 2000Å Ge prepared as discussed above. At 0.10 J/cm^2 slight melting patterns could just be observed, indicating melting of the Ni and Ge just to, and including, the GaAs surface. This energy density corresponded to the threshold for ohmic contact formation. Even at this low energy density there was Ge migration into the GaAs, enough to greatly increase the n-type doping concentration at the GaAs surface. Similar profiles were observed with Ta/Ge laser annealed contacts. These profiles are also typical of Ni/Ge thermal annealed ohmic contacts studied previously.[2]

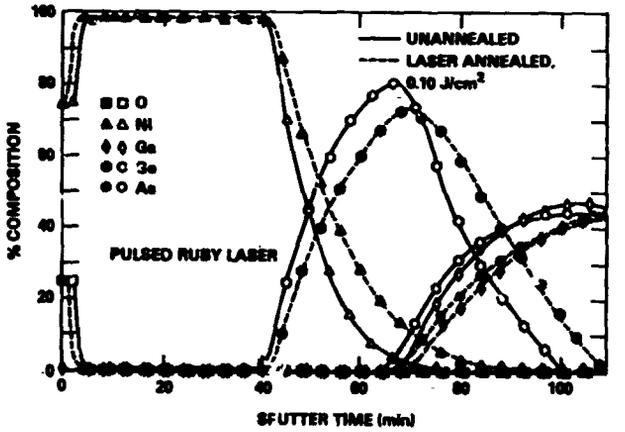

Fig. 5. AES sputter profiles of a 2000Å Ni/2000Å Ge/GaAs contact before laser annealing and after laser annealing at 0.10 J/cm^2, just at threshold for ohmic contact formation.

Discussion of Laser Anneal Results

The curves of specific contact resistance versus energy density, shown in Fig. 4, indicate there is a "window" in energy density which is appropriate for the formation of ohmic contact. This window depends on the layer thicknesses of the metal and epitaxial Ge, the pulse duration, to some extent on the surface morphology, and also on the fundamental interactions[1] of the laser beam with the overlayers and GaAs. The depth of melting and surface temperature are determined in part by the absorption coefficient, specific heat, and thermal diffusivity of the overlayers and GaAs surface. Ohmic contact appeared to occur just at the threshold of melting, but the melting must be deep enough to melt at least the top 50 to 100Å of the GaAs surface to account for the AES profiles in Fig. 5. Solid-state diffusion processes are too slow to account for these profiles. Since the heating and cooling rates are nearly the same in pulse laser annealing dominated by thermal processes,[11] the Ge migration into the GaAs surface must occur in the 50-100 ns that the surface layers are molten. A minimum in the specific contact resistance apparently occurs just above the melting point at an optimum doping level and profile. It is assumed that low contact resistance occurs by electrons tunneling between the top metal layer and the highly doped surface layer in the GaAs.[9] The specific contact resistance begins to rise at higher energy densities as the melt penetration becomes deeper and the surface temperature reaches the boiling point. Surface evaporation and ablation can then result in loss of Ge and As (as well as loss of part of the metal contact), as has been observed with these contacts at high energy densities by electron microprobe x-ray analysis. This was found to result in an increase in the specific contact resistance.

The advantages of laser annealing over thermal annealing for these particular high-temperature contacts is seen in comparison with thermal annealing results. For similar ohmic contacts, the specific contact resistance was more than an order of magnitude higher when thermally annealed[2] and high ambient temperatures (up to 650°C for 5 min) were required. The laser annealed contacts reported here also demonstrate an order of magnitude improvement in contact resistivity over Ag/Si contacts[1] thermally annealed. These contacts also compare favorably with conventional AuGe ohmic contacts, for which a specific contact resistance of 1×10^{-6} Ωcm^2 can be routinely obtained, but which degrade significantly at 350°C.

High-Temperature Aging

The TiW/Ge/I^{2}Si ohmic contacts formed on GaAs epitaxial layers on SI substrates and thermally annealed were studied by high tempeature aging in an ambient of forming gas. Figure 6 shows the change in the specific contact resistance after exposure to temperatures between 350 to 500°C for over 175 hours. The behavior of a typical AuGe/Ni contact, included in the 350°C experiments, is shown for comparison. These results demonstrate the high-temperature reliability advantages of refractory metal/epitaxial Ge ohmic contacts. With these contacts it was found that the contact resistance did not increase appreciably up to 190 hours at 350°C, while that of AuGe significantly increased between 25-35 hours at 350°C.

Preliminary high-temperature aging experiments with the laser annealed ohmic contacts (TiW/Ge/I^{2}Si, Ni/Ge/I^{2}Si, Ni/Ge, Ta/Ge, and Mo/Ge) were also carried out by aging in vacuum at 10^{-4} Torr. No measurable change in specific contact resistance was found after 350°C for 6 hr.

The thermally annealed TiW/Ge ohmic contacts were also subjected to high-temperature aging under DC bias.

Figure 7 shows the results at 300°C and 350°C after exposure for 160 hr. At 300°C the contact resistivity increased initially but stabilized at about [illegible] Ωcm². At 350°C the increase in contact resistivity was much larger. This was partially explained by the large outdiffusion of Ga, shown in the AES sputter profiles in Fig. 8.

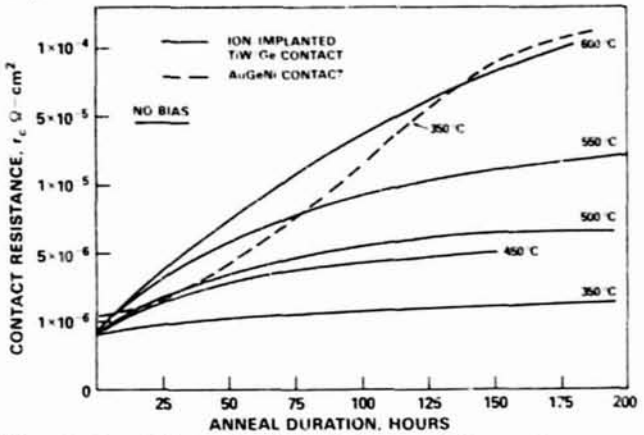

Fig. 6. Specific contact resistance of thermally annealed TiW/Ge and AuGe/Ni ohmic contacts as a function of anneal time at various aging temperatures in forming gas.

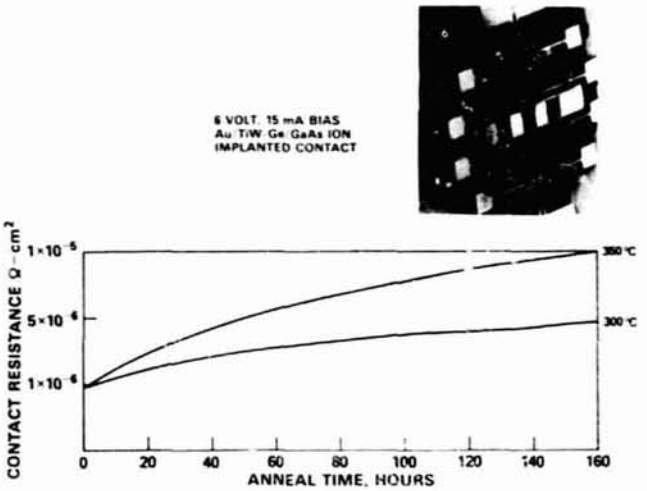

Fig. 7. Specific contact resistance of thermally annealed TiW/Ge contacts as a function of anneal time under bias conditions at 300°C and 350°C in forming gas. Test structure used to measure contact resistivity (center mesa) and to study metal migration (long arms).

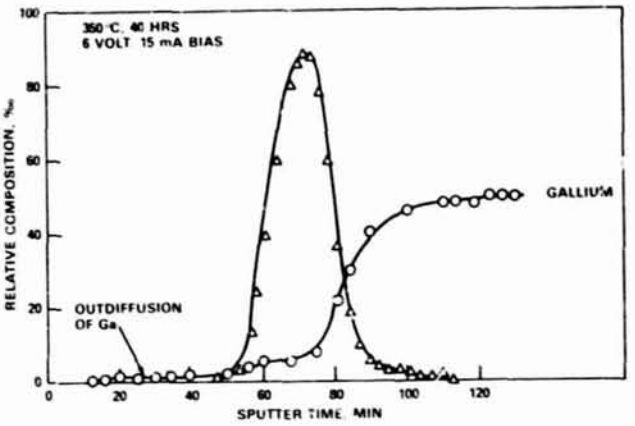

Fig. 8. AES sputter profile (Ge and Ga) of thermally annealed TiW/Ge ohmic contact after 350°C/40 hr anneal in forming gas under bias conditions, showing large Ga outdiffusion.

Acknowledgements

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FABRICATION AND HIGH TEMPERATURE CHARACTERISTICS OF ION-IMPLANTED GaAs BIPOLAR TRANSISTORS AND RING-OSCILLATORS*

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INTRODUCTION

A growing need is developing for monolithic semiconductor circuits for high temperature environments. Si-devices have been reported to operate up to 300°C.[1,2] Because the upper operating temperature of a bipolar device is determined by the bandgap of the semiconductor material, GaAs (1.43eV) has a theoretical advantage over silicon (1.12eV). Based on bandgap considerations exclusively, GaAs could be expected to be useful up to 450°C; in fact, transistors have been operated at this temperature.[3] Based on these assessments a special program to study the high temperature aspects of GaAs bipolar transistors was initiated in 1966. The results of this program, which were reported in 1968[4], showed: GaAs transistors were limited by leakage currents, which exhibited a temperature dependence with an activation energy of 0.7eV. The current gain h_{fe} decreased rapidly with increasing temperature with an activation energy of approx. 0.2eV, apparently due to a decrease of the minority carrier lifetime. Devices which operated above 400°C could be made, but the fabrication yield was extremely small. The technology available at this time was constrained to sulfur and magnesium diffusions at temperatures at which surface decomposition could not sufficiently be suppressed. Doping control was poor. The devices had mesa structures with little surface passivation. The fabrication of a sophisticated GaAs IC was beyond reach.

During the recent years the GaAs technology progressed rapidly, motivated mainly by the excellent performance of microwave FET's. Ion implantation and annealing techniques were developed to form reproducibly thin layers of controlled doping levels. This progress made it desirable to re-evaluate the GaAs bipolar device performance. Potential advantages of a GaAs bipolar technology include: short minority carrier lifetime; high electron mobility at low electron fields; use of saturated drift velocity for load resistors (small area requirements); isolation by boron implantation (requires less area than junction isolation); higher operating temperature than silicon devices. The bipolar technology would permit the application of established Si bipolar circuit concepts and models with only minor modifications. Some disadvantages of GaAs, namely the low hole mobility and the comparatively low maximum donor concentration will remain with us. The possibility of modifying the bandgap by using GaAlAs, e.g. for wide band gap emitters, and of incorporating opto-electronic principles make this technology particularly exciting. The main difference between the situation a decade ago and today is that ion-implantation offers the reproducible production of p-n junctions, avoiding the damaging high temperature diffusions. Originally our present program was designed to study the feasibility of a GaAs bipolar IC technology but not specifically the high temperature aspects. Results obtained with a 15-stage ring-oscillator were reported recently.[5] It will be apparent that specific modifications will have to be incorporated to extend performance and reliability to higher temperatures, such as the replacement of the alloyed gold contacts. This paper will discuss the fabrication and high temperature performance of discrete bipolar transistors and of a 15-stage ring oscillator.

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DEVICE FABRICATION

The fabrication of GaAs bipolar transistors by ion implantation into bulk GaAs has been reported previously.[6] The fabrication of the ring-oscillator requires an epitaxial n/n^+ structure. The starting GaAs substrates, purchased from commercial suppliers, come from Bridgman-grown single crystals. The $AsCl_3$-Ga-H_2 vapor phase epitaxial process is employed to deposit 2 layers: first an approx. 3 micron thick layer with a donor concentration of approx. 8×10^{17} cm^{-3}, followed by an undoped layer, approx. 1 micron thick. The VPE technology, as applied to microwave devices in our laboratory, has previously been described in the literature.[7]

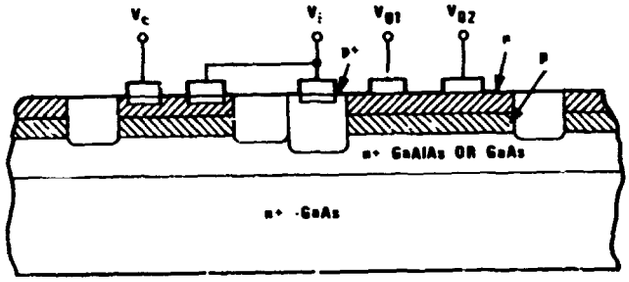

Fig. 1 Cross-section of a bipolar IC structure

The cross-section of a bipolar IC-structure is shown in Fig. 1. The npn transistor operates in the "up"-mode: the n^+-epitaxial layer/substrate acts as emitter, the surface n-layer is the collector. Also shown is the load resistor. The fabricated structures differ from Fig. 1 in one respect: they have only one alloyed collector contact on the n-type surface layer.

The formation of the n- and p- layers employs ion-implantation. The details of the donor implantation are drawn from extensive experience with GaAs FET's.[8] The base-layer is formed by a deep implant of Be, which is known to have high activation at low anneal temperatures.[5,10] Preservation of the GaAs surface morphology during the high temperature

annealing step is achieved by the proximity annealing technique.[8,11] The sequence of fabrication steps for the bipolar structure is as follows:

1. Shallow Se implant (1 x 10^{13} cm^{-2}, 150 keV plus 2 x 10^{13} cm^{-2}, 360 keV at 350°C).
2. Anneal at 850°C for 30 min.
3. Deep Be implant (6 x 10^{12} cm^{-2}, 180 keV) to form the base layer.
4. Anneal at 800°C, 30 minutes.
5. Localized Be implants to form the p^+ contact regions (1 x 10^{14} cm^{-2} at 40 keV plus 1.5 x 10^{14} cm^{-2} at 80 keV).
6. Anneal at 700°C, 30 minutes.
7. Localized Boron implant to form the isolation region (2 x 10^{12}, 4 x 10^{12}, 6 x 10^{12} cm^{-2} at 50, 140, 320 keV, respectively).

Si_3N_4 serves as implant mask and for device passivation. Contacts are alloyed Au-Ge-Ni for the n-type material and alloyed Au-Zn for the p-type base. Ti - Au is used for interconnections. Stripes of GaAs, whose width is adjusted by a Boron implant, serve as load resistor.

The doping profile of the complete structure is presented in Fig. 2. The ion-implanted profiles are calculated according to the LSS-theory, modified by experimentally observed activations. The transition from the n^+ epilayer to the surface n-layer was established by C-V profiling.

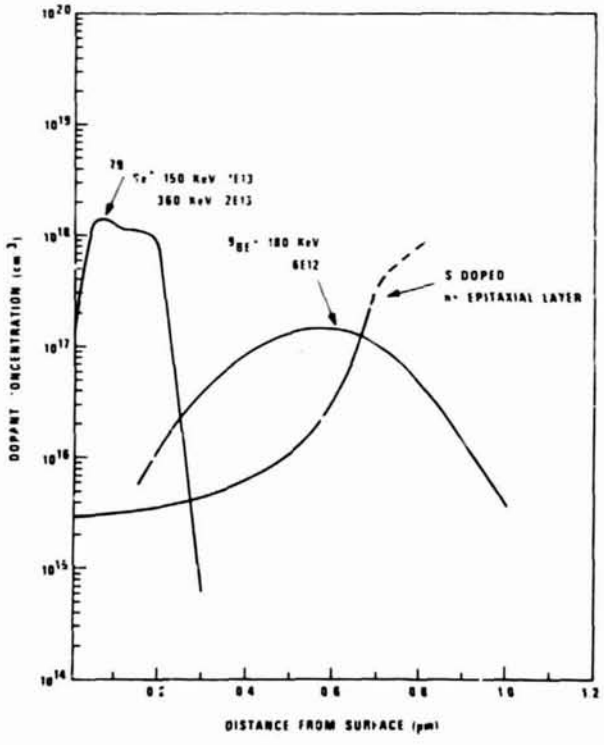

Fig. 2 Doping profile

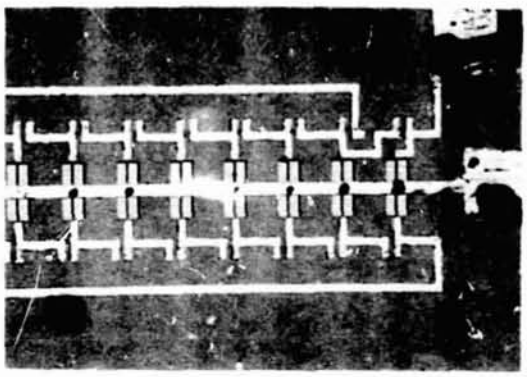

Fig. 3 GaAs Ring-Oscillator

DEVICE PERFORMANCE

A 15-stage ring oscillator was tested in the temperature range of 25°C - 390°C. Fig. 3 shows a micrograph of the circuit after this test. The circuit was mounted in a ceramic IC-package and placed in an oven. The package was not sealed, i.e. the GaAs device was exposed to hot air during the test. The bias voltage was 1.75 volt, resulting in a total input current of 5 mA at 25°C, increasing to 7mA at 385°C. Fig. 4-6 present the output signal at 25°, 240°C, 385°C. The gate delay time increases from 3.3ns at 25°C to 6.7ns at 385°C. The time constant of the circuit is dominated by the product of the capacity of the forward biased emitter diode times the load resistor. The decrease of the electron mobility in the GaAs load resistor causes the time constant to increase. The output signal of the ring oscillator approx. triples with rising temperature. Two effects contribute to this effect: 1. the increased value of the load resistor; 2. The shift of the Fermi levels towards the center of the bandgap with increasing temperature decreases the built-in voltage of the emitter junction, thereby increasing the injection current and decreasing the saturation voltage. The ring oscillator failed at 390°C. The examination of the failed device shows a damaged metallization in the via holes of the voltage supply bar, as shown in Fig. 3. This was probably caused by a realloying of the Au contacts, and a subsequent break in the metallization on the via sidewalls.

A discrete bipolar transistor on this same chip was subsequently characterized in detail. The transistor characteristics were measured both for "down"-mode (surface layer as emitter) and the "up"-mode (surface as collector, corresponding to the mode in the ring-oscillator). Furthermore the leakage currents of the emitter diode, the collector diode and I_{CEO} were determined between 25°C and 400°C. Fig. 7-10 present some curve tracer pictures of the transistor characteristics at different temperatures. The device exhibits current gain beyond 400°C. The useful temperature range is limited by junction leakage currents. Fig. 11 presents plots of I_{CEO}, in both "up" and "down" mode, and the emitter and collector diode leakage currents at 2 volts vs the reciprocal temperature. Both diodes have very similar leakage currents with a temperature dependence corresponding to an activation energy of approx. 1eV. I_{CEO} is temperature insensitive to about 200°C; then it becomes dominated by the leakage current of the reverse biased collector junction. The difference in I_{CEO} in the

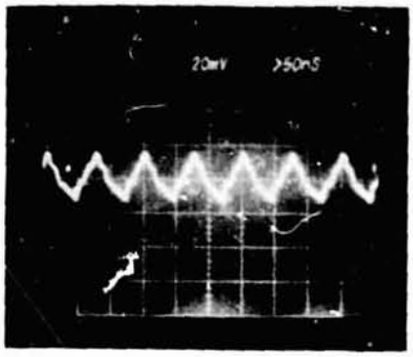

Fig. 4 GaAs Ring-Oscillator, 25°C

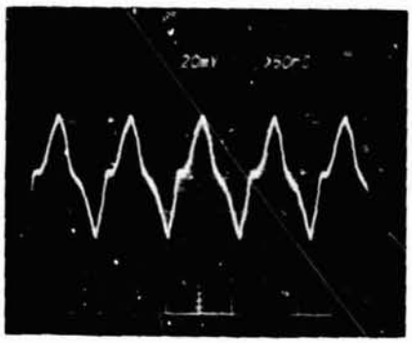

Fig. 5 GaAs Ring-Oscillator, 240°C

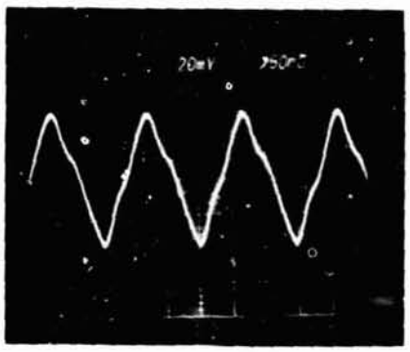

Fig. 6 GaAs Ring Oscillator, 385°C

two modes is probably caused by the asymmetry of the doping profile and the geometry of the transistor structure. The current gain as a function of temperature is presented in Fig. 12. In the "up"-mode h_{fe} is temperature insensitive to approx. 350°C. This performance is in contrast with results obtained previously[4] from diffused transistors where the current gain of the best device began to decrease already below 250°C.

CONCLUSION

Ion-implantation techniques permit the reproducible fabrication of bipolar GaAs IC's. A 15-stage ring oscillator and discrete transistor was characterized between 25° and 400°C. The current gain of the transistor was found to increase slightly with temperature. The diode leakage currents increase with an activation energy of approx. 1 eV and dominate the transistor leakage current I_{CEO} above 200°C. Present

Fig. 7 GaAs bipolar transistor at 25°C, "down"-mode

Fig. 8 GaAs bipolar transistor at 25°C, "up"-mode

Fig. 9 GaAs bipolar transistor at 390°C, "down"-mode

Fig. 10 GaAs bipolar transistor at 400°C, "up"-mode

devices fail catastrophically at ~ 400°C because of the Au-metallization. For the development of a reliable GaAs bipolar IC-techology for the 350°C-range the following subjects have to be addressed: Implementation of refractory-metal contacts; raising of doping levels to minimize the depletion layer width and to decrease the temperature sensitivity; improvement of surface passivation. The performance of GaAlAs structures should be studied with respect to leakage currents and surface degradation. It is known, e.g. that the addition of small Al concentrations to the active zone of injection lasers reduce degradation.

ACKNOWLEDGEMENT

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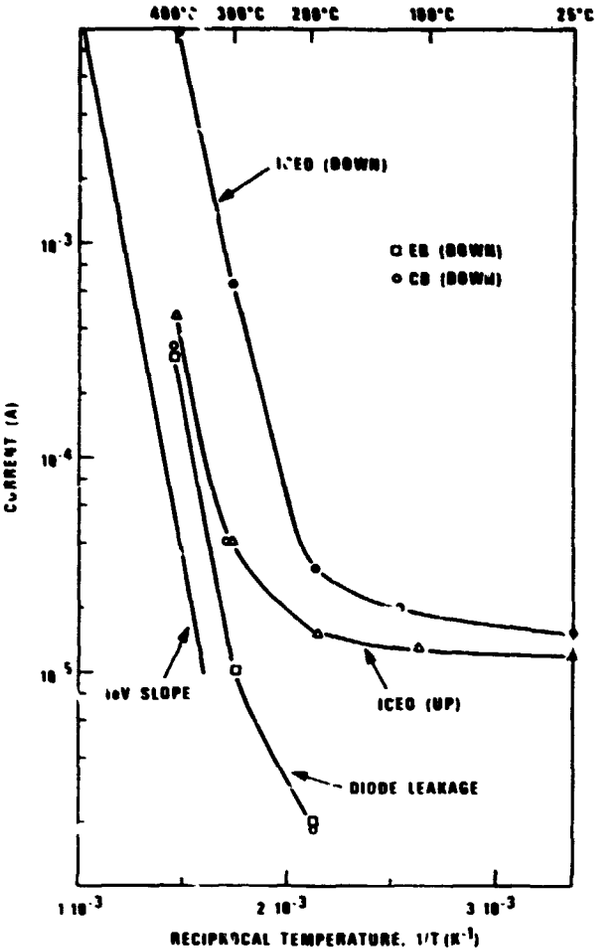

Fig. 11 Diode leakage currents and I_{CEO} as a function of the reciprocal temperature

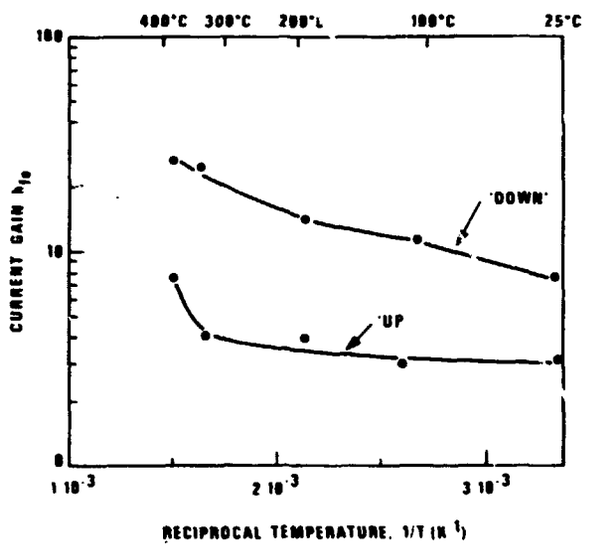

Fig. 12 Current gain as a function of the reciprocal temperature

DEVELOPMENT OF INTEGRATED THERMIONIC CIRCUITS FOR HIGH-TEMPERATURE APPLICATIONS*

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Abstract

This report describes a class of devices known as integrated thermionic circuits (ITC) capable of extended operation in ambient temperatures up to 500°C. The evolution of the ITC concept is discussed. A set of practical design and performance equations is demonstrated. Recent experimental results are discussed in which both devices and simple circuits have successfully operated in 500°C environments for extended periods of time.

Approach

The approach taken for ITC active devices has been to use the intrinsically high-temperature phenomenon of thermionic emission in conjunction with thin-film integrated-circuit technology to produce microminiature, planar, vacuum triodes. The resulting technology uses photolithographically delineated thin films of refractory metals and cathode material on heated, insulating substrates. Typical geometries and dimensions are shown in Fig. 1. Many such devices are simultaneously fabricated on a single substrate, giving high packing density. The integrated grid-cathode structures are intrinsically rugged.

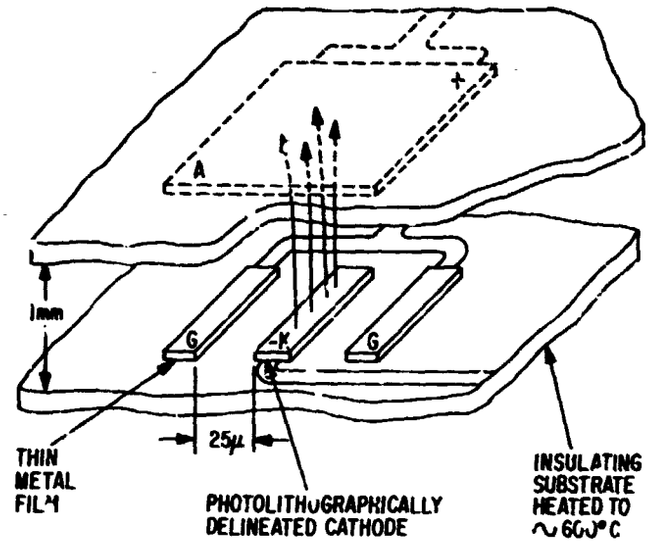

Fig. 1. Basic ITC gain device.

The ITC Structure

Notice in this structure, the anode is in the natural path of the electrons, and the closely interdigitated grids and cathodes are used to maximize grid control. In a sense, this structure is like a standard triode with the grid moved down into the plane of the cathode. In fact, it has been shown through computer simulation and experimentally verified that the fundamental equation governing conventional triode performance may be used to describe the performance of an ITC device.

$$I_p = K\left(V_g + \frac{V_p}{\mu}\right)^{\frac{3}{2}} \qquad (1)$$

where I_p is the place current,

V_g is the grid voltage,

V_p is the plate voltage,

μ is the amplification factor, and

K is a constant called the perveance.

Furthermore, from electrostatic analysis it has been shown that for a device with grid width, cathode width, and grid-to-cathode spacing equal to a and cathode-to-anode spacing equal to d,

$$\mu \cong 0.5611\,\frac{d}{a} - \frac{1}{2}\ . \qquad (2)$$

Thus, μ, the electrostatic amplification factor, is linearly related to the ratio d/a, with no other geometrical factors. This result is remarkably similar to that obtained for a conventional triode. Therefore, depending on the circuit application, the desired amplification factor can simply be selected by determining d/a.

A similar analysis for the device shown in Fig. 2, where a is the width of the cathode, b the distance between the grid and cathode, c the width of the grid, and d the distance between plate and cathode, results in

$$\mu = -\left(\frac{b + c}{a + 2b + c}\right) - \frac{a}{b}\sum_{n=1}^{\infty}\frac{2}{n}\left(\cos\frac{n\pi(a + 2b)}{a + 2b + c} - \cos\frac{n\pi a}{a + 2b + c}\right), \qquad (3)$$

which can easily be summed on a calculator.

Device Processing

To date, device processing has been the most emphasized portion of the ITC development program.

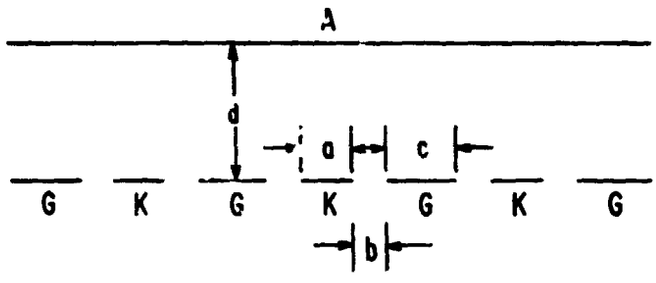

Fig. 2. Unequally spaced device.

* This work was supported by the Division of Geothermal Energy, US Department of Energy.
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Sapphire was chosen as the substrate material for ITC devices because of its high quality surface finish and high electrical resistivity at high temperatures ($\cong 8 \times 10^7$ Ω-cm at 800°C).

Figure 3 is a side view of the ITC metalizations on the circuit or device side of the substrate.

Notice that all the metals are refractory because of the need to withstand high-temperature environments. (This is in contrast to the gold and aluminum used in conventional silicon integrated circuits.) The bond pad is platinum, and the platinum bond wires are attached by parallel-gap or ultrasonic wire bonding. The base metal under the cathode is tungsten.

The cathode coating technique was developed by Geppert, Dore, and Mueller at Stanford Research Institute in 1969. This technique uses photoresist mixed with oxide cathode coating, which is then delineated photolithographically.

In practice, the cathode coating is spun onto the wafer and delineated like photoresist. The circuit is then packaged and placed on a vacuum pump. The package is evacuated and the cathode coating activated by applying power to the heater until the substrate approaches 900°C.

During normal operation, the heaters are used to heat the substrate to 750-800°C in order to provide acceptable electron emission from the cathode (>100 mA/cm²).

Current Technology and Limitations

Figure 4 is a picture of the first Los Alamos ITC device, manufactured in 1977. The lines and spaces are 5 mils. The heater pattern is visible on the back of the sapphire. The darker fingers are the cathodes.

Figure 5 is an array of three devices from 1979. The cathode and grid lines are 1 mil, and spaces between grids and cathode are 0.2 mil.

Because the oxide cathode is granular in nature (with crystals on the order of 1 μm), the 0.2 spacing appears to represent an optimal limit to device size.

This technology yields a minimum device size of approximately 10 by 3.5 mils, which is enough to hold over 12,000 devices on a pair of 3/4-in.-diam sapphire substrates. As will be described later, factors other than minimum device size currently limit the useful density of devices on a substrate.

High-Temperature Operation

The 400°C and 500°C Operations to Date

The high-temperature operation tests conducted to date fall into two categories by time frame and package material. The run September 1979 through February 1980 used the stainless steel (302) or Kovar envelope materials. High-temperature vacuum feedthroughs using stainless steel, aluminum, and high-temperature brazes were designed for these packages by Ceramaseal Corporation, New Lebanon, New York. Initially, these packages had problems with the evolution of manganese, iron, and chromium, (in the form of diatomic oxides, for example Mn_2O_2), plus the liberation of gases at higher temperatures. As a result, these tests, described in the upper portion of Table I, should only be considered preliminary. Even so, the 400°C test device operated successfully for over 7000 hours. A number of simple circuits were also run in high-temperature environments using these initial packages.

CATHODE COATING APPLIED AND DEFINED PHOTOGRAPHICALLY

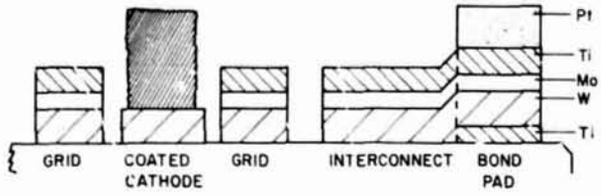

Fig. 3. ITC metalization and photolithography.

Fig. 4. First Los Alamos ITC device (1977).

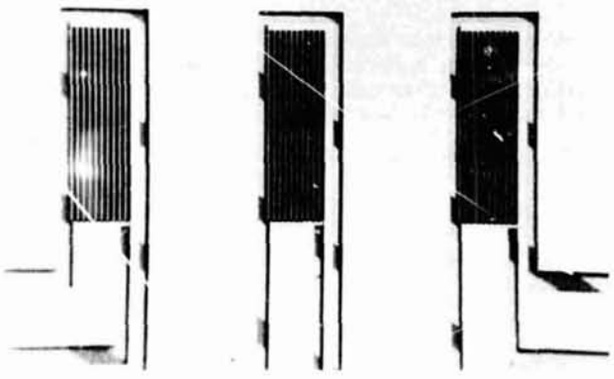

Fig. 5. Three triodes (1979).

TABLE I

HIGH TEMPERATURE LIFE TEST SUMMARY - 1st SERIES

Temp.	Start Date	Hours	Type	Bulb Material	Comments
400°C	9-26-79	7750	Triode	Kovar	No appreciable degradation through 6000 hours; emission loss thereafter stopped at 80% loss.
500°C	9-27-79	1608	Amplifier (2-device)	Kovar	Stopped - gain of 1; individual tests indicated emission loss.
500°C	9-17-79	2590	Triode	Kovar	No emission degradation through 2000 hours; increasing gas load, emission loss thereafter stopped at 50%.
500°C	10-18-79	430	Triode	Kovar	Stopped - loss of emission.
500°C	10-4-79	4464	Triode	S.S.	No degradation through 4000 hours; emission loss thereafter stopped at 50% loss.
600°C	9-20-79	328	Triode	Kovar	Stopped - loss of emission.
500°C	11-2-79	1070	Differential amp (6-device)	Kovar	Stopped - decreasing gain; electrical leakage on substrate.
500°C	11-7-79	6144	Triode in Ti jig	Kovar	Gradual decline in emission with increasing gas loads after 2000 hours; stopped at 50% loss.
500°C	1-31-80	588	5-MHz oscillator	Kovar	Oscillation stopped; electrical leakage on substrate.
500°C	2-19-80	816	5-MHz oscillator	Kovar	Oscillation stopped; electrical leakage on substrate

The above tests have all been terminated. Following tests are ongoing using high-purity nickel bulbs and "clean" welding techniques.

HIGH TEMPERATURE LIFE TEST SUMMARY - 2nd SERIES - IMPROVED BULB

Temp.	Start Date	10-8-80 Hours	Type	Bulb Material	Comments
500°C	5-9-80	3648	Triode	Ni	No degradation in emission; no leakage.
550°C	7-8-80	2208	Triode	Ni	Valved off pump to facilitate gas burst tests; developed loops. Burst test at 1400 hours indicated argon present; evidence of gas cleared and did not

In all cases, failure was due to electrical leakage on the substrate because the metals were being liberated from the package. The 5-MHz Hartley oscillator operated with both the capacitor and inductor at 500°C.

With the understandings evolved from the stainless steel and Kovar tests, a newer package was designed using nickel. The first test began May 19, 1980, and is still running after 6312 hours. Figures 6 and 7 show the device characteristics on May 19 and October 9. The device characteristics are virtually unchanged.

The second test, also ongoing, uses a device operating at 550°C; the device is valved off the pump to allow periodic gas-burst tests. This device is still being evaluated after 2200 hours. The results are tentative because no signs of gas have been seen in the characteristics after the 1400-hour gas burst.

Fig. 6. Improved package (500°C) first day.

Conclusions Regarding High-Temperature Operation

Based on the tests performed to date, ITC technology has demonstrated the ability to operate

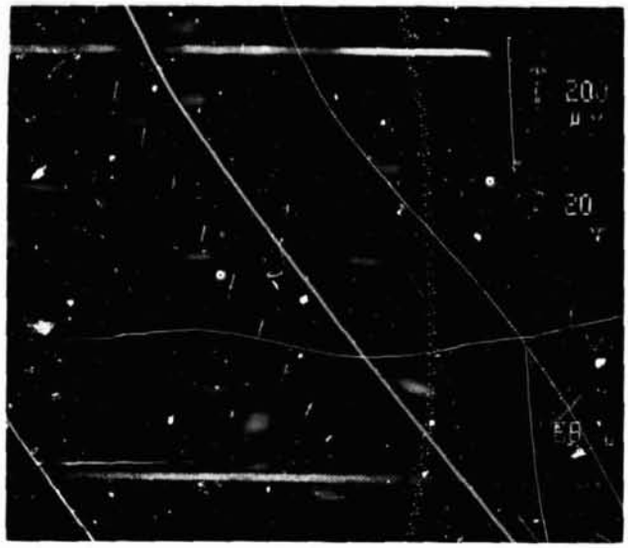

Fig. 7. Device (500°C) after 3600 hours.

successfully and reliably for thousands of hours at temperatures up to 500°C. This temperature is not the fundamental limit for ITC devices, and with the evolution of better gettering techniques (more complex than titanium) and packaging techniques (perhaps glass-ceramic - reference paper to be given at this conference by Dr. Cliff Ballard, Sandia Laboratories), higher temperature operations are expected in the future.

Circuits

The design of ITC circuits is in many ways similar to the design of conventional integrated circuits. Therefore, ITC design techniques use the advantages gained from the simultaneous fabrication of many devices on the same substrate. The inherent matching of device characteristics and the tracking of these characteristics over temperature and life are exploited. Functional circuit elements such as differentional stages, current sources, and circuits that use active devices as loads have been fabricated using discrete ITC devices, and their performance has been verified against theory. The simple active load, shown in Fig. 8, is particularly valuable because its gain

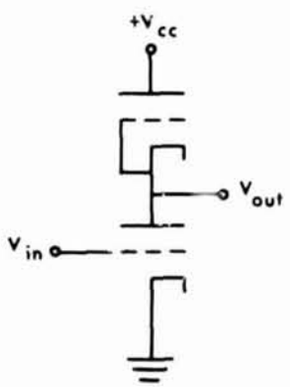

Fig. 8. Gain stage with active load.

$(-\mu/2)$ is only dependent on device geometry, the ratio of line width to cathode-anode spacing. Therefore, the gain of the stage is independent of the transconductances of the two devices and, hence, of the operating temperatures.

As a result of the success of designing functional ITC circuits using discrete devices, the design of integrated ITC circuits has become the recent emphasis of the program. Because these efforts are ongoing, this section will mainly contain general comments and directions for future work.

The design of integrated circuitry with complex functions on a single pair of substrates presents new challenges and possibilities as a result of device matching and, unfortunately, some problems, in particular, electrostatic interactions between devices.

Figure 9 schematically depicts the origin of such interactions.

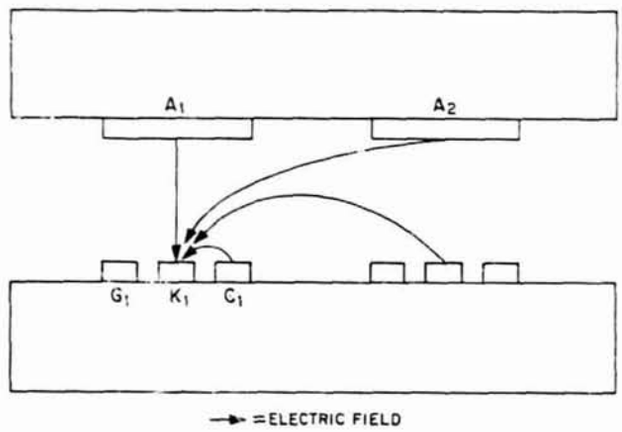

Fig. 9. Electrostatic interactions.

The key to increasing the functional complexity and maximum gain on a single substrate pair will be the development of appropriate techniques for making design tradeoffs between device layout (position on the substrate) and circuit function.

Although results are still tentative, Figs. 10 and 11 show the layout of one experimental pair of substrates for a differential gain stage. In current experiments, a series of device masks are used to photolithographically generate an array of devices, which are then interconnected using a series of masks with line segments. Results suggest that a reasonable 2-year goal for ITC technology is the design of an operational amplifier with a voltage gain of 1000 or more on a pair of 0.75-in.-diam substrates.

Conclusions

Based on the results described above, the future for ITC technology is bright. Programmatic efforts have led to an ITC technology with demonstrated high-temperature capability (500°C for thousands of hours) and to fabrication techniques commensurate with mass production. Physical models and detailed device understandings have been developed. Preliminary circuits using discrete devices, single not integrated, have demonstated the potential of ITCs. All that remains is the final development of integrated circuit

design techniques and the demonstration of integrated circuity.

The results of the ITC development program suggest that ITCs may become an important technology for high-temperature instrumentation and control systems in geothermal and other high-temperature environments.

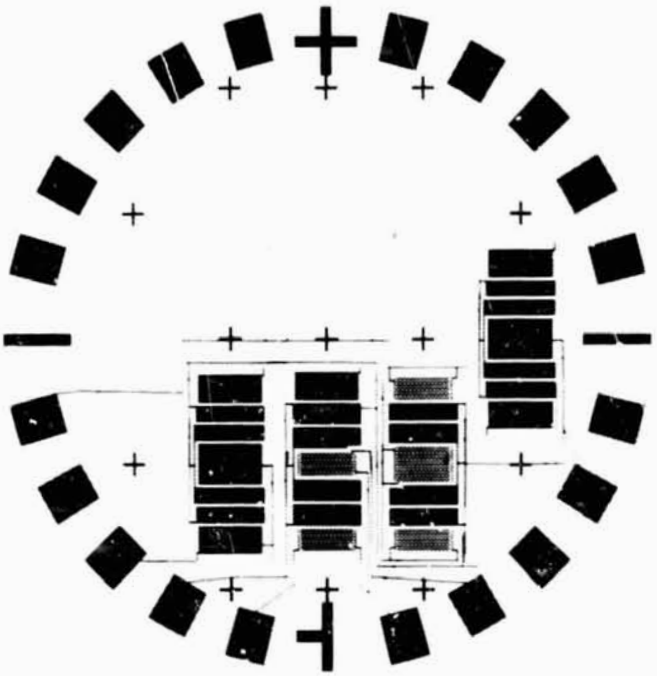

Fig. 10. Substrate 1, differential gain stage.

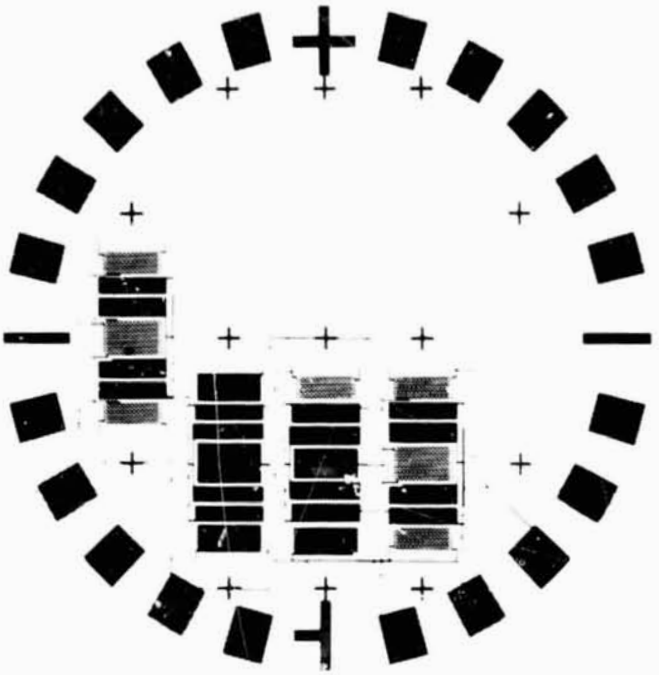

Fig. 11. Substrate 2, differential gain stage.

GALLIUM PHOSPHIDE HIGH TEMPERATURE DIODES*

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SUMMARY

The purpose of this work is to develop high temperature (>300°C) diodes for geothermal and other energy applications. A comparison of reverse leakage currents of Si, GaAs and GaP is made. Diodes made from GaP should be usable to >500°C. An LPE process for producing high quality, grown junction GaP diodes is described. This process uses low vapor pressure Mg as a dopant which allows multiple boat growth in the same LPE run. These LPE wafers have been cut into die and metallized to make the diodes. These diodes produce leakage currents below 10^{-3} A/cm^2 at 400°C while exhibiting good high temperature rectification characteristics. High temperature life test data is presented which shows exceptional stability of the V-I characteristics.

I THEORY

The choice of semiconductor material used to fabricate diodes is dominated by the reverse leakage characteristics desired. The reverse leakage current density of an abrupt P^+ -N junction is given by:[1,2]

$$J_R = e\sqrt{\frac{D_p}{\tau_p}}\cdot\frac{n_i^2}{N_D} + \frac{en_iW}{2\tau_o} \qquad (1)$$

where D_p = hole diffusion coefficient
τ_p = hole lifetime (in the n region)
τ_o = depletion region carrier lifetime
n_i = intrinsic carrier concentration
e = electronic charge
N_D = donor concentration
W = depletion layer width

The first term on the right side of Eq. (1) represents the diffusion of minority carriers within a diffusion length of the junction which produces a reverse leakage current. This component is independent of bias. The second term on the right of Eq. (1) represents generation-recombination current in the depletion region and is dependent on bias through the depletion width. Generally the recombination current term will dominate at low temperatures and the diffusion current term will dominate at higher temperatures. The crossover point is primarily dependent on the semiconductor band gap and carrier lifetime. The appropriate parameters for Silicon (Si), Gallium Arsenide (GaAs) and Gallium Phosphide (GaP) were used to evaluate Eq. (1) as a function of temperature for the three materials. The results for reverse leakage current density at -3V are shown in Figure 1. The arrows on the curves mark the crossover temperature of the two components of leakage current. For temperatures to the left of the arrows generation-recombination current dominates and diffusion current dominates at temperatures to the right.

The figure shows that for temperatures in the 20-300°C range GaAs and Si have similar leakage currents. (The high depletion region generation-recombination current in GaAs offsets its wider bandgap.) Calculations show that GaP diode reverse leakage should be dominated by generation-recombination current up to 650°C and is at least 5 orders of magnitude lower than Si. Hence it can be seen that GaP should be an excellent choice for high temperature semiconductor devices.

This fact is demonstrated in Figure 2. This figure shows a V-I characteristic of a Sandia-made P^+ -N GaP diode at 400°C. The leakage of the GaP diode is not discernable on the figure. The measured current density at -3V and 400°C was 7×10^{-4} amp/cm^2 for the GaP diode.

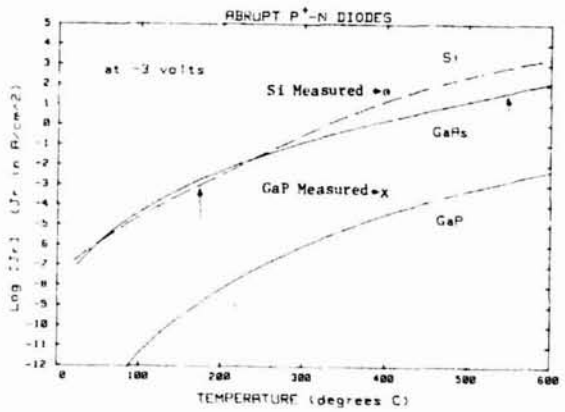

Figure 1. Comparison of reverse leakage current density vs. temperature for GaAs, Si and GaP.

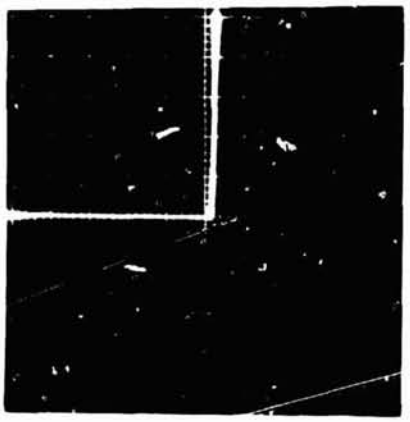

Figure 2. GaP grown junction diode characteristic at 400°C. (Horizontal = 5V/div, vertical = 1 mA/div.)

II DIODE FABRICATION

To realize a device whose operation will not be degraded by the high density of chemical impurities and structural defects present in typical bulk GaP substrate material, the all-epitaxial structure of Figure 3 is used. The N side of the junction is

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†A. U. S. Department of Energy facility.

lightly doped to provide as high reverse breakdown voltage as possible. The P side can then be relatively highly doped to facilitate ohmic contacting of the top surface.

This structure was prepared using liquid phase epitaxy for the growth of both layers during a single growth cycle.

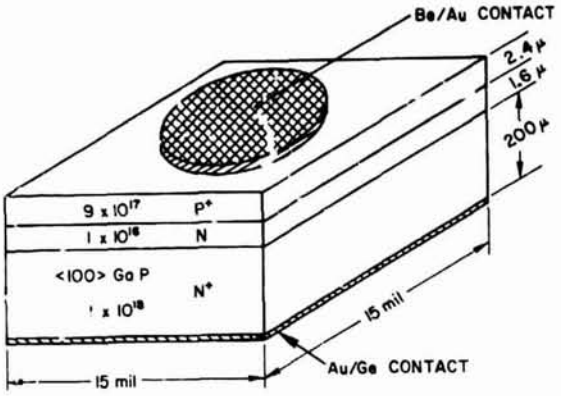

Figure 3. Grown Junction GaP Diode.

The growth apparatus shown in Figure 4 is a sliding boat assembly constructed from high purity graphite. The body of the assembly contains wells for two growth solutions, one for the growth of the N layer, a second for the growth of the P layer. To maintain background (no intentional doping) carrier concentration as low as the 1 x 10^{16} cm^{-3} level desired for the N layer, the growth temperature used was 850°C. At this relatively low growth temperature, Si contamination of the growth solutions from the quartz walls of the system is minimal. To ensure that no cross contamination of the N solution occurs from the heavily doped P solution, relatively non-volatile Mg is used as the P dopant in place of the highly volatile Zn normally used to dope GaP P type.[3] Since Mg possesses a stable oxide, provision is made for adding this dopant after a pre-bake cycle removes residual oxygen from the growth solutions, as in Figure 4A. The system is then permitted to equilibrate at the growth temperature (850°C) for 2 hours, as in 4B, after which the slider is translated to bring the GaP substrate into contact with the first growth solution, as in 4C. Cooling then causes the solution to become super-saturated and epitaxial growth occurs on the substrate. When the N- layer is sufficiently thick, the slider is again translated to bring the substrate in contact with the second melt for growth of the P layer, after which further translation of the slider separates the substrate from the liquid.

The diode metallization system used was:

P^+ contact - Be/Au (3000Å ∿ 1% Be by weight) (7 mil dot) followed by 3000Å of pure Au (vacuum evaporated)

N^+ contact - The contact was sputtered (full surface) in the following sequence:
Au/Ge (8P/12) ∿1000 Å, Au ∿ 250Å,
Ni ∿ 600 Å, Au ∿ 4000 Å,
Contacts annealed at 450°C (10 minutes) in H_2

The first lot of diodes tested were mounted in ceramic flat pack headers (N^+ side down) with a high temperature, polymide silver loaded adhesive. Gold wires (1.5 mil) were used to make contact to the top of the die. However, this configuration was found to be unsatisfactory due to deterioration of the adhesive at high temperatures. The scheme finally chosen was a stress-free configuration using 1.5 mil diameter gold wires bonded to each side of the chip. This was done to eliminate any die attach stresses or material interactions due to the header attachment scheme. These devices are shown in Figure 5. It should be emphasized that the mounting configuration shown in Figure 5 is not proposed for fielded devices, but rather it is a scheme used to remove any contribution of header stress or bonding agent reactions for testing device characteristics.

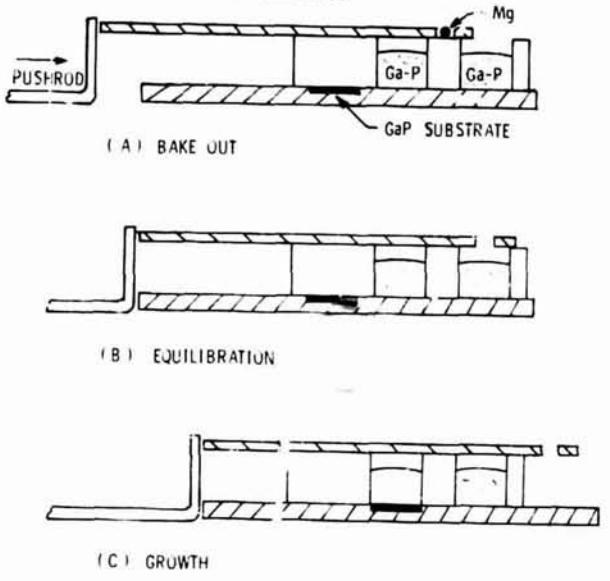

Figure 4. Liquid Phase Epitaxial Growth System.

Figure 5. Stress-Free Diode Mount.

III DIODE CHARACTERISTICS

A typical I-V characteristic of a GaP diode was shown in Figure 2. The breakdown voltage was measured to be 90V at 400°C; the breakdown characteristic remains fairly sharp even at this elevated temperature. The fact that the leakage current is larger than the value predicted (see Figure 1) means that there is some leakage at the sawed edges of the die.

The zero bias capacitance of the 15 mil square chips was measured to be 22 pF. This corresponds to a 0.56 μ zero bias depletion width.

IV ENVIRONMENTAL TESTS

The GaP diodes were subjected to a life test under bias. Three bias conditions were used; forward bias (5 mA), reverse bias (-10 V) and open circuit (zero bias). The diodes were placed in ovens at 300°C. The devices were not sealed and the oven contained room air. The parameters of the diodes were checked as a function of time in the oven.

The results of this test are summarized in Figure 6. This figure shows that no detectable degradation in series resistance occurred in any of the three bias states. The room temperature reverse leakage did show a slight increase, increasing from nominally 10^{-9} amps to 10^{-8} amps after 991 hours at 300°C. There was not a strong correlation between bias state and leakage increase. The reverse leakage at 300°C showed a slight decrease after 991 hours. This stability in diode parameters is interpreted as meaning that the diode metallizations and junction dopants are stable at 300°C with bias for at least 1000 hours.

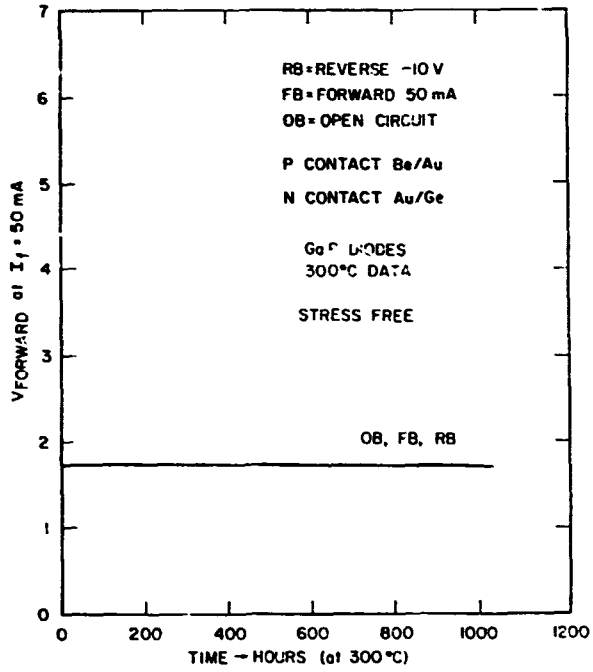

Figure 6. 300°C Life Test Data on Stress Free GaP Diodes.

V CONCLUSIONS

This paper has presented data on gallium-phosphide, grown junction diodes for high temperature applications. Information on fabrication methods were presented. Evaluation data shows: good low leakage rectification characteristics at 400°C and stable junction and metallization parameters at 300°C for at least 1000 hours. The only problem encountered was the "high temperature" polyimide adhesive used to bond the diode chips to the headers. A new eutetic chip bonding procedure is presently being developed to solve this problem.

VI ACKNOWLEDGEMENTS

This work was supported in part by the Dept. of Energy, Division of Geothermal Energy. The authors would also like to thank J. B. Snelling and T. A. Plut for their assistance in fabricating and testing the devices.

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A GALLIUM PHOSPHIDE HIGH-TEMPERATURE BIPOLAR JUNCTION TRANSISTOR*

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SUMMARY

Preliminary results are reported on the development of a high-temperature (>350°C) gallium phosphide bipolar junction transistor (BJT) for geothermal and other energy applications. This four-layer $p^+n^-pp^+$ structure was formed by liquid phase epitaxy using a supercooling technique to insure uniform nucleation of the thin layers. Magnesium was used as the p-type dopant to avoid excessive out-diffusion into the lightly doped base. By appropriate choice of electrodes, the device may also be driven as an n-channel junction field-effect transistor.

The gallium phosphide BJT is observed to have a common-emitter current gain peaking in the range of 6-10 (for temperatures from 20°C to 400°C) and a room-temperature, punchthrough-limited, collector-emitter breakdown voltage of approximately -6V. Other parameters of interest include an f_T = 400 KHz (at 20°C) and a collector base leakage current = -200 μA (at 350°C).

The initial design suffers from a series resistance problem which limits the transistor's usefulness at high temperatures. This is not a fundamental material limit, and second generation structures are presently in process which will alleviate this problem as well as improve the device's output resistance and breakdown voltage.

INTRODUCTION

Recent successful operation[1] of gallium phosphide high-temperature diodes at temperatures and times exceeding 300°C and 1000 hours respectively, has prompted the development of a gallium phosphide bipolar junction transistor (BJT) for geothermal and other energy applications. Using contacting and epitaxial growth technologies similar to the diodes of Ref. 1, a prototype, four-layer $p^+n^-pp^+$ structure has been successfully fabricated and evaluated at temperatures up to 440°C. The processing sequence and device characteristics of the GaP BJT, as well as suggested improvements and predicted characteristics will be discussed.

FABRICATION

The structure of the prototype GaP transistor is shown in Fig. 1. This all-epitaxial device incorporates a double-base stripe geometry, a mesa-isolated emitter region, and a saw-isolated collector region. Important structural information is summarized in Table I below. By appropriate connection of electrodes, the device may also be driven as an n-channel junction field-effect transistor (JFET).

TABLE I

Emitter acceptor concentration	$2.x10^{18}cm^{-3}$
Emitter thickness	0.9 μm
Emitter-Base junction area	$4.6x10^{-4}cm^2$
Base donor concentration	$2.x10^{16}cm^{-3}$
Base thickness	1.1 μm
Epitaxial collector acceptor concentration	$1.5x10^{17}/cm^{-3}$
Epitaxial collector thickness	4 μm
Collector-Base junction area	$4.x10^{-3}cm^2$
Substrate acceptor concentration	$1.x10^{18}cm^{-3}$

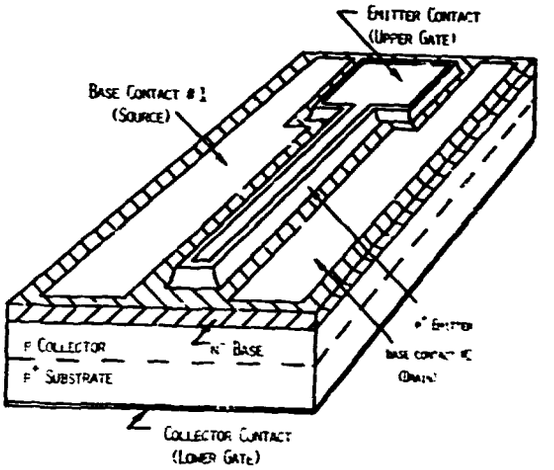

Figure 1. Structure of a prototype GaP high-temperature bipolar junction transistor (BJT) with a mesa-etched emitter, chip size 500x750 μm. The device may also be driven as an n-channel junction field-effect transistor (JFET) where the base region serves as the channel and the emitter and collector regions function as upper and lower gates, respectively.

The device of Fig. 1 is fabricated from a 3-layer p^+n^-p structure prepared by liquid phase epitaxy (LPE) on a p^+ substrate. The graphite sliding boat assembly used to grow these layers is shown in Fig. 2. Non-volatile Mg is used as the p-type dopant to avoid vapor-phase contamination of the lightly doped n-type growth solution. A pre-bake under flowing purified H_2 in position 2a is used to remove residual oxygen from the growth solutions before addition of the Mg dopant. After addition of Mg, the system is raised to the growth temperature (850°C) and held for ~2 hrs. to allow saturation of the solution with phosphorus (Fig. 2b). Growth is initiated by quickly decreasing the system temperature by 15°C, causing each solution to become correspondingly supercooled. The slider is then translated to bring the GaP substrate in contact with the first supercooled solution, as in Fig. 2c. Due to the supercooling, nucleation immediately occurs on the substrate, leading to epitaxial growth. Subsequent translation of the slider brings the substrate in contact with the other growth solutions for the completion of the multilayer structure.

*This work sponsored by the U. S. Department of Energy (D.O.E.) under Contract DE-AC04-76-DP00789.

†A U. S. Department of Energy facility.

By adjusting the amount of supercooling and the duration of contact between substrate and growth solution, layer thicknesses as small as 0.2 μm can be controlled. Interface planarity, as delineated by staining in $1HF:1H_2O_2$, is excellent, owing to the supercooling technique, which avoids nonuniform nucleation and island growth.

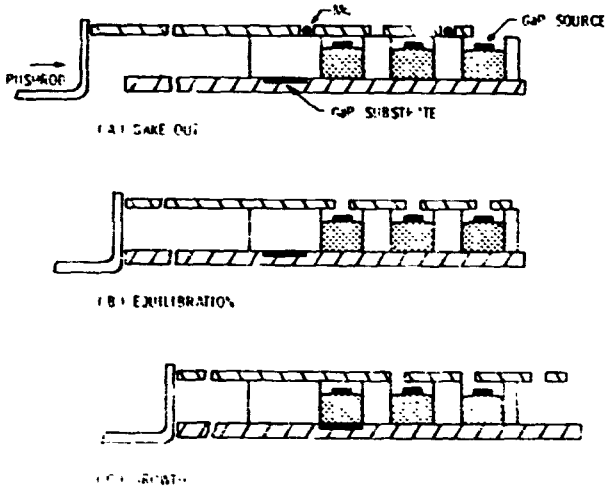

Figure 2. Graphite sliding boat assembly used for liquid phase epitaxial growth of the three active layers of the GaP BJT.

Once the resistivity and thickness of all three active layers are defined by LPE, the processing sequence of Fig. 3 is implemented to uncover the base and contact all three regions. The first step (Fig. 3a) involves definition of a thermally evaporated Au-Be/Au emitter metalization by a single-step optical lift-off process.[2] Next, 300 nm of plasma-enhanced CVD Si-N is deposited and patterned to serve as a masking material for the GaP etchant. The emitter mesa is then formed (Fig. 3b) by chemically removing unwanted p^+ material in a $K_3Fe(CN)_6$ (0.5 molar): KOH (1.0 molar) solution at 17°C. Without agitation this mixture etches p-type GaP at 80 ± 8 nm/min. The Au-Ge/Ni/Au base metalization is then defined (Fig. 3c) by deposition through a shadow mask. After thermal evaporation of the Au-Be/Au collector metalization on the back of the wafer, the contacts are annealed at 500°C for 15 min in H_2. Individual transistors are then formed (Fig. 3d) by sawing the wafer into dice with a high-speed diamond-impregnated saw. The transistors are then mounted in ceramic headers using a silver loaded polyimide adhesive and contact is made using thermocompression-bonded, 1.0 mil Au wire. This packaging technique is unsatisfactory for life testing, however, as the polyimide adhesive is known to fail[3] after extended use at or above 300°C.

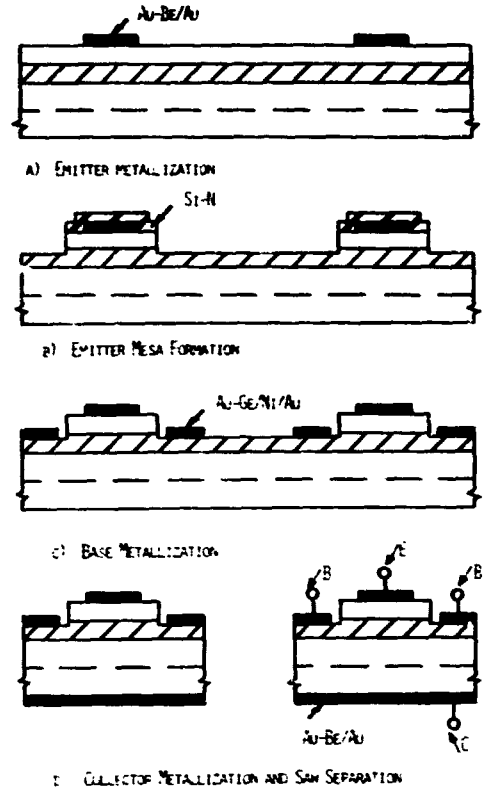

Figure 3. Processing sequence for the prototype GaP BJT

DEVICE EVALUATION AND DISCUSSION

The GaP transistor described above was evaluated in both the bipolar and JFET modes. Common-emitter output characteristics of the device at 20°C and 350°C are shown in Fig. 4. The transistor is observed to have a common-emitter current gain (at 20°C or 350°C) peaking in the range of 6-10 and a room temperature, punchthrough-limited, collector-emitter breakdown voltage of approximately -6V. Other parameters of interest for this device include an f_T = 400 KHz (20°C) and a collector-base leakage current = - 200 uA (T = 350°C, V_{CB} = -4V). A simple amplifier constructed from this transistor produced power gains of: 16dB at 20°C and 350°C; 12.5 dB at 400°C; and 2.2dB at 440°C. Operated as a JFET the transistor had a double-gate pinchoff voltage = 1.8V (20°C) and a common-source transconductance = 120 uS (20°). No extended life tests have been performed on these structures to date.

The low value of the common-source transconductance and the degradation of the common-emitter output characteristics at high-temperature are both due to excessive series resistance in the lightly doped n-type region of the initial design. In the JFET mode, this resistance appears in series with the source and drain. This seriously degrades the JFET properties as any voltage drop across the source resistance appears as negative feedback on the gate.

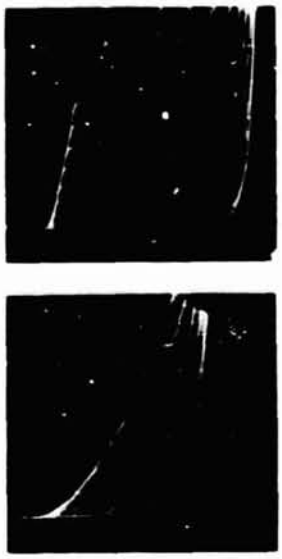

Figure 4. Common-emitter output characteristics of the GaP BJT at 20°C and 350°C. (I_C = -0.5mA/div, V_{CE} = -1V/div, I_B = -0.05mA/step. The curves are inverted for clarity).

In the bipolar mode the resistance of the n-type region appears as a parasitic base resistance. The voltage drop developed across this resistance by the base current causes a decrease in the effective emitter area of the device. This effect is accentuated by the transistors' low value of current gain. The effective emitter area in turn modulates the effective collector and emitter resistances. As hole and electron mobilities decrease at high temperature, all series resistances increase and the common-emitter output characteristics appear to collapse from the saturation side.

Looking at this effect in a different way, Fig. 5 shows common-emitter, a. c. current gain as a function of collector current and temperature. The current gain below the Kirk effect* limit stays relatively constant with temperature whereas the peak in the current gain decreases. The important point to note from Fig. 5 is that the poor high-temperature properties of the device are limited by the series resistance of our rather crude initial geometry and not be any fundamental materials limit.

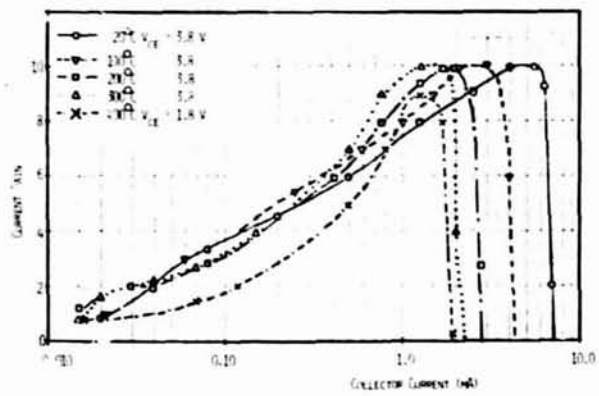

Figure 5. Common-emitter current gain vs. collector current and temperature for the GaP BJT.

An improved structure presently in process which addresses some of these problems is shown in Fig. 6. This device utilizes selective thinning of the base region and a metallorganic CVD deposited emitter to determine active device areas. A thicker inactive base region with an optimized doping concentration should decrease base resistance, increase the collector-emitter breakdown voltage and increase the output resistance. An etched rather than sawn termination of the collector-base junction should reduce collector-base leakage at high-temperatures. Utilizing improved structures such as the one shown in Fig. 6, a GaP device operating at 400°C for periods in excess of 1000 hours is expected in the near future.

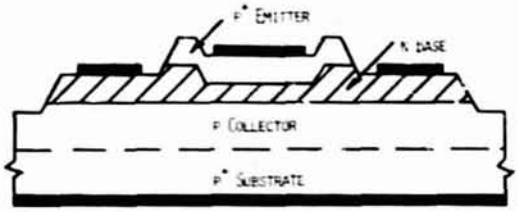

Figure 6. An improved GaP BJT incorporating a selectively thinned base region, an emitter region deposited by metallorganic CVD, and an etch-terminated collector-base junction.

CONCLUSION

Preliminary results have been reported on the development of a GaP bipolar junction transistor for geothermal and other high-temperature applications. A fabrication sequence for the transistor as well as device characteristics have been described. A series resistance problem with the initial design has been identified and suggestions have been made for improved structures.

The authors wish to thank T. A. Plut J. B. Snelling, and R. Chavez for their expert assistance in the preparation and measurement of these samples.

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RELIABILITY STUDY OF REFRACTORY GATE GALLIUM ARSENIDE MESFETS*

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Summary

Refractory gate MESFETs have been fabricated as an alternative to aluminum gate devices, which have been found to be unreliable as RF power amplifiers. The reliability of the new structures has not yet been determined, and this work was undertaken to provide statistics of failure and information about mechanisms of failure in refractory gate MESFETs. Test transistors were stressed under conditions of high temperature and forward gate current to enhance failure; results of work at 150 °C and 275 °C are reported here.

Introduction

Until recently, the semiconductor industry metal standard for MESFET fabrication was aluminum, particularly for the gate. The reliability of aluminum metallized MESFETs has been extensively studied,[1-10] and certain failure mechanisms have been identified, all involving the aluminum gate metallization. The most important of these are aluminum electromigration and gold-aluminum phase formation. The failure problem in aluminum metallized power MESFETs has become so acute that the aluminum gate is being abandoned, and a refractory gate is being introduced in its place. This gate consists of a refractory metal Schottky contact and a conducting gold metallization, separated by some intermediate metal to provide metallurgical stability; the most common refractory gate is titanium-platinum-gold. The reliability of refractory gate MESFETs has been assumed to be better than that of aluminum gate MESFETs. However, electromigration has been observed in gold[11-12] and in titanium-gold[13-14] films, and failure modes in refractory gate devices similar to those in aluminum gate devices are possible. This work was undertaken to obtain statistics on failure for and to determine failure modes of refractory gate MESFETs.

Experimental Procedure

The MESFET used in this work is the Texas Instruments MS801 gallium arsenide transistor in the stripline package. Each packaged chip consists of two individual cells, each cell delivering 250 mW of microwave power at 8 GHz; only one of the cells is used in the MS801. Normally, the chip is sealed in epoxy for protection; however, the epoxy fails near 200 °C, so that the devices tested here were unencapsulated to permit measurements at higher temperatures. Source and drain ohmic contacts are formed by evaporating a gold-germanium-nickel layer over the entire contact region and alloying, evaporating titanium-gold or chrome-gold, then gold-plating the source and drain pad regions. The source-drain separation is 6 μm; four central gate stripes, 2 μm by .006 inch, are connected in parallel at the gate pad. The gate stripes and pad are formed by electron beam evaporating successive layers of titanium (the Schottky contact), platinum and gold.

The test fixture is made from a nickel-clad high temperature laminate; contact is made between a high temperature PC board connector and the device leads by way of striplines patterned in the nickel. The connectors accomodate two fixtures side-by-side; a stainless steel tray holds fourteen connectors, so that up to twenty-eight devices can be stressed simultaneously. The temperature test chamber is a 315 °C inert gas oven configured for nitrogen flow. A three inch diameter feedthrough port, capped with a PTFE feedthrough, completes the test chamber arrangement. A thermocouple measures the temperature at the geometric center of the tray at sample height.

The devices were stressed electrically at two channel temperatures, 150 °C and 275 °C. Electrical stress consisted of biasing each device near I_{dss} and driving the gate into forward condition, in some cases, quite heavily. The devices could not be biased at the same values of I_{dss}, and simultaneously at the same drain-source voltages, because of their different characteristics; in order to maintain equal DC channel power dissipation, and equal channel temperatures for all devices during stress, the device with the lowest I_{dss} curve ($V_{gs} = 0$) was biased at the intersection of the load line and the I_{dss} curve and the other devices (at the same chamber temperature) were biased at a drain current equal to that value of I_{dss}. For equal load lines, all devices then were biased at the same quiescent value of V_{ds}. Although the other devices were biased below their I_{dss} values, forward gate current flowed for sufficient positive gate-source voltage swing. The gate-source voltage swings were set to provide equal drain-source voltage swings, in order to obtain the same AC channel power dissipation.

The output resistance of the MESFET becomes negative at certain values of the drain current and drain-source voltage. If the load line passes through a region of device negative resistance, there is a considerable possibility of oscillation, so that the drain resistance must be such as to limit operation to a safe region, that is, to a region of positive output resistance. The safe value of the drain resistance is obtained by drawing a load line which begins at the drain bias voltage on the V_{ds} axis and which crosses the I_{dss} curve at its corner, just below the point at which the output resistance becomes negative. This value is, of course, different for different devices, and even for a single device at various temperatures. I_{dss} decreases with increasing temperature; for a given transistor, a drain resistor will have its highest safe value at the highest test temperature. If that highest value is chosen as the drain load, the load line will be safe at all lower temperatures. Furthermore, if that safe value is calculated on the basis of the lowest I_{dss} curve out of the entire set of transistors, that value will assure a safe load line for every device in the set, at any temperature below the maximum test temperature. (This assumes that all devices exhibit roughly the same percentage decrease in I_{dss} with increasing temperature; the assumption was validated by comparing the behavior of several devices.) If the same load resistance is used for every test device, each MESFET can be biased to the same quiescent point, and driven with identical AC swings. The average drain power dissipated is the

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same for each device, so that power (of channel temperature) is the same; however, if the gate of each device is driven into forward conduction, the forward current drawn by each gate is different for equal drain current swings (for different I_{dss} values). The statistically significant stress is then the forward gate current.

The gate voltage was varied around its quiescent point, so that forward current flowed only during part of the AC cycle. Very low reverse gate currents flowed when the drain current was below I_{dss}, that is, for negative gate-source swings, so that a roughly half-wave rectified forward gate current was obtained; true sinusoidal behavior could not be obtained because of the non-linearity of the diode curve. The high temperature stress was interrupted at logarithmic time intervals and the devices were cooled down to room temperature for failure characterization. The stress periods were nominally 20, 50, 100, 200, 500, and 1000 hours.

Electrical Measurements

Five measurements were originally planned for high temperature characterization and failure analysis: the characteristic curves, from which the transconductance, g_m, could be obtained; the pinch-off voltage, V_{po}; an I_{dss} *vs.* V_{ds} curve; the gate-source reverse leakage current (drain-source short), I_{rgss}; the forward gate-source current-voltage characteristics (drain-source short), I_{fgss}; and the zero bias gate-source capacitance (drain-source short), C_{gss}. The capacitance measurement could not be performed because of the very high parasitics associated with the test assembly. The gate leakage current measurements were not made at elevated temperatures, inasmuch as the very high reverse gate-source currents made these measurements impractical. The time required to make a complete series of measurements at high temperatures for the total number of devices involved was long enough to be comparable to the stress periods between room temperature measurement; elimination of the reverse leakage measurement, which is primarily of value as a room temperature failure criterion, reduced the total high temperature measurement time significantly. In order to reduce the time even more, high resolution pinch-off voltage measurements were not made at elevated temperatures; that is, V_{po} could be estimated from the high temperature characteristic curves, but no special measurement was made. The pinch-off voltage, like the gate-source reverse leakage, is a useful room temperature failure criterion. However, the characteristic curves, I_{dss}, and I_{fgss}, can be related theoretically to temperature; these measurements were performed for every device at high temperature. The forward gate-source current measurements are particularly important, inasmuch as they provide the n-factors and saturation currents (and barrier heights) for the gate Schottky diodes. Characterization of the devices was performed initially at room temperature and each time the devices were cooled back to room temperature (nominally at 20, 50, 100, 200, 500, and 1000 hours) after a high temperature stress. High temperature measurements were made after the oven temperature had stabilized at its high temperature value, just before the oven power was turned off to cool the devices, and at daily intervals in between.

Results and Discussion

I_{dss} *vs.* V_{ds} curves were obtained and provided values of I_{dss} at V_{ds} = 2.5 V and at V_{ds} = 0.5 V; the latter is essentially the slope of the I_{dss} curve before current saturation, and is related to the channel resistance. The pinch-off voltage was defined as the gate-source voltage required to reduce the drain current, at V_{ds} = 2.5 V, to 20% of the value of I_{dss} at that voltage. Inasmuch as I_{dss} changed during the stress, two pinch-off measurements were made; one was based on the original value of I_{dss} before stress, I_{dsso}, and the other, on the value of I_{dss} at the time of the pinch-off voltage measurement. The characteristic curves were also obtained and the values of the transconductance, g_m, were calculated at the point of intersection of the load line and V_{ds} = 2.5 V. The reverse leakage current, I_{rgss}, was measured at a negative gate-source voltage of 4 V, with a drain-source short. Finally, the forward gate-source diode characteristics, with a drain-source short were measured. The high temperature measurements were made under the same conditions, except that the pinch-off voltage and the reverse gate leakage current were not measured. The zero voltage saturation current, I_s, and the ideality factor, n, were calculated from the measured forward gate-source diode characteristics. The barrier height at the gate-source interface was estimated from the values of I_s at room temperature and at the stress temperature. Failed devices were examined under a microscope, and their appearance was compared with the appearance of similarly stress unfailed devices.

Ten devices out of twenty-one failed as a result of stress at 150 °C; seven failed catastrophically because of damage to the gate lead and pad (five) or to the drain pad (two), and three exhibited electrically degraded behavior. Two of the latter became leaky, while the third exhibited a sharp reduction in I_{dss}; no physical changes could be seen in the three under the microscope. There was no clear change in any of the measured electrical parameters for any device preceding failure, nor for any unfailed device to the end of stress, either at room temperature or at 150 °C; in other words, there was no obvious electrical indication of degradation or as a precursor for catastrophic failure. No evidence of electromigration could be seen by optical microscopy in any device, failed or not. These results at 150 °C are consistent with results obtained in other DC and RF measurements.[15]

Twenty devices were stressed at 175 °C; seventeen failed catastrophically. Six of the catastrophic failures were infant failures, occurring at the stress temperature within five hours of the beginning of the stress. The electrical failure mode here was high gate leakage and high channel resistance; microscopic examination revealed gate pad damage in every case, with a burned area bridging the gate pad and source pad. Some drain-source common damage was also observed, but this may have been spill-over. The other eleven devices failed at times up to 1000 hours; six had high gate leakage and five were open gates. The open gate devices had lost their gate leads; the gate pads were blackened and heavily damaged. Four of the six devices with high gate leakage displayed the same kind of gate pad-source pad damage and bridging as did the infant failures. It was not possible to determine from the microscopic examination whether the gate pad

failed, or if it fused as the result of failure elsewhere in the device.

The eleven devices failed at the stress temperature also. All failed before the final room temperature measurements, at 1000 hours, could be performed. However, certain room temperature trends could be established by 500 hours of stress. In general, I_{dss} decreased from its pre-stress value, on the average, by 12%, although decreases as great as 25% were observed; channel resistance increased by around 15%; differential transconductance remained about the same, although the absolute transconductance decreased because of the compression of the characteristic curves; pinch-off voltage decreased because of the reduction in I_{dss}; the reverse leakage current became very high, in the order of microamperes. The zero bias saturation current showed considerable variation; it is difficult to obtain precise values of I_s inasmuch as an extrapolation to zero voltage is required, and a small change in the slope (the ideality factor, n) of the forward log current vs. voltage curve will introduce considerable inaccuracy. The ideality factor, n, increased from between 1.12 and 1.28 to around 1.18 to 1.47. The barrier height at the gate-substrate interface was estimated, and decreased, in general, from around 0.8 eV to 0.7 eV.

The devices which did not fail catastrophically exhibited the same trends, except that the changes after 1000 hours of stress were greater than those after 500 hours for the failed devices. I_{dss} decreased by an average of 17%; channel resistance increased by around 10%; the reverse leakage current was in the order of tens of microamperes; the change in n was about the same as for the failed devices; and the estimated barrier height decreased from some 0.8 eV to 0.6 eV.

Excluding the infant failures, all devices, including those which did not fail catastrophically, showed significant alterations in the drain stripe metallization. There was also some lifting of the silicon nitride overcoat; this is probably an effect of the high stress temperature, inasmuch as it also occurred in the adjacent cell, which had no gate or drain connection, and carried no current. There was a build-up of metal at the gate pad end of the drain stripes, appearing as raised hillocks, and a thinning of the drain stripes near the drain pad. This is a surprising result, and does not agree with other observations on similar devices under RF conditions,[16] in which the direction of metal migration is toward the drain pad end of the drain stripes. The latter results, however, were obtained with essentially linear operation, and in the stresses imposed in this work, substantial forward gate current (between 50 mA and 100 mA) flowed. No control measurements on only DC biased devices were made at 275 °C, so that it is not possible to assess the effects of the forward gate current at this time

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ELECTRICAL SWITCHING IN CADMIUM BORACITE SINGLE CRYSTALS

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Abstract - Cadmium boracite single crystals at high temperatures (≳ 300°C) were found to exhibit a reversible electric field-induced transition between a highly insulative and a conductive state. The switching threshold is smaller than a few volts for an electrode spacing of a few tenth of a millimeter corresponding to an electric field of $10^2 \sim 10^3$ V/cm. This is much smaller than the dielectric break-down field for an insulator such as boracite. The insulative state reappears after voltage removal. A pulse technique revealed two different types of switching. Unstable switching occurs when the pulse voltage slightly exceeds the switching threshold and is characterized by a pre-switching delay and also a residual current after voltage pulse removal. A stable type of switching occurs when the voltage becomes sufficiently high. Possible device applications of this switching phenomenon are discussed.

Introduction

A series of compounds having a chemical formula $M_3B_7O_{13}X$ (M = divalent metal, X = halogen) have been known to be isostructural with the mineral magnesium chlorine boracite ($Mg_3B_7O_{13}Cl$).[1-3] These compounds have an orthorhombic C_{2v}^5-Pca structure at room temperature and transform to a cubic T_d^5-$F\bar{4}3c$ structure at a higher temperature. Extensive investigations of physical properties of boracite compounds were made in the past and some boracites were found to be ferroelectric and ferromagnetic simultaneously at low temperatures.[5-9] Recently, we have successfully grown single crystals of Cd boracites, $Cd_3B_7O_{13}X$; X = Cl or Br, by a chemical vapor transport method.[10] The crystallographic transition temperatures were 520 ± 5°C for the Cd-Cl boracite and 430 ± 5°C for the Cd-Br boracite. During measurements on these crystals, we found that the crystals abruptly became conductive when a dc bias voltage was applied at above 300°C, temperatures considerably below the transition temperature. The switching was reproducible and closely resembled that observed in chalcogenide glasses.[11] However, the critical field strength required for such switching ($10^2 \sim 10^3$ V/cm) was at least one or two orders of magnitude smaller than that in the case of amorphous semiconductors. The results of dc and pulse measurements of this interesting switching phenomenon are described below. Possible device applications of this phenomenon will also be discussed.

Sample Preparation and Measuring Technique

The Cd boracite crystals were grown by a method described elsewhere.[10] The crystals (max. edge length ~5 mm) were cut into slices having a simple crystallographic face such as (100), (110), and (111) in pseudo-cubic indices. Each slice was ground and polished with diamond paste. Electrodes of Au/Cr film were evaporated. The Cr inner layer adheres rigidly to boracite surface to make a good supporting film for the Au overlayer. Gold lead wires were attached to the electrodes with Ag-conducting paste. In the dc measurements, the sample was connected in series with a large protective load resistance R_L ($10 \sim 100$ KΩ). A voltage across the sample (X) and a current through the load resistance (Y) were recorded on an X-Y recorder.

In the pulse measurements, the pulse generator (Toyo Telesonics) was capable of delivering a square pulse of maximum amplitude 10 V with various pulse lengths (1 μsec ~ 10 msec) and pulse repetition rates (single sweep ~10^6 pulses/sec). Both the dc pulse and the current through a 50 KΩ load resistance were recorded on a storage oscilloscope (Tektronix type 564).

DC Measurement

When a crystal was heated to above a certain critical temperature T_c, the crystal could be made conductive upon the application of a dc voltage. Figure 1 is a schematic illustration of current-voltage characteristics for such switching. As can be seen, the switching is symmetrical with respect to voltage polarity. Before switching, the current is determined by the sample resistance since it is much larger than R_L.

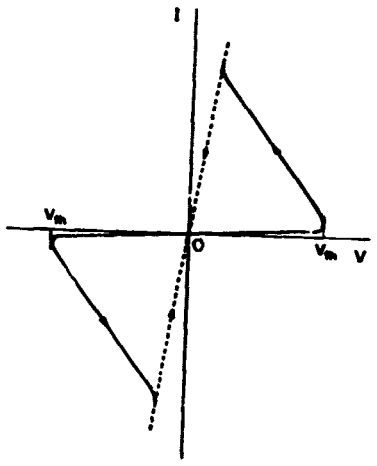

Fig. 1. dc current-voltage characteristics of a Cd-X boracite crystal (X = Cl or Br) at $T \geq T_c$.

After the threshold is exceeded, a negative resistance region appears. In the 'on' state, the dynamic resistance of the sample dV/dI takes a small positive or zero value. Unlike the case of threshold switching in amorphous semiconductors, there does not exist a critical current, or a so-called holding current at which the sample abruptly switches back to the 'off' state.[11] It seems that the sample gradually returns to the 'off' state as the current is decreased. Therefore, the sample resistance in the 'on' state cannot be clearly defined. The threshold voltage V_{th} is dependent upon temperature and decreases with temperature increase. In Fig. 2, the temperature variation of V_{th} for Cd-Cl boracite sandwich electrode samples of two different thickness are shown. Figure 3 is a similar result for a Cd-Br boracite sandwich electrode sample that shows the presence of temperature hysteresis on cooling. An apparent critical temperature T_c, obtained by extrapolating V_{th} to infinity, is dependent upon sample thickness. The thicker the sample, the higher T_c. The

threshold voltage V_{th} is not a linear function of thickness; the critical field increases with thickness. The V_{th} vs temperature curve does not show any anomaly at the crystallographic transition temperature T_{tr} at which the peculiar twin lamellar structure disappears.[10] It may be pointed out that T_c for thinner samples is indeed very close to the inflexion temperature which appeared in differential thermal analysis (DTA) curves of the crystal which are believed to show the existence of a higher order phase transition. Much the same results were obtained in the case of coplanar electrode samples.

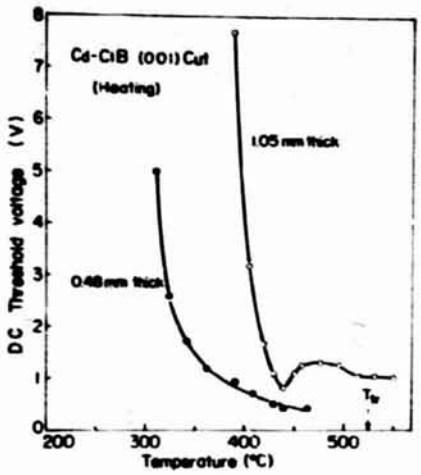

Fig. 2. Threshold voltage V_{th} as a function of temperature for two Cd-Cl boracite sandwich electrode samples with different electrode spacings.

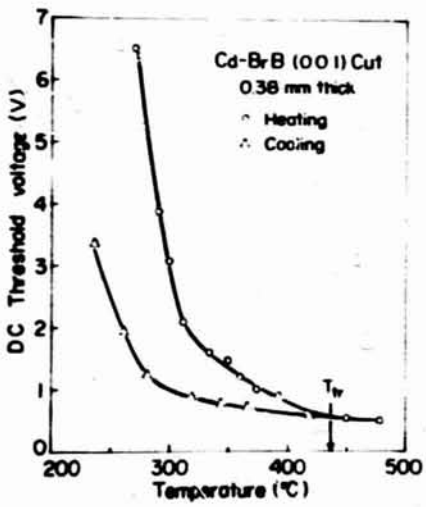

Fig. 3. Threshold voltage V_{th} as a function of temperature for a Cd-Br boracite sandwich electrode sample.

When a sample is kept in the 'on' state at a certain temperature, stabilization of the conductive state seems to set in. That is, if the 'on' state is maintained for a short time, V_{th} measured immediately afterwards is considerably smaller than its previous value. After repeated switchings, the 'on' state is temporarily stabilized. The stabilization of the 'on' state, or 'memory switching,' is always preceded by threshold switching in Cd boracites, just as in the case of memory switching in chalcogenide glasses.[11] The stabilized 'on' state in Cd boracites eventually returns to the 'off' state after the removal of a dc voltage. Complete recovery requires times ranging from seconds to hours. The occurrence of stabilization of an 'on' state makes interpretation of dc measurements somewhat ambiguous. Accordingly, pulse measurements were carried out with results as next discussed below.

Pulse Experiments

Threshold switching was clearly observed in the pulse experiments. The critical temperature for switching was comparable to that observed in the dc experiments. However, there occurred several other peculiar phenomena not observed in the dc experiments.

Two different types of switching were distinguished in the pulse experiments. The first type appears near the voltage switching threshold and is characterized by a time delay before switching and by an unstable current. There also exists residual current after the pulse is removed. In Fig. 4, an example of such 'unstable' switching is shown. The photograph was taken by multiple exposures at various pulse voltages.

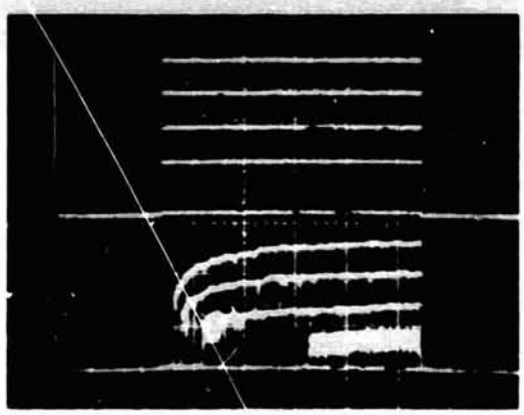

Fig. 4. Scope trace of unstable switching pulse (multiple exposure). Cd-Br boracite sandwich electrode sample with electrode spacing 0.38mm; voltage (upper trace) of 2V/div; current (lower trace) of 40μA/div; time of 2 msec/div; single sweep trace; and temp of 340° ± 2°C.

As can be seen, the delay time shortens as the voltage increases. After the removal of the pulse, the current disappears with a decay time of 15 ∿ 20 μsec. An example of such a decaying current is shown in Fig. 5. When the applied voltage becomes much larger than the threshold voltage for unstable switching, the switching begins to take place with almost no delay. The current is stable and disappears instantaneously after the removal of voltage (Fig. 6). Typical threshold voltage values for unstable switching V_{th}(USSW) and threshold voltage values for stable switching V_{th}(SSW) for various pulse lengths are shown in Table I. These voltage data were taken under constant duty operation, i.e., pulse length (sec) X pulse repetition (sec^{-1}) = 0.1. As can be seen, both V_{th}'s increase as the pulse length decreases. V_{th}(SSW) is at least 3 ∿ 4 times V_{th}(USSW). When the applied voltage is kept constant, there exists a critical pulse repetition rate at which unstable switching takes place. The critical pulse repetition

rate increases with decreasing pulse length as expected. In all cases, little or no stabilization effect was observed after repeated applications of voltage pulses.

Fig. 5. Scope trace of unstable switching pulses. Cd-Cl boracite sandwich electrode sample with electrode spacing of 0.48mm; voltage (upper trace) of 5V/div; current (lower trace) of 40 μA/div; time of 5 μsec/div; pulse repetition rate of 2 KPPS; and temp of 345° ± 2°C.

Fig. 6. Scope trace of stable switching pulses. The sample is the same as in Fig. 5 with voltage (upper trace) of 2V/div; current (lower trace) of 40μA/div; time of 5 μsec/div; pulse repetition rate of 10 KPPS; and temp of 345° ± 2°C.

Table I
V_{th}'s for Constant Duty Operation

Pulse Width (sec)	Pulse Repetition (Pulses/sec)	V_{th}(USSW) (V)	V_{th}(SSW) (V)
10^{-6}	10^5	2	7 ∿ 8
10^{-5}	10^4	1.2	3
10^{-4}	10^3	0.2 ∿ 0.4	4
10^{-3}	10^2	0.2 ∿ 0.3	4
10^{-2}	10	0.2 ∿ 0.4	3

Sample: Cd-Cl boracite (001) cut, 0.48 mm thick, T = 340 ± 2°C.

Throughout the present switching experiments, dc or pulse, the aforementioned switching characteristics changed little with crystallographic orientation of the sample.

In the present experiment, Au lead wires were attached to the sample with Ag-conducting paste. In this case, a Ag-boracite contact is presumably formed at high temperatures by the diffusion of Ag through the Au/Cr film. It was found that the sample did not switch when a Au lead wire was thermally bonded onto the Au/Cr film. It seems that Ag is indispensable to form a good electric contact to a boracite crystal. However, little is understood about the electrode effect as well as the switching phenomenon in general at present. Several mechanisms that had been proposed to account for the other switching phenomena have been discussed in connection with the switching in Cd-boracite crystals elsewhere.[12]

Device Applications

A number of functional devices can be fabricated by making use of the newly found threshold switching in Cd-boracite single crystals. Since the switching takes place only at high temperatures (≳ 300°C), such devices may be found to be useful in the fields where a high ambient temperature or a lack of workable heat sink prevents the use of ordinary solid state devices. Such devices include:

1. Current controlling devices having non-blocking Ag electrodes for dc, dc pulse and ac circuits (symmetric devices).
2. Current controlling devices having one blocking and one non-blocking electrode (asymmetric devices). Such asymmetric electrode devices can be used in a logic circuit for dc and dc pulse voltages.
3. Current rectifiers for low frequency ac.

Since the operative principle of devices of first and second categories are obvious from the foregoing discussion, only the current rectifiers will be described in some detail. Figures 7 and 8 show the circuits for half-wave and full-wave rectifiers, respectively. The half-wave rectifier of Fig. 7 consists of an ac source, a load resistance R_L, a blocking capacitance C_b, a boracite crystal element, and a dc

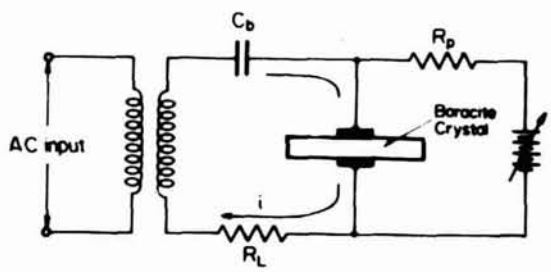

Fig. 7. Circuit of half-wave boracite rectifier.

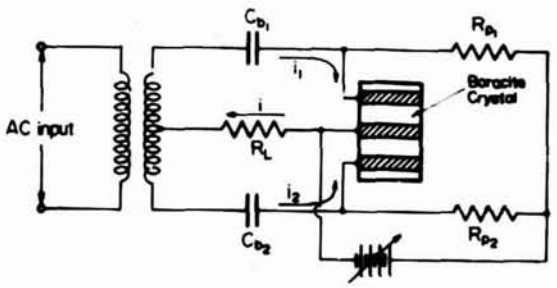

Fig. 8. Circuit of full-wave boracite rectifier.

control circuit. The boracite element in this case can be either a symmetric or asymmetric device. The dc control circuit consists of a variable dc voltage source and a large protective resistance R_p to block ac current. When a small ac voltage is applied followed by a dc voltage, a regulated current begins to flow at a critical dc voltage. Figure 9 shows a scope trace of such a regulated current. Because of

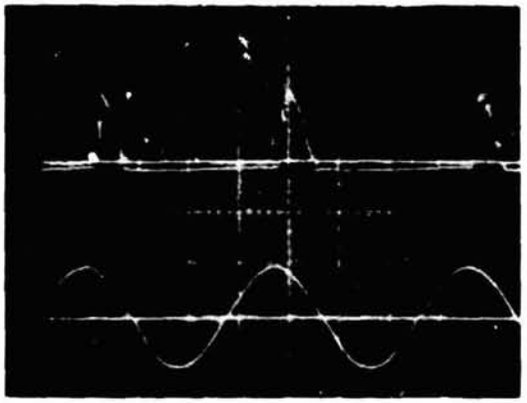

Fig.9. Scope trace of ac half-wave rectified current. Cd-Br boracite sandwich electrode sample with electrode spacing = 0.30mm, R_L = 100 Ω, R = 100KΩ, C_b = 10 μF, V_{dc} = 8.0V, and temp = 395° ± 2°C. Ac rectified current (upper trace): 0.05V/div. Applied 50Hz ac voltage (lower trace): 0.5V/div. Time: 5msec/div.

the threshold switching characteristics of boracite crystal, the current appears in the form of regularly repeated pulses. The direction of current is reversed when the polarity of dc voltage (V_{dc}) is reversed. For stable operation of the half-wave rectifier, an upper limit (maximum) exists for both V_{dc} and V_{ac}. For V_{dc}, it is about ten times the minimum voltage. The maximum of V_{ac} is much smaller than that of V_{dc}. The bias dc voltage, both minimum and maximum, required for the rectifying effect to take place increases with increasing current or power in the ac circuit. This observation cannot be explained but it seems that the response of the Cd boracite element is different when ac and dc are applied simultaneously as compared to the case of dc or ac used alone.

The full-wave rectifier of Fig. 8 consists of an ac source, a load resistance R_L, two blocking capacitances

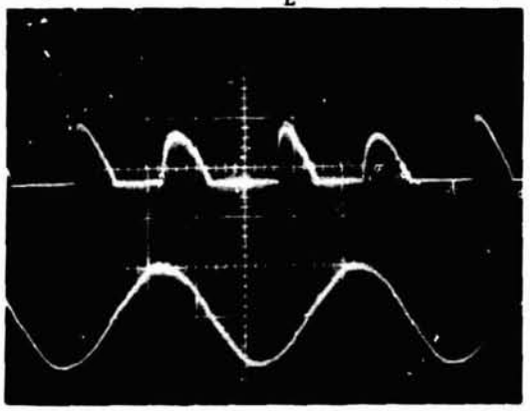

Fig.10. Scope trace of ac full-wave rectified current. Cd-Br boracite coplanar trielectrode sample with electrode spacing = 0.20mm; R_L=100Ω, R_p=100KΩ; C_{bI}, C_{bII}=10μF; V_{dc}=15V; and temp = 301° ± 2°C. Ac rectified current (upper trace): 0.1V/div. Applied 50 Hz ac voltage (lower trace): 0.5V/div. Time: 5 msec/div.

C_{b1}, C_{b2}, a boracite element, and a dc controlling circuit. The boracite element in this rectifier has three electrodes. In Fig. 8, the two side electrodes are positively biased with respect to the middle one. The current through R_L will be i_1 in the first half cycle of ac and i_2 in the next half cycle so that the full-wave rectification will be completed. The direction of current through R_L reverses when the polarity of side and middle electrodes is reversed. Figure 10 shows a scope trace of such a rectified current obtained by the circuit of Fig. 8. As in the case of half-wave rectification, the minimum dc bias voltage increased with increasing ac voltage.

The above examples are illustrative of potential usefulness. Other circuit applications of the Cd boracite switching devices seem possible.

Acknowledgments

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WHATEVER HAPPENED TO SILICON CARBIDE

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Summary

Silicon carbide has been used extensively as an abrasive, but only in the last twenty-five years has its potential as a semiconductor been exploited. The rationale for SiC semiconductor devices is their high temperature performance. Rectifiers, field effect transistors, charged particle detectors, and other devices operate efficiently at temperatures about 800°K.

It is the purpose of this paper to examine the progress made in SiC devices in the 1955-1975 time frame and suggest reasons for the present lack of interest in this unique material. The data given in this paper has been abstracted from previously published work.

Introduction

In the last seventy years, considerable use has been made of the abrasive characteristics of silicon carbide (hereafter SiC); however, only recently were its potentialities as a semiconductor exploited.[1-4] It is the purpose of this paper to discuss SiC devices in the 1955-1975 time frame. Since SiC device properties are intimately connected with its material properties, crystal growth and fabrication techniques will also be discussed. Finally, I will suggest reasons it is no longer considered a viable product for exploitation.

The work discussed in this paper was performed at various industrial and college research laboratories. These programs are no longer active, and there are no known plans or interest in their reactivation.

Physical and Chemical Properties

Silicon carbide exists in the hexagonal (α) and cubic (β) phases with the α phase occurring in a variety of polytypes. The various forms of SiC have the largest energy gaps found in common semiconductor materials, ranging from 2.39 eV (cubic) to 3.33 eV (2H). The bonding of Si and C atoms is basically covalent with about 12% ionic bonding. The structures are temperature stable below 1800°C and thus form a family of semiconductors useful for high temperature electronic devices. Table 1 shows the lattice parameters and energy gap (0°K) for the common polytypes.

Table 1. Lattice Constants and Energy Gap of Common SiC Polytypes

Structure	Lattice Parameters (Å)	Energy Gap (0°K)
2H	a = 3.09 , c = 5.048	3.33
4H	a = 3.09 , c = 10.05	3.26
6H	a = 3.0817, c = 15.1183	3.02
33R		3.01
15R	a = 3.079 , c = 37.78	2.986
21R	a = 3.079 , c = 52.88	2.86
8H		2.80 - 2.90
cubic-3c	a = 4.359	2.39

SiC is inert to nearly all laboratory reagents, and the usual techniques for chemical etching employ molten salt or salt mixtures (NaOH, Na_2O, borax) at temperatures above 600°C. Electrolytic etching, suitable for p-type material and etching with gaseous chlorine near 1000°C, may also be used.

The physical hardness and chemical inertness impose great restraints on device fabrication techniques. Although SiC technology has progressed along the same lines as that of silicon, many techniques had to be developed which were peculiar to SiC and which inevitably made the fabrication more difficult and expensive.

Methods of Preparation

The oldest and perhaps the best known method of SiC crystal growth is the sublimation method. This technique uses the vaporization of a SiC charge at about 2500°C into a cooler cavity with subsequent condensation. Initially the charge formed its own cavity, but more uniform crystals are grown when a thin graphite cylinder is used in the center of the charge. This thin cylinder also reduces the number of nucleations so that fewer but more perfect crystals are grown. The crystals are grown as thin hexagonal platelets, perpendicular to the growth cavity. Doped crystals, containing p-n junctions, can be prepared by adding proper dopants to the ambient during growth. The power rectifiers, to be described later, were prepared by this method.

Other methods of crystal growth are epitaxy, traveling solvent and solution growth.

The hexagonal α phase is grown epitaxially from 1725° to 1775°C with the cubic phase being grown from 1660°C to 1700°C. In both cases, equal molar percentages of CCl_4 and $SiCl_4$ are used. Polished and etched SiC crystals were generally used as substrates although Ryan and co-workers at Air Force Cambridge Research Laboratory have investigated the growth of SiC onto carbon substrates using the hydrogen reduction of methyltrichlorosilane (CH_3SiCl_3) (called the vapor-liquid-solid growth). At 1500°C, α-SiC whiskers on the order of 5 mm long by 1 mm diameter were grown. These whiskers were of the relatively rate 2H polytype.

SiC crystals have been grown together, and p-n junctions formed by passing a heat zone through two SiC crystals separated by a solvent metal (traveling solvent). The temperature gradient across the thin solvent zone causes dissolution at both solvent-solid interfaces. However, the equilibrium solubility of SiC in the solvent is greater at the hotter interface, a concentration gradient is established. The solute, then, will diffuse across the liquid zone and precipitate onto the cooler crystal. In this way, two dissimilar conductivity type SiC crystals can be grown together.

In the solution growth technique, a small amount of SiC is dissolved in molten Si (or in some cases Fe or Cr). As the melt is slowly cooled, the SiC becomes less soluble; and SiC crystals nucleate and grow in the crucible on prepared graphite substrates. The grown crystals are normally of the β-phase. Improvements in the crucible geometry and cooling rates have led to

cubic crystals up to 4 mm across and 0.1 mm thick. With the use of pure starting materials and extensive degassing, quite pure crystals can be grown; and electron mobilities of 500 cm^2 per volt-sec have been measured.

Device Techniques

The specific device techniques used will vary from device to device, and it is the purpose of this section to discuss fabrication methods in a general manner. In later sections when the individual devices are described, any special techniques required will be discussed.

The mechanical shaping of a hard crystal such as SiC is generally accomplished by scribing and breaking, lapping and polishing, ultrasonic cutting and air abrasive cutting. Boron carbide and/or diamond are used for these purposes since they are the only materials sufficiently hard.

Scribing the crystal with a diamond point and breaking it along the scribe line can also be used. As will be discussed later, a number of field effect transistors were fabricated on a single crystal; and these transistors were separated by scribing. Obviously this is best carried out on a scribing machine.

All of these mechanical shaping operations inevitably leave surface and bulk damage in the crystal. Some studies have indicated that the damage may propagate into the crystal by microcracks to a depth of tens of microns. For optimum device performance this damage must be removed, e.g., by chemical etching.

The etching of SiC using molten salts has been described in detail by Faust in 1959. In his paper, Faust describes the side of the SiC crystal which etches in a rough "wormy" pattern using molten salt on the carbon side and the side where the etch is smooth as the silicon side. This data has also been confirmed by Brack in 1965, using X-ray techniques.

Chang and co-workers studied the diffusion of aluminum into SiC from 1750°C to 2100°C, using both closed tube and open tube flowing gas techniques. Since the SiC crystals will decompose at these temperatures, it was necessary to provide an equilibrium pressure of Si and C vapor species around the crystals during the diffusion process. Griffiths in 1965 and Vodakov et al in 1966 reported further experiments using similar techniques. The activation energy for the diffusion of aluminum into SiC found in these three studies agreed within 5% (~4.8 eV).

Further refinements in unpublished work by Canepa and Roberts of the Westinghouse R&D Center resulting in junction depletion widths up to 25 μm were obtained using a combination of infinite source and finite source diffusion techniques.

Another technique is to use gaseous etching, e.g., Cl_2 at 950°C to 1050°C (Thibault) or $Cl_2 + O_2$ at 1000°C (Smith and Chang).

Characteristics of SiC Devices

Figure 1 shows the reverse characteristics of the IV properties of a SiC rectifier prepared by the grown junction method, operating at one ampere and 30°C and 500°C. The forward voltages of these devices, even at 500°C, are always larger than 1 volt (half wave average). Thus far, rectifiers operating up to 10 A have been fabricated, and specially processed low current devices have exhibited reverse capability of 600 PIV. The reverse characteristic of SiC rectifiers generally show a "soft" breakover, rather than the avalanche breakdown sometimes noted in silicon. This is generally attributed to the carrier generation mechanism at the junction and to local areas breaking down at different voltages, so that the total effect is one of gradually increasing reverse current.

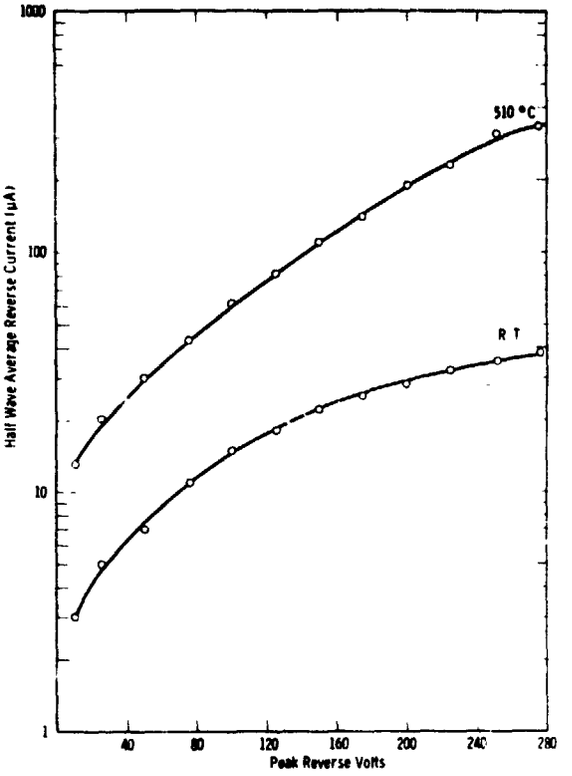

Figure 1. Representative properties of silicon carbide grown junction rectifiers - reverse characteristics

Although very limited life test data have been obtained for these grown junction rectifiers, a few devices have been operated at several amperes for up to 200 hours at 500°C in air, with no change in electrical characteristics. Devices operating at one ampere and using approximately the same encapsulation have been successfully life tested for 1000 hours at 500°C.

The operation of a p-n junction nuclear particle or photon detector depends on the collection of electron-hole pairs produced by the ionizing particle or photon as it passes through the detector. The electron-hole pairs are separated in the junction region, collected, and give rise to a charge or voltage pulse.

Silicon photovoltaic diodes have been developed for the detection of infrared and visible radiation. These diodes exhibit a sharp drop in response as the wavelength of the incident light approaches the ultraviolet region with most detectors showing negligible response below 3000 Å. This decreasing response is due to the increase in the absorption coefficient with decreasing wavelength. A large absorption coefficient indicates nearly all the light will be absorbed at the surface of the device, and electron-hole pairs generated may be at a great distance from the p-n junction. Thus, surface effects, such as carrier recombination, will decrease the response of the detector.

SiC, with a band gap near 3.0 eV, has an absorption coefficient several orders of magnitude less than that of Si at 4000 Å, and therefore surface effects would not be so important. Detectors have been prepared from SiC, and these devices were found to have a spectral response which were a maximum in the ultraviolet region and which could be shifted by varying the junction depth.

A simple theoretical model was originally derived by Chang and Campbell which quantitatively explained the dependence of the peak wavelength on the junction depth and the depletion width of the diode. Considered in this model were the wavelength and temperature dependences of the absorption coefficient in SiC below the band edge. An approximation was made that at the peak response wavelength the total number of electron-hole pairs generated in the depletion layer is a maximum for a given intensity of transmitted radiation at the surface

Figure 2 shows the variation of peak response wavelength calculated from this model. The curves are shown for values of the effective depletion width (w) from w = 1 micron to w = 10 microns.

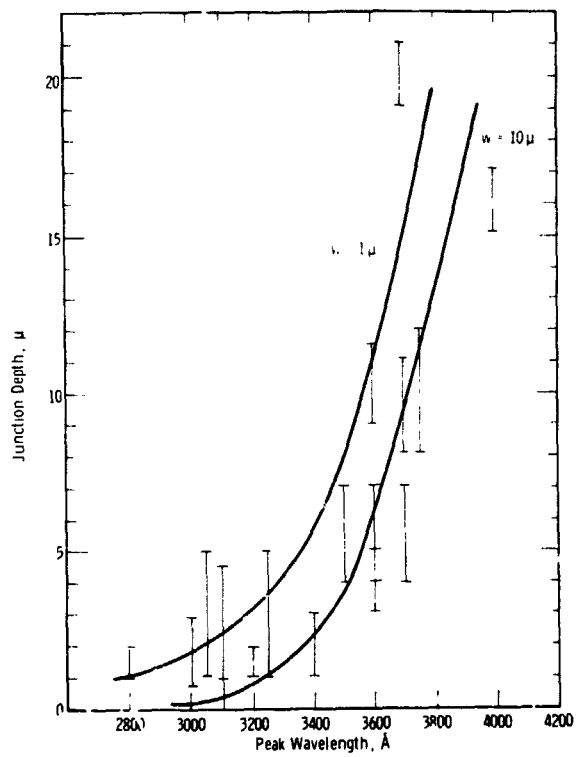

Figure 2. Peak spectral response of silicon carbide junction diode as a function of junction depth (after Campbell and Chang)

In addition to these photon detectors, SiC diode structures, specially prepared with graded junctions, have been used to detect alpha particles; and with the addition of a conversion layer, thermal neutrons have been counted.

The fission products of U-235 irradiated with thermal neutrons are not unique but have a distribution with two peaks occurring in the fission product mass distribution curve. The total energy liberated is 157 MeV with peaks at 66 and 91 MeV. Figure 3 shows a comparison of the alpha and fission product spectra for a SiC diode. The fission products spectra are very close to those predicted from the α-particle response taking into account the different distribution in the incident energy. The SiC diode, which had a peaked α-spectra, also shows a peak fission product spectra; in fact, the fission spectra of the diode resolves the double peaks.

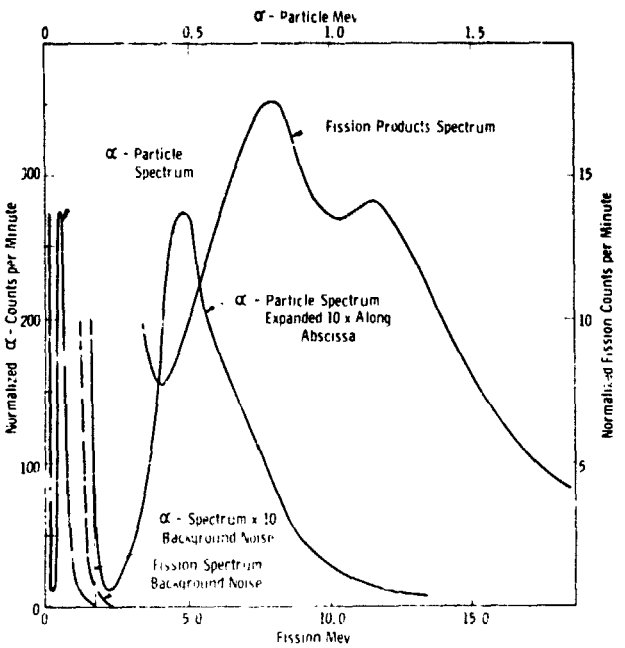

Figure 3. Comparison of alpha particle and fission fragment counting of silicon carbide junction diode (after Canepa et al)

Tunnel diodes in SiC can be made by forming a heavily doped alloyed junction in either n- or p-type degenerate SiC crystals, using a very fast alloying cycle similar in principle to that originally used to produce Ge tunnel diodes. Degenerate n-type SiC can be grown readily with heavy nitrogen doping. The p-type degeneracy in SiC cannot be established until the uncompensated acceptor level approaches 10^{20} - 10^{21} cm^{-3}, which has not been achieved.

An operable SiC tunnel diode was reported by Kutz in 1964. The junction was formed by alloying Si in a nitrogen-containing atmosphere to very heavily Al-doped α-SiC crystals (4.5×10^{20} - 9×10^{20} uncompensated acceptors cm^{-3}). The highest peak-to-valley current ratio achieved was 1.37 at room temperature, but negative resistance was observed at temperatures as high as 500°C. The peak voltage is unusually high, approximately 0.9V and 24°C. Figure 4 shows the IV characteristics of a SiC tunnel diode at several temperatures.

The channel dimensions and other device dimensions in a SiC junction gate field effect transistors are quite small due to the low carrier lifetime and correspondingly short diffusion lengths. Thus, the fabrication of these devices require photolithographic techniques. Using a self-masked diffusion process and gaseous etching (see Figure 5), Chang et al fabricated SiC FET's which exhibited current gain from room temperature to 500°C.

A silicon carbide thermistor was described by Campbell in 1973. This device takes advantage of the exponential decrease in resistance of a SiC junction

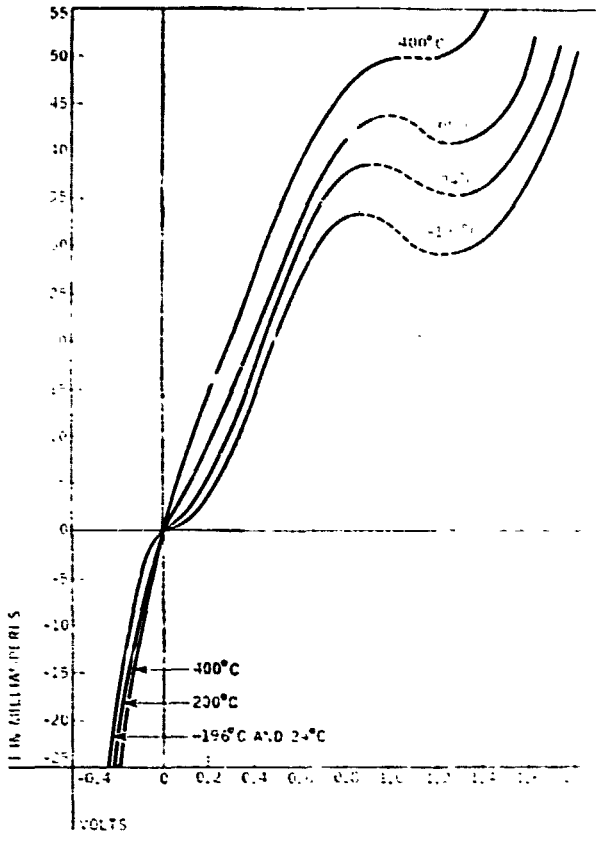

Figure 4. IV characteristics of silicon carbide tunnel diode from -196°C to 400°C (after Rutz)

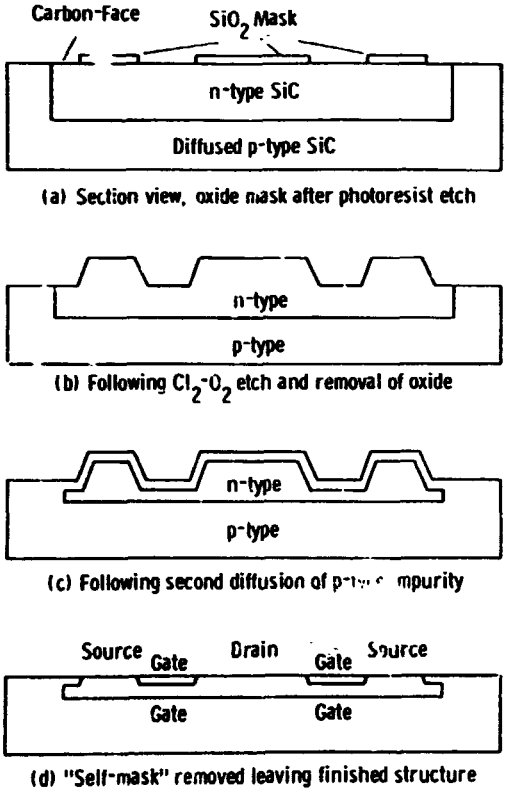

Figure 5. Self-masked diffusion technique

with temperature. Since this resistance changes by an order of magnitude for every 100°C temperature change, a change of a few tenths of a degree is easily detected. Prototype devices have been operated several thousand hours (with frequent cycling) without degradation.

Conclusions

Thus far I have given a brief outline of SiC semiconductor devices and methods for their fabrication. The data given show that SiC devices are feasible and have properties that should be of interest to several high technology fields. The question then arises: Why is there so little interest in this material today, and why are there no SiC devices current in use?

I believe there are three specific reasons for this. First, in the later 1960's there was a decline in corporate and Government R&D funding due to economic conditions. At this time, SiC had not carved out its niche in the semiconductor device market and thus was a prime candidate for any cutback. A second, somewhat related, cause was the disappearance of the small market where SiC devices did have a chance to make an impact. These were high technology areas such as near sun space missions, supersonic and hypersonic aircraft, etc. When these markets disappeared, much of the interest in SiC also disappeared. Finally, the fabrication techniques for SiC devices (including growth methods) did not improve appreciably in the twenty years under question. This lack of progress may have been due to misplaced emphasis in device programs, but the net result was that the fabrication techniques for SiC devices improved only slightly in this time span.

Now, where do we go from here? I see no viable market for SiC semiconductor devices in the near future. Improved Si devices, better insulation, improved circuit design all mitigate against any extensive use of SiC devices. This may be viewed as an unfortunate circumstance to many of us who were professionally and emotionally involved with this interesting material for a number of years.

Acknowledgments

I would like to thank my colleagues for their contributions to the given data. I also wish to thank the Executive Committee and fellow members of the International Committee on Silicon Carbide for their encouragement.

References

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-55 TO +200°C 12 BIT ANALOG-TO-DIGITAL CONVERTER

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The 12 bit successive approximation A/D converter offers moderately high speed precision data conversion at a reasonable level of cost and complexity. The ADC10HT[1] extends this capability over a temperature range of -55 to +200°C. No missing-code performance is maintained over the entire temperature range. The converter is completely self-contained with internal clock and +10 volt reference. Figure 1 shows a block diagram of the ADC10HT.

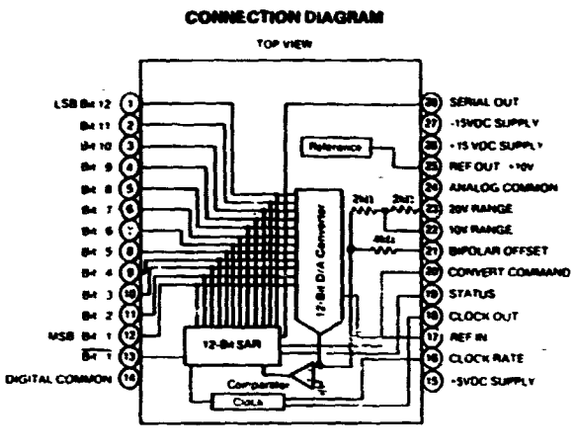

Figure 1

The internal 12 bit D/A converter is a monolithic dielectrically isolated chip.[2] The successive approximation register (SAR) is a commercially available CMOS chip. The clock and the comparator were designed with a single LM119 dual comparator made with conventional junction isolated bipolar technology. The clock also contains an MOS capacitor chip and a nichrome thin film resistor network chip. These five chips make up the basic A/D converter. The reference circuit consists of a dielectrically isolated op amp chip, zener diode and nichrome thin film resistor network.[3] The ADC10HT can be used with an external +10V reference, if desired.

The SAR could have been either bipolar TTL or CMOS since both technologies exhibit altered but useful characteristics at temperatures well above 200°C. However, CMOS devices offer low power dissipation, so that the internal temperature of the hybrid circuit does not rise as much from self-heating. Also, CMOS SAR's have better noise margins than TTL devices at high temperatures.

A major problem at high temperature is that caused by pn junction leakage currents. The largest of these currents is the epi to substrate current in junction isolated circuits due to the very large size of the isolation pn junction relative to the device junctions. In CMOS circuits, these leakages are returned to the supplies, and therefore, do not degrade performance. Therefore, the logic keeps working at temperatures up to 250°C. Above that temperature, a four layer latch mechanism, inherent to junction isolated CMOS, limits the devices performance.

Since the internal D/A converter is dielectrically isolated, there is no epi to substrate leakage component. By eliminating this error mechanism, the useful temperature range of the device is increased. Dielectric isolation is also used in the reference circuit operational amplifier for similar reasons.

Although the dual comparator is junction isolated, the epi to substrate leakage currents are second stage effects and[4] furthermore, tend to cancel out. Another potential difficulty in bipolar circuits is the poor performance of lateral pnp transistors at high temperature. This particular comparator does not contain any lateral transistors. Instead, resistors are used for level shifting purposes.

The nichrome thin film resistor networks are stabilized at over 500°C and, therefore, are stable[5] at temperatures well above 200°C. The current densities have been reduced by a factor of three from those densities used in normal commercial practice to prevent electromigration at high temperature.[6]

The absolute value of resistors in the converter is not critical, but resistor tracking with time and temperature is very important. For this reason, critical resistors of different values are comprised of equal resistance elements. Thus, even though the resistors may shift due to the extreme ambient conditions, the linearity, gain and offset of the A/D converter itself should remain stable

The converter is packaged in a conventional 28 pin side-brazed ceramic package. Figure 2 shows the placement of the various chips in this package. The eight chips are eutectically attached to the substrate and ultrasonic wire-bonded to a double layer thick film substrate. The substrate is then attached to the header using a high temperature gold tin preform.

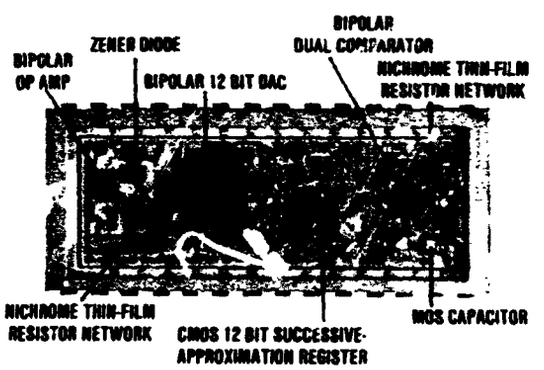

Figure 2

A platinum/palladium doped thick film gold system is used to minimize purple plague. Average wirebond pull strengths of three grams after 1000 hours at 250°C have been obtained. A 1000 hour test at 250°C exhibited only an 80%

increase in bond resistances.

Connection between the double layer substrate and the ceramic side-brazed package is made with gold wire. The converter is hermetically sealed using a gold germanium preform to attach the ceramic cap.

To ensure the reliability of the converter, all parts are burned-in at 200°C and all parts are 100% screened. Due to the limited life of the connectors, the temperature testing and burn-in fixtures use printed circuit boards that pass through the oven doors, thus allowing board connection to be made at room temperature. The test sockets themselves are zero insertion force types made of Torlon with berrylium/nickel contacts. The boards are made of Norplex copper clad polyimide with nickel plating. A high-temperature solder with a 300°C melting point is used for the test boards.

Table I shows the important electrical specifications for the ADC10HT. Figure 3 shows linearity error vs. conversion speed and indicates that 12 bit accuracy can be attained at 25μs. The clock frequency can be adjusted externally.

TABLE I

Typical Performance

Resolution	12 bits
Accuracy at 25°C	
Gain error: ±0.05% (adjustable to zero)	
Offset error: ±0.05% (adjustable to zero)	
Linearity error: ±0.005%	
Drift ($-55^{\circ}C \leq T_A \leq +200^{\circ}C$)	
Gain: ±15 ppm/°C	
Offset (unipolar): ±1 ppm/°C	
Linearity: ±0.5 ppm/°C	

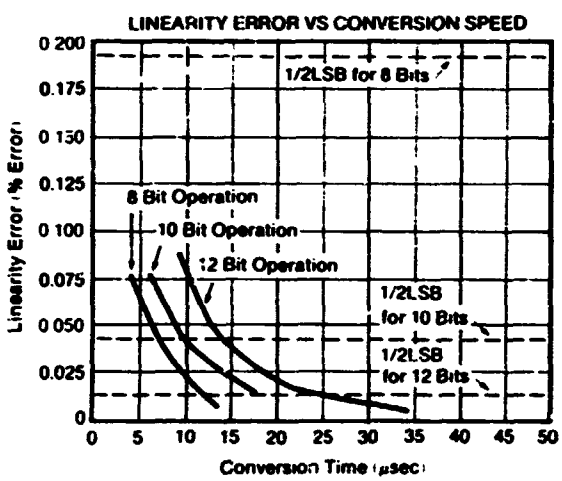

Figure 3

Shift in bipolar offset and gain vs. time during operation at 200°C are shown for three devices in Figures 4 and 5. Both parameters can be adjusted to zero initially by the use of external trim resistors. Offset in the unipolar mode is much less than the bipolar shift shown in Figure 4. Differential nonlinearity shifts with time during operation at 200°C

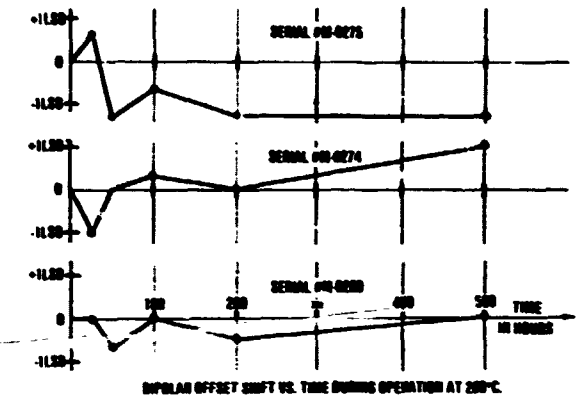

Figure 4

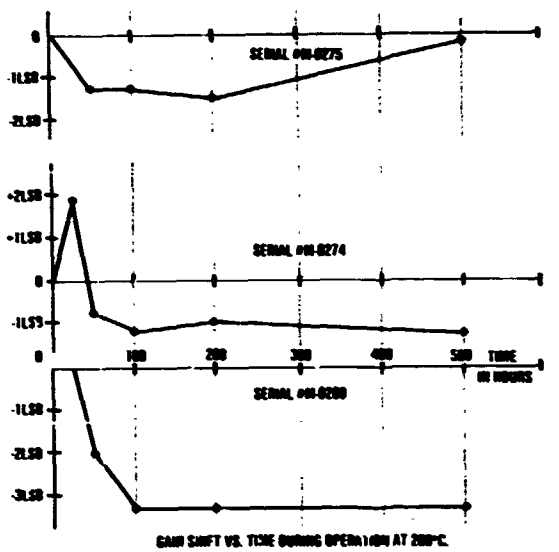

Figure 5

are shown in Figure 6. Differential nonlinearity is defined as the deviation from the ideal one LSB step size. Overall nonlinearity is not shown but has similar shift vs. time character-

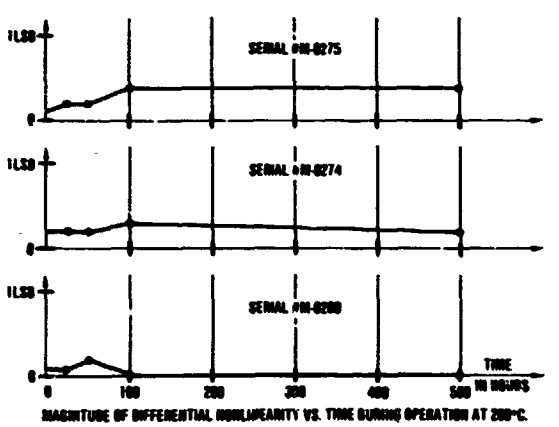

Figure 6

istics to that of differential nonlinearity. Figure 7 shows differential nonlinearity vs. temperature. All parts are tested for no missing codes over the temperature range.

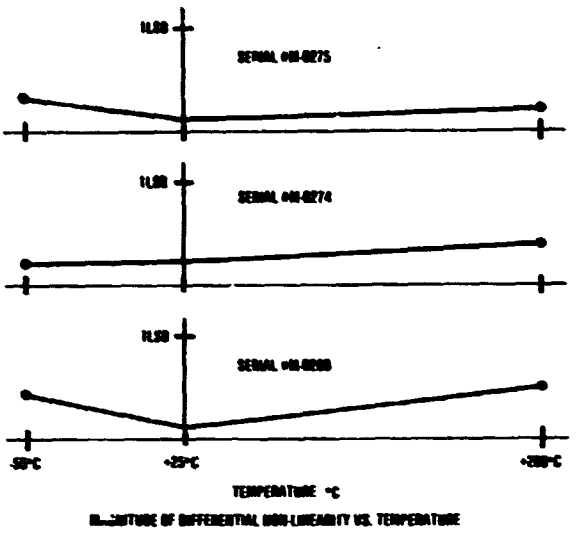

Figure 7

Future Direction

Although the present design was not intended for use above 200°C, it is believed that a successive approximation analog-to-digital converter could be built for 300°C operation with 8 bit performance. Lower power circuitry will reduce peak junction temperatures. The present circuit dissipates most of its power in the digital-to-analog converter chip and in the reference. Both circuits could be redesigned to operate at lower supply voltage and hence lower power.

Although the zener diode used in the reference exhibits a nonlinear temperature coefficient above +125°C, acceptable performance was obtained to +200°C. At much higher temperatures, a nonlinear zener temperature coefficient compensation method is likely to be required.

Very careful attention must be paid to matching of the internal D to A converter's collector-base leakage currents if nonlinear transfer characteristics are to be avoided at high temperatures. Although leakage currents can still cause gain and offset errors, these can be removed using digital techniques.[7]

The CMOS high temperature latch condition can be eliminated by using dielectric isolation. I^2L logic circuitry also has potential for use in the SAR.

Finally, a high temperature metal system such as the P_t, T_i Au metallization reported on by Peck and Zierdt [8] is required if reasonable MTBF is to be obtained at 300°C.

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PROCESS CHARACTERISTICS AND DESIGN METHODS FOR A 300° QUAD OP AMP

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SUMMARY

There is a growing need for electronics which operate over the 125°C to 300°C temperature range in such applications as well logging, jet engine control and industrial process control. This paper presents the results of an IC process characterization, circuit design and reliability studies whose objective is the development of a quad op amp intended for use up to 300°C to serve those requirements.

PROCESS CHARACTERIZATION

A dielectrically isolated complementary vertical bipolar process was chosen to fabricate the op amp. DI eliminates isolation leakage and the possibility of latch up, two of the major high temperature sources of circuit failure which are present in junction isolated processes. The complementary vertical PNP offers superior AC and DC characteristics compared to a lateral PNP allowing simpler stabilization methods. The junctions are relatively deep (> 3u) to minimize sensitivity to interconnect pitting. Device cross sections are shown in Figure 1.

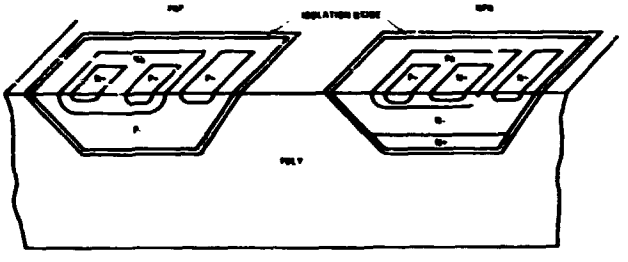


Figure 1. Device Cross Sections

Characterization of the NPN and PNP show them to be quite suitable for use up to 300°C, however certain parameters change drastically over the temperature range and require special consideration in a high temperature design. Leakage currents increase to micro amps as shown in Figure 2. An important point illustrated in the figure is the fact that I_{CES} is several times larger than I_{CBO}. Significant, but not shown on the figure, is the fact that the leakage currents for matched devices on the same chip typically match to 10%. These characteristics are exploited in the circuit design.

The effect of leakage current on NPN common emitter characteristics can be seen in the 300°C photo of Figure 3. The base current has been offset by 4.5 ua to compensate for I_{CBO} bringing the first trace to the origin. This illustrates the base current reversal which occurs before 300°C. One can also observe the monotonic increase in h_{fe} with temperature in the photos.

V_{BE} decreases with the well known -2mV/°C slope to about 100mv as shown in Figure 4.

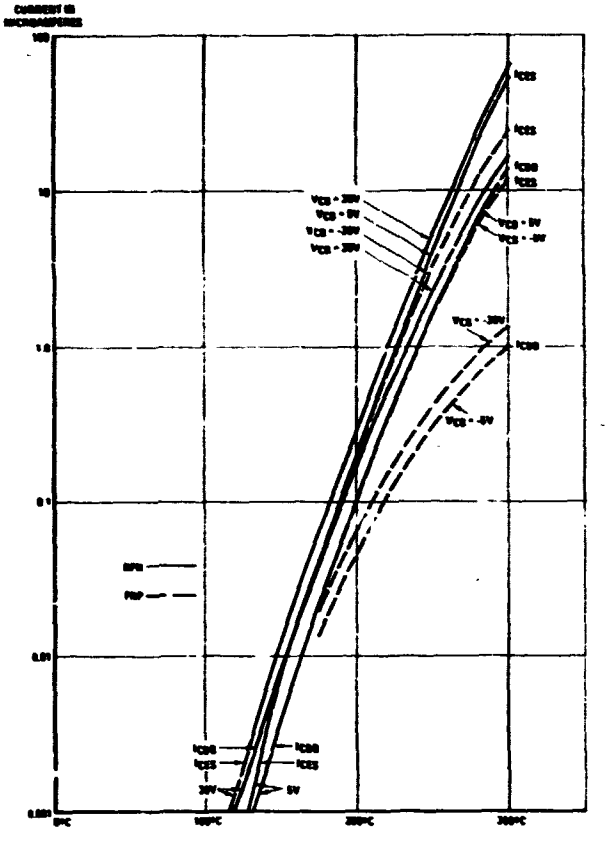


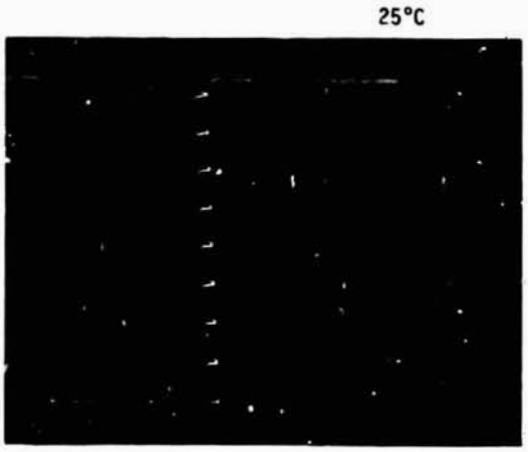
Figure 2. Leakage Current vs. Temperature

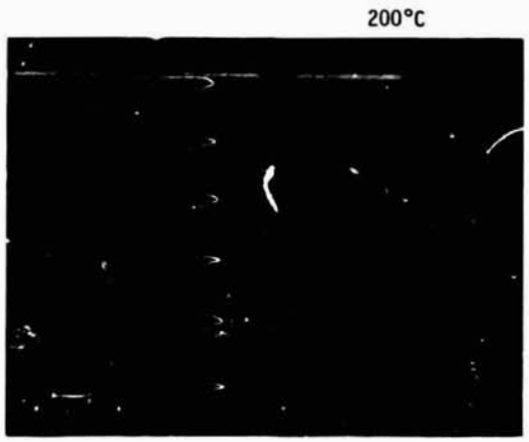
RELIABILITY

Reliability is a particularly important consideration in high temperature circuit design because most failure mechanisms have exponential temperature dependence. Perhaps the greatest concern is that of interconnect reliability. Calculations using Black's expression[1] for electromigration in Al interconnect predict MTF of greater than 4 years for the maximum current density to be used in the op amp. This far exceeds the goal of 100 hours operating life. 325°C life tests have been conducted on Al interconnect test structures at $J = 3.3 \times 10^4$ A/cm^2, on small geometry transistors at 1 ma and V_{CE} = 30V and on minimum area contacts to P+ and N+ silicon at 4 ma all fabricated with the proposed process for more than 500 hours each. No failures have been observed.

Another potential source of failure, parasitic MOS formation, is eliminated by isolation of each device in its own dielectrically isolated island. This eliminates the isolation diffusion which can act as drain for a parasitic PMOS in JI circuits.

*Work sponsored by Sandia Laboratories, Albuquerque, New Mexico





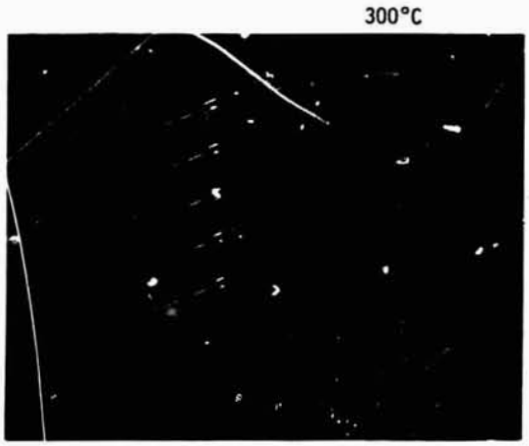


Figure 3. NPN Common Emitter Characteristics at Three Temperatures

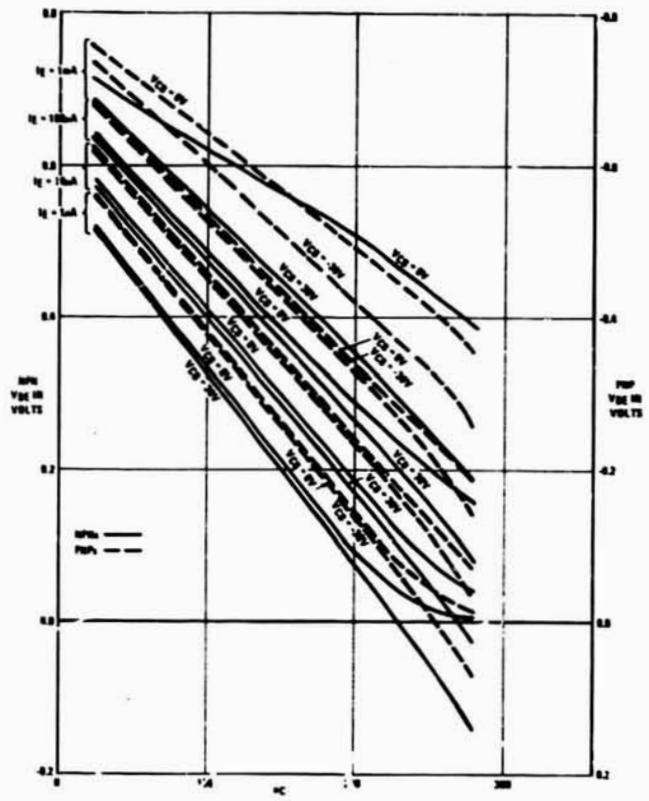


Figure 4. Temperature Dependence of V_{BE}

SPECIFICATIONS

An initial set of target specifications was arrived at. They were based on preliminary high temperature device measurements and extrapolations from available data. The target specifications are given in Table 1.

CIRCUIT DESIGN

Conceptually, certain things had to be done differently from a similar design for the commercial or military temperature ranges. Leakage currents put practical limitations on minimum operating bias current levels. Diode connected transistors are unworkable because of low forward biased junction voltages. Base current reverses because of increasing collector to base leakages and increasing beta. This last consideration means that the base voltage node for strings of current sources must have current sinking as well as sourcing capability at high temperatures. Diffused resistors are almost twice their room temperature values at 300°C. While this must be borne in mind, this high positive temperature coefficient can be used to offset changes in the forward biased junction voltages.

The primary bias circuit consists of a buried zener, Z2, in Figure 5, biased by a pair of 12K resistors, R1, and R16, going to the positive and negative power supplies, which develops a current through the 9K resistor, R11, and diodes, D5 and D6, through the four Q11's and the four Q20's (whose bases and emitters are parallel but whose collectors go to separate amplifiers). A buried zener was chosen because it is quieter than a surface zener. The temperature coefficients of the zener, the transistor base-emitters,

and the diodes approximately cancel the temperature coefficient of the resistor, R11, keeping the current delivered to the positive and negative current source base nodes approximately constant over the temperature range.

The input stage of the amplifier consists of the differential PNP pair, Q21 and Q22, along with Q16, Q17 and R13 (which make up a leakage current compensation network) and the current source consisting of Q5 and R4. PNP devices were chosen for the input pair because their collector to base leakage is significantly lower than that of the NPN devices. R13 provides most of the collector base voltage for Q16 and Q17 whose ICBO's cancel those of Q21 and Q22 to within the limits of their match. The collectors of Q21 and Q22 go to the following stage which consists of Q26 and Q27.

NPN transistors Q26 and Q27 along with R18 and R19 constitute grounded base stages. They translate the signal toward the positive side of the circuit. The stage consisting of Q27 and R19 shields the input device, Q22, from the large voltage excursions of the high impedance node to which its collector is common. The collector of Q26 drives the current mirror stage.

The current mirror consists of Q2, Q3, Q7, Q8, Q12, Q13, D1, D2, D3, D4, Z1 and R3. The primary part of the mirror consists of Q7, Q8 and Q13. Q12 is added to make the collector to base voltage of Q7 equal to that of Q8. This removes a small offset problem due to h_{rb} effects but (more importantly in this case)

TABLE 1

TARGET SPECIFICATIONS AND BREADBOARD RESULTS

Parameter	Temperature	Limit	BB	Units
Offset Voltage	25°C	3.0 <	0.2	mV
	300°C	6.0 <	-5.3	mV
Avg. Offset Voltage Drift	25°C to 300°C	10 <	20	uV/°C
Input Bias Current	300°C	5 <	2.1	uA
Input Offset Current	300°C	1.3 <	3.4	uA
Common Mode Input Range	25°C to 300°C	> ±10	±13.9	V
Differential Input Signal	25°C to 300°C	7 <		V
Common Mode Rejection Ratio	300°C	> 60	71.7	dB
Voltage Gain	300°C	> 70	71.9	dB
Channel Separation	300°C	> 80		dB
Gain Bandwidth	300°C	> 3		MHz
Output Voltage Swing	25°C to 300°C	> ±10	13.7	V
Slew Rate	300°C	> ±2		V/usec
Output Current	300°C	5 <		mA
Power Supply Rejection Ratio	300°C	> 60	71.7	dB
Noise	25°C	8 <		$nv/\sqrt{Hz}$

equalizes the collector base leakages of Q7 and Q8. Ordinarily, Q8 and Q12 would be connected as transdiodes but, because the forward biased junction voltages are so low at high temperatures, D2 and D3 are used to tie the base to the collector of Q8 and Z1 is used to tie the base to the collector of Q12. At low temperatures D2 and D3 are forward biased by the base drive requirements of Q7 and Q8 as Z1 is reverse biased by the base drive requirements of Q12 and Q13. At high temperatures Q2 and Q3 supply ICES to forward bias D2 and D3 and reverse bias Z1 as well as supply the reversed base current of Q7 and Q8 and of Q12 and Q13. D1 and D4 provide a voltage drop equal to D2 and D3 to make the voltage across Q2 more nearly the same as that across Q3. R3 provides most of the voltage for Q3 (and, therefore, Q2). The collector of Q13 is common with the high impedance node.

The next stage consists of a complementary pair of emitter followers, Q15 and Q18, biased by current sources consisting of Q6 and R5 and of Q28 and R20 respectively. There is also a leakage current compensation network associated with each follower consisting of Q9 and R7 for Q15 and Q24 and R14 for Q18. The bases of Q15 and Q18 are common to the high impedance node. Difference in ICBO between Q15 and Q18 at high temperature would be reflected to the amplifier input as an offset.

No special design considerations because of high temperature were necessary in the output stage design which consists of Q14 and Q19 driven by Q15 and Q18 respectively.

The positive and negative current source base nodes remain to be discussed. The positive node is set up by Q4 and R2. Emitter follower Q10 supplies the base drive requirements of Q4, Q5 and Q6 until the base currents reverse at high temperature. Then they are supplied by Q1's ICES whose excess is then supplied by the emitter follower. This excess flowing through R6 and Q10 provides some collector to base voltage for Q4. ICES seems to be a minimum of three times ICBO at 300°C so Q1 is made a double sized device because three sources of ICBO (one of them, Q5, is double sized) have to be supplied by it along with excess for the emitter follower. The same considerations apply to the negative node which is set up by Q25 and R17. Q23 serves as the emitter follower, Q29 the source of ICES and Q25, Q26, Q27 and Q28 receive their base drive from the node.

BREADBOARD

In order to test the validity of the design it was breadboarded using four subcircuit chips made from an existing circuit by custom interconnect patterns. A schematic of the breadboard is shown in Figure 6. The package pins are designated as follows. The first number designates the type of package then there is a dash and the second number designates the pin on that package type. Package type 1 contained the primary bias circuitry. Package type 2 contained the negative bias circuitry. Package type 3 contained the input stage and positive bias circuitry. Package type 4 contained the current mirror and output circuitry.

Several breadboards made up of packaged subcircuits were socket mounted inside an oven door, externally connected as in Figure 6 and tested over temperature. Results are shown in Table 1.

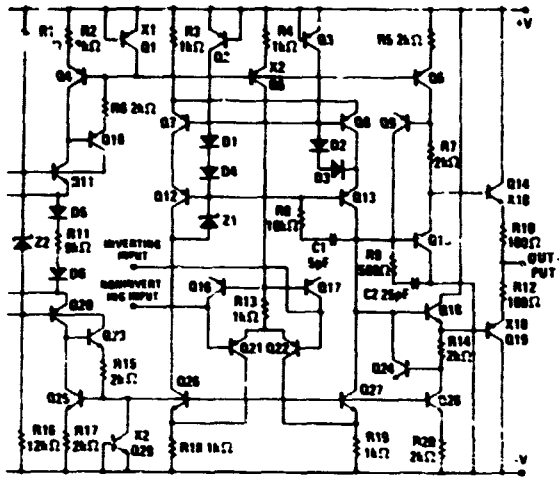


Figure 5. Circuit Schematic

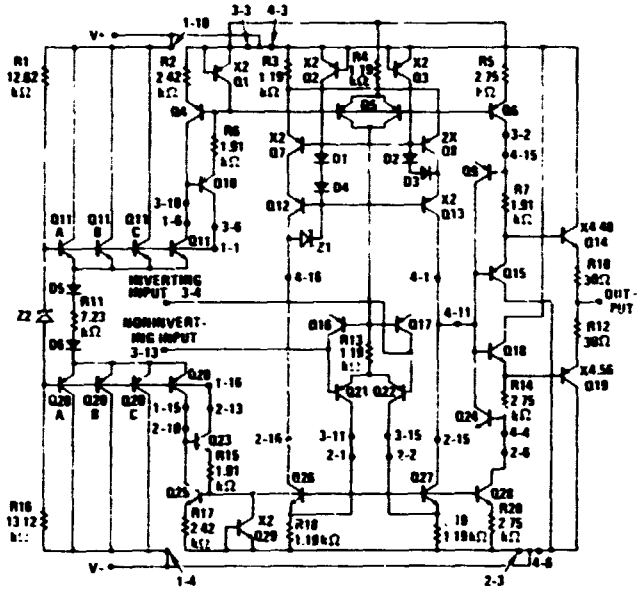


Figure 6. Breadboard Schematic

COMPUTER SIMULATIONS

The computer simulations were done using a Harris version of SPICE called SLICE. Problems arose with the models at 300°C.

Saturation current for the reverse biased diode is modeled as having a linear voltage dependence matching the true value at $V_F = 0$ to solve an underflow problem in the computer. At 300°C I_S is so high that this approximation has the effect of placing a shunt resistor of less than 10K Ω across each reverse biased junction. The problem was circumvented by using a smaller value for saturation current which results in the model giving higher V_{BE} than true value but otherwise accurately representing the device. Leakage current was modeled by placing a current source shunted by a resistor (to simulate voltage dependence) across each reverse biased junction.

The simulations were used to set the values for the compensation networks C1 - R8 and C2 - R9. They predict 3.5 MHz gain bandwidth, 2.6V/us slew rate at 300°C. Simulated noise at 25°C is 8.7 nv/$\sqrt{Hz}$.

CONCLUSION

A dielectrically isolated complementary vertical bipolar process has been characterized for use at 300°C and been shown to be useful and reliable for linear design at that temperature. Circuit design methods for a 300°C op amp have been developed and demonstrated on IC test chips and an entire op amp design has been proposed.

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HYBRID A/D CONVERTER FOR 200°C OPERATION

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ABSTRACT

This paper describes the design and development of a high performance hybrid 12 bit analog to digital converter, which will operate reliably at 200°C. A product of this type was found to be necessary in areas such as geothermal probing, oil-well logging, jet engine and nuclear reactor monitoring, and other applications where the environments may reach temperatures of up to 200°C. This product represents an advancement in electronics as it proved the operation of integrated circuits at high temperature, as well as providing information about both the electrical and mechanical reliability of hybrid circuits at 200°C. Because the circuit design of the A/D converter involved both digital and linear circuitry, this produced an opportunity to evaluate the performance of both technologies at 200°C. Initial mechanical failure modes led to researching more reliable methods of wire bonding and die attachment. The result of this work was a 12 bit A/D converter which will operate at 200°C with .05% linearity, 1% accuracy, 350 µSec conversion time, and only 455mW power consumption. This product also necessitated the development of a unique three metal system in which aluminum wire bonding is done utilizing aluminum bonding pads, gold wire bonding to all gold areas, and employment of a nickel interface between gold and aluminum connections. This sytem totally eliminates the formation of intermetallics at the bonding interface which can lead to bond failure.

INTRODUCTION

Recently the electronics industry has been made aware of the need for electronic components and systems which will operate at temperatures as high as 200°C. These applications include geothermal probing, oil well logging, jet engine and nuclear reactor monitoring and other hostile environments where the temperature may reach 200°C or higher. In some of these applications, as in oil well logging and geothermal probing, it is necessary to transmit data through long lengths of cable which run from deep into the earth to the surface.[1] These applications are where a high temperature A to D converter becomes highly desirable. Transmitting low level analog data over a long distance such as this would be very difficult without introducing significant extraneous errors. Through the use of an A to D converter it becomes possible to take outputs from strain gauges and thermocouples, convert them to "ones" and "zeros" and then transmit this data digitally to the surface.

ADVANTAGES OF HYBRIDS

An A to D converter can be fabricated in many different forms such as a module, printed circuit board, or hybrid circuit. Hybrid reliability at 125°C has been proven to be excellent through many thousands of hours of qualification tests. This reputation makes hybrid technology a wise choice for 200°C operation. A hybrid circuit can contain several different I.C.s in one small package, which is advantageous in applications where space is limited.

A TO D CIRCUIT DESIGN

An A to D converter proved to be a challenging product to design and evaluate at 200°C due to the fact that little information concerning the different types of components and their properties at high temperature was available. Passive components, such as resistors and capacitors and active components including transistors and integrated circuits required extensive analysis and evaluation. The final A/D design employs both linear and digital circuitry.

In the design of the MN5700, reliability was considered of prime importance. Two factors that significantly effect the reliability of any circuit are power and level of complexity. Research in high temperature electronics has shown that the rate of aging, those factors that produce changes in parameter of key components, will approximately double with each 10°C temperature rise.[2]

For a hybrid circuit the substrate temperature will increase as the power consumption increases. As a design goal the typical substrate to ambient temperature rise was not to exceed 10°C. The 32 pin double PIP Package, selected primarily for its form factor, has a typical substrate to ambient rise of 27°C/Watt.[3] Thus to keep this rise under 10°C, the typical power consumption was limited to 311 milliwatts. To reduce the complexity, as few I.C.s were used as possible.

There are several different approaches to A to D conversion which are currently used. The MN5700 uses the successive approximation method. This allows a converter to be made using few components and has good characteristics in speed, resolution, and accuracy. A successive approximation A to D converter consists of four sections, D to A converter, reference, comparator, and successive approximation register (SAR). See Figure 1. Each of these sections will be discussed showing the design considerations for 200°C operation.

D to A Converter

The D to A section of the MN5700 utilizes a voltage switching R-2R ladder network. The switch is CMOS and connects each leg of the ladder either to ground or a reference voltage. See Figure 2. A CMOS switch was chosen because of its low power consumption and evaluations showed it to be reliable at 200°C.

Reference

The reference circuit shown in Figure 3 consists of a temperature compensated zener diode and a dielectrically isolated op-amp. The zener was found to be accurate to about 10ppm/°C from 25°C to 125°C. From 125°C to 200°C the temperature coefficient increased to 40ppm/°C. Figure 4 shows a graph of zener voltage vs. temperature.

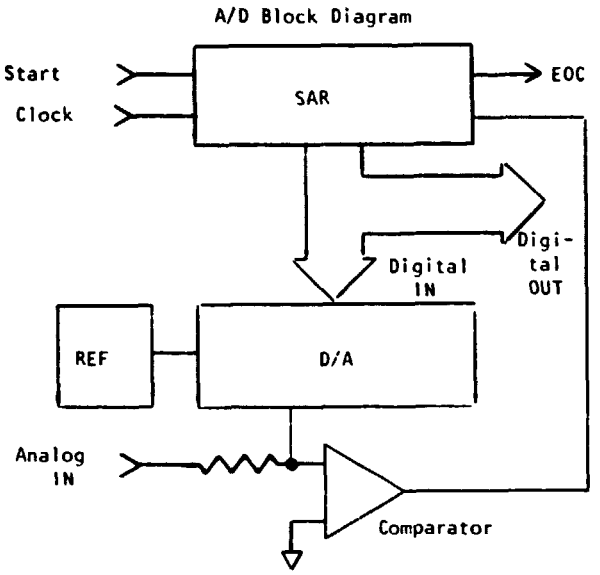

FIGURE 1

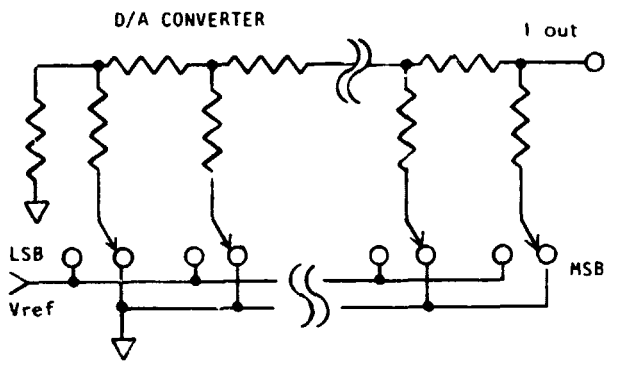

FIGURE 2

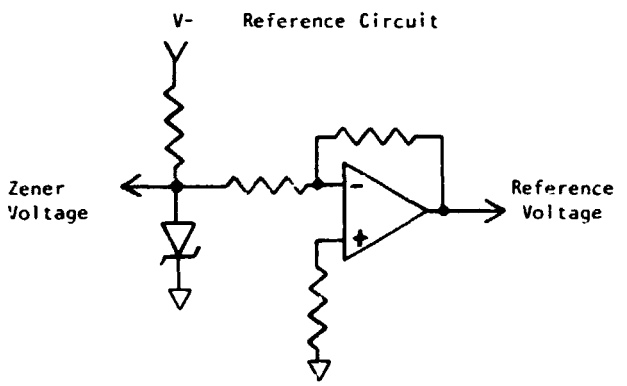

FIGURE 3

Research and evaluation showed that a dielectrically isolated op-amp was the best choice for 200°C operation. Most silicon bipolar I.C.s use junction isolation between transistors. These types of circuits show transistor interaction at 200°C.[3] I.C.s which are manufactured using dielectric isolation have the active areas separated by an insulating layer of material. This reduces transistor interaction and also reduces leakage current to the substrate under high temperature conditions.[4]

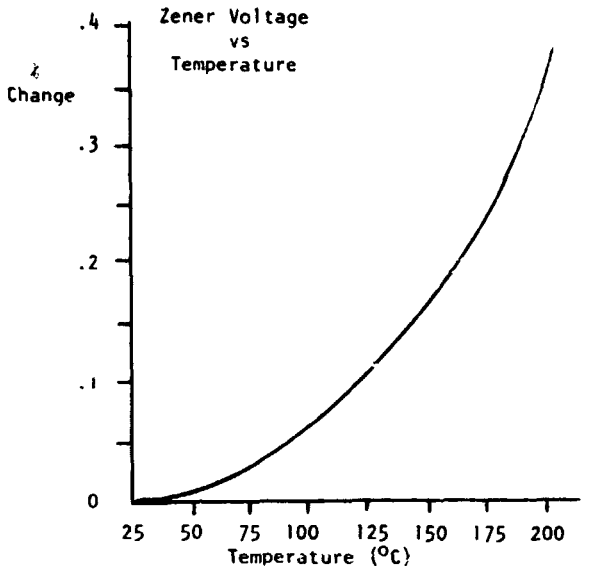

Figure 4

The change in the reference voltage at 200°C was found to be typically .2%. The circuit was evaluated to see why the change in reference voltage was less than the change in zener voltage. Evaluation showed that the offset of the op-amp had its largest change between 150°C and 200°C, as shown in Figure 5. This change was in the opposite direction to the drift of the zener, and therefore the accuracy of the reference became the difference of the two.

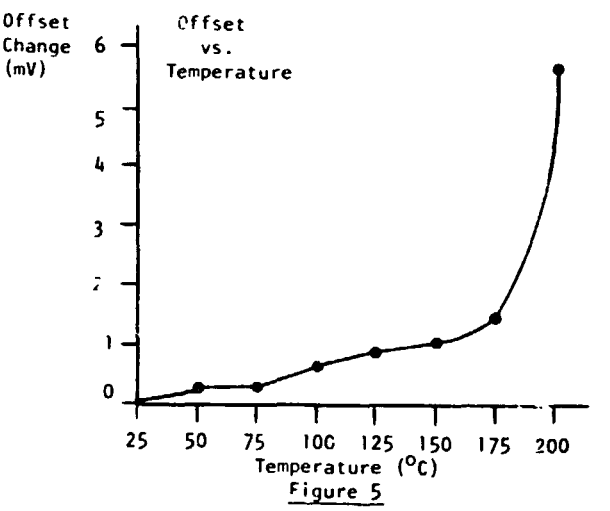

Figure 5

The central component of the D to A circuit is a resistor network. The network used is a thin film chip using nickel-chromium resistors deposited on silicon. The change in resistance over temperature will determine the accuracy and linearity of the device. An absolute change in resistance results in an accuracy change and a change in resistor ratios will result in a linearity change. The graph in Figure 6 shows typical changes in resistance from 25°C to 200°C. Figure 7 shows changes in resistor ratios. In order to meet design requirements of ±1/2 LSB to the 10 bit level, the resistor ratios must track to better than ±.05% from 25°C to 200°C.

The thin film resistor chip also has the advantage of being actively laser trimmed. This results in an A to D which will meet all specifications without any exter-

nal adjustments. Any external components added would be another source of error when raised to 200°C.

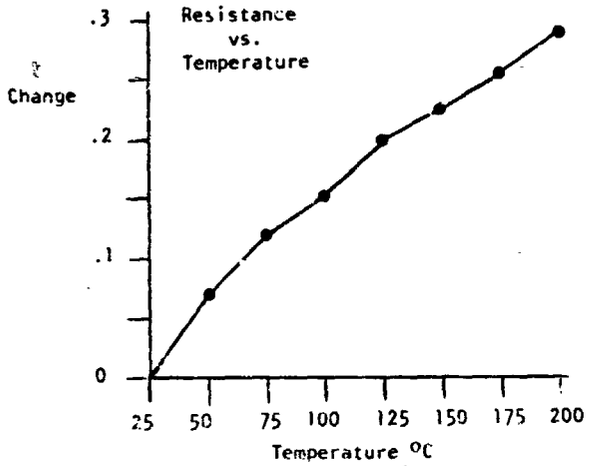

Figure 6

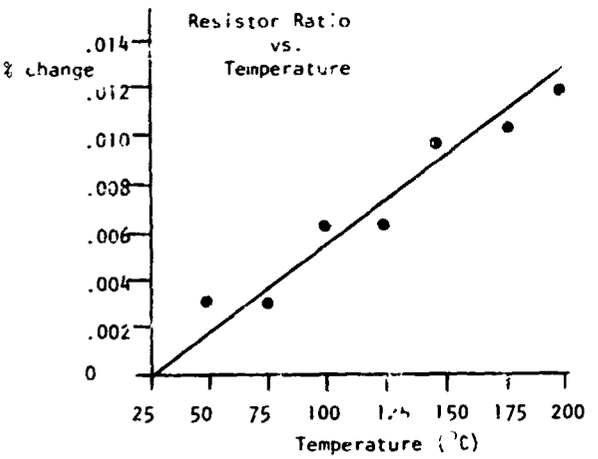

Figure 7

Comparator

In most hybrid A to D converters, the comparator is a single I.C. chip. These are usually bipolar devices. Tests done on most available bipolar I.C.s indicated they were not the most reliable choice for 200°C operation. This is due to the problems of junction isolation previously stated. Because of this, a comparator was designed using a dielectrically isolated op amp and discrete transistors which operated reliably at 200°C.

Successive Approximation Register

The SAR used in this design is a CMOS I.C. This was chosen because of the good characteristics of CMOS at high temperatures and the low power consumption. CMOS I.C.s have been constructed which were functional at 300°C for over 1000 hours.[6] While leakage current on CMOS devices operating at 200°C may be large when compared to +25°C operation, their voltage thresholds do not change appreciably. Thus devices operated from low impedance sources work very reliably at 200°C.

ELECTRICAL TEST RESULTS

The first prototype units were evaluated for conformance to the 200°C specifications. Test results showed that these performed as expected. These units were then put on a 200°C burn-in with frequent monitoring to observe changes or shifts that occured. After approximately 25 hours, large shifts were seen in linearity and accuracy. The cause of a shift such as this indicated a change in resistors or a change in the output resistance of the switches. The parts were burned-in longer and catastrophic failures were seen. Visual inspection showed that gold ball bonds were lifting off of the aluminum pads on the I.C. chips.

BONDING FAILURES

The bonding failures which occured at the aluminum/gold interface arose from the formation of an intermetallic compound at that point. As the time at high temperature increases, these compounds do not exhibit sufficient mechanical strength to insure bond integrity. As a result, the bonds have a tendency to break and cause an open circuit.

DEVELOPMENT OF METALIZATION SYSTEM

It was concluded that the most reliable hybrid could be fabricated if all wire bonding was done to similar metals. This was a problem because available I.C. chips use aluminum bonding pads, while the substrate, resistor chips, and posts have gold bonding areas.

To accommodate this bonding scheme, a substrate was needed with both gold and aluminum bonding areas.

Three Metal-Metalization Process

In order to construct the type of substrate described, it was necessary to use three metals - gold, aluminum, and nickel. The gold is used for conductor runs and bonding areas, and the aluminum is used only for bonding areas, at the I.C. chips. The aluminum bonding pads sit on top of gold pads, but have a layer of nickel in between the gold and aluminum layers to act as a diffusion barrier, which eliminates the formation of intermetallic compounds.

Figure 8 depicts the major process steps. Starting with a wholly metallized Al_2O_3 ceramic plate (Fig.8a) a gold conductor pattern is defined using standard photo lithographic and etching techniques (Fig. 8b). Next a nickel layer and an aluminum layer are vacuum deposited (Fig.8c). Finally, the aluminum pads are formed by selective removal of unwanted film (Fig. 8d).

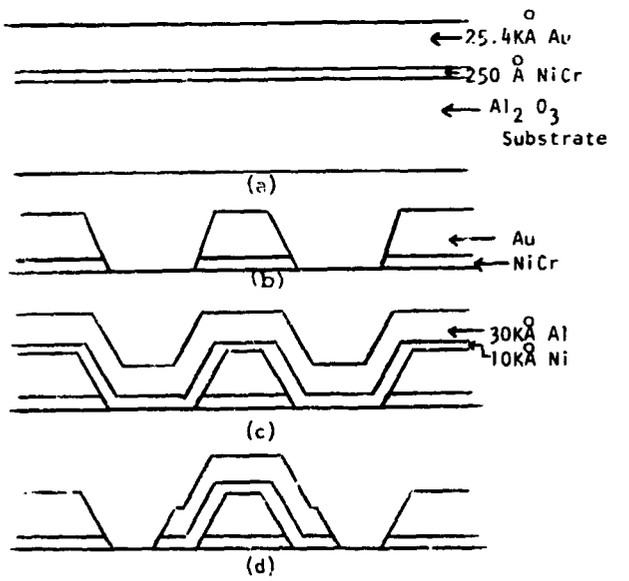

Figure 8

The process steps, thicknesses, and material selection have been chosen on the basis of compatibility with present fabrication techniques, as well as performance criteria.

Au/Ni/Al Substrate Evaluation

For evaluation purposes, a substrate was made which had a pattern allowing gold and aluminum wire bonding to be done between pins of a hybrid package. Connections were made which consisted of 26 bonds (13 wires) between pins of the package. The bonds consisted of aluminum wire on gold pads, aluminum wire on aluminum pads, gold wire on aluminum pads, and gold wire on gold pads. The aluminum pads were deposited on gold using a nickel barrier as described in the previous section. The resistance was measured between the pins of the package at various intervals of 200°C bake. This measurement included the bond resistances along with the resistance through the aluminum/nickel/gold interface. Figure 9 shows a graph of change in resistance versus time at 200°C for the four different bond interfaces. It can be seen that the best results are obtained when bonding is done between similar metals.

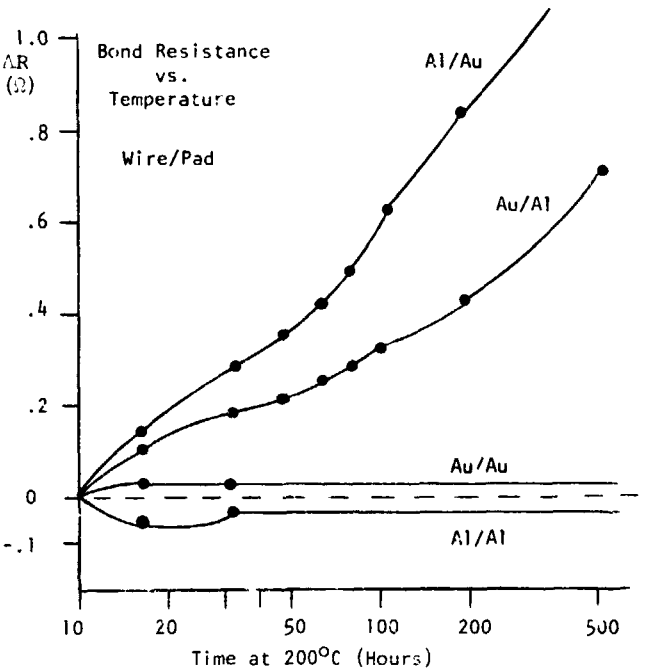

Figure 9

Figure 10 shows a section of the substrate used in the MN5700. The shaded areas indicate aluminum pads which are properly located for aluminum wire bonding to the I.C. Chip.

Other Failure Modes

The next group of catastrophic failures were seen in the 500-750 hour range. When these units were inspected, it was seen that some of the epoxy mounted chips had lifted off the substrate and caused some bonds to break. This was corrected by using a different type of epoxy with better high temperature characteristics. Evaluation of this epoxy after 1000 hours at 200°C showed little or no degradation in its bonding and adhesive characteristics.

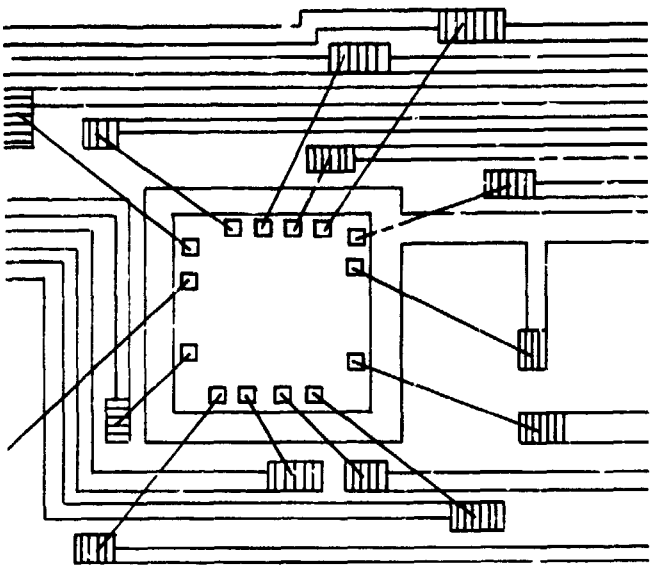

Figure 10

CONCLUSIONS

Tests have shown that units will operate reliably and remain within 200°C specifications in excess of 500 hours. Beyond 500 hours, some units will exhibit a slow shift in linearity and accuracy. This appears to be caused by resistor aging and changes in the characteristics of the CMOS switches in the D/A section. Life tests have shown that most units remain within specification in excess of 1000 hours. Tests have also shown that most catastrophic failures and units with large shifts will show up in the first 24 hours of operation at 200°C. To help assure reliability, all units are tested, burned-in for 24 hours at 200°C, and retested.

All 200°C specifications are also guaranteed at -55°C. The MN5700 is available with high reliability screening according to MIL-STD-883 for Military/Aerospace Applications.

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WIRELESS, IN-VESSEL NEUTRON MONITOR FOR INITIAL CORE-LOADING OF ADVANCED BREEDER REACTORS*

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Abstract

An experimental wireless, in-vessel neutron monitor is being developed to measure the reactivity of an advanced breeder reactor as the core is loaded for the first time to preclude an accidental criticality incident. The environment is liquid sodium at a temperature of ∿220°C, with negligible gamma or neutron radiation. With ultrasonic transmission of neutron data, no fundamental limitation has been observed after tests at 230°C for >2000 h. The neutron sensitivity was ∿1 count/s-nv, and the potential data transmission rate was ∿10^4 counts/s.

I. Introduction

An experimental in-vessel monitor was designed and fabricated and is being further developed to ultrasonically transmit reactivity data from advanced breeder reactors. Since such reactors have potentially high reactivity cores, their initial fuel-loading operation will require careful surveillance as the core is loaded to preclude an accidental criticality incident.

An in-vessel neutron detector is preferred to an ex-vessel detector because it is closer to the fuel elements and is not shielded by blanket assemblies. Thus, data from an in-vessel detector are received at a greater rate (up to 10^4 counts/s for this model) and are more easily interpreted. Also, with an in-vessel detector, the neutron source required to make the subcriticality measurements can be reduced in size and possibly eliminated.

A wireless, completely remote in-vessel detector can be located at any core position, giving much greater versatility to the measurements. In addition, the wireless detector does not need expensive instrument thimbles and does not inhibit the motion of fuel handling equipment.

The in-vessel environment for this initial start-up monitor is liquid sodium at a temperature of about 220°C. No existing neutron monitor has the wireless capability and adequate sensitivity for this application. The experimental model described herein has been successfully tested at 230°C for >2000 h.

II. Wireless Neutron Monitor Concept

The current concept of the wireless neutron monitor system is shown in Fig. 1. In the sodium-filled reactor vessel (~6 m diam × 18 m high), the neutron monitor is positioned in the reactor core region within a dummy fuel element. The ultrasonic transmitter is mounted at the top end of the dummy element where it can transmit signals along an unobstructed path through the sodium to a receiver which is also immersed in the sodium.

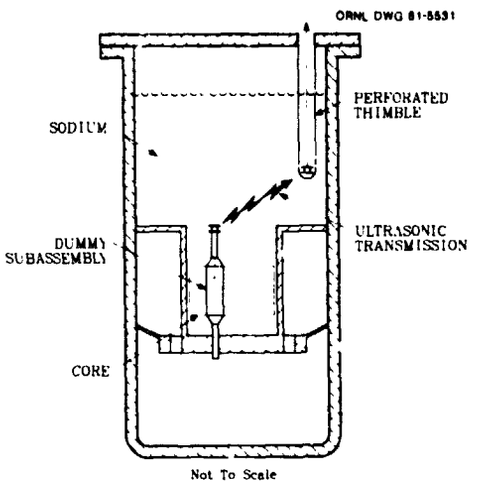

Fig. 1. Concept of a wireless, initial core-loading neutron monitor for an advanced breeder reactor.

III. Instrumentation

A diagram of the instrumentation is shown in Fig. 2. A fission counter senses the neutrons, and the resulting electrical pulses are processed by a pulse amplifier and a bandpass filter with single-pole upper and lower cut-off frequencies (RC-CR filter). Electronic noise and alpha pile-up noise are rejected by a discriminator. The discriminator output pulses trigger a driver circuit which excites a 2 MHz ceramic crystal to create an ultrasonic burst for each neutron pulse exceeding the discriminator threshold level. The primary electrical power, which will be derived from a radioisotopic thermoelectric generator, is transformed by a dc-dc converter to positive and negative 10 V levels to bias the fission counter and to drive the active circuitry.

The total quiescent power of the instrumentation at a temperature of 230°C is ∿0.56 W with a dc-dc converter efficiency of ~60%. The ultrasonic driver is expected to require ~0.1 W at an output pulse rate of 10^4 counts/s. The primary source requirement is 8.0 V at ∿1.6 W.

A. Fission Counter

A commercial fission counter (Reuter-Stokes model RSN-10A) with a 4-mm electrode spacing, 1000-cm^2 of sensitive area, and a 300°C maximum operating temperature was selected for our use. These features were required for our special application, and the availability of the counter eliminated a costly in-house fabrication program. However, some special alterations[1] were needed to ensure adequate performance (voltage

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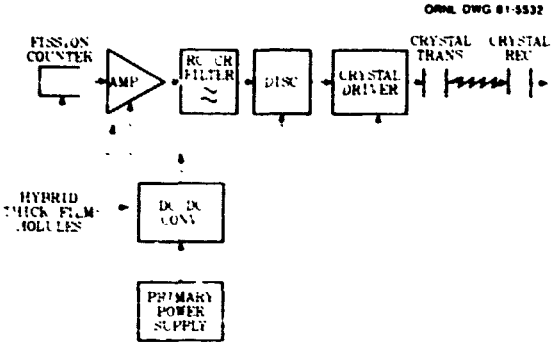

Fig. 2. Block diagram of the instrumentation.

saturation, collection time, and ratio of fission pulse amplitude to alpha pile-up) at a limited counter bias of 10 V. These alterations included an electrode coating of highly enriched ^{235}U (99.6%) and a gas-filling of Ar-0.01% CO_2 at $\sim 10^5$ Pa of absolute pressure.

B. Amplifier-Filter-Discriminator (AFD)

This module[2] processes signals from a fission counter with an electron collection time near 1.0 μs. The input amplifier is voltage sensitive. To achieve input bias stability at temperature, the input resistor is 20 kΩ maximum. This resistor value, coupled with the 150 pF counter capacitance, determines the input integration time constant and a significant fraction of the input noise of the pulse amplifier.

Two other gain stages, each with a voltage gain of ~16 per stage, produce output pulses in the range of 1-1-3 V amplitude. A bandwidth of 5 MHz per stage is more than adequate to amplify the voltage pulse developed at the input.

Capacitive coupling between stages eliminates dc instability problems. One coupling time-constant determines the high-pass frequency of the filter; the low-pass response is controlled by integration in the output stage.

A monostable multivibrator-discriminator generates a logic pulse of 5.6 V amplitude and 5 μs width for each amplifier pulse that exceeds its threshold.

Except for two diodes and a 1-MΩ, thin-film resistor chip in the discriminator, the entire circuit is fabricated around four, dielectrically isolated, IC, differential operational amplifiers, Harris type HA2625. One of these amplifiers with appropriate positive feedback constitutes the monostable multivibrator-discriminator combination.

C. Ultrasonic Transmitter

From an analysis of the system,[3] a 2-MHz carrier frequency with pulsed modulation was judged to be most power efficient for the ultrasonic, data transmission process. With an assumption that the receiver bandwidth must be 200 kHz to obtain the maximum data rate, ~240 μW/m^2 of received signal power is required to yield a signal-to-noise power ratio of >100. This assumes an acoustic noise power density of +10 dB referenced to 10^{-12} W/m^2-Hz. To create a transmitted beam having a cylindrical wavefront with this intensity at ~4 m, nearly 70 mW of pulse power is required to allow for losses in the transmitter drive circuit, the crystal transducer, and the liquid-sodium signal transmission path.

The transducer will contain a PZT-5A ceramic crystal similar to that used by the Hanford Engineering Development Laboratory (HEDL)[4] in their under-sodium viewing systems. It is attached to the transducer face-plate with either a Pb-Sn-Ag solder alloy or a high temperature epoxy. Both have been successfully tested.

The transducer is driven by two VMOS transistors in parallel, with the power being obtained directly from the primary power source. A 2.5-μF Teflon capacitor is currently used as an energy storage element to reduce the ripple on the primary power source.

The crystal impedance is integrated into a resonant tank in the drain circuits of the VMOS transistors. A step-up transformer wound on a high-temperature ferrite toroid reduces the amplitude of the voltage pulses on the drain circuitry.

D. DC-DC Converter

The dc-dc converter[5] is an astable multivibrator that drives an n-channel VMOS switch (two in parallel) in a dual-coil switching regulator. A dielectrically isolated, IC, differential operational amplifier in conjunction with a 6.9 V zener diode (an emitter-to-base junction of a Dionics DI3424 dielectrically isolated transistor) senses the positive 10 V output variations and adjusts the off-time of the VMOS (on-time is fixed). Integration in the operational amplifier determines the dominant pole of the forward loop. The astable circuits comprise dual, dielectrically isolated, pnp and npn transistors, Intersil IT137 and IT127, respectively.

The coil is a high-permeability, silicon-steel toroid with a Curie temperature of 730°C and is wound with 30 gauge, Teflon-insulated copper wire. The switching frequency is ~60 kHz, and 10-μF electrolytic capacitors reduce the ripple to acceptable value for a total load of 12.5 mA for a positive and negative 10 V output.

The internal, drain-substrate, p-n junction diode of n-channel VMOS transistors are used as rectifiers. At 230°C, the forward drop is 0.3 V, with a leakage current of <200 μA, and a reverse voltage of 60 V.

E. Primary Power Source

Because of its ruggedness and proved performance in numerous space problems, a radioisotopic generator is being considered for the primary power source. Plutonium as $^{238}Pu_2O_3$ is the heat generator, and silicon-germanium forms the thermocouple junctions. The liquid sodium serves as the "cold leg" of the generator system. For an electrical power output requirement of ~1.5 W, a heat source of ~125 W_{th} is considered adequate. Contracts are being prepared for the procurement of this source.

IV. Hybrid Thick-Film Circuits Fabrication Details

The AFD circuit and the dc-dc converter are fabricated with thick-film technology on 51- by 51-mm (2- by 2-in.) and 32- by 32-mm (1.25- by 1.25-in.), 96% alumina substrates, respectively. Figures 3 and 4 are photographs of these two thick-film circuits. The AFD circuit (Fig. 3) was operated at temperatures near 230°C for nearly 2800 h. The metallization is gold (Du Pont 9910). The thick-film resistors are screened

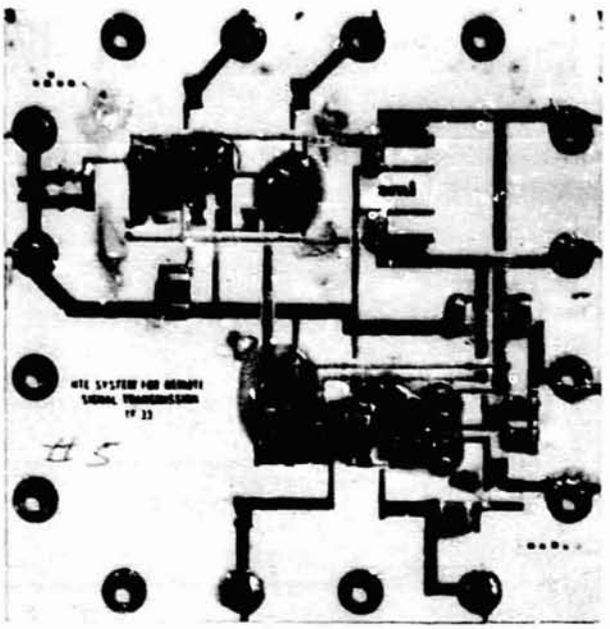

Fig. 3. Photograph of the amplifier-filter-discriminator hybrid thick-film circuit (after 2800 h at ~230°C).

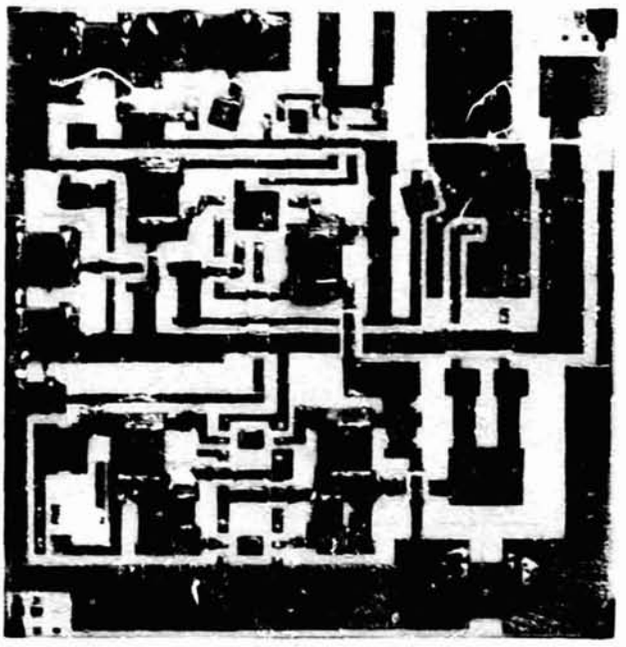

Fig. 4. Photograph of the dc-dc converter hybrid thick-film circuit.

from the Du Pont 1600 Birox series. All semiconductor chips are attached with a silver-filled epoxy (Ablestik 71-1) for electrical attachment to the substrate or with an insulating epoxy (Ablestick 71-2) for isolation. Electrical connections between chip and substrate metallizations are made with 25-μm-diam (1.0 mil) aluminum -0.5% magnesium wire by ultrasonic bonding. All bonds to the gold metallization are mechanically reinforced with an epoxy, either Ablestik 71-1 or Epo-tek P-77. Ceramic covers and a protective semiconductor coating (Dow-Corning R6100) are both used to protect areas of the circuit containing the active elements.

The capacitors contained in these two circuits are monolithic, ceramic capacitor chips with 50- to 100-V ratings. The bypass and decoupling capacitors were formed from a high-dielectric-constant material (X7R), but filter and compensation capacitors were formed from a more stable, low-dielectric material (NPO). A gold-germanium alloy solder (360°C mp) was used to make electrical connections to the capacitor chips and to the external wires of the substrate using a reflow technique. Later, a parallel-gap welder was obtained to make the external connections with a 25- by 500-μm (0.001- by 0.020-in.) nickel ribbon.

V. Description of the Experimental Monitor

The experimental monitor is shown in Fig. 5. Its construction does not represent the construction that would be used in the prototypical monitor. Instead, it was designed to facilitate data taking and to accommodate modifications and improvements as they became apparent during the testing program. From left to right in the figure is the fission counter wrapped in an electrically insulating Teflon jacket to protect the shell of the counter, which is maintained at a negative 10 V biasing potential, followed by the AFD module, the dc-dc converter, and the transformer for the ultrasonic transmitter. At the extreme right is an oil-filled test chamber with a transmitter and receiver crystal at opposite ends. The entire system is mounted on a high-temperature, printed circuit board (Du Pont Pyralin) with a small number of discrete resistors (Caddock) and ceramic capacitors (San Fernando Electric). The resistors, capacitors, and the hybrid thick-film modules were attached with 90% lead-10% tin solder. A test pulse, dc and pulse monitor points, oil drain and fill tubes, and thermocouples are all brought out of a flanged end of the assembly. The entire assembly, ~1.0 m (40 in.) long, is installed in a cylindrical enclosure, giving a pressure tight containment for an inert cover gas.

VI. Test Results and Discussion

The results of the temperature tests of the experimental monitor are summarized in Table 1. The performance of the solid-aluminum electrolytic capacitors was poor, a result not expected based on previous work in high temperature electronics[6,7] and on preliminary tests. Preliminary tests were made in air up to 275°C for hundreds of hours, showing only a slight degradation of performance. The cause of the capacitor failures is believed to be outgassing from oil that leaked out of the ultrasonic test chamber. The oil initially used in the tests possessed inadequate high-temperature properties. Also, the high porosity of the printed circuit board material prevented an adequate clean up of the test assembly.

Two failures of aluminum wire bonds at the gold metallization of the dc-dc converter were the first experienced after nearly 300 successful bonds on other hybrid circuits. This failure rate is not considered excessive at this time, and no changes in our bonding procedures are planned.

Integral bias responses obtained for two measurements at ~230°C and covering a time span of nearly 1600 h show only slight differences. Projection of the 1.0 count/s noise curve threshold to the neutron curve shows an ~75% counting efficiency for the monitor.

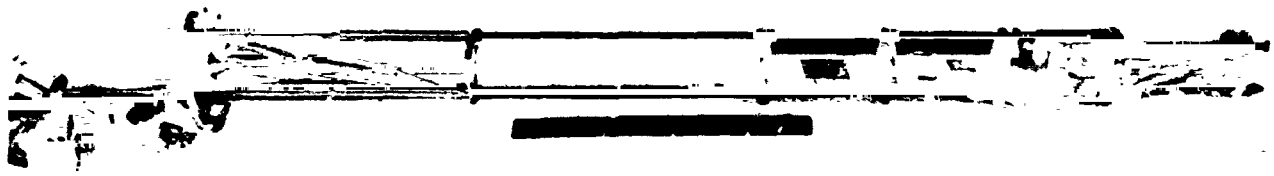

Fig. 5. Photograph of the experimental wireless, initial core-loading neutron monitor (externally powered).

Table 1. Summary of performance of neutron monitor components

Component	Hours at 230°C	Performance
Fission counter	2400	More than adequate
AFD module	2800	Adequate[a]
DC-DC converter	384[b]	Adequate[c]
Ultrasonic transmitter	2200	More than adequate[d]
Solid-aluminum electrolytics	176[b]	Not adequate[e]
Printed circuit board, with discrete resistors and ceramic capacitors	2800	More than adequate

[a]Some drift in pulse gain (or amplitude of test signal) not seen in prior 2100-h tests at 250°C.

[b]Maximum time to failure.

[c]Failures caused by two faulty wire bonds at substrate metallization.

[d]Does not include a gated oscillator.

[e]Capacitor failure from outgassing effects.

VII. Problem Areas

The failure of the solid-aluminum electrolytics must be resolved. Although the prototypical neutron monitor will not contain an oil source, the apparent sensitivity of these capacitors to outgassing must be determined.

Presently, we are working on a design for a gated, 2-MHz oscillator that will provide the input drive signal for the transmitter. Tests are still to be made on the cylindrical ultrasonic beam generator. The concept for this ultrasonic beam generator is shown in Fig. 6.

VIII. Conclusions

Temperature tests on an experimental assembly of an initial-core loading neutron monitor show no unresolvable problems. Failure of solid-aluminum electrolytics because of off-gassing indicates a need for a vapor-free environment for these devices. Bond failure on the dc-dc converter substantiates the need for pretesting of all hybrid thick-film modules.

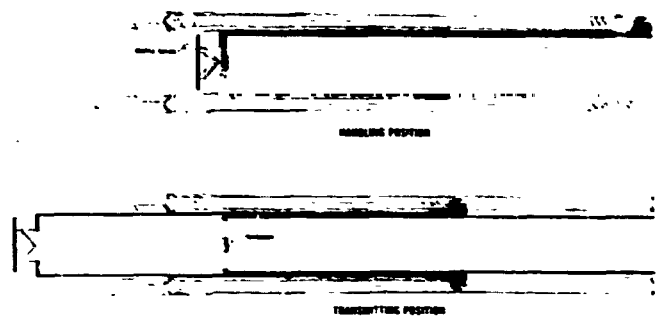

Fig. 6. Conceptual sketch of the cylindrical ultrasonic beam generator.

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Acknowledgments

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SOLID STATE MICROELECTRONICS TOLERANT TO RADIATION AND HIGH TEMPERATURE

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Abstract

The nuclear and space industries require electronics with higher tolerance to radiation than that currently available. The recently developed 300°C electronics technology based on JFET thick film hybrids was tested up to 10^9 rad gamma (Si) and 10^{15} neutrons/cm^2. Circuits and individual components from this technology all survived this total dose although some devices required 1 hour of annealing at 200 or 300°C to regain functionality. This technology used with real time annealing should function to levels greater than 10^{10} rad gamma and 10^{16} n/cm^2.

Introduction

The need for high temperature electronics in many fields has been amply defined in the past.[1] Recent events suggest an urgently needed technology extension: temperature and radiation hardened microelectronics. The salient applications are nuclear reactor instrumentation and space probes. In particular, instrumentation within the containment structure of a nuclear power plant must be capable of withstanding a peak of 200°C and a total of 2 x 10^8 rad gamma dose during a 40-year plant lifetime followed by a loss of coolant accident. Additional temperature and radiation resistance is needed for monitors placed within the reactor vessel over the lifetime of the power plant: 325°C with 5 x 10^8 rad gamma and 10^{14}n/cm^2 near the vessel top and 350°C with 10^{10} rad gamma and 10^{18}n/cm^2 closer to the fuel assembly. Intense radiation belts near Jupiter and the Sun demand enhanced radiation tolerant electronics in certain extended space missions. Although critically dependent on orbit parameters, a dose of 10^7 rad over one year may be absorbed by a Jupiter satellite. Radiation levels elsewhere within the solar system and interstellar space are expected to be relatively low; however, the accumulated dose for long missions can easily exceed existing electronic tolerances.

Typical tolerances for present electronics are 2 x 10^4 rad gamma and 10^{12}n/cm^2 for commercial hybrids and ICs, and 10^6 rad gamma and 10^{14}n/cm^2 for specially fabricated or selected rad hard devices (Harris, for example). The numbers in Table I are somewhat arbitrary since different degrees of device parameter degradation are possible in different circuits.

Most radiation tests on electronics to date have been motivated by nuclear weapon applications. These tests therefore predominantly involve pulses of fast neutrons and X-rays, with a gamma dose that is only incidental to the neutron presence and usually less than 10^6 rad. Therefore, tests involving large gamma dose alone have not been common. Also because of the weapon orientation of most radiation-electronics tests, the interaction of operational temperature and sustained irradiation was not investigated. The recent development of circuitry operational to 300°C opens the possibility of real time annealing at high radiation levels.

Table I

Hardness / Technology	Gamma (rad Si)	Neutrons (cm^{-2})	Temp. (°C)
Consumer	2x10^4	1C^{12}	85°C
Military Hardest	10^6	10^{14}	125°C
Thick Film/ JFET	>10^9	>10^{15}	>300°C

The components and hybrid circuits chosen for this initial investigation were from Sandia's high temperature circuitry development. There are two basic ideas behind this choice: first, to maximize the rate of annealing the operational temperature must be as high as possible, and secondly, several main failure modes are initiated both by elevated temperature and radiation (ion mobilization, lattice and chemical reactions).

We will discuss both gamma and neutron tests. Each section will briefly describe the radiation facility and the effects on passive components, active components, and hybrid microcircuits.

Gamma Tests

Two facilities for gamma irradiation were used. Both used Cobalt 60 (1.17 and 1.33MeV photons) with dose rates of 1.7 and 4.3Mrad (Si)/hr. respectively. Both sources generated enough heat to raise the sample temperature by about 15°C. Interactions between gamma photons and a steel liner between the weaker source and the sample chamber created some Compton electrons which also had measurable effects on the devices.

Passive

Passive components were tested in the weaker source with no biasing during irradiation. At 5 points during exposure, the samples were removed, tested, and returned for more radiation. The components were exposed for a total of 800 hours or 1.36 x 10^9 rad gamma (Si).

Thick film resistors in the 500 and 900 series of Cermalloy and axial lead units from Caddock were found to change less than 0.1% during this exposure. This constancy was somewhat surprising due to positive drifts seen in earlier tests[3] and attributed to Compton electron bombardment.

The high temperature capacitors tested were: Philips solid aluminum electrolyte, K&D Mica, Erie red cap, and several thick film dielectrics (TFS 1005, ESL 4515, ESL 4301, Cermalloy 905HT). Most capacitor systems tested remained functional throughout the test (ESL excepted) but all showed some change in capacitance and degradation in dissipation factor and insulation resistance (Figures 1 and 2). The best performers were the discrete mica and the 500°C thick film formulation 9015HT. The ESL thick film dielectric systems that showed considerable change and instability due to exposure were returned to near pretest parameters by a 1 hour bake at 300°C. Capacitance and dissipation factor were measured at 0.12, 1, and 10KHz. Insulation resistance was measured at 10 volts, with the reading being taken 15 seconds after voltage application.

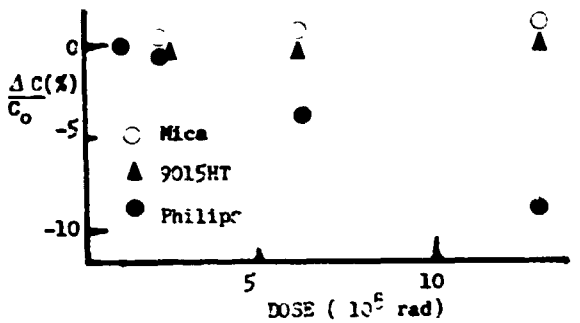

Fig 1. Capacitance Change with Gamma Dose

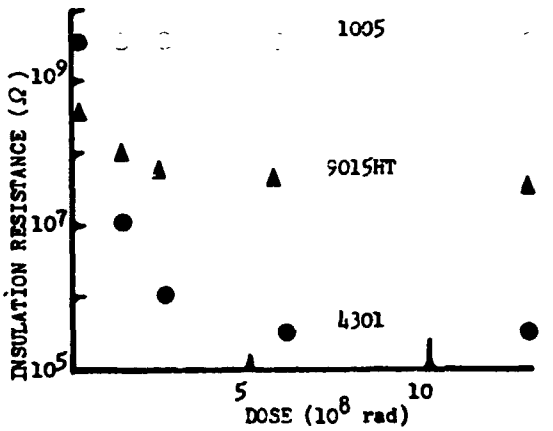

Fig 2. IR change with Gamma Dose

Active

To test the effects of gamma radiation on p-n junctions at various temperatures, 24 diodes were exposed at a dose rate of 4.3Mrad/hr. (Si) for 23 hours, yielding a total dose of ~1 x 10^8 rad (Si). The diodes were grouped into 3 modules, each containing 2 gallium phosphide, 2 gallium arsenide, 2 low minority carrier lifetime (gold doped) silicon, and 2 high lifetime silicon diodes. The thick film hybrid modules were then heated to 50, 175, and 300°C respectively. During most of the test one of each type of diode at each temperature was AC biased. Each diode was monitored periodically for reverse leakage current, forward resistance, reverse breakdown voltage and sharpness of reverse breakdown.

In general radiation effects were minimal. Measured photocurrents were negligible (<16μA/cm²) for all devics. AC biasing had no measurable effect on diode performance over the span of the test. Low lifetime diodes (GaAs, GaP, and gold doped Si) displayed little or no change in characteristics over the 23 hour test; however, the high lifetime silicon diode reverse leakage current increased appreciably. This effect was, presumably, caused by degradation of minority carrier lifetime (increase in generation rate) due to lattice imperfections created by gamma/silicon interactions. A control group of identical high lifetime silicon diodes aged for 24 hours at 300°C without radiation was found not to show this increase in leakage current, indicating that the effect was not caused by junction poisoning due to unwanted diffusion at elevated temperature.[4]

In another experiment, several types of n-channel silicon JFETs (Motorola 2N4220 and 2N4391 series) were exposed at room temperature to a gamma dose rate of ~1.7Mrad/hr. (Si) up to 1.36 x 10^9 rad (Si) total dose. The transconductance and I_{DSS} vs. accumulated dose for a typical transistor are plotted in Figure 3. Cutoff voltage, $V_{GS\ off}$, remained essentially constant for all transistors during the test, indicating that carrier removal effects were minimal. However, transconductance (and I_{DSS}) decreased monotonically for all devices, an effect most likely due to a reduction of carrier mobility in the channel. Both gamma photons and Compton electrons could have created the lattice damage necessary for this phenomenon to occur.

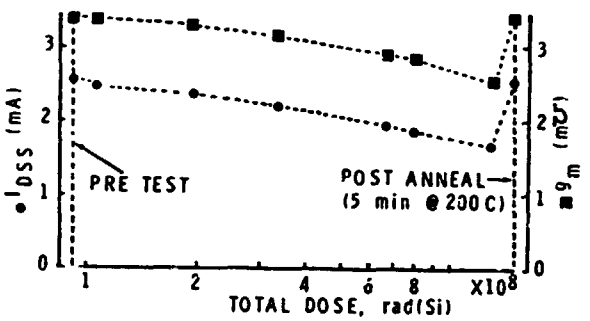

Figure 3. Motorola 2N4220A JFET Parameters vs. Total Dose

Because of the layout of the gamma test facility used in this JFET experiment, it was impossible to study the simultaneous effects of radiation and elevated temperature. Instead, the devices were annealed for 5 minutes at 200°C after a total dose of 1.36×10^9 rad was reached. As Figure 3 shows, 100% recovery was obtained with respect to g_m and I_{DSS}. This indicates that extremely high total doses (>10^{10} rad) may be tolerated by JFETs if accompanied by moderate heating, as expected in a loss of coolant accident. It should be noted that devices held below 30°C for several weeks after irradiation showed no annealing.

Hybrid

Tests were also performed on a simple hybrid microcircuit containing 6 JFETs and 3 thick film 500-series Cermalloy resistors. Circuit performance did not change throughout the test (1.36×10^9 rad total). The same technology used for this circuit is employed in the complete line of Sandia's geothermal high temperature instrumentation, including voltage regulators, V/F converters, pulse stretchers, and multiplexers.[5]

Neutrons

The neutron tests have not been concluded as of this writing. A pulsed reactor with a fast neutron product was used. The pulse is about 70μsec long and exposes the samples to approximately 3×10^{14}n/cm² during each pulse. This source also produces sample irradiation of 6×10^5 rad gamma for each 10^{14}n/cm².

Passive

Initial exposures of 7×10^{13}n/cm² were used in order to induce only a small change in passive component parameters. As in the case of gamma tests, the resistors remained stable. This is in agreement with previously reported investigations.[3] Although several capacitors showed slight changes in dissipation factor due to this neutron flux, they were all circuit functional. The extreme tolerance of these components suggested an ongoing test series which will reach 10^{17}n/cm². As with gamma tests the source time and cost may eventually necessitate extrapolation to higher expo ures.

Active

To study the effects of neutron irradiation and thermal annealing on diode reverse leakage current, several silicon diodes (all TRW SA1813) were exposed to 10^{14}n/cm². The results of thermal annealing runs on one particular (but typical) diode are shown in Figure 4. Unfortunately, pre-irradiation data was not available for these early tests, but measurements made on a non-irradiated control group yielded 25°C leakage currents ranging from 5.5 to 11nA at -10 volts, with most values in the 6 to 8nA range. As can be seen, recovery of the reverse characteristics is initially rapid but not complete. Similar effects were noted for JFETs. The higher temperatures within the reactor vessel (the only anticipated application where significant neutron fluences would be encountered) may improve annealing.

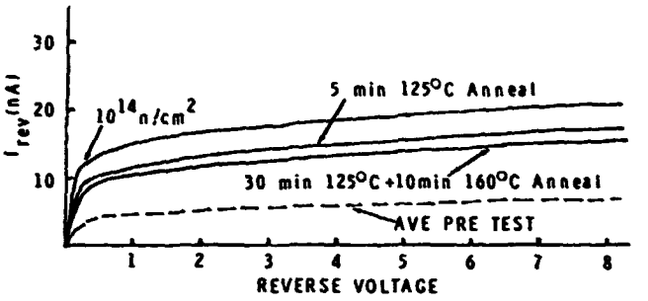

Figure 4. Diode Neutron Irradiation/ Thermal Annealing Behavior

An interesting and, as yet, unexplained phenomenon was discovered in another phase of this experiment. While attempting to anneal the neutron damage by injecting forward current across the p-n junction, it was found that short applications (~1 minute or less) actually caused an increase in reverse leakage current. This increase could, in turn, be annealed by subsequent heat treatment. Non-irradiated parts did not exhibit this effect, and currents applied for much longer times initiated thermal annealing. While the exact mechanism behind this behavior is not certain, it is thought that charge trapping in gamma induced states in the passivation layer near the edge of the junction may play an important role. (As mentioned previously, the neutron facility also has a significant gamma output.) If this is the case, a similar effect should be noted on gamma irradiated devices. This experiment is still in the planning stage.

Neutron effects on JFETs used extensively in Sandia's high temperature circuits (Motorola 2N4220 and 2N4391 series) were examined in another set of experiments in which the devices were irradiated to a level of ~7×10^{13}n/cm². As can be seen in Table II drastic changes occurred in transistor characteristics. In most cases the magnitude of $V_{GS,off}$ increased markedly (average ~8%), indicating carrier removal effects were occuring. Transconductance and I_{DSS} decreased by more than an order of magnitude. Partial annealing was obtained after 1.5 minutes at 200°C, with only slightly greater annealing effected at 300°C. The relatively slow recovery confirms the fact that, unlike the simple defects created by γ photons and Compton electrons, neutron damage is additionally composed of more stable cluster defects. It is interesting to note that, at each temperature used in the annealing experiments, recovery was extremely slow after 2 minutes; even when the device was held at temperature for periods of up to an hour, no further improvement was evident. An increase in temperature was required to effect further annealing. While operation at high temperature may provide the simultaneous annealing necessary for operation in high neutron fluence environments, it is doubtful that JFET operation will survive levels much above 10^{16}n/cm².

Table II

	$V_{gs,off}$	g_m (m℧) @V_{gs} = -0.2	I_{dss} (mA)
PRE TEST	1.15	2.00	1.160
$7X10^{14}$ n/cm^2	1.24	0.20	0.073
ANNEAL: 1.5 min@200°C	(1.36)	0.80	0.360
ANNEAL: 11.5 min@200°C	1.15	0.84	0.362
ANNEAL: 11.5 min@200°C +10 min @300°C	1.13	1.08	0.439
ANNEAL: 11.5 min@200°C +80 min@300°C	1.14	1.04	0.488

Motorola 2N4220 JFET Parameters

Hybrid

The same hybrid circuit which saw 1.3 x 10^9 rad gamma was exposed to 7 x 10^{14}n/cm^2. After a 5 minute. 200°C post exposure anneal the circuit functioned normally.

Summary

It is clear from these initial tests that the traditional limits ascribed to solid state electronics in radiation environments can be vastly exceeded. For example, the thick film/JFET technology with no modifications to its high temperature form can survive more than 10^9 rad (Si). The quick annealing of passive and active devices at 200°C strongly suggests that operation to 10^{10} rad is possible, a level exceeding any application now envisioned. Annealing effects seen in diodes and passive components after neutron exposure also demonstrate the enhanced radiation tolerance possible by high temperature operation. The JFET response to neutrons defines the extent of radiation possible with this hybrid technology. Additional tests with high temperature operation during irradiation up to 10^{17}n/cm^2 are necessary before the circuitry tolerance to neutron flux can be ascertained. This limit is projected as well above 10^{15}n/cm^2, however.

This investigation is only the first step toward ultra high rad electronics. Several programs must follow. For example, the development of JFET ICs will allow increased complexity and reliability. During the next year, hybrid prototypes of a control rod position sensor and a containment vessel pressure monitor will be fabricated and tested to the appropriate radiation level. Device tests will be expanded to include bipolar transistors, op amps, I^2L microprocessors, and MOS structures.

Although this thick film/JFET technology appears suitable for reactor instrumentation in both the containment and reactor vessels, power and volume restrictions on space probes may demand the CMOS technology which is now used for similar reasons in weapons.

Analysis by other researchers has indicated that CMOS should not necessarily be discarded for use in extremely high radiation environments, as long as elevated temperature provides some annealing of the trapped charge in the oxide.[6,7] Detailed experiments along these lines are planned for the near future. Although the CMOS technology has not been addressed in this report nor extensively tested at these high radiation levels, it is important to note that at least two solid state microelectronics options exist which have capability to the highest radiation levels expected for nuclear reactor and space needs.

Acknowledgements

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HIGH TEMPERATURE LSI

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Summary

The General Electric Company has been involved in developing Integrated Injection Logic (I^2L)[1,2] tech ology for reliable operation under a -55°C to +300°C, temperature range. Experimental measurements indicate that an 80 mv signal swing is available at 300°C with 100 μA injection current per gate. In addition, modeling results predict how large gate fan-ins can decrease the maximum thermal operational limits. These operational limits and the long-term reliability factors associated with device metallizations are being evaluated via specialized test mask.

The correct functional operation of large scale integrated circuits in a -55°C to +300°C temperature environment for long periods of time will provide substantial immediate benefits for digital jet aircraft engine control and geothermal or deep fossil-fuel well logging. Most commercially available LSI technologies are inoperable or suffer long-term instabilities under these conditions.

Introduction

There is no inherent reason why silicon bipolar devices will not operate at +300°C for extended periods of time, provided the circuit has been properly designed to tolerate leakage currents in that environment. A calculation using extrapolated diffusion coefficients for aluminum in silicon (the worst-case dopant) at 500°C indicates that p-n junctions would not move appreciably in 1000 years. However, other contaminants such as gold or copper not commonly desired in unlimited quantities have diffusion coefficients at least ten orders of magnitude higher. In addition, the metal interconnection system on the chip's surface must provide good ohmic contact and resist the effects of electromigration. This paper will report on the effort at General Electric to develop reliable high-temperature integrated circuits. That work has been and is focused on both the design of silicon bipolar devices and the metallization system.

SILICON I^2L-DEVICE DESIGN CONSIDERATIONS

The operational limits of I^2L gates at high temperatures may be described by a variety of methods. Measurements of ring-oscillator propagation delays as a function of current and temperature provide a direct indication of the operating regions with unity fan-in but do not provide any information on noise margins.

A second method of determining I^2L operating limits enables an evaluation of the noise margin and signal swing. Two I^2L gates are connected in series with the first connected to a switch to provide a zero or one input (see Figure 1). Voltage measurements at the point between the gates are V_{BE} of the second gate's NPN transistor, with a zero input by the switch and V_{SAT} on the first gate collector with a one input.

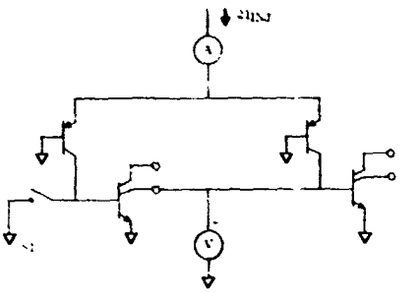

Figure 1. Measurement Method for Determining I^2L Voltage Swing.

Figure 2 plots the measured base-emitter forward-biased voltage drop for a gate input and the NPN collector saturation voltages for a gate output as a function of temperature. During operation, the PNP injection forward biases the NPN base-emitter junction and, with the collector conducting, a low (zero) logic level is supplied to the following stage. The collector sinks injection current intended for the following stage, bringing its input voltage down to the V_{SAT} level of the collector. This turns off the following stage, producing a high (one) output-logic level.

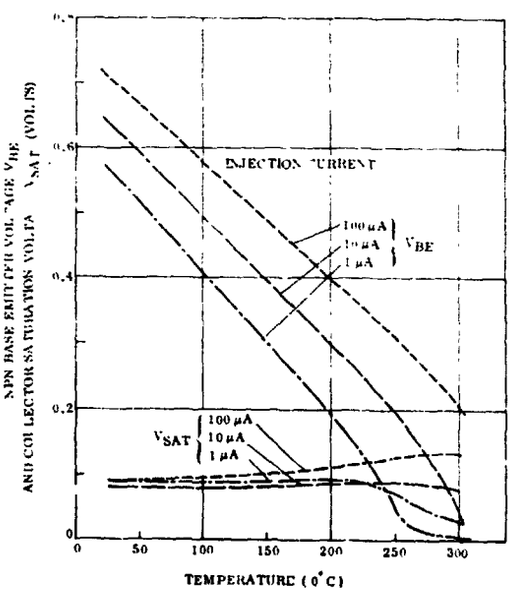

Figure 2. Measured NPN Base Emitter Voltage and Collector Saturation Voltage versus Temperature

The effect of the voltage-swing margin may be observed from the data presented in Figure 2. The V_{BE} for 100 μA injection current is about 550 mV at about 125°C and steadily decreases with rising temperatures to about 200 mV at +300°C. The V_{SAT} for a 100 μA injection increases to a 120 mV level at this same temperature, resulting in a voltage noise margin of 80 millivolts. The voltage noise margin may be obtained for the complete operating region from the difference between the voltages at similar injection currents.

Figure 2 indicates that signal amplitude and noise margin can be improved by increasing the injection-current density.

A third method of determining I^2L thermal operating regions is provided by the digital effective gain, which may be measured or calculated by computer modeling techniques. The effective gain is defined as

$$\beta_{eff} = \frac{\text{collector current sinking capability}}{\text{base current removed from gate input}} \quad (1).$$

I^2L logic signals will propagate as long as the digital effective gain is greater than one. The mechanism by which the effective digital gain decreases at high temperatures is through collector leakage. The total leakage currents in all the OR-tied collectors (fan-in) connected to a gate input rob that gate of some fraction of its injected base current and thus its collector-current sinking capability. This phenomenon is observed in Figure 3. As the fan-in is increased, the total collector leakage removes an appreciable fraction of the injected base current in the I^2L gate at lower temperatures. The effective gain is forced to less than one. This also imposes a design rule on the gate fan-in for a given gate to perform correct logical operations at some specified temperature and injection current.

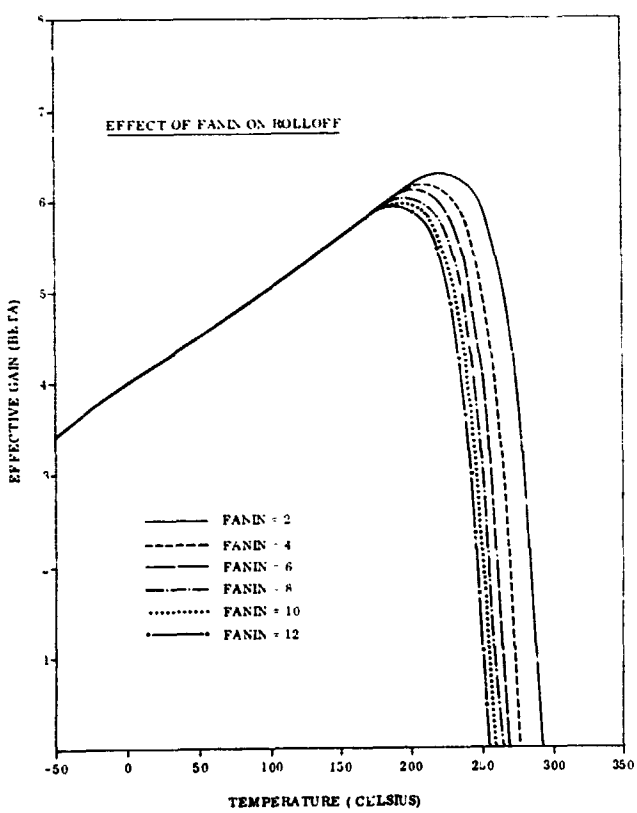

Figure 3. Modeled Temperature and Gate Fanin Influences on Effective Digital Gain

HIGH TEMPERATURE METALLIZATION

The production of a stable, highly-reliable metallization system is equal in importance to the silicon gate design in the production of high-temperature LSI. The metal system chosen for the high-temperature applications is platinum silicide/titanium-tungsten/gold.

Platinum silicide forms stable ohmic contacts to silicon, and gold was chosen for its ability to interface easily the chip to the outside world. However, unlimited gold diffusing into the silicon would seriously affect device performance, and silicon diffusing into the gold metallization can produce reliability problems due to the creation of voids. As a result, a thin titanium-tungsten barrier metal system is employed to separate those materials.

Verification of high reliability metallizations and silicon devices require accelerated aging to compress time scales to reasonable durations. Since most failure mechanisms in integrated circuits are temperature dependent, an activation energy may be obtained for the dominant failure modes. A reaction rate or failure rate may then be predicted at various other temperatures by the Arrhenius equation:

$$R = Ae^{-E/kT} \quad (2).$$

However, activation energies determined from high-temperature testing may be invalid if a phase change has occurred. This is a problem that provides considerable complications in producing high reliability circuits for 300°C operation; these circuits must be accelerated-life tested at temperatures above 350°C.

An independent test mask was designed for metallization evaluations. The mask consists of a repetition of the 190 × 186 mil master cell shown in Figure 4. The master cell is divided by scribe lanes into four separable chip types. Each chip, therefore, has an area of 95 × 93 mils. Within each chip are two different test element cells. Cells A1, A2, A3, A4, B1, B2, and B3 are metallization test elements. The final cell is an I^2L active test circuit.

The metallization test cells were designed to investigate the electromigration effect on the thin metal layer as a function of the metal linewidth and metal line spacing at elevated temperature. The electromigration effect could eventually cause metal-line runoff and resulting open circuits and short circuits between separated metal lines. The metal test elements were designed with a four-point probe capability to enable precise measurements to be made in order to detect effects of electromigration long before catastrophic failure.

The test elements were also designed in a manner that enables ohmic contact resistance to be accu-

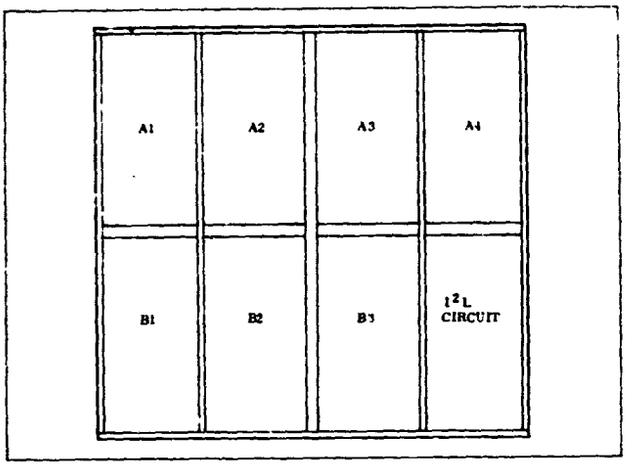

Figure 4. Master Cell Block Diagram

rately measured from external package leads, series resistance to be accurately measured while arbitrary current levels are passed through a metal thin-film conductor element, arbitrary voltage levels to be applied between adjacent metallization runs using external package leads, I^2L logic-gate digital gain to be measured from external package leads, and I^2L propagation delay to be externally measured using seven-stage ring oscillators. In addition, various gate sizes and styles were used in the ring oscillators to provide a convenient method of comparing the effects of different current densities.

Figure 5 shows a plot of a typical metallization test pattern. To cover the range of the current I^2L fabrication process, four different minimum dimensions were chosen: 0.2, 0.25, 0.3, and 0.4 mil. The metal stripe spacing was matched to the metal stripe width in each test element. The metallization test elements also investigate the effect of contact-hole size on the ohmic contact resistance for each type of doped region.

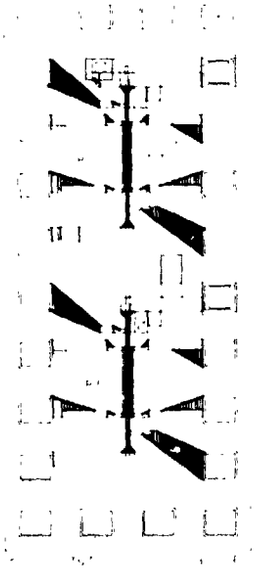

Figure 5. Plot of the Mask Pattern for a Typical Metallization Test Element

On each metallization test cell (from A1 to B3), the top and bottom four pads were used for ohmic contact studies. For reliability studies of the electromigration effect at elevated temperature, each of the two electromigration test vehicles contains three parallel metal stripes that are greater than 10 mils in length. The stress pull test on wire bonding can be done on the 8 mil × 8 mil enlarged metal pad near the center of the test chip.

Steps in the surface contour of a monolithic circuit are known to degrade the useful resolution capability of any given metallization system as well as to increase electromigration effects. To reveal possible problems, various combinations of these steps were intentionally designed into the metal test elements. Thus, seven test-element cells are devoted to the evaluation of conductor line-width, spacing, and ohmic contact resistance. Table I summarizes the permutations provided on the metal test cells.

TABLE I. METAL TEST CELL FEATURES

Cell Designation	Cell Features		
	Oxide Feature Under Four-Probe Electro-Migration Line	Contact Opening, Line Width, and Line Spacing (mils)	Contact Test
A1	p p	0.25 0.3	p p
A2	n n	0.25 0.3	n n
A3	pn -	0.25 0.25	np Schottky
A4	pn -	0.3 0.3	np Schottky
B1	pn -	0.4 0.4	np Schottky
B2	p n	0.4 0.4	p n
B3	n -	0.2 0.2	np p

Figure 6 shows a comparative photograph of the B3 metal test configuration along with the I^2L test cell. The test cell's purpose is to evaluate I^2L active circuits with the barrier metallization system. The I^2L circuits' test cell consists of the following components: a rectangular symmetrical gate cell and a slanted, symmetrical gate cell[3], each cell containing a dual output logic gate and a quad output logic gate; seven-stage ring oscillators using these basic gates; and a reduced geometry rectangular symmetrical gate seven-stage ring oscillator.

INITIAL EVALUATION RESULTS

Accelerated life tests are being carried out on the integrated-injection-logic ring oscillators. The oscillators were powered at 100 microamperes per gate during stress tests at 340°C. Out of 23 initial samples, one failure occurred at 24 hours, leaving 22 active devices. Of these remaining devices 6 have been under test for 580 hours, while the remaining 16 have been stressed for 247 hours. None of the has degraded.

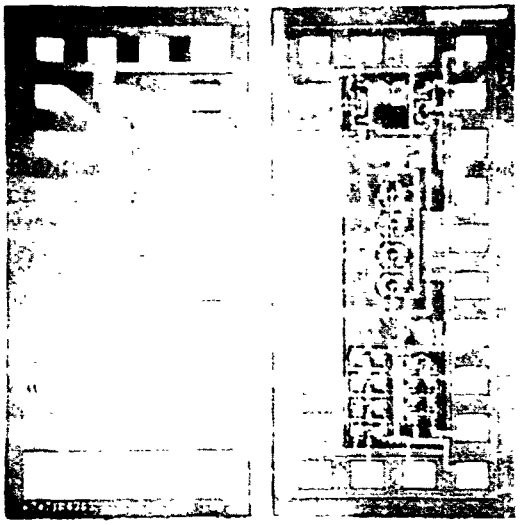

Figure 6. Photograph of the B3 Metallization Test Element and the Active I^2L Circuits

CONCLUSIONS

Integrated Injection Logic is a viable approach for large-scale integrated circuits that will tolerate 300°C. Silicon I^2L gate designs have been shown to be operable at these temperatures. In addition, a high-temperature barrier-metallization system has been chosen and an evaluation mask designed. Initial stress test results are encouraging, even though the metallization system has not been optimized.

ACKNOWLEDGEMENTS

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HIGH-TEMPERATURE COMPLEMENTARY METAL OXIDE SEMICONDUCTORS (CMOS)

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Introduction

The theory on which silicon (Si) metal oxide semiconductors (MOS) technology is founded states that this type semiconductor will perform adequately at 300°C. High temperature tests conducted on commercially available MOS field effect transistors (FET) have confirmed this hypothesis.[1-3] In this report, we present the results of an investigation into the possibility of using CMOS technology at Sandia National Laboratories (SNLA) for high temperature electronics. A CMOS test chip (TC) was specifically developed as the test bed. This test chip incorporates CMOS transistors that have no gate protection diodes; these diodes are the major cause of leakage in commercial devices.

We decided to use CMOS technology because both n- and p-channel devices could be evaluated. We also looked at small-scale integration, e.g., an inverter using CMOS junction isolation and a simulation of dielectric isolation.

Theory and actual data have been compared before.[3] In this paper we intend to report on the aging and stability of CMOS devices; especially where requirements call for minimal drift when subjected to 300°C for 1000 hours. This drift must be less than that in devices taken from room temperature to 300°C.

Physics

From semiconductor physics, the following generalization can be made:

- As temperature increases, the Fermi level moves toward the middle of the band gap, causing the built-in potential to decrease, thereby decreasing the threshold voltage.
- As temperature increases, the band gap narrows, causing a minor increase in the intrinsic carrier concentration, (n_i).
- Carrier mobility decreases with increasing temperature, causing transconductance to decrease.
- Increasing temperature increases leakage of generated and diffused currents.
- The more the doping, the greater the variation in threshold voltage as temperature increases.
- The zero temperature coefficient point occurs at higher gate voltages as the doping is increased.
- The overall transconductance decreases rapidly as temperature and doping increases.

With these generalizations in mind, we made the process variation listed in Table 1.

Table 1

Processing Variation

Wafer	Substrate	P-well
1	.8 -1.2 -cm n-type $\sim 5\times10^{15}\ cm^{-3}$	Boron 60 keV 7×10^{13} $N_S \approx 4\times10^{16}cm^{-3}$
5	.8 -1.2-cm n-type $\sim 5\times10^{15}cm^{-3}$	Boron 60 keV 2×10^{14} $N_S \approx 4\times10^{17}cm^{-3}$
7	.2 -.4-cm n-type $\sim 2\times10^{16}cm^{-3}$	Boron 60 keV 1×10^{14} $N_S \approx 2\times10^{17}cm^{-3}$
9	.2 -.4-cm n-type $\sim 2\times10^{16}cm^{-3}$	Boron 60 keV 2×10^{14} $N_S \approx 4\times10^{17}cm^{-3}$

These variations are adjustments of the various doping levels that compose the MOSFETs, and they require many trade-offs in electrical performance, making optimization difficult (Tables 2 and 3). Table 2 shows that, although wafer 1 produces symmetrical gate voltages, leakage and transconductance vary greatly between the two channels. Wafer 9 performs well in leakage and voltage but not in transconductance.

All wafers except No. 5 performed as predicted by theory. The anomaly of wafer 5 remains unexplained. The tables show the average values derived after subjecting the wafers to 300°C for 1000 hours. Threshold voltages for the surviving devices are within ±0.1V of those listed in Tables 2 and 3; leakages are within ±5μA of those listed in Table 2, and 25μA of those in Table 3. According to theory, the following pattern should appear.

For wafers 1 and 5, p-channel data should be similar.

For wafers 7 and 9, p-channel data should be similar.

For wafers 5 and 7, n-channel data should be similar.

Table 2

TC-1 Process Comparison at 300°C

Wafer	Average Leakage (μA) n-Channel	p-Channel	Average Gate Voltage (V_G) @ 10μA n-Channel	p-Channel	Average Transconductance (mmhos) n-Channel	p-Channel
1	12.41	18.85	1.45	-1.45	0.45	0.24
5	21.44	25.86	2.72	-1.26	0.22	0.26
7	3.90	6.15	1.60	-2.41	0.34	0.21
9	4.43	6.07	2.56	-2.50	0.10	0.14

Table 3

TC-4 Process Comparison at 300°C

Wafer	Average Leakage (μA) n-Channel	p-Channel	Average V_G @ 100 μA n-Channel	n-Channel	p-Channel	p-Channel	Average Gm (mmhos) n-Channel	n-Channel	p-Channel	p-Channel
1	280	460	1.54	1.55	- .79	- .78	1.10	1.07	1.82	1.75
5	88	163	3.08	3.08	-1.18	-1.21	0.61	0.61	1.79	1.79
7	107	139	1.77	1.78	-2.12	-2.14	1.07	0.99	1.27	1.27
9	88	139	2.77	2.49	-2.02	-2.22	0.66	0.68	1.16	1.14

The tables show that, except for wafer 5, the theory and the actual data generally agree.

The guard-ring, junction isolated CMOS process is quite clean and uses Q_{ss}, N_{st} reduction techniques and other schemes to reduce oxide contamination.[8-11] For example, by annealing with N_2 we decrease Q_{ss}, and by annealing with H_2 we decrease N_{st}. Careful and clean processing decreases sodium and potassium contamination. The circuits were metallized with standard aluminum 1μm thick, and standard p-glass passivation was used over the metal. The components were packaged in a ceramic, 16-pin flat pack.

Stability

Although we will not discuss all the parameters tested, as an indication of stability, we will discuss data for gate voltage at 10μA (TC-1) and 100μA (TC-4), and leakage currents.

To determine gate voltage, each transistor was measured separately. The source and substrate were connected to ground, and the drain was connected to an 8-V source. The voltage on the gate was slowly increased until 10μA was measured between source and drain; this voltage was recorded. The 10μA value includes the reverse leakage current from drain to substrate but not from p-well to n-substrate. In all data obtained, 10μA was not exceeded in the gate voltages measured for TC-1 (10μA) or for TC-4 (100μA). See Table 3.

Leakage Current

The leakage currents discussed are drain-to-source channel leakage, drain-to-substrate reverse bias leakage, and p-well to n-substrate leakage. They were measured with the transistors connected as a CMOS inverter. With one transistor biased strongly on, we then measured the current that the other transistor allowed to pass while it is turned off (Figure 1). Thus, we have a worst case measurement for leakage. In all cases, leakage was small enough ($I_L < I_{ds}$) to allow the semiconductor to remain useful in actual circuits.

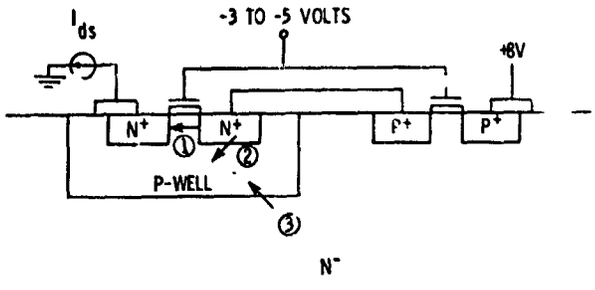

Figure 1

Measurement of Leakage Current for n-Channel

(1) Drain to Source Leakage
(2) Drain to p-well Leakage
(3) P-well to n-substrate Leakage

In all cases, we determined that the n- and p-channel devices were reasonably stable and functional except for wafer 5 which remains an unexplained anomaly.

Wafer 9 demonstrated good stability, low leakage, and a reasonable V_G at 10μA on both the n- and p-channel devices. TC-4 data supports this finding but has an order of magnitude increase in leakage because of its larger size.

Inverters

Data from transistors connected as inverters, show that they will perform as a small-scale integrated circuit (SSIC) at high temperatures for extended periods of time (300°C for 1000 hours).

V_{NL} and V_{NH}

In this test, we measured the output voltage with the inputs at 1.5V (V_{NL}) and 3.5V (V_{NH}) obtaining functionality and noise margin parameters.

I_{DN} and I_{DP}

With these tests we determined the drive current capability of the n- and p-channel devices when hooked together as an inverter.

Results

The data for inverters show that all processes were functional at 300°C after 1000 hours. In all cases, drive currents decreased with increasing temperatures as theorized; current is lost to ground through several leakage paths (Figure 1) as temperature increases.

Judging from the data obtained, there seems to be no outstanding advantage in one process over the other. There should be more dynamic testing to determine this. The data do suggest that drive currents for the higher doped devices (wafer 9) are more symmetrical for a given geometry and are less temperature dependent than lower doped devices. Furthermore, CMOS, when digitally operated, works in a complementary mode; that is, when one transistor is on, the other is off. This is helpful for reliable high-temperature performance because it allows both devices to go depletion yet still perform a given digital function (Figure 1). Therefore, we can leave the threshold voltages closer to zero than when the devices must remain enhancement at 300°C, making higher speed devices possible. Wafer 5 has not been discussed because of its unexplainable behavior.

Simulated dielectric isolation inverters showed similar trends but with a vast improvement in leakages. This makes a big difference in noise margin and absolute temperature optimization.

Many trade-offs are necessary to determine the best way to build high-temperature CMOS circuits. The principal parameters that must vary are doping profiles and size; oxide growth and overall cleanliness make the circuit possible.

Process (Doping Profile)

Judging from the results of this study, doping profiles like those of wafers 7 and 9 are best for high-temperature use. Application is extremely important because we must know what is expected from the circuit before the right process is found. For example, wafer 9 (n^- sub ≈2 x 10^{16} cm^{-3} and p-well N_S ≈4 x 10^{17} cm^{-3}) might appear to be the best choice for high-temperature electronics --- it has good symmetry, exhibits small variation with temperature, and has reasonable drive current capability. However, in some applications, it may have too high a threshold voltage and too low a breakdown voltage (≈12V). Therefore, depending on the circuits used, increasing the doping to increase the temperature range of the CMOS does not always produce an ideal circuit. In fact, some electrical requirements may make it impossible to develop a high-temperature circuit by using silicon planar technology.

Geometry

When designing the mask set for high-temperature circuits, we must include several considerations not necessary when designing room temperature circuits. For example, of major importance is the fact that the area between the p-well and the n-substrate must be as small as possible to decrease reverse leakage. This means that each n-channel transistor should have its own p-well. The price for this is an undesirable increase in the silicon area.

The mobility of holes and electrons decreases with increasing temperature but not at exactly the same rate. However, the ratio of Z/L n-channel to Z/L p-channel should be the same as in room temperature circuits to keep the circuits complementary. Keeping their ratio the same as in room temperature circuits seems to be a good compromise.

For high temperature circuits, the area from the drain to the substrate junction should be as small as possible to decrease reverse leakage. This is accomplished by horseshoeing the Z/Ls, thereby increasing circuit density -- this method is already in common use.

To make high-temperature circuits more reliable, metal lines should be as broad and deep as possible, again sacrificing chip area.

Conclusions

Existing CMOS technology can be used to produce stable and useful circuits that operate at 300°C for 1000 hours. This accomplishment, however, sacrifices some chip area and does not provide gate protection. For this latter problem, high-temperature GaAs and GaP diodes should be developed as protection devices. Although these diodes would probably be outside the CMOS chip, they could be part of the same flat pack.

Dielectric isolation CMOS would be a great improvement over junction isolation and work has begun in this area. New solar cell diodes show promise as input protection devices. This would allow us to be completely integrated again.

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"A PRESENTLY AVAILABLE ENERGY SUPPLY FOR HIGH TEMPERATURE ENVIRONMENT (550-1000° F)"

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ABSTRACT

Sodium-sulfur cells are an attractive electric energy storage for long service, in strong environment.

State of art is given. More than 200 Wh/kg cells have been tested. The known range of working temperature is 550 - 750° F. Self-discharge is quite nonexistent for months in operation.

Technical basis for expecting an operating range up to 1 000° F under high pressure atmosphere are given. Possibilities to adapt size and characteristics to particular interplanetary mission are discussed.

1) - OPERATION AND TECHNOLOGY OF THE SODIUM-SULFUR CELL

Figure 1 is a schematical view of a sodium-sulfur cell. The sodium, which is the negative pole, is inside a β-alumina glove finger. β-alumina is a ceramic having the property of transiting Na^+ ions ; it is therefore a solid electrolyte. Outside the β-alumina glove finger is located the positive electrode which is formed from sulfur held in a graphite-fibre conducting network. The whole is enclosed in two steel containers, separated electrically from each other by a ceramic insulating ring α-alumina.

The cell is manufactured in the charged condition. During discharge, the sodium passes through the solid electrolyte in the form of Na^+ ions and reacts with the sulfur while giving off polysulfides.

For the operation to be correct, it is necessary for the reagents, sodium, sulfur, polysulfides, to remain liquid. For that, the temperature must be greater than 500° F and preferably close to 650° C.

The cell may be recharged and so operate as an accumulator, able to effect a large number of successive charging cycles. But for that, the sulfur-graphite electrode must have special properties which are obtained through complex and elaborate manufacture. However, even the primary sodium-sulfur cells are capable of being partially recharged and of operating for a long time as an accumulator, but with a capacity of only one-third of the normal capacity.

The open-circuit voltage is 2.08 volts. The practical operating voltage may be chosen between 1 volt and 2 volts depending on the power and on the discharge conditions.

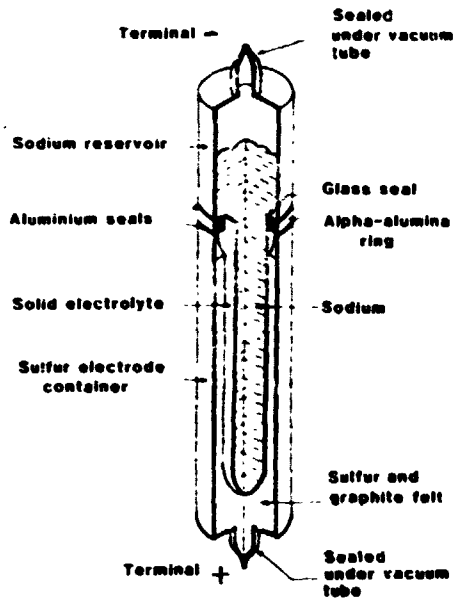


Fig. 1 : Schematic section of a sodium-sulfur cell

2) - STATE OF THE ART

The principal technological problems have been resolved during recent years.

It was a question of :

- the manufacture of the solid electrolyte
- soldering of the solid electrolyte to the insulating α-alumina ring
- perfectly tight sealing of the steel containers on the α-alumina ring
- the manufacture of the sulfur electrode
- and different other practical filling problems and sealing in an atmosphere perfectly free of any trace of water or of other polluting molecules.

At the L.d.M. sodium-sulfur cells are at present manufactured in two sizes.

Fig. 2 . Size of standard sodium-sulfur cells

A small-size cell model (4.5 Ah) is manufactured and used solely for laboratory research and experimentation purposes. A large-size model (260 Ah) is also at present manufactured in the laboratory. Its dimensions are optimized for load leveling.

The principal characteristics of these cells are given in the following table :

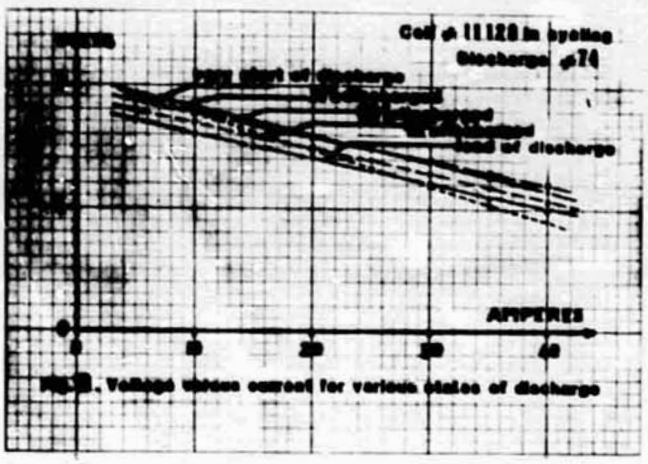
Performances for discharges within 10 hours	Small-size cell	Large-size cell
Effective capacity	4.5 Ah	260 Ah
Average voltage	1.6 V	1.5 V
Effective energy	7.2 Wh	390 Wh
Weight	100 g	1730 g
Energy per mass unit	72 Wh/kg	230 Wh/kg

The above characteristics relate to cells fitted with sulfur electrodes able to operate as accumulators (secondary generator). Similar cells, but provided with primary electrodes (primary batteries) would have capacities and energies about 20 % greater.

Figure 3 gives the electrical characteristics of a cell depending on the charging condition.

It should be noted that manufacture is easier and more reproducible in the large size than in the small size, which favours then high-energy applications on board and not miniaturized applications.

One very interesting characteristic of the sodium-sulfur generators is the absence of self-discharge. There is no self-discharge at ambient temperature and even after a long period of storage (greater than 1 year) at 650° F no self-discharg was measured.



3) - SPATIAL APPLICATION

The operating temperature (650° F) which is a difficulty and a handicap for ground applications may become an extremely favourable factor for some spatial applications.

We think immediately of the cases of interplanetary probes which must travel through high-temperature atmospheres. Such is the case of probes whose mission is the explaration of VENUS. For example, at an altitude of 17 km, the temperature is 630° F and under these conditions the sodium-sulfur cells operate freely, without needing any heating or heat insulation. The high pressure (28 bars) which reigns at this altitude can be withstood by the containers because of their cyclindrical shape and small diameter. Nothing stands in the way of very long duration missions, which may be considered in months or even in years.

However, it must be recognized that the present cells have not been optimized for such spatial applications and that certain modifications would have to be made. For example, for operating in any position and with any orientation, it would be necessary to provide the inside of the solid electrolyte with a porous layer wettable by the sodium which is designated sodium wick.

A great number of experimental checks remain to be made, during which certain imperfections might appear and involving studies and modifications with respect to the present state of the technique. These tests relate for example to :

- resistance to high accelerations (several hundred g)
- resistance to shocks and vibrations
- possible problems of thermal shocks on rapid entry into hot atmospheres
- the problems of checking and guaranteeing reliability.

4) - FUTURE POSSIBILITIES

From the mechanical and sealing point of wiew, present cells are able to withstand substantially 1 000° F. But the problems of corrosion of the containers, which are overcome at about 650° F, limit the serviceable life for higher temperatures.

However certain simple solutions may be considered. For high-pressure atmospheres, the use of deformable containers would be a neat solution, both for reducing the weight and for resolving the operating problems. In fact, it would be possible to balance the internal pressure with the external pressure, which would allow operation at practically unlimited pressures. Under high pressures, boiling of the sulfur only occurs at much higher temperatures and consequently operation close to 1 000° F would become possible (at 1 000° F, it is sufficient for the pressure to be greater than 3.3 bars).

Figure 4 shows the possible operating range.

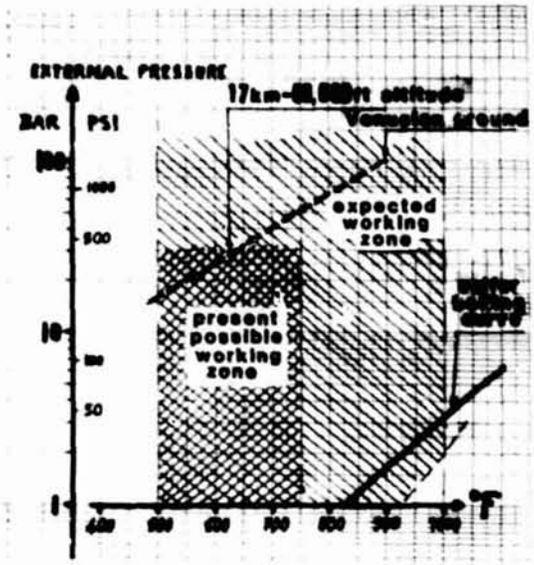


Fig. 4 . Sodium-sulfur working zones.

The principal problem would become that of high-temperature corrosion of the container by the polysulfides. The anticorrosion protection used at the present time and limited by its cost, could be substantially increased and solutions using more studied materials and techniques may be considered.

In any cas, the corrosion problems are less serious when the missions are limited to a few days or a few tens of days and not to years.

It is then not utopian to put forward the sodium-sulfur generators as extremely valid candidates for future ground explorations on VENUS (900° F, 100 bars), for missions of fairly long duration.

STUFFED MO LAYER AS A DIFFUSION BARRIER IN METALLIZATIONS FOR HIGH TEMPERATURE ELECTRONICS

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Abstract

Auger electron spectroscopy (AES) was employed to characterize the diffusion barrier properties of molybdenum in the $CrSi_2$/Mo/Au metallization system. The barrier action of Mo was demonstrated to persist even after 2000 hours annealing time at 300°C in a nitrogen ambient.

At 340°C annealing temperature, however, rapid interdiffusion was observed to have occurred between the various metal layers after only 261 hours.

At 450°C, the metallization degraded after only two hours of annealing.

The presence of controlled amounts of oxygen in the Mo layer is believed to be responsible for suppressing the short circuit interdiffusion between the thin film layers. Above 340°C, it is believed that the increase in the oxygen mobility led to deterioration of its stuffing action, resulting in the rapid interdiffusion of the thin film layers along grain boundaries.

The $CrSi_2$/Mo/Au barrier metallization system lent itself easily to fine line patterning.

Introduction

Thin film metallizations play a critical role in the reliability of microelectronic devices. The deleterious effects of aluminum alloy penetration[1-2] and the "purple plague"[3-4] in gold-aluminum thin film couples are well-known examples. Thin film metallizations are made up of very small grains, high densities of grain boundaries and dislocations. It is well established that grain boundaries and dislocations increase atomic mobility by acting as short circuit diffusion paths.[5-6]. Gjostein[6] has shown that for face centered cubic metals, thin film interdiffusion is controlled by dislocation pipe diffusion and grain boundary diffusion in the temperature range 30-60 percent of the melting point. Below this temperature range, interdiffusion is not very significant. Above this temperature range, lattice diffusion predominates. Diffusion barriers[7] such as stuffed barriers, passive barriers, sacrificial barriers and thermodynamically stable barriers, are intended to suppress short circuit controlled interdiffusion. The purple plague mentioned earlier can be ascribed to Kirkendall voiding through short circuit interdiffusion.

Harris et al[8] reported that the diffusion of Ti in Mo was inhibited by the presence of oxygen in the Mo layer of a Ti/Mo/Au system. Nowicki and Wang[9] observed the suppression of Au-Si intermixing in Si/Mo/Au system if the Mo layer was reactively sputtered in N_2-Ar mixture. They attributed the enhanced Mo barrier action to N_2 occupation of the octahedral sites around the Mo atoms. Neither of the above studies dealt with prolonged annealing effects at high temperatures.

The need for high temperature (up to 300°C) microelectronics applications in such diverse fields as aircraft engine controls, nuclear reactor core monitoring instrumentation and oil and gas well downhole instrumentation has further imposed stringent reliability requirements on microelectronic interconnections. Diffusion barrier protection of the ohmic contact layer and metal conductor layer thus assumes new importance. This paper will discuss the enhanced high temperature diffusion barrier properties achieved through the introduction of controlled amounts of oxygen in the Mo barrier layer of the Cr/Mo/Au metallization system.

A barrier metallization system is shown schematically in Figure 1. It consists of an ohmic contact layer ($CrSi_2$), a diffusion barrier layer (stuffed Mo) and an interconnect or conductor layer (Au). Figure 2 illustrates a tri-metal system where diffusion barrier protection is lost during heat treatment.

Experimental Procedure

Sequential deposition of the thin film layers of Cr, Mo, and Au on (111)-oriented, N-type silicon single crystal wafers was carried out using planar r.f. magnetron sputtering (Perkin-Elmer Ultec Model 2400-8SA). Sputtering pressures were less than 10 mtorr using argon. Oxygen-argon gas mixtures were utilized for reactive sputtering of the Mo. Prior to sputtering, the silicon wafers were etched in dilute HF, rinsed thoroughly in de-ionized water, air dried and transferred immediately into the sputtering chamber.

After sequentially depositing the Cr/Mo/Au system, sintering was performed in a quartz tube in a flowing nitrogen ambient at 450°C for 15 minutes to affect $CrSi_2$ formation.

Annealing experiments were subsequently carried out at 300°C, 340°C and 450°C. The 300°C anneals were performed in nitrogen ambients in a quartz tube for 168 hours, 1000 hours and 2000 hours.

Annealing experiments above 300°C were carried out in vacuum. AES was employed to study the extent of thin film interdiffusion between the various metal layers. Fine line pattern definition was evaluated using a combination of photolithographic and chemical etching techniques.

Results and Discussions

AES profiles of the Cr/Mo/Au system before and after sintering at 300°C are shown in Figures 3-6. There was limited penetration of the Cr layer by the Mo layer during the sputter deposition. After annealing at 300°C for 2000 hours, the diffusion barrier properties of the Mo layer were found to be intact. Some redistribution of the oxygen in the Mo layer occurred during the 300°C annealing. The suppression of the expected grain boundary interdiffusion may be

ascribed to the oxygen incorporated into the Mo layer. The stuffing behavior of oxygen may be similar to that of nitrogen in Ti-W observed by Nowicki et al[10] in the Al/Ti-W/Au system. Nowicki and Wang[9] also reported that controlled incorporation of nitrogen into molybdenum significantly reduced the rate of grain boundary interdiffusion in Mo/Au couples.

Annealing above 300°C revealed that oxygen stuffing does not completely suppress short circuit controlled interdiffusion such as shown in the AES profile of Figures 7 and 8. In fact, at 450°C, the oxygen mobility was so high that stuffing action was lost with a resultant loss of Mo barrier action after only 2 hours of annealing. This observation is consistent with the equations of Gjostein[6] and other recently observed thin film interdiffusion phenomena[6]. Fine line patterning was accomplished using photolithography and chemical etching such as shown in Figure 9. The fine lines are two microns in width.

Summary

The diffusion barrier action of stuffed Mo layers has been demonstrated to be reliable at 300°C for at least 2000 hours in a nitrogen ambient. The incorporation of oxygen in the Mo layer is believed to be responsible for the enhanced diffusion barrier action of the Cr/Mo/Au metallization system at temperatures below 300°C. Above 300°C, the Mo barrier action rapidly deteriorates.

The cooperation of Dr. Joseph Peng (formerly of ARACOR, Sunnyvale, California, and now with Fairchild) and Dr. Aristotelis Christou (NRL, Washington, D. C.) in the AES analysis is gratefully acknowledged. Our thanks also to Dr. Christou for many helpful disucssions.

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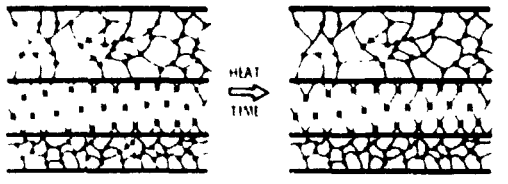

Figure 1:
SCHEMATIC ILLUSTRATION OF A STUFFED BARRIER. NOTE THE ABILITY OF THE SYSTEM WITH SEGREGATES TO GRAIN BOUNDARIES

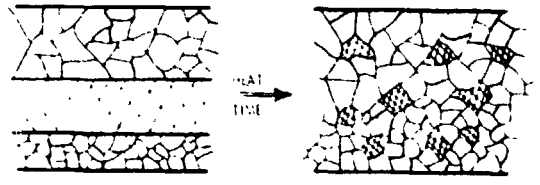

Figure 2:
SCHEMATIC ILLUSTRATION OF A TRI METAL SYSTEM WHERE BARRIER PROPERTIES IS LOST DURING HEAT TREATMENT

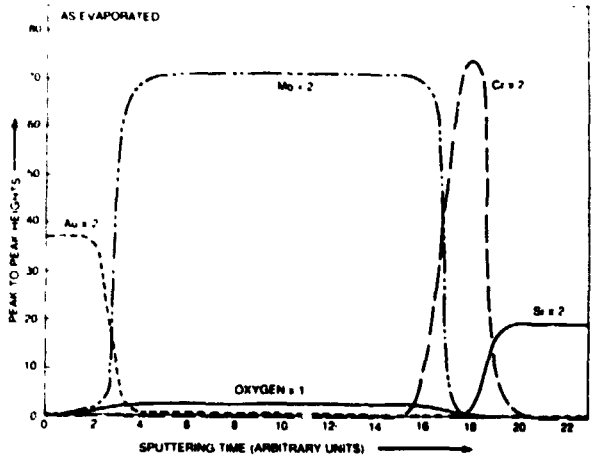

Figure 3:
AES SPUTTER PROFILE OF THE Cr/Mo/Au SYSTEM AFTER $CrSi_2$ FORMATION

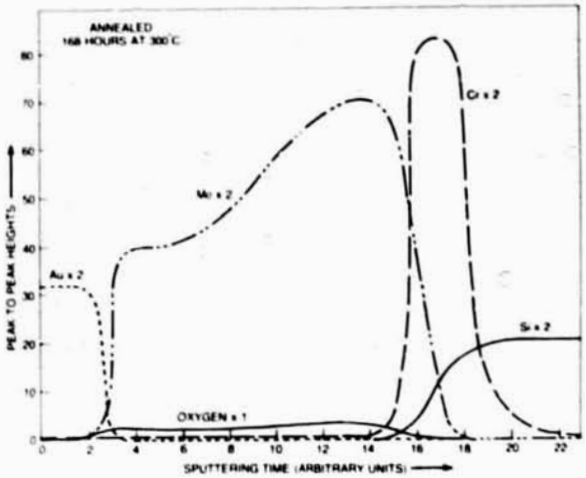

Figure 4: AES SPUTTER PROFILE OF THE Cr/Mo/Au SYSTEM AFTER A 168 HOUR ANNEAL AT 300°C FOLLOWING THE $CrSi_2$ FORMATION

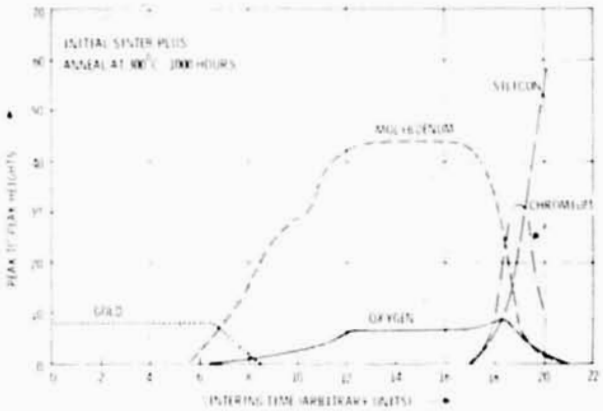

Figure 5: AES SPUTTER PROFILE OF THE Cr/Mo/Au SYSTEM AFTER A 1000 HOUR ANNEAL AT 300°C FOLLOWING THE $CrSi_2$ FORMATION

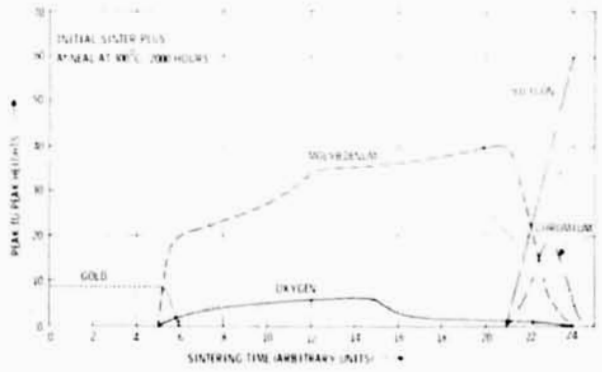

Figure 6: AES SPUTTER PROFILE OF THE Cr/Mo/Au SYSTEM AFTER A 2000 HOUR ANNEAL AT 300°C FOLLOWING THE $CrSi_2$ FORMATION

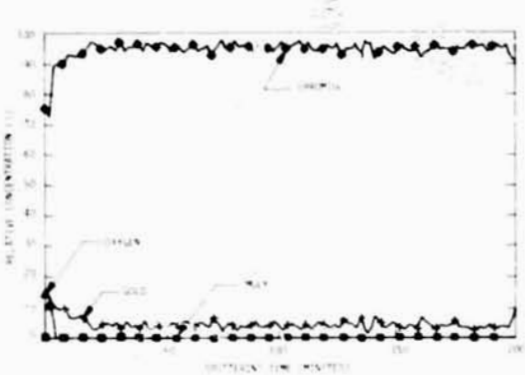

Figure 8: AES SPUTTER PROFILE OF THE Cr/Mo/Au SYSTEM AFTER VACUUM SINTERING AT 450°C FOR 2 HOURS

Figure 9: PHOTOMICROGRAPH OF FINE LINE PATTERNING OF THE Cr/Mo/Au SYSTEM. THE FINE LINES ARE 2 MICRONS IN WIDTH.

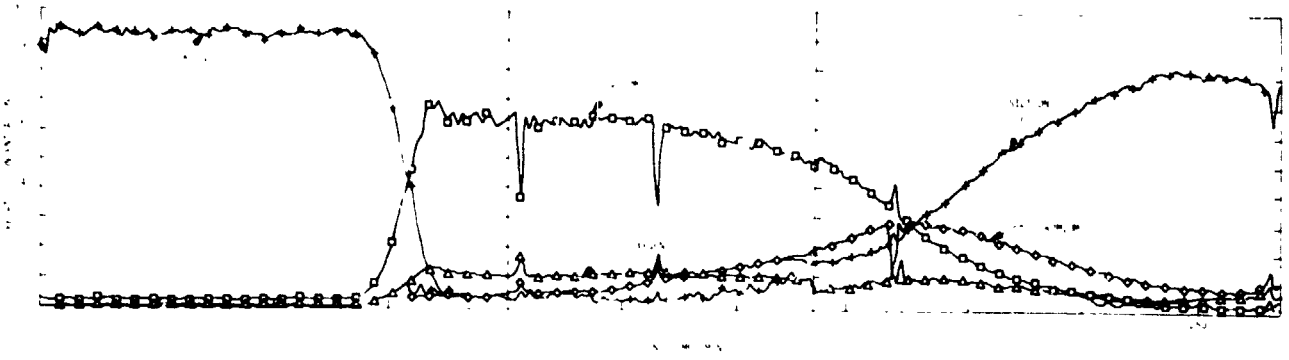

Figure 7: AES SPUTTER PROFILE OF THE Cr/Mo/Au SYSTEM AFTER VACUUM SINTERING AT 340°C FOR 264 HOURS

REFRACTORY GLASS AND GLASS CERAMIC TUBE SEALS

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Complex vacuum tube envelopes are required to house and support integrated thermionic circuits (ITC) during long-term operation at elevated temperatures. Li_2O-ZnO-SiO_2 glass ceramic and CaO-Al_2O_3 glass seals were investigated because they are refractory, moldable, have relatively high thermal expansion coefficients and bond directly to a variety of metals.

Materials and techniques were developed to fabricate the silicate glass ceramic (ρ500°C = $10^5\Omega$m; Tg = 450°C) into a toroidal tube design containing 64 Pt/Rh feedthroughs. Subassemblies were exposed to 600°C for periods in excess of 140 hours with no deterioration of vacuum seal integrity. However, lithium ion conductivity reduced lead-to-lead resistance below 1 megohm at 350°C, yielding a device unacceptable for ITC applications.

The calcium aluminate glass (ρ500°C = $10^9\Omega$m; Tg = 900°C) contains no alkali but is more difficult to fabricate into complex shapes. Special transfer molding techniques were developed using pre-enameled metal piece parts. These subassemblies were vacuum tight, had a lead-to-lead resistance of 20 megohms at 600°C and are believed acceptable for ITC applications.

PACKAGING TECHNIQUES FOR LOW-ALTITUDE VENUS BALLOON BEACON

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Summary

This report presents the results to date of a specific design project in which a microwave beacon is required to operate for a limited time at high temperature (~325°C) and at high pressure (~10 bars), in a chemically hostile environment, after surviving large mechanical shock forces (up to 280 gs). One of the most interesting results of this work is the finding that many existing, commercially-available components can be used in such a design with only minor modifications. A further result of some interest is that a crude (and consequently low-cost) testing program can be designed to identify and select promising commercial components.

Symbols

COS	ceramic-oxide-semiconductor
DC	direct current
g	acceleration of gravity
HF	hydrogen fluoride
MHz	megahertz
MOS	metal-oxide-semiconductor
P/P	peak to peak
R-C	resistor-capacitor
RF	radio frequency
V	volt
VBB	Venus balloon beacon

Introduction

The goals of this low-cost design effort are to develop a short-lived microwave beacon which is capable of intermittent operation while suspended from a balloon floating in the atmosphere of Venus, and to do it within a relatively modest budget ($160K). It should be made clear from the start that we are discussing the beacon developmental model, not flight hardware. The flight model has not yet been built and, in view of recent changes in the Venus mission's scope, may not be built for some time. Still, the design exercise is an interesting example of what can be done with limited funds and with existing commercial components, modifying them where necessary, and by using also a bit of that famous American ingenuity.

The low-altitude Venus Balloon Beacon (VBB) was conceived as one approach to studying the winds of Venus. VBB is a small, L-band microwave transmitter to be suspended from a high-pressure French balloon, one-meter diameter, filled with water vapor and flotation gas. The beacon is designed to transmit a series of 1 microsecond, 1% duty cycle pulses which will permit Earth ground stations to track the balloon as it gets blown about by various Venusian atmospheric disturbances.

At the proposed 18-km flight altitude, the expected ambient conditions are 325°C (617°F) and 10 bars (160 psia), with wind velocities as high as 20 meters/sec. The atmosphere is primarily carbon dioxide, with traces of other gases including HF. The forces on the beacon-balloon system during entry into the Venusian atmosphere are calculated at 280 gs for two minutes. The total time of flight of the balloon will be 240 hrs, with the transmitter on during 96 five-minute periods, spaced equally during those ten Earth days.

Discussion

The VBB electronic system comprises batteries, power supply, RF cavity, cavity modulator, timer switch, and antenna (Figure 1). The major problem areas are the power supply (1000 VDC needed to fire the RF cavity), and the cavity modulator (pulse timing accuracy better than 1 part in 10^7 required). The power supply was designed to use reed switches both as input choppers and output rectifiers. The cavity modulator is a large hybrid circuit using an especially cut crystal as the timing element. Both will be discussed in detail shortly, but first a word about the easier parts.

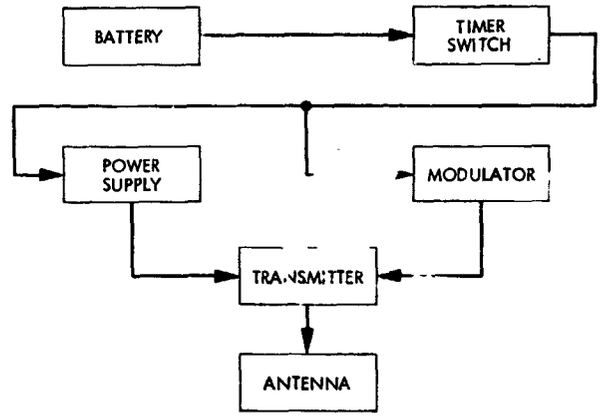


Figure 1. VBB Block Diagram

Batteries

Power is supplied by 1.5 V sodium cells, whose electrolyte melts at ~280°C and can operate in the liquid phase up to ~350°C. These cells hold a charge indefinitely in their solid state and produce 20 watt-hr per cell when in the liquid state (see Figure 2). Since these batteries produce no power when solid, i.e., below 280°C, they become a built-in on-switch for the system, thus eliminating one set of potential headaches including the mass of a main power switch. To get the power needed for 8 hours of operation requires four cells. These use up half of VBB's 2-kg total mass limit.

Timer

A timer was needed to spread the power usage out over the 240-hour flight. A mechanical timer (either a motor- or solenoid-driven escapement) was considered, but these had both mass and power-consumption penalties. In view of the high Venus ambient temperature and other higher temperature sources (e.g., the RF cavity operating temperature is on the order of 450°C), a bimetallic switch seemed an attractive solution. Several bimetallic switches of suitable time constant were found avail-

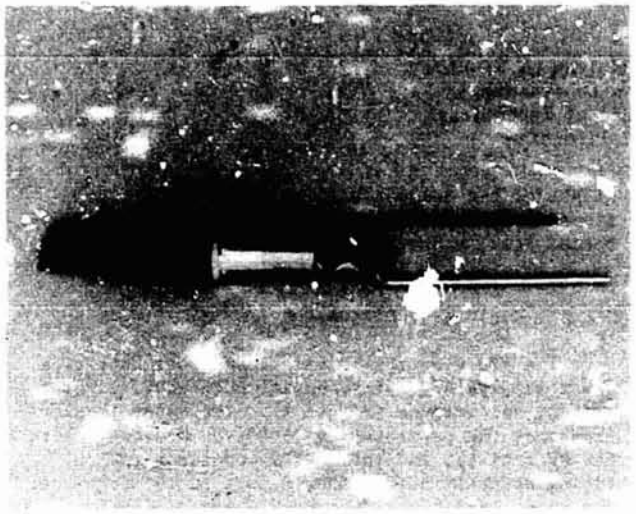


Figure 2. Sodium Battery Cell

able commercially, so this approach was considered the primary solution to the timing problem. The motor- and solenoid-driven escapement were relegated to back-up status.

RF Cavity

The RF cavity used for the development model is a standard aircraft transponder RF cavity, made by General Electric Company, modified by the manufacturer to withstand the 325°C environment. The engineering staff of the GE tube division was interested in the project and made us an offer that, from both schedule and financial standpoints, we could not refuse. In principal the conversion of the standard RF cavity to a high temperature device was not too complicated. The major changes centered around the materials used to make the cavity and the type of soldering/welding used in its assembly. The tube itself was already designed to operate well above 325°C.

Antenna

An antenna with the proper radiation pattern was found and scaled down to operate in L-band. (See Figure 3.) There is no obvious reason why the pattern should change at the high temperatures expected of this project, but the optimum operating frequency will change if dimensions change. Hence, a test antenna was built from solid copper for pattern verification and for frequency-shift evaluation at L-band frequencies and high temperatures. The test model is too massive for flight use; but given additional time and money, the flight unit mass could be reduced greatly, e.g., by designing the flukes hollow, by incorporating the ground plane into the transmitter box, and by using lighter construction materials.

Antenna Cable

One problem which we had to solve that was not so simple as it at first seemed, was conducting the RF signal from the cavity to the antenna. The coax cable industry currently produces high temperature semirigid coax cable that will withstand 325°C for extended periods. This cable uses powered magnesium oxide as the dielectric. Since this material is hygroscopic, both ends of the cable must be sealed. Unfortunately, no commercially available hermetically-sealed connectors

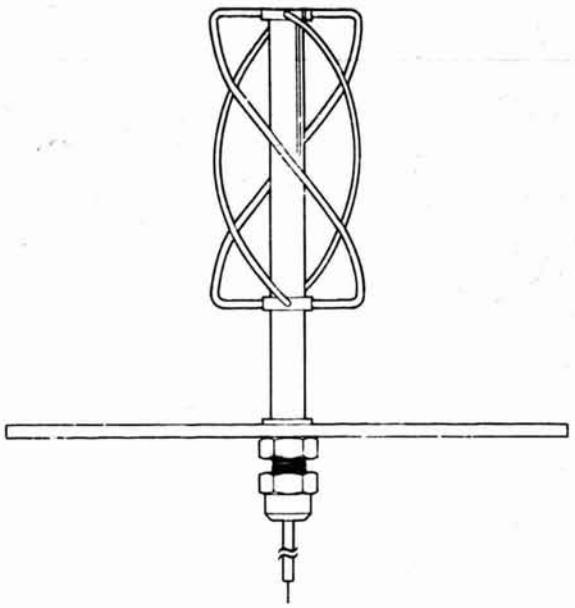


Figure 3. VBB Antenna

could be found, for any temperature range. Hence we decided to do it ourselves.

It had been noted that the standard type OSM connectors for 0.141 semirigid cable, used for testing some multiplier transistors for a possible oscillator/modulator, were made entirely of metal. Since the connector leaves the cable dielectric exposed, plugs of some material were needed to create seals at both ends of the cable.

Various types of epoxies were considered, but were found too vulnerable to water. Previous experience with hybrid construction suggested using ceramics. After some investigation Macor, a machinable ceramic manufactured by Corning Glass Works, was selected and machined into several thick-walled washers. Inner and outer wall surfaces then were coated with low frit gold and fired at 850°C to create solderable surfaces. These surfaces next will be coated with a gold germanium solder, the washer placed in the end of the cable, and the cable end heated above 360°C to complete the solder joint. Post-soldering helium leak tests will be performed to assure that no detectable leaks larger than 10^{-9} cc/sec are present. Given that no surprises develop from soldering plug and connector simultaneously, this problem is solved.

Power Supply

Figure 4 is a schematic of the power supply-chopper-rectifier-driver circuit. The principal component of the circuit, the transformer, proved to be the simplest to find. In the literature study at the beginning of the work, a reliable supplier of high temperature transformers (General Magnetics) was located. The test transformers procured from this source have functioned without problems in all testing performed to date.

The tougher problem has been posed by the chopper/rectifier requirements. When first considered, it was thought that the only practical solution to this problem lay in the reed switch approach. Since the reed switches were large and relatively heavy, we were motivated to look for other possibilities.

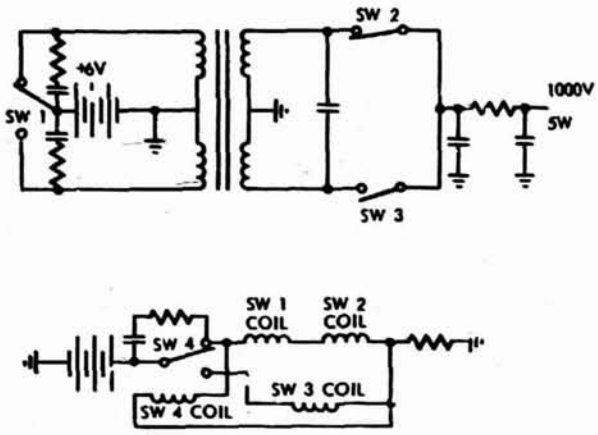


Figure 4. Schematic Circuitry

One of these led us to test some very small (TO-5 can) reed relays to get an idea of their useful life and voltage-switching capabilities. When run as self drivers at room temperature and 9 volts, these relays ran for 23 days at 3350 Hz with no apparent degradation. At about 700 V, however, the contacts were burnt at a few microamps. Since they worked so well at their rated winding voltage of 9 volts, it was felt that they might suit the low-voltage side of the chopper/rectifier circuitry.

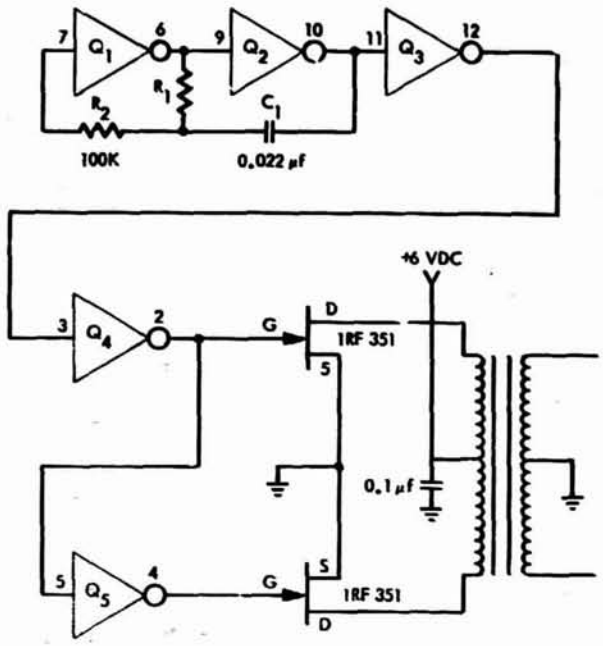
Accordingly, one of these devices was dissected and examined to determine what modifications they would need to survive at 325°C. These modifications, which consisted mostly of substituting high temperature wire insulation and structural components for their existing counterparts, would have required procedural changes during manufacture, rather than post-assembly retrofits. The changes were modest enough to be quite feasible for typical development projects, but were not feasible within the time and cost limits available for VBB. Consequently, we feel that this approach is worth stating for consideration in future high-temperature projects, even though we could not use it in our case.

Another approach explored was based on the use of semiconductor devices as low-voltage switches. The chief advantage of such an approach would be a significant simplification of the chopper/rectifier synchronization problem.

Preliminary tests indicated that the Harris CD 4009D Ceramic Pack COS/MOS inverter and the IRF 351 HEXFET power transistor would function at temperatures above 250°C. A DC/DC converter was designed, using the CD 4009D as the oscillator and driver of a pair of the 351's (see Figure 5).

For the converter tests, the 1 kV secondary was rectified by off-the-shelf diodes (not shown in Figure 5). These diodes functioned satisfactorily up to about 200°C, at which point they were removed from the oven and operated at room temperature for the higher temperature part of the tests.

The test converter (see Figure 6) functioned for 50 hours at 250°C. Efficiency dropped from 93% at room temperature (20°C) to 73% at 250°C. In view of the limitations on power available in the VBB mission, this approach was rejected. For cases not so limited, however, this approach should be quite useful.



NOTE: $Q_1 - Q_5$ CD4009D
+6V ON PIN 1 AND 16
GND ON PIN 8

Figure 5. Solid State Chopper

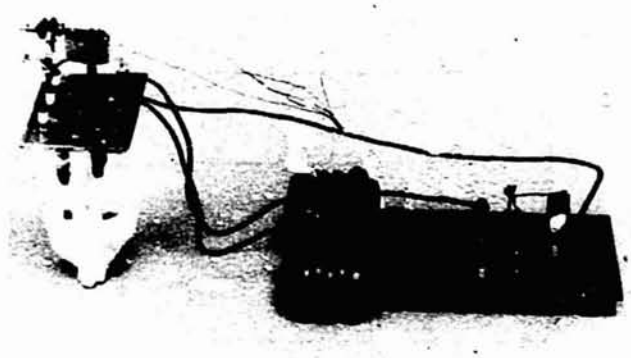


Figure 6. VBB Test Converter Unit

The approach finally selected for VBB uses reed switches supplied by Gordos Corporation. These high-voltage switches are packaged with driver coils similar to one of their standard lines. The contact bounce on these switches was markedly less severe than some others tested, and are capable of switching the 1 kV secondary without difficulty.

We found in our testing that improper synchronization can result in destruction of the switches, but that if a very precise R-C circuit is employed contact burnout on the 1 kV side of the circuitry can be avoided. We have found also that type C switches (i.e., SPDT, see Figure 4) can be used on the low-voltage side and in the driver circuit, but the standard type A (i.e., SPST) switches are required in the secondary side to survive the 1 kV.

Hybrid Modulator

Earth station tracking of VBB requires the timing accuracy of the transmitted pulses to be at least as good as 1 part in 10^7. This requirement precluded the self-blocking mode of tube operation, and imposed a need for some sort of modulator. A high-temperature test program at JPL several years ago had established that properly cut crystals were capable of maintaining the required accuracy. Three crystals (3 MHz, 5 MHz, and 10 MHz, respectively) cut for minimum drift at 325°C, have been acquired from a commercial supplier. As of this writing, these crystals are being tested at temperature to verify turnover points and drifts.

The crystal control circuit designed as a result of the above considerations is shown in Figure 7. A breadboard model of this circuit, shown in Figure 8, was fabricated from materials known to function satisfactorily at high temperatures. The principal testing goal was to evaluate the 2N5911 dual JFET's operations and to determine what would be required to keep it operating satisfactorily at high temperature.

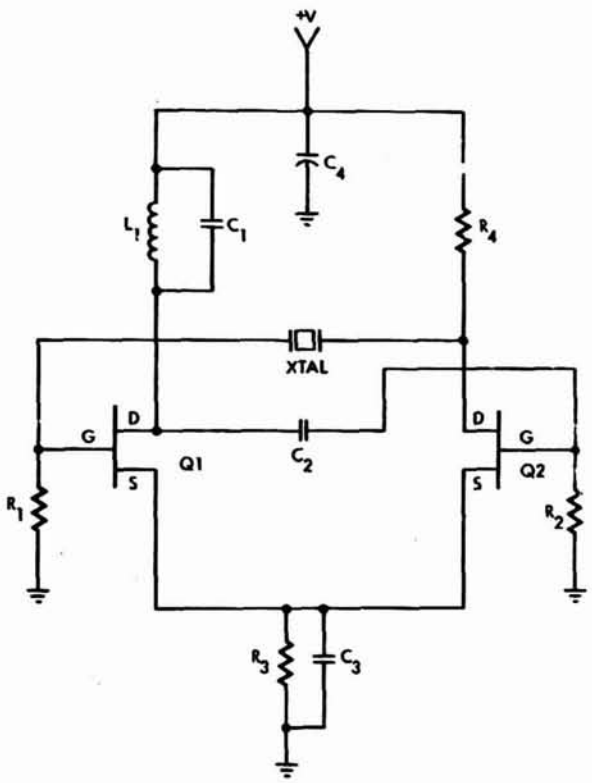


Figure 7. Crystal Control Circuit

Testing showed that a tuned circuit feeding Q1 (as shown in Figure 7) was required for satisfactory operation. The results of operating the test circuit at 280°C for 100+ hours, which produced no failures, are shown in Figure 9. It will be noted from these data that increasing the temperature reduces the output amplitude. If the rate at which the output drops remains fixed, a second tuned circuit, feeding Q2, will have to be added to achieve satisfactory performance at 325°C. This presents no obvious problems.

It should be noted in passing that it was not absolutely necessary for all materials in the test circuit to be high-temperature substances. Low

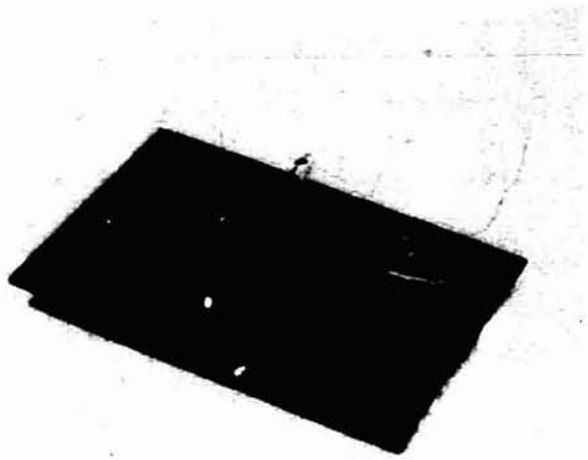


Figure 8. Breadboard Model

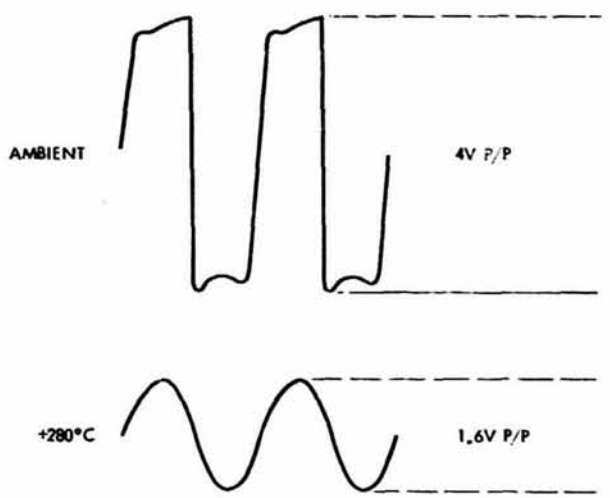


Figure 9. Output Wave Forms

temperature solder, for example, melted at the test temperature, but remained in puddles around the component leads and performed its electrical functions satisfactorily.

As of this writing, a refined test circuit has been laid out on a 2 in x 2 1/2 in, 96% alumina core substrate. Thanks to extensive testing of hybrid inks for high temperature service conducted previously by Sandia Laboratories, a satisfactory ink (Du Pont 9910) was found easily. Gold-germanium solder has been chosen for connecting discrete component leads to substrate inks. The high temperature epoxies and/or potting compounds for bonding the discretes to the substrate have not yet been chosen.

The refined test will be conducted using all discrete components. For later tests and flight hardware, 2N5911 and 2N3821 dies have been ordered, along with chip resistors rated for 325°C operation. It is anticipated that the complete circuit will fit on a much smaller substrate.

Conclusions

The principal conclusion to be drawn from the work reported here is that many ordinary components, designed for operation under Earth-normal condi-

tions, may be used in extreme environments -- either "as is," or with minor-to-moderate changes in their construction. A catalog of such extendabilities was started by previous researchers, and has been augmented by the present work.

In addition, a great deal of useful extendability information pertinent to a particular project may be gained at relatively low cost, by employing "rough and dirty" test procedures, custom-designed to fit the needs of that project. In our case, even though the development model has not yet been tested as a complete system, the prospects for a positive, within-budget outcome of the May-June time-frame development-system tests (schedule dependent upon receipt of the final-design cavity, reed switches, etc.), appear quite bright. At that time, our principal problem will become meeting the 2-kg mass limit. Given the results to date, it appears that the only section requiring extensive redesign here will be the antenna, and this does not appear to pose any significant problems.

Acknowledgment

This paper is based upon research performed at the Jet Propulsion Laboratory, California Institute of Technology, under contract NAS7-100, sponsored by the National Aeronautics and Space Administration.

HIGH TEMPERATURE (Al_2O_3) INSULATION AND LIGHT WEIGHT CONDUCTORS

by

Henry Walker, Director of Research, Permaluster, Inc., Burbank, California

SUMMARY

The search by the electronic industry for components that are light weight, more compact, are capable of operating in very high temperature and all environmental conditions is now proving rewarding.

The properties of such a flexible, transparent, thin film of aluminum oxide insulated wire or strip (with a melting point of 2050°C.) is unique for applications in the electronic, missile, atomic reactor, aerospace, and aircraft industries. The oxide film is highly flexible, suitable for all windings of any size and shape of coil (magnetic). Briefly touched upon are the ultraviolet, proton gamma radiation uses, as well as high vacuum and cryogenic applications.

Since the film is inorganic and chemically inert, it does not age or deteriorate in storage and has good dielectric properties (1000 volts per mil). In brief, components designed around this unique material will keep abreast of present day and future technology.

Designers of electro-magnetic components can now achieve higher ratings per unit of weight and a reduction in size. With proper design, less insulation will be required and the dielectric losses are reduced.

The use of an aluminum conductor (round or rectangular wire or strips) will save 50% in weight, which is a distinct improvement in commercial applications such as linear motors, medical instruments, etc., where lower mass will result in lower inertia. Rotary equipment with low mass simplifies dynamic balancing. As vibration from dynamic imbalance is reduced, greater sensitivity and improved high frequency response in moving coil applications results from this lower mass. In all, it is a dream come true for most engineers.

INTRODUCTION

Compared to copper, aluminum with Al_2O_3 insulation operates cooler and will not oxidize. When operating temperatures of above 100° C., copper will form an invisible film of cuprous oxide; above 200° C. cuprous and cupric oxide are formed readily on the surface, thus reducing the conductance as ultimately severe corrosion occurs and eventually the conductor is rendered useless. Even nickel coated copper is subject to a galvanic action of the two metals. In a high temperature operation, migration of atoms is created.

Performance of electrical components in high temperature is seriously handicapped due to the lack of suitable insulating materials as the components are subjected to severe physical stresses in environmental conditions. When failure occurs in organic insulation, the failure remains permanent owing to the electrically conductive carbon paths that are formed throughout the insulation as well as other endangering problems, such as lack of adhesion, oxidation, evaporation, and aging.

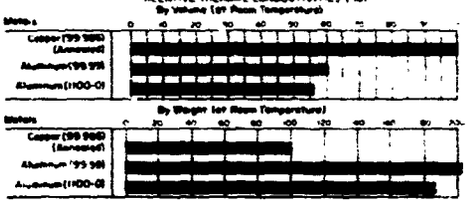
Aging is accompanied by weight loss in organic material where shrinkage results in the resin portion causing it to lose its bond in the slot cells, thus creating failure. Variation of temperature or rotating speed causes mechanical abuses of the insulation. Thermal degeneration is faster close to the current-carrying conductors where the temperature is at a maximum; Therefore, the failure is induced at the hottest spot of the winding.

Aluminum conductor and Al_2O_3 insulation, which is ceramic in nature, is free of galvanic action or oxidation. In case of a breakdown, the insulation does not create tracking of a permanent conductive path throughout the insulation. In fact, oxide from the air creates a new insulated oxide and could repair itself. Therefore, it is a good reason to consider the relation between operating temperature and insulation life. A component made with high temperture insulated material will be more reliable and will protect itself and its payload from instant heat and pressure.

CONDUCTORS

For several decades aluminum has been successfully employed in the electrical engineering field and in various other applications such as in transformers, generators, etc., using bulky interleaving materials such as paper, plastics, or laquer as insulation—far from satisfactory.

TABLE I—Thermal and electrical conductivities of aluminum and copper.



Aluminum for electric conductors has a resistance of about 34.5 ohms/mm^2, which is equal to approximately 62% of the conductivity of electrolytic copper. The specific weight is 2.7 gm/cm^2, or about 30% of that of copper. This means that an aluminum conductor of equal conductivity weighs only 50% of that of a comparable copper conductor. In many cases, depending upon design, the conductive weight can be further reduced depending on the dielectric loss, as aluminum operates cooler, and dissipates heat more rapidly.

Copper clad aluminum wire is re-inforced with EC grade aluminum conductor of an improved design developed to give electric power new versatility in construction. In addition to the contribution of its high strength to the conductor, it adds to the total conductivity of the conductor, so that it performs a dual function of strength and conductance. Of

course, it is lightweight in all given gauges of wire. It is also corrosion resistant, making it easily applicable to magnet wire, cables, etc. Copper clad aluminum is a composite material; The interdiffusion of copper and aluminum atoms occurs so that the materials are inseparable. They are joined in a metallurigical bond. Furthermore, when the composite rod is drawn to fine wire sizes, its concentricity and the proportions of both metals remain unchanged. The same concept can be applied for copper clad steel, which is a lead cable for the semiconductor industry, among others.

CONDUCTOR CHARACTERISTICS

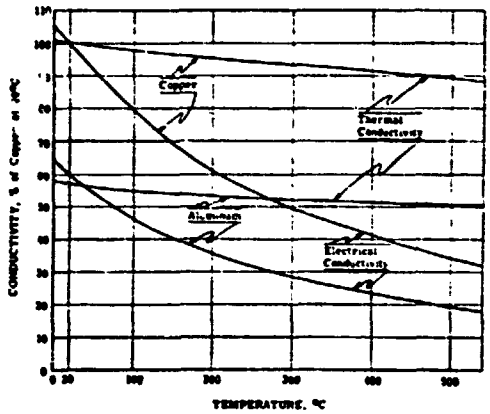
	Copper	Cu/Al	Aluminum
Density LBS/IN^3	0.323	0.121	0.098
Density GM/CM^3	8.91	3.34	2.71
Resistivity OHMS/CMF	10.37	16.08	16.78
Resistivity Microhm-CM	1.724	2.673	2.790
Conductivity IIACS %)	100	61-63	61
Weight % Copper	100	26.8	- - - -
Tensile K PSI-Hard	65.0	30.0	27.0
Tensile KG/MM^2-Hard	45.7	21.1	19.0
Tensile K PSI-Annealed	35.0	17.0	17.0*
Tensile KG/MM^2-Annealed	24.6	12.0	12.0
Specific Gravity	8.91	3 34	2.71

*Semi-annealed

Copper clad aluminum lends itself to shaping, forming, and drawing. Wire is produced from .003" diameter and rectangular wire from .001" and is very suitable for winding fine, small coils. Larger wire is suitable for lightweight cables.

The adaptation of aluminum wire or foil and/or copper clad aluminum conductor is a step to attain improved operation and reliability through better balance in components with the following results:

1) This material can be operated at a greater speed than copper wire using less power in movable coils.
2) "Ihm" has been reduced so that a decible measurement of so ... levels in stationary coils has been reduced.
3) Load capacity of given ratings have been effectively increased.
4) Core losses have been decreased and efficiency increased.
5) Operating temperatures are from -450° F. to 1000° plus F.



Comparison of thermal and electrical conductivities of copper and aluminum at various temperatures.

FORMATION

Note the increasing demand in the electronic industry for wire or strip to be lighter in weight—almost weightless—and an insulation so thin—almost spaceless—that should withstand 1000° F. or higher temperatures, and survive almost any environmental conditions.

Additionally, there is an increasing demand that it be:

a) Sufficiently flexible, to allow winding in any form, including miniature coils and edgewinding of rectangular wire wound under great stress.

b) Sufficiently thick, to insure good insulation and abrasion resistance, as well as thermal shock resistance, etc.

Permaluster, Inc., has pioneered in this technical advancement after years of research and has obtained such an inorganic, flexible insulated film that is produced continuously on wire and strip aluminum.

The oxide film is formed by an electo-chemical method which is a conversion process for thickening the naturally occuring film several hundred times or more. This method is known as "anodizing." Permaluster's patented process is similar to anodizing except:

1) It is performed with high speed (justifying cost).

2) It eliminates mechanical contact to avoid racking spots.

3) It is controlled to eliminate crazing when bent.

Owing to the strict control methods employed in the processing, the oxide coating may be formed homogeneously in varying thicknesses and pre-structures. The resistance of the formed alumina film is about 1800 ohms per cm^2.

The mechanism of the anodic film formation and the fine structure of the film are not fully understood, but information is derived from the available evidence that under the influence of the elctrolyte and the mechanical solvent action, aluminum ions migrate from the metal surface through the barrier layer to the oxygen rich upper portion of the film where the ions react with the aluminum oxide to form an anhydrous alumina. The oxide layer formed differs in character from the more porous outer layer. The alumina has an electrostatic charge and can function to absorb other inorganic or organic material.

PROPERTIES OF Al_2O_3

This step in the creation of aluminum oxide insulated film is an advancement in the technology of processing for applications in electo-magnetic coils. Thinner insulation with high dielectric strength, lower dielectric losses, and more compact components are the results. The inorganic insulated film with its advantageous dielectric properties will withstand:

1) Higher temperature (to the melting point of the conductor).
2) Fungus, corona and contaminants
3) Thermal or storage aging
4) Oxidation
5) Radiation
6) Corona
7) Thermal shock
8) High frequencies

9) Cryogenics (liquid gasses)

In addition, it will not outgas in high vacuum.

ELECTRICAL PROPERTIES

1) Breakdown Voltage: The porous film of Al_2O_3 as produced on EC[2] grade and high purity material without impregnation is approximately 30 to 40 volts per micron (0.00004"). The material composition affects the breakdown voltage which increases with the increasing purity of the metal. The film is homogeneous, uniformly thick without cracks, controlled to any thickness. The dielectric strength varies nearly in a linear fashion with the thickness as per Figure 3.

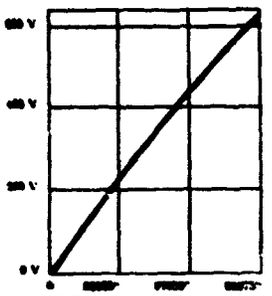


Fig. 1—Thickness of film vs. breakdown voltage (rms). The dielectric strength of the oxide film is approximately 35 to 40 volts rms per micron (0.00004").

2) Resistivity: The resistivity of the aluminum oxide varies with temperature and humidity. When the film is unsealed, it may vary 7×10^7 to 3×10^{12} ohms/cm. Under ideal conditions in a dry atmosphere, resistivity of 5×10^{15} ohms/cm. was obtained at 20° C. after charging for 60–80 seconds.

TABLE IV—Properties of thin film Al_2O_3 insulation.

Specific gravity (20° C)	4 (approx.)
Apparent average density (20° C)	2.5
Melting point	2050° C. (3722° F)
Elongation (%)	10 (maximum)
Coef. of linear thermal expansion	8×10^{-6}
Refractive index	1.59
Reflectivity (%)	70
Emissivity (at 0 a thickness)	≃ 30%
Specific resistivity (ohms cm) (20° C)	*10^{14} (average)
(250° C)	10^{10} (average)
Dielectric strength (volts rms micron)	*35-40
Dielectric constant (20° C) (at 1 Mc./s)	**8.5-9.5
Loss factor (tan delta) (20° C)	**0.0004

NOTES:
*Since aluminum oxide is hygroscopic and shows a considerable water absorption at relative humidities in excess of 90%, these figures relate to values obtained in air with relative humidity between 35% and 85%
**These figures relate to values obtained in dry air

3) Dielectric Constant: The dielectric constant (permittivity) of Al_2O_3 film lies between 8.5 and 9.5 when measured in dry air at one megahertz. Similarly, loss factor (tan delta) is 0.0004 under like conditions.

MECHANICAL PROPERTIES

1) Hardness: The film is ceramic in nature and will resist surface scratches and abrasion. The degree of hardness depends on the porosity and the depth of the oxide layer. Tests made on numerous samples of varying degrees of porosity by means of scratching the surface with a needle having a constant load of 130 grams showed that breakthrough was achieved in the most porous sample after 16 strokes and the least porous sample after 48 strokes.

2) Flexibility: The film is highly flexible, unlike other forms of ceramic insulation, and retains the inherent qualities as long as the metallic base material is not subjected to undue strains. If the base material is over stretched or sharply bent, it exhibits cracking, when separation of the film may occur. A hard temper metal will not allow small diameter bending. In bare state, such wire will over stretch on the upper part of the bend, and the surface will be distorted at the lower bend. Owing to the firm bond between the aluminum substrate and the innermost layer of aluminum oxide, the insulated conductor can be made flexible, provided also that the temper of the conductor is such that it exhibits a good degree of ductility. Ductile wire and strip were wound around a mandrel having diameter four times the thickness of the conductor without flaking or cracking of the insulation.

3) Fatigue: Tests have indicated that there is no fatigue loss due to the anodic film, even with a film thickness more than fifteen microns. This is owing to the flexibility of the film; there is no stress concentration between the metal and the film.

4) Strength: Tensile strength and elongation are not altered by the anodic film. With very thin material, allowance should be made for the thickness of the metal that is converted to oxide. There is no reduction in fatigue strength even at relatively high stresses. The alumina film has significant strength when detached from the metal.

5) Corona: As insulation is exposed to high voltage, the critical voltage is reached when visible or audible discharge occurs. This is the corona start voltage (CSV), and it is here that the ambient air becomes ionized and permits free flow of current. Most insulations exposed to this corona effect suffer erosion. It is also attacked by ozone produced from the oxygen of the atmosphere. Such chemical erosion within the body of the insulation is concentrated and results in a serious degradation of the quality of the insulation and causes premature failure of the system.

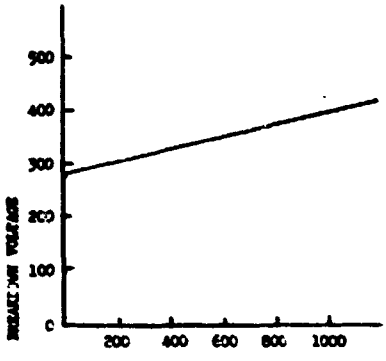
6) High Temperature: Heat is a very important factor in the use of a barrier type electrolyte, as it thickens the barrier layer for higher dielectric strength. Heating changes the electrical resistance and modifies the physical constance of the film; therefore, the pre-anodized aluminum heated up to 1000° F. leads to an increase in resistance and an apparent thickening of the barrier layer. It also influences the flexibility of the film. It will not blister or peel, although the thermal expansion of the film and the conductor is different.

Since the aluminum oxide melts at 3722° F. (2050° C.), the temperature maximum at which Permaluster insulated conductor may be safely employed is dictated by the melting point of the metallic conductor, which for aluminum is 1218° F. (659° C.). The insulation properties of the oxide film improves as the temperature increases as the moisture factor is eliminated. It holds its dielectric properties whether it is operated at 50° C., 500° C., or -400° F. (cryogenic), thus making it suitable for Classes H and C insulation as well as exceeding Mil-Spec. for high temperature application.

It is insensitive to thermal shock. The insulated conductor can safely carry short term overload currents while in a high ambient temperature and can be subjected to sudden changes of temperature having a wide differential without deterioration.

Thermal conductivity of the Al_2O_3 is relatively close to the aluminum conductor as the film is minute. It has the ability to radiate heat rapidly in high temperature. A small coil with less weight and with high thermal conductivity will facilitate the transmission of heat. To achieve

such a performance, the round wire has been replaced with flat wire or aluminum foil where all voids in the windings are filled.



TEMPERATURE IN °F.

Annealed EC aluminum wire, Permaluster anodically processed of aluminum oxide Film thickness 8 microns (.0003")

7) Radiation: Inorganic Al_2O_3 film has in initial conductivity at zero dose rate of 10^{-12} (ohms/cm)$^{-1}$, the conductivity increases at the same magnitude the dose rate increases; thus the dose rate of 10^3 roentgens/sec., the conductivity will have increased to 10^{-9} (ohms/cm)$^{-1}$. When materials are subjected to a short duration extreme intensity gamma pulse as encountered in nuclear explosions (where the intensity may reach to more than 10^7 roentgens/sec. in a fraction of a microsecond) the resistance of most organic insulations diminishes in value, while the inorganics including Al_2O_3 will recover rapidly after 10 to 100 microseconds.

Al_2O_3 is successfully applied in a radiation environment. A typical reaction environment of 8 x 10^{12} NV/cm^2/sec. for neutrons and 6 x 10^{12} 1 mev/cm^2/sec. for gamma radiation, where the equivalent absorbed dose for each is approximately equal to 1 x 10^8 rads, has shown no deleterious effects.

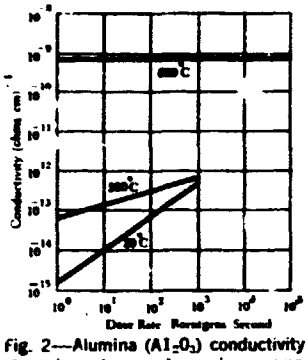


Fig. 2—Alumina (Al_2O_3) conductivity at various temperatures in gamma radiation.

In a report by Idaho Nuclear Radiation and Argonne National Laboratories was described the design of an Annular Linear Induction Pump for the Mark II Loop, placing the most stringent requirements on the sodium pump. The four-pole version of the pump used 24 coils, and the five-pole version used 30 field coils. The field coils were designed to consist of flat ribbon wound pancake type coils of fully anodized EC aluminum. The Al_2O_3 insulated conductor was wound without interleaving and was successfully operated as the primary of a 60 herts, one phase, 230 volts AC stepdown transformer at 425° C. for over 500 hours without malfunction or failure (ANL-7369-Argonne National Laboratory), THE DEVELOPMENT OF PUMPS FOR USE IN FAST-REACTOR-SAFETY INTEGRAL-LOOP EXPERIMENTS by L. E. Robinson and R. D. Carlson.

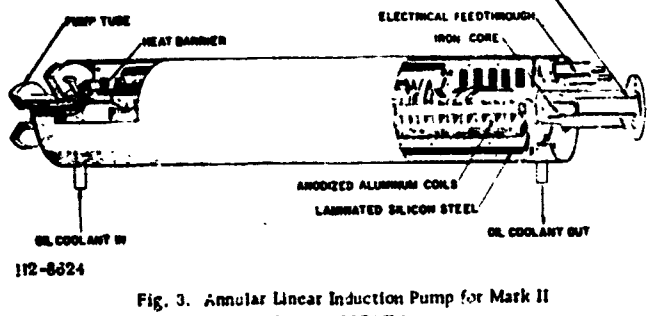
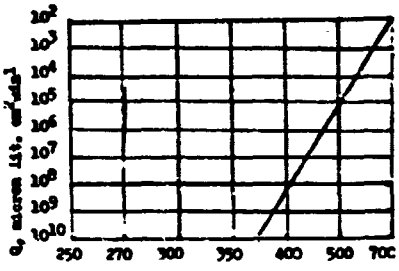


Fig. 3. Annular Linear Induction Pump for Mark II Integral Sodium TREAT Loop

8) Low Temperature: Aluminum with oxide film excels in super cold environments; it is insensitive to abrupt changes at low temperatures, remains tough, ductile and strong. The high thermal conductivity of aluminum (the ability to transfer heat rapidly) makes it especially effective in high energy absorption.



Temperature in degrees Kelvin
Under pressure in liquid hydrogen

At sub-zero temperatures the tear resistance is as high or higher than that at room temperature. Aluminum has been used to stabilize super-conducting magnets and reacts only slightly in increases in magnetic field in resistivity or about 5KG. In a typical room temperature, under zero stress, zero field resistivity of high purity aluminum is at 2.53 + 10^{-5} ohm/cm. Pure aluminum, oxidized with low strain was found to have low resistivity even in a high magnetic field. In cryogenic applications at -450° F. in a magnetic field, such material operated easily at 120,000 gauss. The less strained aluminum retained its properties in high magnetic field. Its magno-resistance exhibited a predominately saturating behavior.

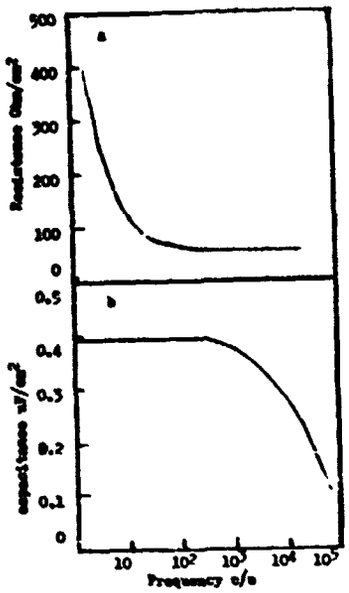
9) Frequency: Specific resistance of anhydrous and partially hydrated alumina is very high. The anodic film is approximately 5MΩ/cm^2 per 1.5 x 10^{-3} cm film. There is no significant change over a wide frequency range. At frequencies above 1KHz/S R, it is nearly constant. At 25Ω/cm^2 changes will appear with varied film thicknesses. At frequencies below 10 KHz/S, capacitance is nearly constant at 0-99u F/cm^2. Figure shows some indication of fair representation of the impedance component of Permaluster tested base Al_2O_3 insulated material at room temperature.

Different values and properties can be obtained if the pores are sealed or impregnated.

The impedance obtained in high frequency gives a more uniform response, as the mass of a moving system limits high frequency response of acoustic transducers.

By reducing the weight of the mass by more than 50%, frequency can be increased. The more dense the material, the faster the sound waves travel. For a given frequency, mass of the magnetic coil exhibits a major portion for the length of the wave to cycle. Lightweight aluminum rectangu-

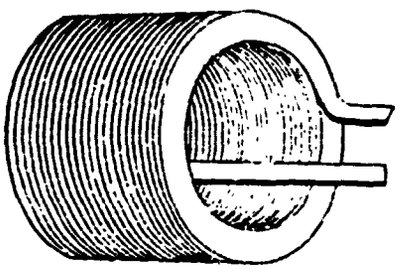
lar wire, edge wound, with thin Al_2O_3 insulation, improved the design objective in obtaining the maximum power output per pound of weight and condensed unit for moving transducer coil and waveguides.



Frequency dependence of balancing series (a) resistance (b) capacitance for annealed aluminum oxide - Film thickness 1.5×10^{-3} cm.

Steady state low frequency voltage would be distributed across a sheet winding in direct proportion to the turn impedance giving an essentially linear distribution of such voltage across the turns.

The capacitance and inductance between adjacent or physically close turns and the capacitance to ground are uniform throughout a continuous sheet coil. Coils wound from Al_2O_3 thin insulated strip have no interlayer capacitance, but only interturn capacitance; total capacitance of the coil is thus reduced.



Waveguide wound, for transmission of signals, using coil made of anodized aluminum rectangular wire, edge wound. Such coils are fast moving, lightweight, suitable for actuators, voice coils, servo systems, shakers, etc.

10) Vibration: An edge wound flat wire coil produced a flux density of 18 kilogauss in an air gap (using 3 lbs. of Alnico 5 - 7 magnetic core) to provide a 6 lb. force for displacement and acceleration as shown in chart. The improved moving voice coil unit has an efficiency of 50% in the frequency range from 400 - 10,000 Hz. in a maximum acoustic output of 20 watts with a high degree of reliability. Of course, higher frequency is no problem. The film is extremely tough and exhibits little deterioration under extensive mechanical vibration for extended periods of time. Coils wound with thin film insulated aluminum conductor have been successfully subjected to vibration tests both at room temperatures and elevated temperatures. Under 24 G vibration, applied at various frequencies between 50 cps and 5000 cps for one hour along each axis, no change in resistivity and only a slight change in inductance was recorded. During the test the current flowing through the coil increases to raise the temperature to its limiting value and then reduces again.

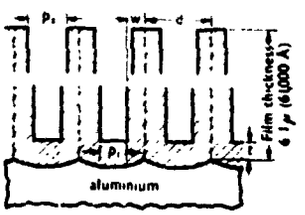
11) High Vacuum: Aluminum oxide insulation may be used effectively in high vacuum. The film showed no effects under pressure below 10^{-12} Torr at 500° C. Other tests indicated that when Al_2O_3 was impregnated with carbon-free silicons, there was no evidence of any hydrocarbon residue when operated above 400° C. in extremely low pressure.

12) Design Consideration: Aluminum also has a high heat capacity with high capacitance for even voltage distribution. Aluminum strip or rectangular wire winding permits higher current density, due to each turn having lateral radiating edges exposed to the cooling medium, thus providing effective heat dissipation. This permits considerable design latitude in either reducing the cross section of the aluminum used or increasing the current rating for equivalent heat rise. Layer-to-layer temperatures are nearly uniform; hot spots inherent in conventional windings are virtually eliminated. The use of a thin high temperature dielectric film on flat material will require 1) less voltage, 2) minimal amount of insulation, 3) minimal amount of thermal insulation. It renders greater volume in equal space and affords greater mechanical strength.

Consideration is given to life expectancy, reliability and normal stresses in performance. It is important to choose a dielectric with thermal stability when the rate of heat generation at some point will exceed the ability of the material to dissipate it. Heat is generated by conduction current flow, principally ionic or by hysteresis under alternating stress. The heat generation rate is an increasing function of temperature in the electric field. An insulation with thermal stability should not be the limiting factor as it is the most important part of the component.

13) The Oxide Film Structure: The Al_2O_3 insulated film can be varied in processing to meet different requirements. Permaluster produces such film that is flexible to allow winding in any form, including miniature coils and edge winding of rectangular wire under great stress. A film thickness sufficiently thick to insure good insulation and abrasion resistance can be produced.

Owing to the porosity of the oxide surface, the film exhibits hydroscopic properties, and its resistivity changes with relative humidity as well as with temperatures ranging from 10^8 Ohm/cm to 10^{12} Ohm/cm. If relative humidity is a factor, additional inorganics or organics can be impregnated into the pores of the film.



Structure of pores on anodic porous fig. type film. Pore varies with operating conditions.

14) Impregnated Films: Inorganic coatings have the advantage of resistance to environmental conditions, with no degradation by exposure to radiation. Al_2O_3 produced anodically is an intergral part of the conductor. The inner layer of the oxide film is relatively compact and anhydrous, and on the surface is highly absorbent and ready to absorb either dissolved substances or molecules in state of colloidal dispersion. It is axiomatic that absorbing is a function of the porosity of the outer layer of the film. It is probable the oxy-type anions are a part of the pores that are capable of hydrogen bonding.

The conductivity of the outer layer provides the means of transporting anions hydroxyl ions from solvents or water toward the condensed layer, and hydrogen ions are easily bonded or fused with other substances. The transistion frequency of protons in a hydrogen bond has been found to be on of the order of infrared frequencies (10^{13} to 10^{14} per second). On this basis, the proton mobility in hydrogen bonded structures differs from the electron mobility in metal itself by only 1 or 2 orders in magnitude. The pore diameter of the surface of the film is in the order of 10.50 millimeter microns, or their density is between 100 to 800 pores per square micron, sufficient to absorb other materials. In some areas of applications, porous surface could have value, since it is chemically active surface. It acts as a good agent for mechanical bonding; other advantages include its retention of photo-litho emulsions, and it serves as a base for electroplating, printed circuitry and painting.

Pores can be impregnated with various materials, i.e., organics to inhibit water absorption, organo-ceramics for use in high temperatures. The Georgia Institute of Technology (WADC Tech. Report 58-13) sealed the film with Colloidal Silica in an electrophoresis deposition, also with a true liquid of ceramics that wet the inside pores by gelling a hydrolized solution of ethyl silicate so the particles of silica were trapped in the pores of the coating.

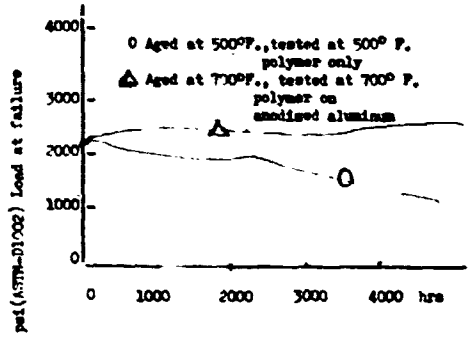
Actually, the barrier layer of the oxide is sufficiently protective for organo-ceramic filling of the pores. There is no danger that a carbon conductive path will pass the barrier layer in high temperature operation. In fact, even the organic material will operate at twice the temperature without effect.

15) Impregnation With Inorganic Material: The anodic porous base coating with a barrier layer is a refractory, flexible film and can absorb or seal other organic and inorganic film with or without an organic vehicle. Another anodic or eletrophoretic process can be applied for forming another composite film that is absorbed into the pores of the anodic base insulated layer. Barrier type electrolytes can be used. Tests performed showed that higher dielectric strength and flexibility were obtained after vacuum annealing at 450° to 500° C.

Oxide pores can be "sealed" with Tetraethyl orthosilicate, which is a refractory binder, a gelling agent for impregnation of porous material and is highly heat resistant. A hydrolized silicate gel heated to silica becomes a hard, vitreous type material; a pure silica bonding agent which has the advantage of being insoluble in water. It is impervious to most acid and is excellent in high temperatures. Hydrolization, using ethyl silicate solution, can be accomplished, as it penetrates completely into the porous Al_2O_3 to a complete hardness after heating.

A water solution of porcelain enamel or combinations of inorganic frits with or without resin combination, can be applied to create a strong bond with the oxide base. A strong intermolecular bond is responsible for the inertness of the base coating.

16) Organic Impregnation: A silicon-oxygen network interspersed with organic groups can be stabilized to a valuable film in conjunction with aluminum oxide. The solvent of the silicon mixture will oxidize and vaporize with other organic components, while the inorganic silica matrix remains (crosslined organopolysiloxans) are almost unsurpassed for heat resistance. With aluminum oxide, the structure can withstand over 1400° F. without deterioration. A number of modified silicon resins have been used, such as silicon alkyds, or modifications with acrylics, epoxies or phenolics with a silicon content of about 25%. Such different varieties of resin combinations can be formulated either by blending or co-polymerization to obtain heat resistance up to 1000° F. Such combinations are excellent in thermal shock resistance. Resin can be applied in pure form or can be combined with other resinous material. A mixture of resins put together to develop suitable properties that are compatible with the base Al_2O_3 can be achieved.



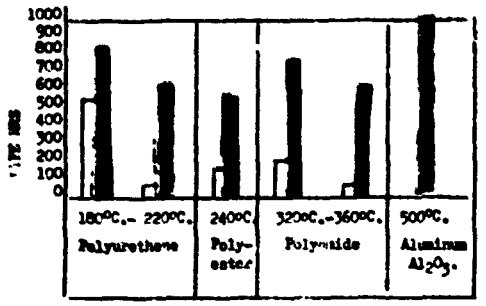
Heat aging of poly-(amide-imide) adhesive on aluminum and anodized aluminum.

The choice of resin to be impregnated into the pores depends upon the application. The choice of an organic binder is made where little or no carbon residue remain, though it will have no effect on the insulation, as the pores are protected by the refractory oxide film that has a melting point three times that of aluminum.

High temperature polymers offer versatility for use in electronic insulation and show stability in performance when impregnated into the Al_2O_3 "prime coat"; Greater dependability has been achieved at high operating temperatures (about 850° F.).

Thermal aging of insulation in organic material is probably responsible for most failures found in the component. Thermal aging itself does not produce failures, but it renders insulation vulnerable to other factors, such as moisture, penetration, brittleness, loss of thermal expansion before complete failure. Figure shows some experiments with organic film over Al_2O_3.

Such organic overcoat is produced in a cured or quasi-cured state. A coil can be formed and wound in any shape when a quasi-cured state is required. When heated, the turns bond together to form a solid structure. By employing this method, cores are eliminated; The coil becomes very strong and self-supporting.



Thermal aging of EC aluminum wire, anodically insulated films. Dark bars indicate aluminum and oxide wire.

CONCLUSION

Most insulations are based on a thermal theory. Should a weak area in the organic insulation be heated more than other areas, and if the heat is not removed as rapidly as it is generated, the weak spot grows hotter and the resistance will be lower. As the temperature continues to rise in operation, instability occurs; this will be followed by a breakdown in the weakest point of the insulation. This will not occur in Al_2O_3 insulation. In fact, the aluminum oxide insulation improves at temperatures above 220° F. The choice of insulation is often a decided factor that will govern the performance and reliability of the components. In applications where peak load is energized during low demand period, overall losses are always less in high temperature design. Examples are transformers, generators, solenoids, alternators, magnets, etc., whether for environmental or terrestrial operation.

It will make good sense to construct electronic components by using lightweight conductors to improve operation: better balance and higher efficiency operation through the reduction of mass. It will make good sense to use aluminum oxide thin film insulation for better dissipation of heat, higher current flow, and consequently higher temperature operation in adverse environments.

SESSION VI

SPECIAL KEYNOTE ADDRESS

A CONFERENCE PERSPECTIVE

Technology Transfer and Commercialization of High Temperature Electronics

Dr. Robert Fry
Gould, Inc.
Rolling Meadows, Illinois

Dr. Robert Fry, Executive Vice President for R and D, Gould, Inc., has been invited to the conference to listen to the proceedings, have discussions with the authors and attendees and from this background provide insights on the status of effort, interfaces between, and perception of the research, manufacturing and user communities in high temperature electronics. The progress of R and D, fabrication technology and commercialization of useful measurement systems at temperatures greater than 200°C will be assessed. The gaps between user needs, R and D results and on-going projects will be summarized yielding market expectations as projected from user applications and manufacturer viewpoints. The apparent determinants for commercialization of current research projects and the perceived interface barriers to technology transfer will be detailed.