ASSESSMENT OF HIGH TEMPERATURE METALLIZATIONS FOR I^2L AND CMOS TECHNOLOGIES

A. Christou and B. R. Wilkins
Naval Research Laboratory
Washington, D. C. 20375

Introduction

As part of the Navy's high temperature electronics program, high temperature barrier metallizations were assessed and tested for I^2L and CMOS applications. Life tests were accelerated to 375°C in view of the -55°C to +300°C temperature range established for engine-located electronics without fuel cooling.

The gold-refractory metallizations evaluated were Au-TiW-PtSi, Au-TiW/TiO_2/TiW-PtSi and Au-TiW(N)-PtSi. These metallization systems were thermally annealed to at least 375°C for up to 250 hours. The critical requirement for stable diffusion barrier is the TiW grain size. Small grain (250Å-500Å) films were observed to be stable up to 375°C. Deposition to TiW diffusion barrier in the presence of oxygen and nitrogen also results in an effective diffusion barrier. Life tests at 340°C up to 100 hours have been completed.

AES profiles of the PtSi indicates some penetration by the TiW. In the case of PtSi/TiW interface, the redistribution of oxygen further passivates the system by forming a TiO_2 layer at the interface. Characterization of I^2L devices subjected to 340°C anneals will also be presented.

High Temperature Metallizations

The Au-TiW System

Previous investigations[1-3] on the interdiffusion and reliability of Au-refractory films used in devices have neglected "substrate" effects. It is recognized that the substrate can be a very active member of diffusion couples which may in many cases accelerate degradation observed in the gold conductor and refractory barrier.

In assessing the high temperature reliability of Au-Ti(W) films for high temperature applications, we compare the role that 3 different intervening layers on silicon substrates play in the stability of these metallizations. These layers are PtSi, SiO_2 and Si_3N_4. Each of the layers have, on occasion, been incorporated in MPTS. The Si_3N_4 is used for passivation and the PtSi layer is used as the ohmic contact.

Table I summarizes the deposition conditions, giving film thickness, sputter target, substrate temperature and film characteristics.

TABLE I

Deposition Conditions for Small Grain Size TiW Diffusion Barriers

Film Thickness	1200Å - 1800Å
RF Sputtered	$Ti_{0.3}W_{0.7}$ Target
Substrate Temperature	120°C
Resistivity of TiW	77 μ Ω-cm
Grain Size	250 - 750Å

The differences in the Ti(W) reaction with Si, SiO_2 and PtSi are shown in Figur 1. At 375°C there is no enhancement of the diffusion between Si and Ti(W). This

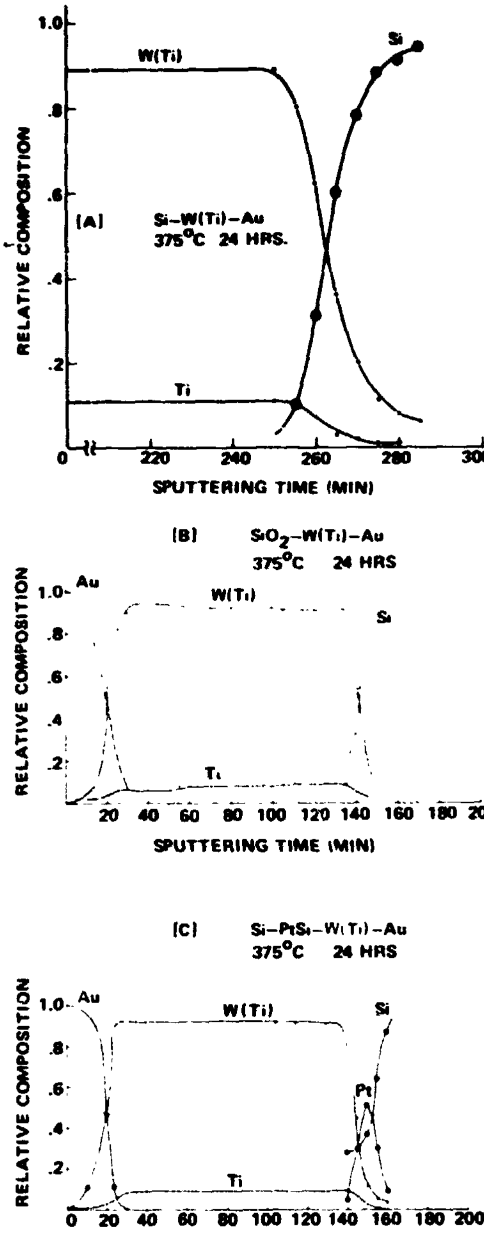

Figure 1. Diffusion profilesof the TiW diffusion barrier. (A) Silicon substrate, (B) SiO_2/Si substrate, (C) PtSi/Si

is as expected from the diffusivities of these systems which is of the order of 10^{-20} cm/sec. Likewise, the interdiffusion effects are minimal between SiO_2 and Ti(W) at this temperature. However, when the layer is PtSi, it acts as a source and sink for Silicon atoms resulting in the outdiffusion of Si into the refractory film. The amount of Si detected in the Ti(W) film is not satisfactorily explained from a solid solubility argument. These results agree with our previous work with Ta on Si and PtSi and with Sinha's work with WSi_2 formation on PtSi-Si substrates. The excess silicon in the TiW will result in a refractory silicide formation at higher temperatures. Our conclusion, to date, is that the Au-TiW system with small grain TiW is stable up to 375°C.

The Oxide/Nitride Assisted Diffusion Barriers

The deposition of TiW in the presence of oxygen overpressure or nitrogen has been determined to improve the overall thermal stability of the TiW diffusion barrier. An overpressure of 10^{-3} Torr of oxygen or nitrogen was used in each case resulting in Titanium nitride passivation of the TiW grain boundaries.[4,5] Since the primary diffusion mechanism at temperatures below 500°C is grain boundary diffusion, the formation of TiN at the TiW grain boundaries inhibits significant grain boundaries up to 450°C. The Au-TiW(TiN)-PtSi system was found to be stable up to 450°C as shown in Table II, where the at. % Si and Au detected in the bulk of the TiW by energy dispersive x-ray analysis i summarized.

TABLE II

Evaluation of the TiW(TiN) Diffusion Barrier up to 450°C

Anneal Temperature (100 hrs)	at. % Si (Detected in TiW(TiN))	at. % Au (Detected in TiW(TiN))
300°C	ND	ND
340°C	1.1	1.0
350°C	1.8	2.0
400°C	2.5	3.0
450°C	4.2	6.5

However, at 450°C, the significant observation is that Silicon was not observed in the Au overlayer thus showing the overall stability of TiW(TiN) as a diffusion barrier.

I^2L Test Elements With Au-TiW Metallizations

As part of the Navy's High Temperature Electronics a custom I^2L metallization test mask set has been processed using the Au-TiW-PtSi system. The test mask includes a number of different test elements which are aimed at determining design constraints on ohmic contacts, metal width and spacing. Also included are symmetrical cell I^2L logic gates and ring oscillators. The initial test results look promising in that 2 of 6 (8%) of the oscillators failed within 275 hours. A total of six oscillators have now reached 580 hours with no failures. These tests are continuing and additional refinements to the metallization will be incorporated in the I^2L devices to be processed in the future.

References

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