-55 TO +200°C 12 BIT ANALOG-TO-DIGITAL CONVERTER

Lewis R. Smith and Paul R. Prazak
Burr-Brown Research Corporation
Tucson, Arizona

The 12 bit successive approximation A/D converter offers moderately high speed precision data conversion at a reasonable level of cost and complexity. The ADC10HT[1] extends this capability over a temperature range of -55 to +200°C. No missing-code performance is maintained over the entire temperature range. The converter is completely self-contained with internal clock and +10 volt reference. Figure 1 shows a block diagram of the ADC10HT.

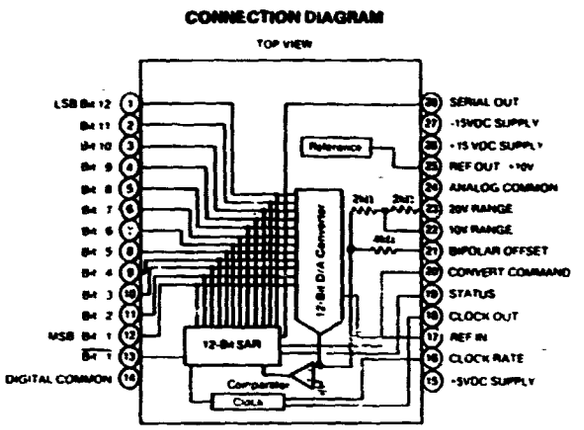

Figure 1

The internal 12 bit D/A converter is a monolithic dielectrically isolated chip.[2] The successive approximation register (SAR) is a commercially available CMOS chip. The clock and the comparator were designed with a single LM119 dual comparator made with conventional junction isolated bipolar technology. The clock also contains an MOS capacitor chip and a nichrome thin film resistor network chip. These five chips make up the basic A/D converter. The reference circuit consists of a dielectrically isolated op amp chip, zener diode and nichrome thin film resistor network.[3] The ADC10HT can be used with an external +10V reference, if desired.

The SAR could have been either bipolar TTL or CMOS since both technologies exhibit altered but useful characteristics at temperatures well above 200°C. However, CMOS devices offer low power dissipation, so that the internal temperature of the hybrid circuit does not rise as much from self-heating. Also, CMOS SAR's have better noise margins than TTL devices at high temperatures.

A major problem at high temperature is that caused by pn junction leakage currents. The largest of these currents is the epi to substrate current in junction isolated circuits due to the very large size of the isolation pn junction relative to the device junctions. In CMOS circuits, these leakages are returned to the supplies, and therefore, do not degrade performance. Therefore, the logic keeps working at temperatures up to 250°C. Above that temperature, a four layer latch mechanism, inherent to junction isolated CMOS, limits the devices performance.

Since the internal D/A converter is dielectrically isolated, there is no epi to substrate leakage component. By eliminating this error mechanism, the useful temperature range of the device is increased. Dielectric isolation is also used in the reference circuit operational amplifier for similar reasons.

Although the dual comparator is junction isolated, the epi to substrate leakage currents are second stage effects and[4] furthermore, tend to cancel out. Another potential difficulty in bipolar circuits is the poor performance of lateral pnp transistors at high temperature. This particular comparator does not contain any lateral transistors. Instead, resistors are used for level shifting purposes.

The nichrome thin film resistor networks are stabilized at over 500°C and, therefore, are stable[5] at temperatures well above 200°C. The current densities have been reduced by a factor of three from those densities used in normal commercial practice to prevent electromigration at high temperature.[6]

The absolute value of resistors in the converter is not critical, but resistor tracking with time and temperature is very important. For this reason, critical resistors of different values are comprised of equal resistance elements. Thus, even though the resistors may shift due to the extreme ambient conditions, the linearity, gain and offset of the A/D converter itself should remain stable

The converter is packaged in a conventional 28 pin side-brazed ceramic package. Figure 2 shows the placement of the various chips in this package. The eight chips are eutectically attached to the substrate and ultrasonic wire-bonded to a double layer thick film substrate. The substrate is then attached to the header using a high temperature gold tin preform.

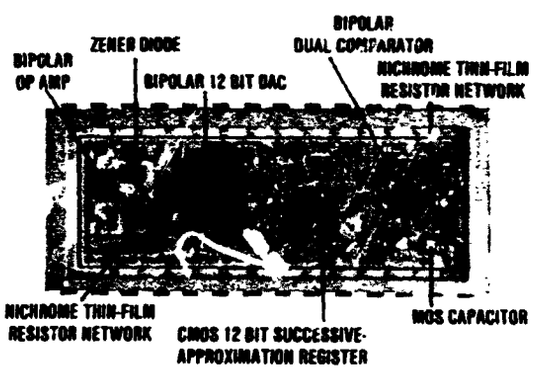

Figure 2

A platinum/palladium doped thick film gold system is used to minimize purple plague. Average wirebond pull strengths of three grams after 1000 hours at 250°C have been obtained. A 1000 hour test at 250°C exhibited only an 80%

increase in bond resistances.

Connection between the double layer substrate and the ceramic side-brazed package is made with gold wire. The converter is hermetically sealed using a gold germanium preform to attach the ceramic cap.

To ensure the reliability of the converter, all parts are burned-in at 200°C and all parts are 100% screened. Due to the limited life of the connectors, the temperature testing and burn-in fixtures use printed circuit boards that pass through the oven doors, thus allowing board connection to be made at room temperature. The test sockets themselves are zero insertion force types made of Torlon with berrylium/nickel contacts. The boards are made of Norplex copper clad polyimide with nickel plating. A high-temperature solder with a 300°C melting point is used for the test boards.

Table I shows the important electrical specifications for the ADC10HT. Figure 3 shows linearity error vs. conversion speed and indicates that 12 bit accuracy can be attained at 25μs. The clock frequency can be adjusted externally.

TABLE I

Typical Performance

Resolution	12 bits
Accuracy at 25°C	
Gain error: ±0.05% (adjustable to zero)	
Offset error: ±0.05% (adjustable to zero)	
Linearity error: ±0.005%	
Drift ($-55^{\circ}C \leq T_A \leq +200^{\circ}C$)	
Gain: ±15 ppm/°C	
Offset (unipolar): ±1 ppm/°C	
Linearity: ±0.5 ppm/°C	

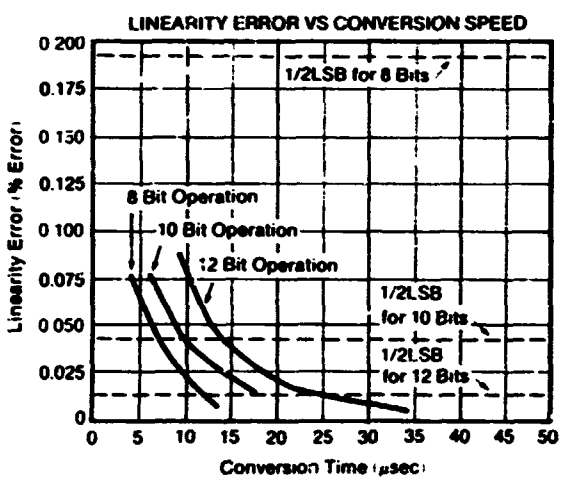

Figure 3

Shift in bipolar offset and gain vs. time during operation at 200°C are shown for three devices in Figures 4 and 5. Both parameters can be adjusted to zero initially by the use of external trim resistors. Offset in the unipolar mode is much less than the bipolar shift shown in Figure 4. Differential nonlinearity shifts with time during operation at 200°C

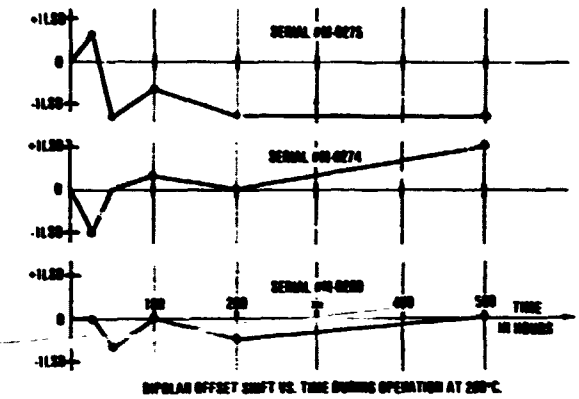

Figure 4

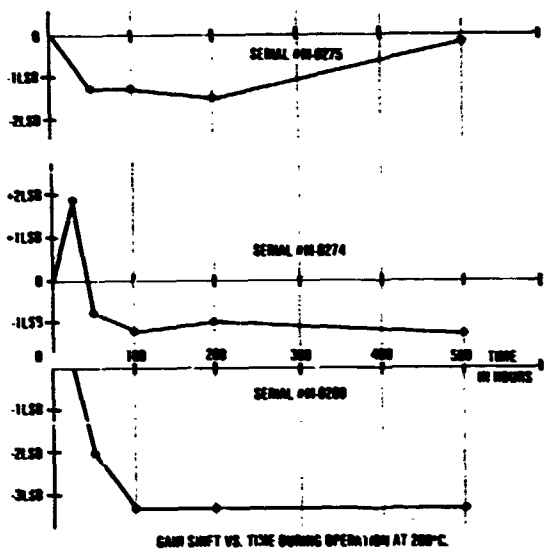

Figure 5

are shown in Figure 6. Differential nonlinearity is defined as the deviation from the ideal one LSB step size. Overall nonlinearity is not shown but has similar shift vs. time character-

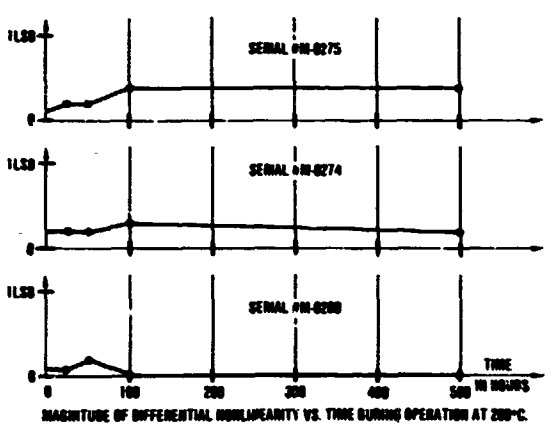

Figure 6

istics to that of differential nonlinearity. Figure 7 shows differential nonlinearity vs. temperature. All parts are tested for no missing codes over the temperature range.

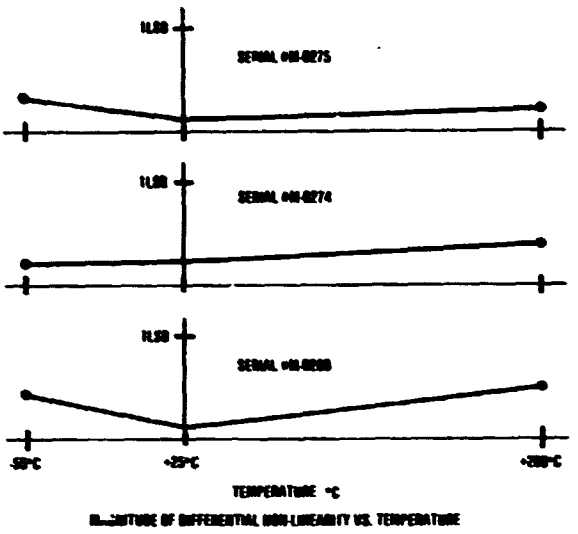

Figure 7

Future Direction

Although the present design was not intended for use above 200°C, it is believed that a successive approximation analog-to-digital converter could be built for 300°C operation with 8 bit performance. Lower power circuitry will reduce peak junction temperatures. The present circuit dissipates most of its power in the digital-to-analog converter chip and in the reference. Both circuits could be redesigned to operate at lower supply voltage and hence lower power.

Although the zener diode used in the reference exhibits a nonlinear temperature coefficient above +125°C, acceptable performance was obtained to +200°C. At much higher temperatures, a nonlinear zener temperature coefficient compensation method is likely to be required.

Very careful attention must be paid to matching of the internal D to A converter's collector-base leakage currents if nonlinear transfer characteristics are to be avoided at high temperatures. Although leakage currents can still cause gain and offset errors, these can be removed using digital techniques.[7]

The CMOS high temperature latch condition can be eliminated by using dielectric isolation. I^2L logic circuitry also has potential for use in the SAR.

Finally, a high temperature metal system such as the P_t, T_i Au metallization reported on by Peck and Zierdt [8] is required if reasonable MTBF is to be obtained at 300°C.

REFERENCES

1. Paul R. Prazak, "Hybrid data converters like it hot (200°C) and cold (-55°C)", Electronic Design, November 8, 1980.

2. Robert W. Webb, ISSCC Digest of Technical Papers, 1978, p. 142.

3. Jerald G. Graeme, Operational Amplifiers, Design & Applications, McGraw-Hill, 1971, pp. 230, 231.

4. S. J. Gillespie, "Stability of Lateral pnp Transistors during Accelerated Aging", IBM, J. Res. Develop., Vol. 23, No. 6, Nov. 1979.

5. J. L. Prince, E. A. Rapp, J. W. Kronberg, and L. T. Fitch, "High Temperature Characteristics of Commercial Integrated Circuits", High Temperature Electronics and Instrumentation Seminar Proceedings, Dec. 3-4, 1979, Sandia Laboratories.

6. J. R. Black, "Electromigration, a Brief Survey and Some Recent Results", IEEE Transactions, E.D., Vol. ED-16 #4, Apr. 1969, pp. 338-347.

7. Paul Prazak and Andrij Mrozowski, "Correcting errors digitally in data acquisition and control", Electronics, Nov. 22, 1979.

8. D. S. Peck and H. Zierdt, "The Reliability of Semiconductor Devices in the Bell System", Proceedings of the IEEE, Vol. 62, No. 2, Feb. 74, pp. 185-211.