PROCESS CHARACTERISTICS AND DESIGN METHODS FOR A 300° QUAD OP AMP

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SUMMARY

There is a growing need for electronics which operate over the 125°C to 300°C temperature range in such applications as well logging, jet engine control and industrial process control. This paper presents the results of an IC process characterization, circuit design and reliability studies whose objective is the development of a quad op amp intended for use up to 300°C to serve those requirements.

PROCESS CHARACTERIZATION

A dielectrically isolated complementary vertical bipolar process was chosen to fabricate the op amp. DI eliminates isolation leakage and the possibility of latch up, two of the major high temperature sources of circuit failure which are present in junction isolated processes. The complementary vertical PNP offers superior AC and DC characteristics compared to a lateral PNP allowing simpler stabilization methods. The junctions are relatively deep (> 3u) to minimize sensitivity to interconnect pitting. Device cross sections are shown in Figure 1.

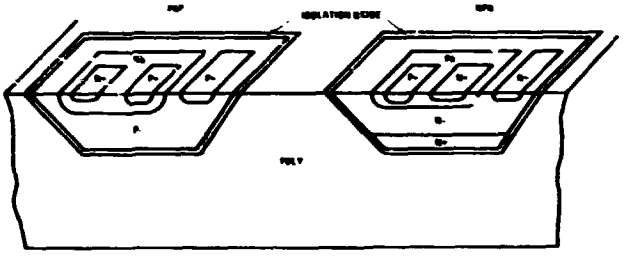

Figure 1. Device Cross Sections

Characterization of the NPN and PNP show them to be quite suitable for use up to 300°C, however certain parameters change drastically over the temperature range and require special consideration in a high temperature design. Leakage currents increase to micro amps as shown in Figure 2. An important point illustrated in the figure is the fact that I_{CES} is several times larger than I_{CBO}. Significant, but not shown on the figure, is the fact that the leakage currents for matched devices on the same chip typically match to 10%. These characteristics are exploited in the circuit design.

The effect of leakage current on NPN common emitter characteristics can be seen in the 300°C photo of Figure 3. The base current has been offset by 4.5 ua to compensate for I_{CBO} bringing the first trace to the origin. This illustrates the base current reversal which occurs before 300°C. One can also observe the monotonic increase in h_{fe} with temperature in the photos.

V_{BE} decreases with the well known -2mV/°C slope to about 100mv as shown in Figure 4.

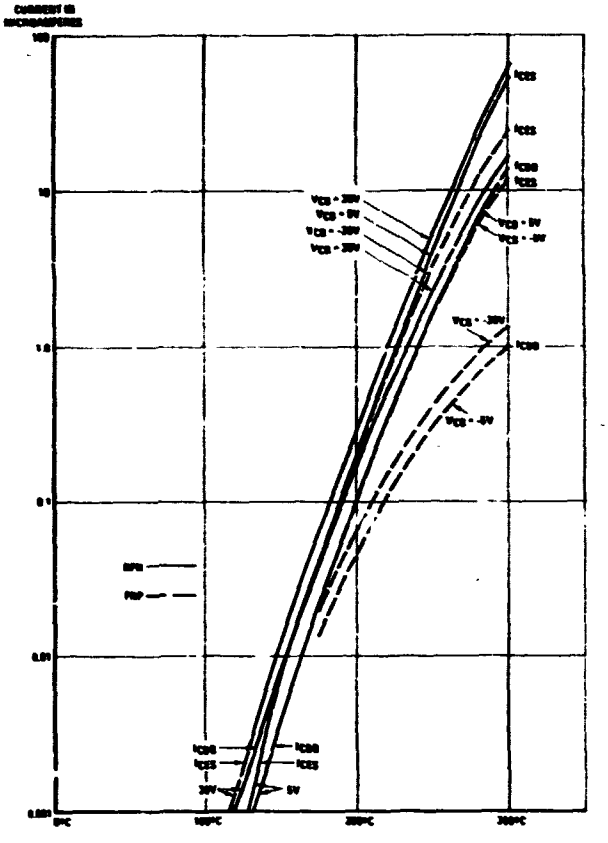

Figure 2. Leakage Current vs. Temperature

RELIABILITY

Reliability is a particularly important consideration in high temperature circuit design because most failure mechanisms have exponential temperature dependence. Perhaps the greatest concern is that of interconnect reliability. Calculations using Black's expression[1] for electromigration in Al interconnect predict MTF of greater than 4 years for the maximum current density to be used in the op amp. This far exceeds the goal of 100 hours operating life. 325°C life tests have been conducted on Al interconnect test structures at $J = 3.3 \times 10^4$ A/cm^2, on small geometry transistors at 1 ma and V_{CE} = 30V and on minimum area contacts to P+ and N+ silicon at 4 ma all fabricated with the proposed process for more than 500 hours each. No failures have been observed.

Another potential source of failure, parasitic MOS formation, is eliminated by isolation of each device in its own dielectrically isolated island. This eliminates the isolation diffusion which can act as drain for a parasitic PMOS in JI circuits.

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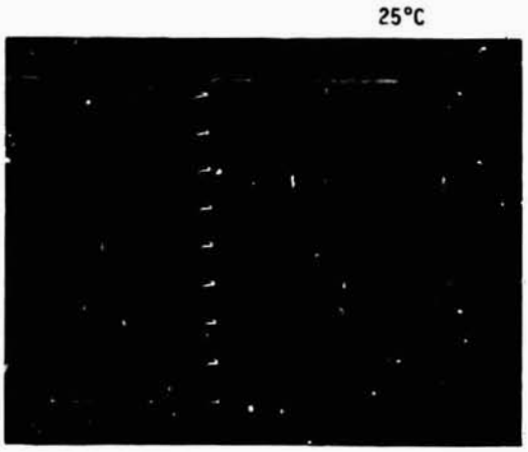

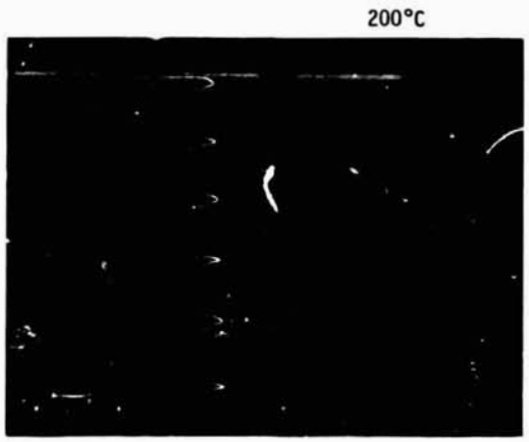

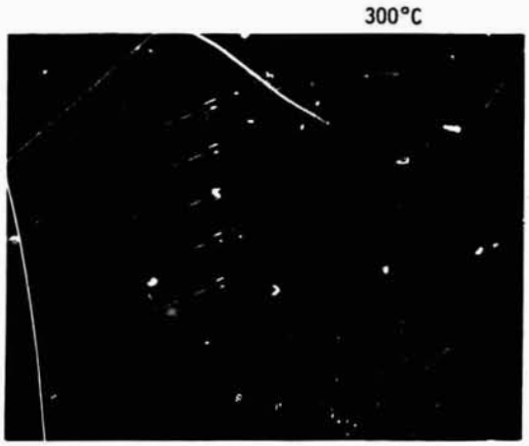

Figure 3. NPN Common Emitter Characteristics at Three Temperatures

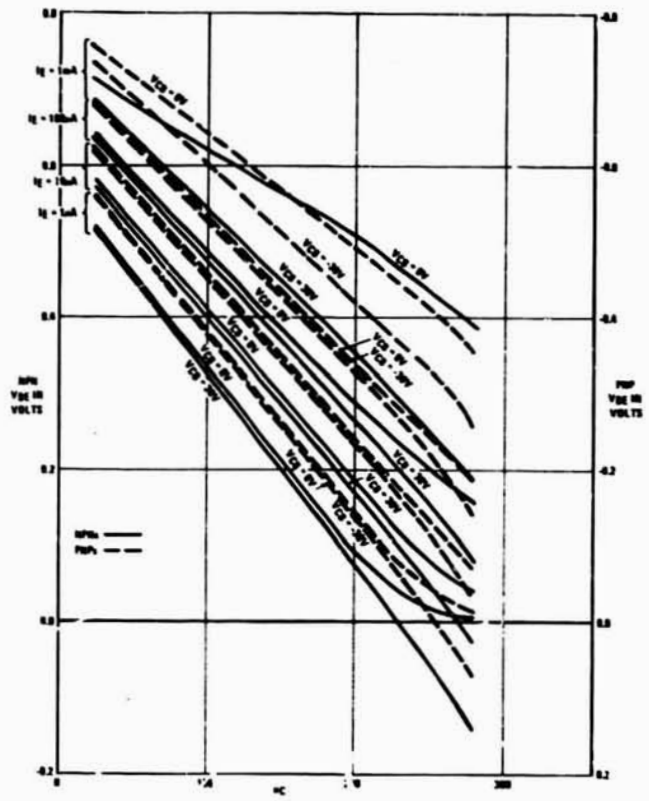

Figure 4. Temperature Dependence of V_{BE}

SPECIFICATIONS

An initial set of target specifications was arrived at. They were based on preliminary high temperature device measurements and extrapolations from available data. The target specifications are given in Table 1.

CIRCUIT DESIGN

Conceptually, certain things had to be done differently from a similar design for the commercial or military temperature ranges. Leakage currents put practical limitations on minimum operating bias current levels. Diode connected transistors are unworkable because of low forward biased junction voltages. Base current reverses because of increasing collector to base leakages and increasing beta. This last consideration means that the base voltage node for strings of current sources must have current sinking as well as sourcing capability at high temperatures. Diffused resistors are almost twice their room temperature values at 300°C. While this must be borne in mind, this high positive temperature coefficient can be used to offset changes in the forward biased junction voltages.

The primary bias circuit consists of a buried zener, Z2, in Figure 5, biased by a pair of 12K resistors, R1, and R16, going to the positive and negative power supplies, which develops a current through the 9K resistor, R11, and diodes, D5 and D6, through the four Q11's and the four Q20's (whose bases and emitters are parallel but whose collectors go to separate amplifiers). A buried zener was chosen because it is quieter than a surface zener. The temperature coefficients of the zener, the transistor base-emitters,

and the diodes approximately cancel the temperature coefficient of the resistor, R11, keeping the current delivered to the positive and negative current source base nodes approximately constant over the temperature range.

The input stage of the amplifier consists of the differential PNP pair, Q21 and Q22, along with Q16, Q17 and R13 (which make up a leakage current compensation network) and the current source consisting of Q5 and R4. PNP devices were chosen for the input pair because their collector to base leakage is significantly lower than that of the NPN devices. R13 provides most of the collector base voltage for Q16 and Q17 whose ICBO's cancel those of Q21 and Q22 to within the limits of their match. The collectors of Q21 and Q22 go to the following stage which consists of Q26 and Q27.

NPN transistors Q26 and Q27 along with R18 and R19 constitute grounded base stages. They translate the signal toward the positive side of the circuit. The stage consisting of Q27 and R19 shields the input device, Q22, from the large voltage excursions of the high impedance node to which its collector is common. The collector of Q26 drives the current mirror stage.

The current mirror consists of Q2, Q3, Q7, Q8, Q12, Q13, D1, D2, D3, D4, Z1 and R3. The primary part of the mirror consists of Q7, Q8 and Q13. Q12 is added to make the collector to base voltage of Q7 equal to that of Q8. This removes a small offset problem due to h_{rb} effects but (more importantly in this case)

TABLE 1

TARGET SPECIFICATIONS AND BREADBOARD RESULTS

Parameter	Temperature	Limit	BB	Units
Offset Voltage	25°C	3.0 <	0.2	mV
	300°C	6.0 <	-5.3	mV
Avg. Offset Voltage Drift	25°C to 300°C	10 <	20	uV/°C
Input Bias Current	300°C	5 <	2.1	uA
Input Offset Current	300°C	1.3 <	3.4	uA
Common Mode Input Range	25°C to 300°C	> ±10	±13.9	V
Differential Input Signal	25°C to 300°C	7 <		V
Common Mode Rejection Ratio	300°C	> 60	71.7	dB
Voltage Gain	300°C	> 70	71.9	dB
Channel Separation	300°C	> 80		dB
Gain Bandwidth	300°C	> 3		MHz
Output Voltage Swing	25°C to 300°C	> ±10	13.7	V
Slew Rate	300°C	> ±2		V/usec
Output Current	300°C	5 <		mA
Power Supply Rejection Ratio	300°C	> 60	71.7	dB
Noise	25°C	8 <		$nv/\sqrt{Hz}$

equalizes the collector base leakages of Q7 and Q8. Ordinarily, Q8 and Q12 would be connected as transdiodes but, because the forward biased junction voltages are so low at high temperatures, D2 and D3 are used to tie the base to the collector of Q8 and Z1 is used to tie the base to the collector of Q12. At low temperatures D2 and D3 are forward biased by the base drive requirements of Q7 and Q8 as Z1 is reverse biased by the base drive requirements of Q12 and Q13. At high temperatures Q2 and Q3 supply ICES to forward bias D2 and D3 and reverse bias Z1 as well as supply the reversed base current of Q7 and Q8 and of Q12 and Q13. D1 and D4 provide a voltage drop equal to D2 and D3 to make the voltage across Q2 more nearly the same as that across Q3. R3 provides most of the voltage for Q3 (and, therefore, Q2). The collector of Q13 is common with the high impedance node.

The next stage consists of a complementary pair of emitter followers, Q15 and Q18, biased by current sources consisting of Q6 and R5 and of Q28 and R20 respectively. There is also a leakage current compensation network associated with each follower consisting of Q9 and R7 for Q15 and Q24 and R14 for Q18. The bases of Q15 and Q18 are common to the high impedance node. Difference in ICBO between Q15 and Q18 at high temperature would be reflected to the amplifier input as an offset.

No special design considerations because of high temperature were necessary in the output stage design which consists of Q14 and Q19 driven by Q15 and Q18 respectively.

The positive and negative current source base nodes remain to be discussed. The positive node is set up by Q4 and R2. Emitter follower Q10 supplies the base drive requirements of Q4, Q5 and Q6 until the base currents reverse at high temperature. Then they are supplied by Q1's ICES whose excess is then supplied by the emitter follower. This excess flowing through R6 and Q10 provides some collector to base voltage for Q4. ICES seems to be a minimum of three times ICBO at 300°C so Q1 is made a double sized device because three sources of ICBO (one of them, Q5, is double sized) have to be supplied by it along with excess for the emitter follower. The same considerations apply to the negative node which is set up by Q25 and R17. Q23 serves as the emitter follower, Q29 the source of ICES and Q25, Q26, Q27 and Q28 receive their base drive from the node.

BREADBOARD

In order to test the validity of the design it was breadboarded using four subcircuit chips made from an existing circuit by custom interconnect patterns. A schematic of the breadboard is shown in Figure 6. The package pins are designated as follows. The first number designates the type of package then there is a dash and the second number designates the pin on that package type. Package type 1 contained the primary bias circuitry. Package type 2 contained the negative bias circuitry. Package type 3 contained the input stage and positive bias circuitry. Package type 4 contained the current mirror and output circuitry.

Several breadboards made up of packaged subcircuits were socket mounted inside an oven door, externally connected as in Figure 6 and tested over temperature. Results are shown in Table 1.

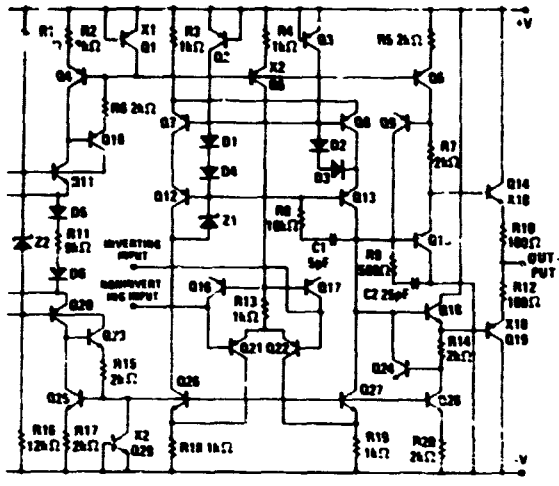

Figure 5. Circuit Schematic

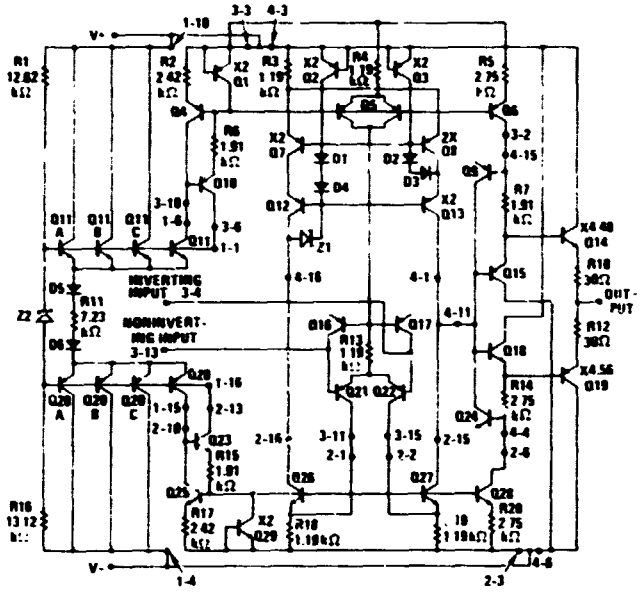

Figure 6. Breadboard Schematic

COMPUTER SIMULATIONS

The computer simulations were done using a Harris version of SPICE called SLICE. Problems arose with the models at 300°C.

Saturation current for the reverse biased diode is modeled as having a linear voltage dependence matching the true value at $V_F = 0$ to solve an underflow problem in the computer. At 300°C I_S is so high that this approximation has the effect of placing a shunt resistor of less than 10K Ω across each reverse biased junction. The problem was circumvented by using a smaller value for saturation current which results in the model giving higher V_{BE} than true value but otherwise accurately representing the device. Leakage current was modeled by placing a current source shunted by a resistor (to simulate voltage dependence) across each reverse biased junction.

The simulations were used to set the values for the compensation networks C1 - R8 and C2 - R9. They predict 3.5 MHz gain bandwidth, 2.6V/us slew rate at 300°C. Simulated noise at 25°C is 8.7 nv/$\sqrt{Hz}$.

CONCLUSION

A dielectrically isolated complementary vertical bipolar process has been characterized for use at 300°C and been shown to be useful and reliable for linear design at that temperature. Circuit design methods for a 300°C op amp have been developed and demonstrated on IC test chips and an entire op amp design has been proposed.

REFERENCE

1. "Electromigration - A Brief Survey and Some Recent Results", J. R. Black, IEEE Trans. E. D., vol. ED-16, No. 4, Apr. '69 pp 338-347.