SAND81-0345C

HIGH-TEMPERATURE COMPLEMENTARY METAL OXIDE SEMICONDUCTORS (CMOS)

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Introduction

The theory on which silicon (Si) metal oxide semiconductors (MOS) technology is founded states that this type semiconductor will perform adequately at 300°C. High temperature tests conducted on commercially available MOS field effect transistors (FET) have confirmed this hypothesis.[1-3] In this report, we present the results of an investigation into the possibility of using CMOS technology at Sandia National Laboratories (SNLA) for high temperature electronics. A CMOS test chip (TC) was specifically developed as the test bed. This test chip incorporates CMOS transistors that have no gate protection diodes; these diodes are the major cause of leakage in commercial devices.

We decided to use CMOS technology because both n- and p-channel devices could be evaluated. We also looked at small-scale inte-tration, e.g., an inverter using CMOS junction isolation and a simulation of dielectric isolation.

Theory and actual data have been compared before.[3] In this paper we intend to report on the aging and stability of CMOS devices; especially where requirements call for minimal drift when subjected to 300°C for 1000 hours. This drift must be less than that in devices taken from room temperature to 300°C.

Physics

From semiconductor physics, the following generalization can be made:

- As temperature increases, the Fermi level moves toward the middle of the band gap, causing the built-in potential to decrease, thereby decreasing the threshold voltage.
- As temperature increases, the band gap narrows, causing a minor increase in the intrinsic carrier concentration, (n_i).
- Carrier mobility decreases with increasing temperature, causing transconductance to decrease.
- Increasing temperature increases leakage of generated and diffused currents.
- The more the doping, the greater the variation in threshold voltage as temperature increases.
- The zero temperature coefficient point occurs at higher gate voltages as the doping is increased.
- The overall transconductance decreases rapidly as temperature and doping increases.

With these generalizations in mind, we made the process variation listed in Table 1.

Table 1

Processing Variation

Wafer	Substrate	P-well
1	.8 -1.[illegible] Ω-cm n-type $\sim 5\times10^{15}\ cm^{-3}$	Boron 60 keV 7×10^{13} $N_S \cong 4\times10^{16} cm^{-3}$
5	.8 -1.2 Ω-cm n-type $\sim 5\times10^{15} cm^{-3}$	Boron 60 keV 2×10^{14} $N_S \cong 4\times10^{17} cm^{-3}$
7	.2 -.4 Ω-cm n-type $\sim 2\times10^{16} cm^{-3}$	Boron 60 keV 1×10^{14} $N_S \cong 2\times10^{17} cm^{-3}$
9	.2 -.4 Ω-cm n-type $\sim 2\times10^{16} cm^{-3}$	Boron 60 keV 2×10^{14} $N_S \cong 4\times10^{17} cm^{-3}$

These variations are adjustments of the various doping levels that compose the MOSFETs, and they require many trade-offs in electrical performance, making optimization difficult (Tables 2 and 3). Table 2 shows that, although wafer 1 produces symmetrical gate voltages, leakage and transconductance vary greatly between the two channels. Wafer 9 performs well in leakage and voltage but not in transconductance.

All wafers except No. 5 performed as predicted by theory. The anomaly of wafer 5 remains unexplained. The tables show the average values derived after subjecting the wafers to 300°C for 1000 hours. Threshold voltages for the surviving devices are within ±0.1V of those listed in Tables 2 and 3; leakages are within ±5μA of those listed in Table 2, and 25μA of those in Table 3. According to theory, the following pattern should appear.

For wafers 1 and 5, p-channel data should be similar.

For wafers 7 and 9, p-channel data should be similar.

For wafers 5 and 7, n-channel data should be similar.

Table 2

TC-1 Process Comparison at 300°C

Wafer	Average Leakage (μA) n-Channel	p-Channel	Average Gate Voltage (V_G) @ 10μA n-Channel	p-Channel	Average Transconductance (mmhos) n-Channel	p-Channel
1	12.41	18.85	1.45	-1.45	0.45	0.24
5	21.44	25.86	2.72	-1.26	0.22	0.26
7	3.90	6.15	1.60	-2.41	0.34	0.21
9	4.43	6.07	2.56	-2.50	0.10	0.14

Table 3

	Average Leakage (μA)		Average V_G @ 100 μA				Average Gm (mmhos)			
Wafer	n-Channel	p-Channel	n-Channel	n-Channel	p-Channel	p-Channel	n-Channel	n-Channel	p-Channel	p-Channel
1	280	460	1.54	1.55	- .79	- .78	1.10	1.07	1.82	1.75
5	88	163	3.08	3.08	-1.18	-1.21	0.61	0.61	1.79	1.79
7	107	139	1.77	1.78	-2.12	-2.14	1.07	0.99	1.27	1.27
9	88	139	2.77	2.49	-2.02	-2.22	0.66	0.68	1.16	1.14

TC-4 Process Comparison at 300°C

The tables show that, except for wafer 5, the theory and the actual data generally agree.

The guard-ring, junction isolated CMOS process is quite clean and uses Q_{ss}, N_{st} reduction techniques and other schemes to reduce oxide contamination.[8-11] For example, by annealing with N_2 we decrease Q_{ss}, and by annealing with H_2 we decrease N_{st}. Careful and clean processing decreases sodium and potassium contamination. The circuits were metallized with standard aluminum 1μm thick, and standard p-glass passivation was used over the metal. The components were packaged in a ceramic, 16-pin flat pack.

Stability

Although we will not discuss all the parameters tested, as an indication of stability, we will discuss data for gate voltage at 10μA (TC-1) and 100μA (TC-4), and leakage currents.

To determine gate voltage, each transistor was measured separately. The source and substrate were connected to ground, and the drain was connected to an 8-V source. The voltage on the gate was slowly increased until 10μA was measured between source and drain; this voltage was recorded. The 10μA value includes the reverse leakage current from drain to substrate but not from p-well to n-substrate. In all data obtained, 10μA was not exceeded in the gate voltages measured for TC-1 (10μA) or for TC-4 (100μA). See Table 3.

Leakage Current

The leakage currents discussed are drain-to-source channel leakage, drain-to-substrate reverse bias leakage, and p-well to n-substrate leakage. They were measured with the transistors connected as a CMOS inverter. With one transistor biased strongly on, we then measured the current that the other transistor allowed to pass while it is turned off (Figure 1). Thus, we have a worst case measurement for leakage. In all cases, leakage was small enough ($I_L < I_{ds}$) to allow the semiconductor to remain useful in actual circuits.

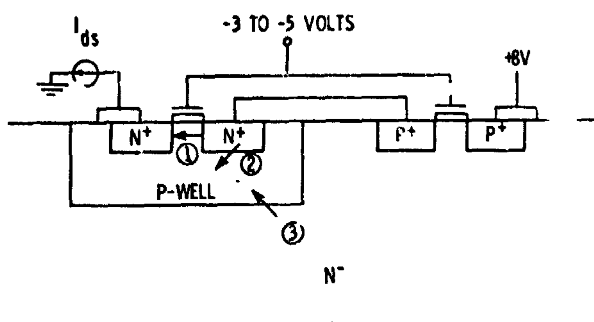

Figure 1

Measurement of Leakage Current for n-Channel

(1) Drain to Source Leakage
(2) Drain to p-well Leakage
(3) P-well to n-substrate Leakage

In all cases, we determined that the n- and p-channel devices were reasonably stable and functional except for wafer 5 which remains an unexplained anomaly.

Wafer 9 demonstrated good stability, low leakage, and a reasonable V_G at 10μA on both the n- and p-channel devices. TC-4 data supports this finding but has an order of magnitude increase in leakage because of its larger size.

Inverters

Data from transistors connected as inverters, show that they will perform as a small-scale integrated circuit (SSIC) at high temperatures for extended periods of time (300°C for 1000 hours).

V_{NL} and V_{NH}

In this test, we measured the output voltage with the inputs at 1.5V (V_{NL}) and 3.5V (V_{NH}) obtaining functionality and noise margin parameters.

I_{DN} and I_{DP}

With these tests we determined the drive current capability of the n- and p-channel devices when hooked together as an inverter.

Results

The data for inverters show that all processes were functional at 300°C after 1000 hours. In all cases, drive currents decreased with increasing temperatures as theorized; current is lost to ground through several leakage paths (Figure 1) as temperature increases.

Judging from the data obtained, there seems to be no outstanding advantage in one process over the other. There should be more dynamic testing to determine this. The data do suggest that drive currents for the higher doped devices (wafer 9) are more symmetrical for a given geometry and are less temperature dependent than lower doped devices. Furthermore, CMOS, when digitally operated, works in a complementary mode; that is, when one transistor is on, the other is off. This is helpful for reliable high-temperature performance because it allows both devices to go depletion yet still perform a given digital function (Figure 1). Therefore, we can leave the threshold voltages closer to zero than when the devices must remain enhancement at 300°C, making higher speed devices possible. Wafer 5 has not been discussed because of its unexplainable behavior.

Simulated dielectric isolation inverters showed similar trends but with a vast improvement in leakages. This makes a big difference in noise margin and absolute temperature optimization.

Many trade-offs are necessary to determine the best way to build high-temperature CMOS circuits. The principal parameters that must vary are doping profiles and size; oxide growth and overall cleanliness make the circuit possible.

Process (Doping Profile)

Judging from the results of this study, doping profiles like those of wafers 7 and 9 are best for high-temperature use. Application is extremely important because we must know what is expected from the circuit before the right process is found. For example, wafer 9 (n⁻ sub ≈2 x 10^{16} cm^{-3} and p-well N_S ≈4 x 10^{17} cm^{-3}) might appear to be the best choice for high-temperature electronics --- it has good symmetry, exhibits small variation with temperature, and has reasonable drive current capability. However, in some applications, it may have too high a threshold voltage and too low a breakdown voltage (~12V). Therefore, depending on the circuits used, increasing the doping to increase the temperature range of the CMOS does not always produce an ideal circuit. In fact, some electrical requirements may make it impossible to develop a high-temperature circuit by using silicon planar technology.

Geometry

When designing the mask set for high-temperature circuits, we must include several considerations not necessary when designing room temperature circuits. For example, of major importance is the fact that the area between the p-well and the n-substrate must be as small as possible to decrease reverse leakage. This means that each n-channel transistor should have its own p-well. The price for this is an undesirable increase in the silicon area.

The mobility of holes and electrons decreases with increasing temperature but not at exactly the same rate. However, the ratio of Z/L n-channel to Z/L p-channel should be the same as in room temperature circuits to keep the circuits complementary. Keeping their ratio the same as in room temperature circuits seems to be a good compromise.

For high temperature circuits, the area from the drain to the substrate junction should be as small as possible to decrease reverse leakage. This is accomplished by horseshoeing the Z/Ls, thereby increasing circuit density -- this method is already in common use.

To make high-temperature circuits more reliable, metal lines should be as broad and deep as possible, again sacrificing chip area.

Conclusions

Existing CMOS technology can be used to produce stable and useful circuits that operate at 300°C for 1000 hours. This accomplishment, however, sacrifices some chip area and does not provide gate protection. For this latter problem, high-temperature GaAs and GaP diodes should be developed as protection devices. Although these diodes would probably be outside the CMOS chip, they could be part of the same flat pack.

Dielectric isolation CMOS would be a great improvement over junction isolation and work has begun in this area. New solar cell diodes show promise as input protection devices. This would allow us to be completely integrated again.

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