DIGITAL PROCESSING CLOCK

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ABSTRACT

The Digital Processing Clock SG 1157/U has been developed by Naval Research Laboratory and is:

(1) compatible with the PTTI world where it can be driven by an external cesium and built in test equipment shows synchronization with that cesium through the 1 PPS

(2) built to be expandable to accomodate future time keeping needs of the Navy as well as any other time ordered functions.

Examples of this expandibility are the recent inclusion of an unmodulated XR3 time code and the 2137 modulated time code (XR3 with 1 kHz carrier)

INTRODUCTION

The Digital Processing Clock is designed to make precision time available in visual and electronic form. The system consists of one digital processing clock (SG 1157/U) four remote display units (ID 2170/U) and contains state-of-the-art electronic devices. In all instances where it has been available, military-specified hardware has been utilized. The clock provides all necessary timing information to enable the generation of a wide range of time codes and time related information for future applications.

The clock is human engineered for easy setting. It is designed to be driven by precision frequency standards such as cesium beams, rubidium vapor standards, disciplined time and frequency standards, or any other precision frequency standard providing an adequate 1 MHz output, but will operate on its own internal oscillator if no precision standard is available. The clock is capable of being set to an accuracy within 1 microsecond to an applied external pulse. This pulse need not occur on precise 1 second intervals; prior knowledge of when the pulse will occur is used to preset the thumbwheel switches on the front of the clock.

In addition to the display of the precise time in days, hours, minutes, and seconds, the Digital Processing Clock produces (a) a parallel time code output that is capable of driving from one to four remote display units at distances well removed from the clock itself,

(b) two separate selectable time of event output pulses which can be used to synchronize other equipments, and (c) pulse outputs of 1 PPS and 1 PP10S.

The Digital Processing Clock is presently incorporated in the 688 Class Navy Submarines and applications of it may be extended into other Navy platforms in the future.

FUNCTIONAL DESCRIPTION

Figure 1 shows the Digital Processing Clock as it is presently being installed in the 688 class submarines. Sixteen of these clocks have been delivered to the Navy at this time.

Figure 2 is a Block Diagram showing the Digital Processing Clock with four remote readout units daisy-chained to it. The remote display units are located at distances up to 100 ft. from the SG 1157/U clock on the submarines. The remote display units are fed by a 20 line parallel bus which allows the use of very simple and easily replaceable electronic parts. BCD to seven segment decoders are included on the LED readout chip.

Figure 3 is a block diagram for the Digital Processing Clock showing signal flow and functional operation and inputs on front and back of clock. The Digital Processing Clock takes the 1 MHz input signal from a frequency standard, for example a cesium beam standard, and divides it down to produce a one-pulse-per-second (1PPS) output tick and the time-of-day information. Should the external 1 MHz signal disappear from the input, an internal 1 MHz signal generated from an internal oscillator within the clock itself is automatically applied at the input. The accuracy of this signal, however, is one part in 10^7 over a temperature range of 0°C to 50°C and, therefore, the clock will accumulate time error rapidly when this mode of operation exists. The internal oscillator may be retuned with the screw-covered screwdriver adjustment on the top of the oscillator. Buffered outputs from all dividers in the countdown chain are available internally, and the 20 parallel lines of information containing hours, minutes, and seconds in a binary-coded decimal (BCD) format are fed to a multipin connector (Time Code Out) on the rear panel of the clock to drive the remote readout units.

Synchronization, time setting, or both, are accomplished by applying an external positive going transition to the External Sync Input on the front panel. If no external time signal is available, the lower Sync switch on the front panel can be put in the INT position and after the Arm button is pushed the next internally generated (1-pulse-per-10-s) 1 PP10S signal will set and synchronize the Digital Processing Clock.

An output pulse may be generated at any time desired with the Time-of-Event (TOE) output. There are two TOE output BNCs, A and B, on the back of the clock. The repetition rate of this event pulse is internally selectable at five different rates (1 PPS, 1 PP10S, 1 PPM, 1 PPHR, and 1 PPDAY) with DIP packaged rocker switches on the TOE Circuit Board. The TOE output (e.g., 10 microsecond wide one pulse per sec (1 PPS) output) can be delayed by the time set up on the subsecond (millisecond and microsecond) thumbwheel switches on the front of the clock. If the subsecond thumbwheel switches were set to zero, this 1 PPS signal would be synchronized with the 1 PPS output signal available on the front panel.

The Digital Processing Clock normally receives its power from an external power source of 115 V, 60 Hz, single phase. If the power source fails or is disconnected, or the power module develops a fault, the clock is diode switched to battery operation with zero time error.

Figure 4 shows the Clock Time Base and Display printed circuit card. This circuit contains the TCXO (temperature controlled crystal oscillator) and switching circuit which allows the transfer of external frequency reference with minimal time loss (in the order of one microsecond (μs).

Figure 5 shows the 1 MHz to 1 PPS Countdown and Sync Function printed circuit card. The function of this circuit is to count pulses of the input 1 MHz square wave and produce an output of one-pulse-per-second (1 PPS). In addition, the occurrence of this output pulse must be capable of being set to within one microsecond (μs) of any time relative to an externally applied synchronizing pulse or any preset number of microseconds from the external pulse.

Figure 6 shows the Day, Hour, Minute, Second Counter Function printed circuit card. The function of this circuit is to take the 1 PPS signal produced by the card just described and divide it down further to produce second, minute, hour, and finally, day of the year information, which will be displayed on the clock's front panel. With external sync, it can be preset to any desired day, hour, minute, second with front panel thumbwheel switches.

Figure 7 shows the Time of Event Function printed circuit card. The function of this circuit is to compare the BCD output information from the clock's divider chain with the setting of the digital thumbwheel switches on the front panel. When this comparison indicates total agreement, this circuit gates out a 10 μs Time of Event pulse whose leading edge occurs at the precise time when coincidence was achieved. The TOE card presents two selectable outputs on the back of the clock.

Figure 8 shows the Power Supply printed circuit card. This circuit regulates the 9.7 vdc from the power supply to 5 vdc for the printed circuit cards and provides diode switching for battery operation.

OPERATOR CONTROLS

Figure 9 shows the operator controls.

1. Thumbwheel Switches--15 unit decade used for time setting, delay insertion, and time of event operations.
2. Battery Standby/Off Switch--in Standby position supplies backup power for clock for 1/2 hour; in Off position battery is taken out of circuit to prevent discharging during shipping or storage.
3. LED Display--when on battery power, push to get display of day of year and time of day.
4. LED Test--when pushed display shows all 8s and decimal points lit.
5. Event Output/Inhibit--Time of Event outputs on back of clock are enabled in Output position.
6. Sync 1 PPS/Clock--in Clock position sets clock to time on thumbwheel switches and syncs to within one microsecond with sync signal when it arrives. In 1 PPS position only the subsecond timing is changed.
7. Sync Int./Ext.--in Int. position syncs clock with internally generated 1 PPlOS. In Ext. position syncs clock to applied Ext. Sync signal.
8. Sync Arm--push button to arm clock for arrival of sync signal.
9. Display--7 segment LED display of Day, Hour, Minute, Second information and flashing decimal point indicators for (1) clock armed (3 points to left of each day digit), (2) clock on Internal Oscillator (1 point to left of tens of minutes), (3) coincidence of Sync to within one microsecond (2 points to left of second digits).
10. Fuses--two 1.5A Line fuses and one spare.

The clock is started by tick start. It is easily started by an external tick which is the preferred method, but can also be started from the internal oscillator in several steps. This design is used to facilitate starting with information from other reference standards and for precision setting, the pulse need not arrive on an even second. However, if time of arrival is known in advance, this advanced information is set in the thumbwheel switches on the front and the clock armed before the arrival of the pulse. The clock starts on the positive going transistion which may typically start at 0.5 vdc and rise to 5 vdc.

BUILT-IN TEST EQUIPMENT

The Digital Processing Clock has built-in test equipment (BITE) to ease the checking of proper operation. The status of the BITE indicators should be checked on a regular basis depending on usage. BITE indicators are:

1. LED test--when pushbutton switch on front panel is pushed, the display shows all 8's and decimal points are lit.

2. Flashing decimal point indicators:
   a. Clock Armed (3 decimal points to left of each day digit light)
   b. Clock on Internal Oscillator (1 decimal point to left of tens of minutes flashes)
   c. Coincidence of Sync to within one microsecond (2 decimal points to left of seconds digits flash).

EXPANDIBILITY

Figure 10 shows the SG 1157/U clock with the newly developed XR3 serial time code printed circuit card installed. This is the first of the additional add-on capabilities which uses the basic timing information available in the clock and delivers specific outputs, i.e., XR3 level shift code, 2137 code (XR3 time code, AM modulated on a 1000 Hz carrier), and 200 KHz. There is still additional room for future development of time ordered capability.

Figure 11 shows the SG 1157/U clock's back panel which has the output BNC connectors for the above mentioned three outputs as well as the original 1 PPS, 1 PP10S, TOE (time of event), and 20 line parallel time code outputs.

BATTERY POWER

Figure 11 also shows the Gel-cell batteries used to power the SG 1157/U clock in case of Ship-to-Shore changeover power interruptions. The batteries will power the clock in excess of one hour in case of power interruption. The batteries are charged by a 9.7 vdc regulated power supply.

SPARE CARDS

Figure 12 shows an SG 1157/U clock with a set of spare cards stored in the card cage. The reliability of the printed circuit cards has been very high and availability of spare cards from a supply center is made difficult by the high reliability of the cards themselves. Therefore a set of spare cards for possible future failures

and storage of these cards in the clock itself is recommended. This also eases the submarine's requirements on space and difficulty in attaining spares at sea.

FUTURE CAPABILITIES

Figure 13 shows possible future capabilities for the Digital Processing Clock.

1) Timekeeping station capability - The inclusion of a microprocessor card such as the Intel 8085 would enable the clock to monitor external precision standards and calculate the time differences between the external standards and the time in the SG 1157/U clock. This time difference information could then be multiplexed to the clock's LED readout and present the information to the operator via the display. The time difference information could be also made available by an RS232 output on the back of the clock.

2) Upgrade to 100 ns time steps - If increased accuracy is required a high precision sync card could take an external 5 MHz signal and double it to 10 MPPS, thus allowing the clock to be synchronized to the nearest 100 nanosecond pulse rather than nearest microsecond pulse as is now the case.

3) High Speed Recorder - With the basic timing information available in the SG 1157/U clock, a high speed recorder capability could be developed using an A/D converter storing the digitized information along with the time it was sampled. This information could be stored in RAM under the control of a microprocessor. The output could be displayed at a much slower rate and fed through a D/A converter to an external recorder for visual presentation.

It takes many years for new ideas to be implemented into the Fleet. This equipment represents several ideas on how technology transfer can be implemented in progressive steps without necessitating total equipment replacement.

ACKNOWLEDGEMENTS

The author would like to acknowledge the contributions of Joseph J. O'Neill and Ruth E. Phillips.

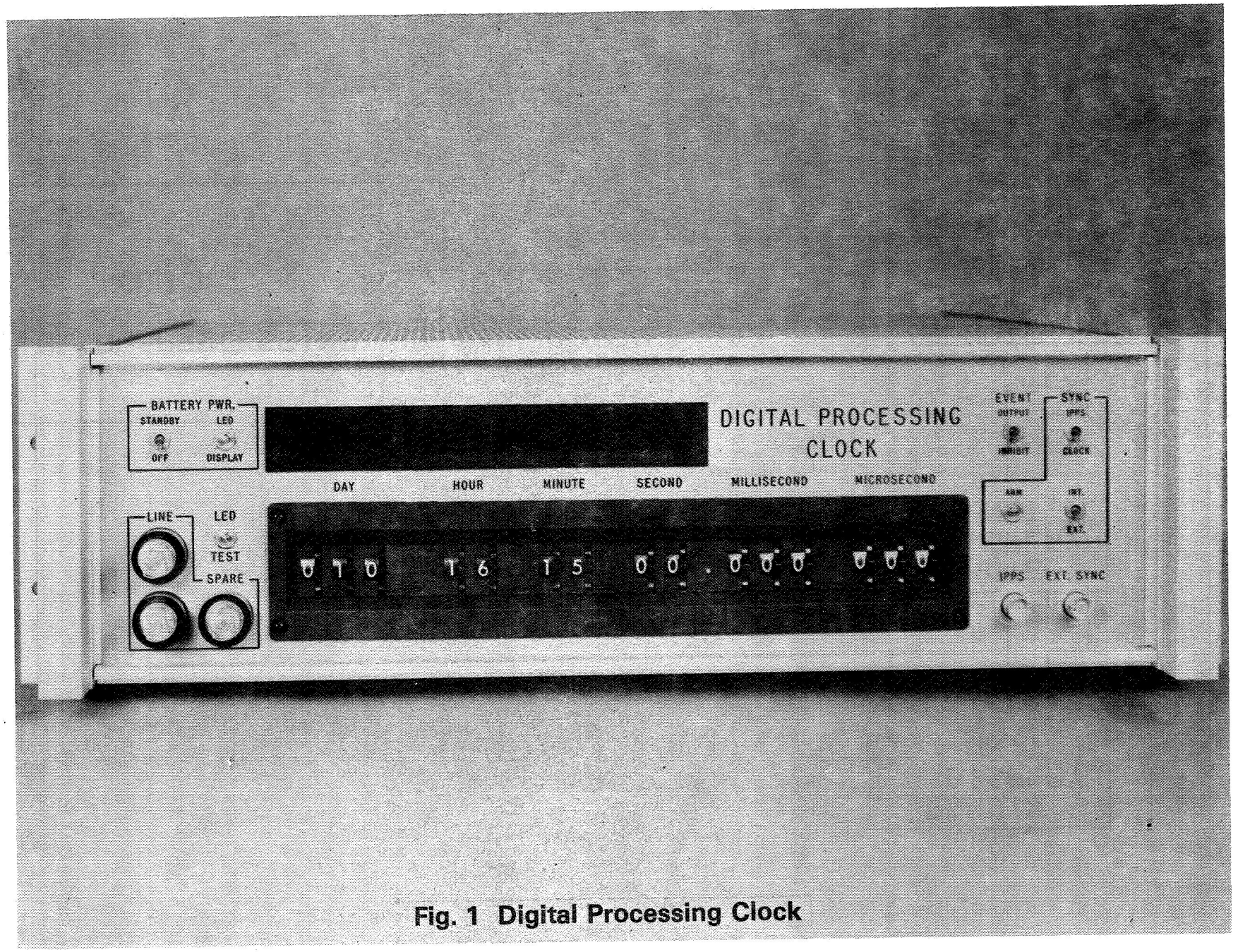


Fig. 1 Digital Processing Clock

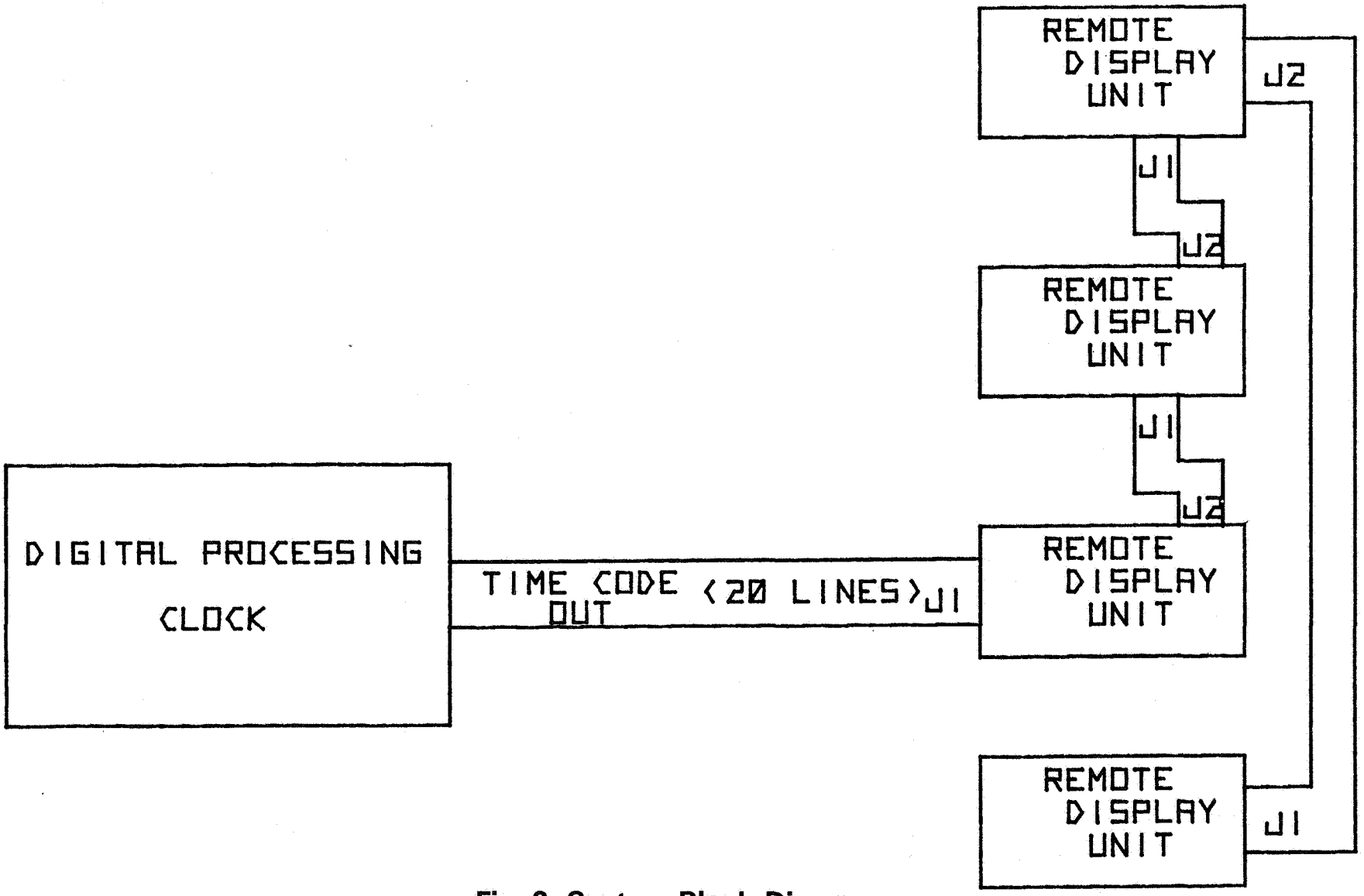


Fig. 2 System Block Diagram

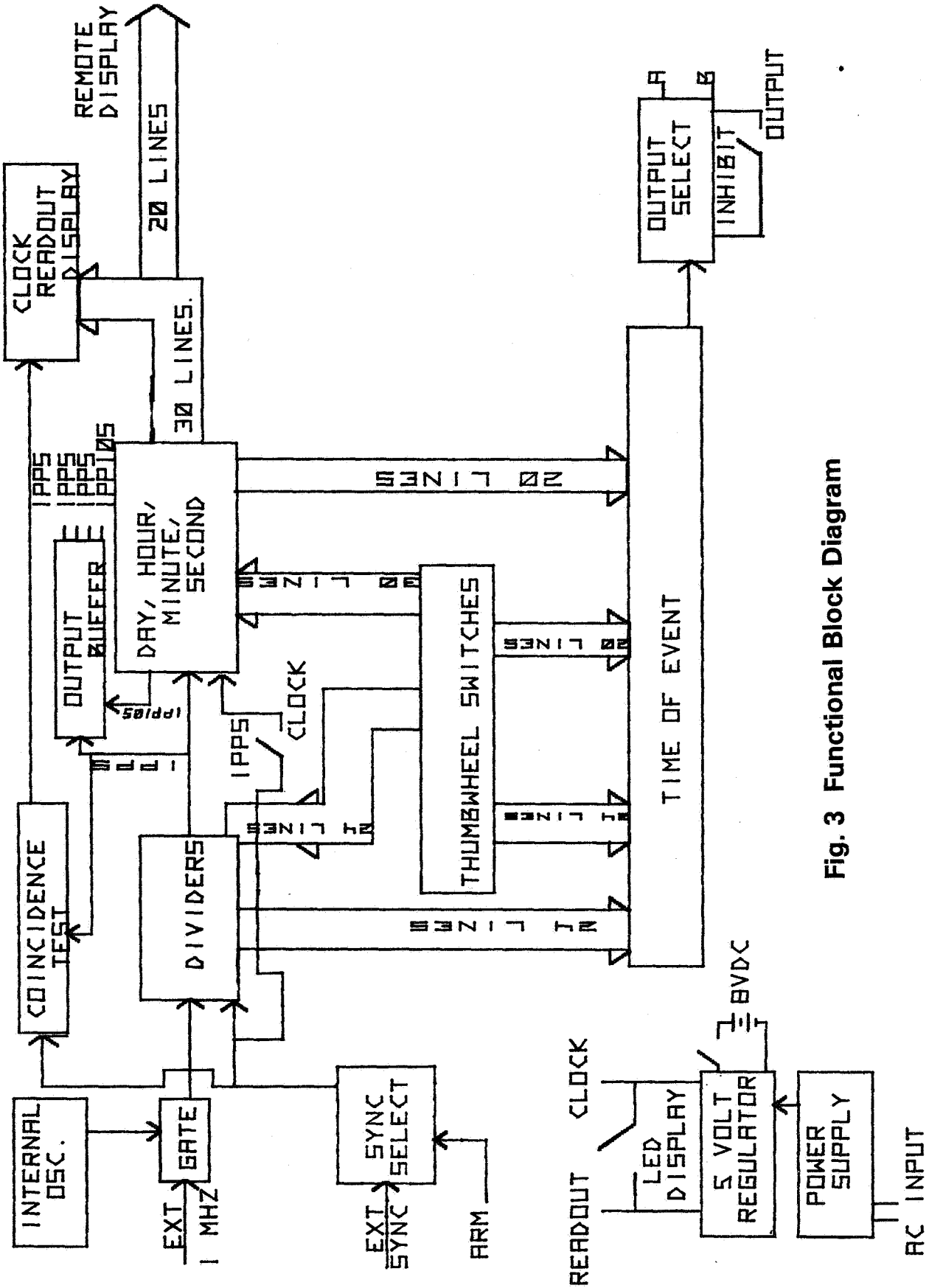


Fig. 3 Functional Block Diagram

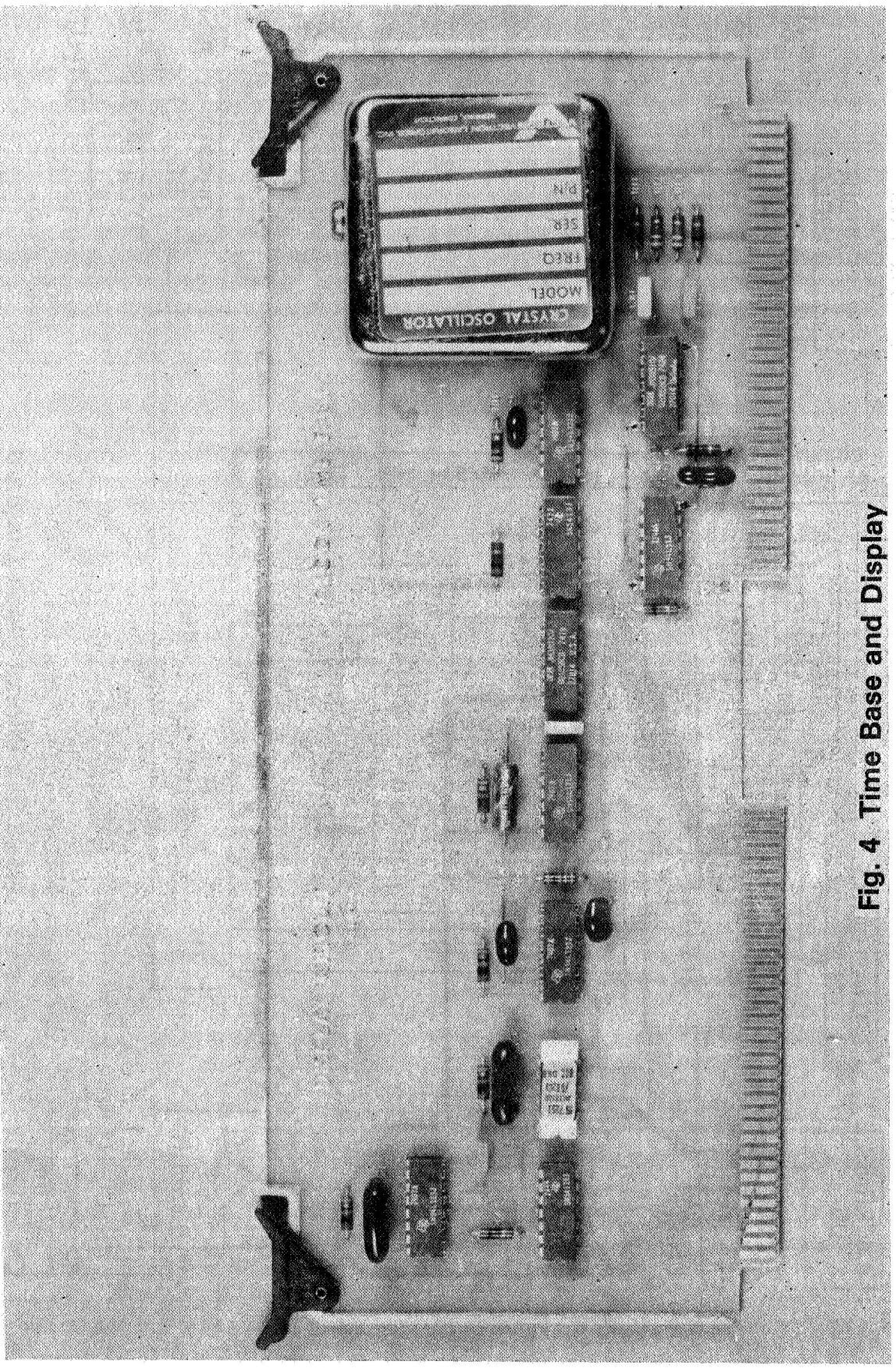


Fig. 4 Time Base and Display

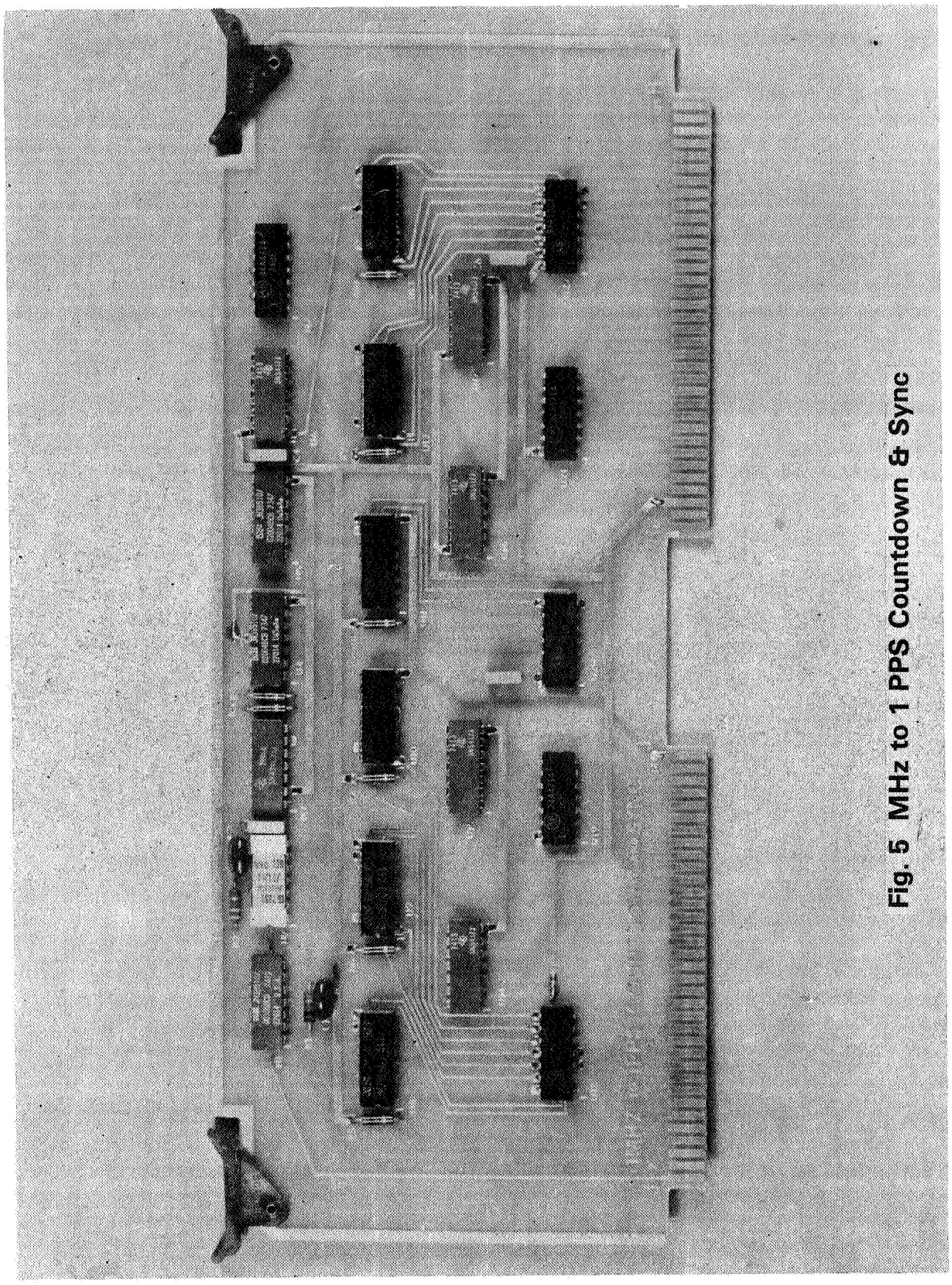


Fig. 5 MHz to 1 PPS Countdown & Sync

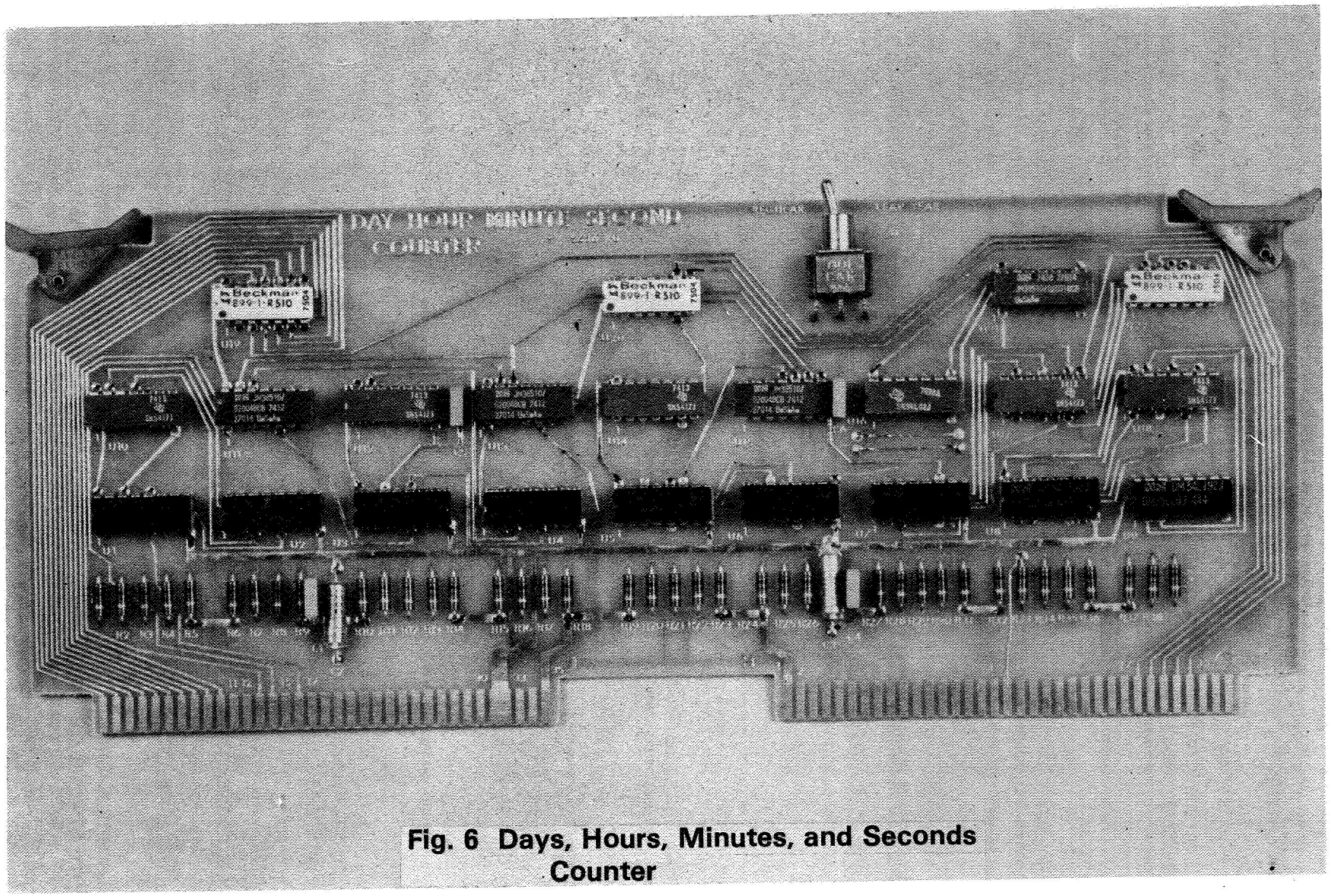


Fig. 6 Days, Hours, Minutes, and Seconds Counter

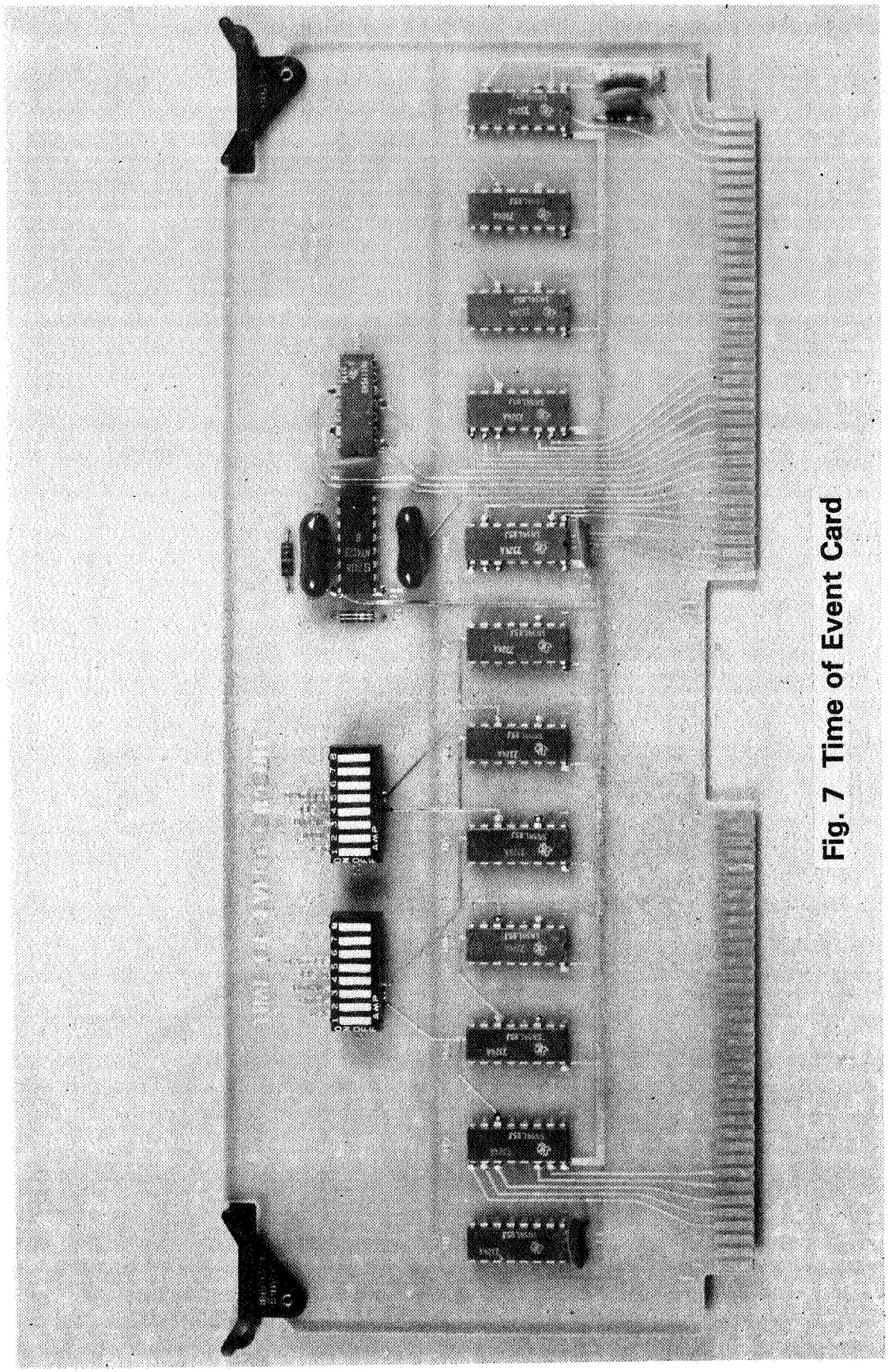


Fig. 7 Time of Event Card

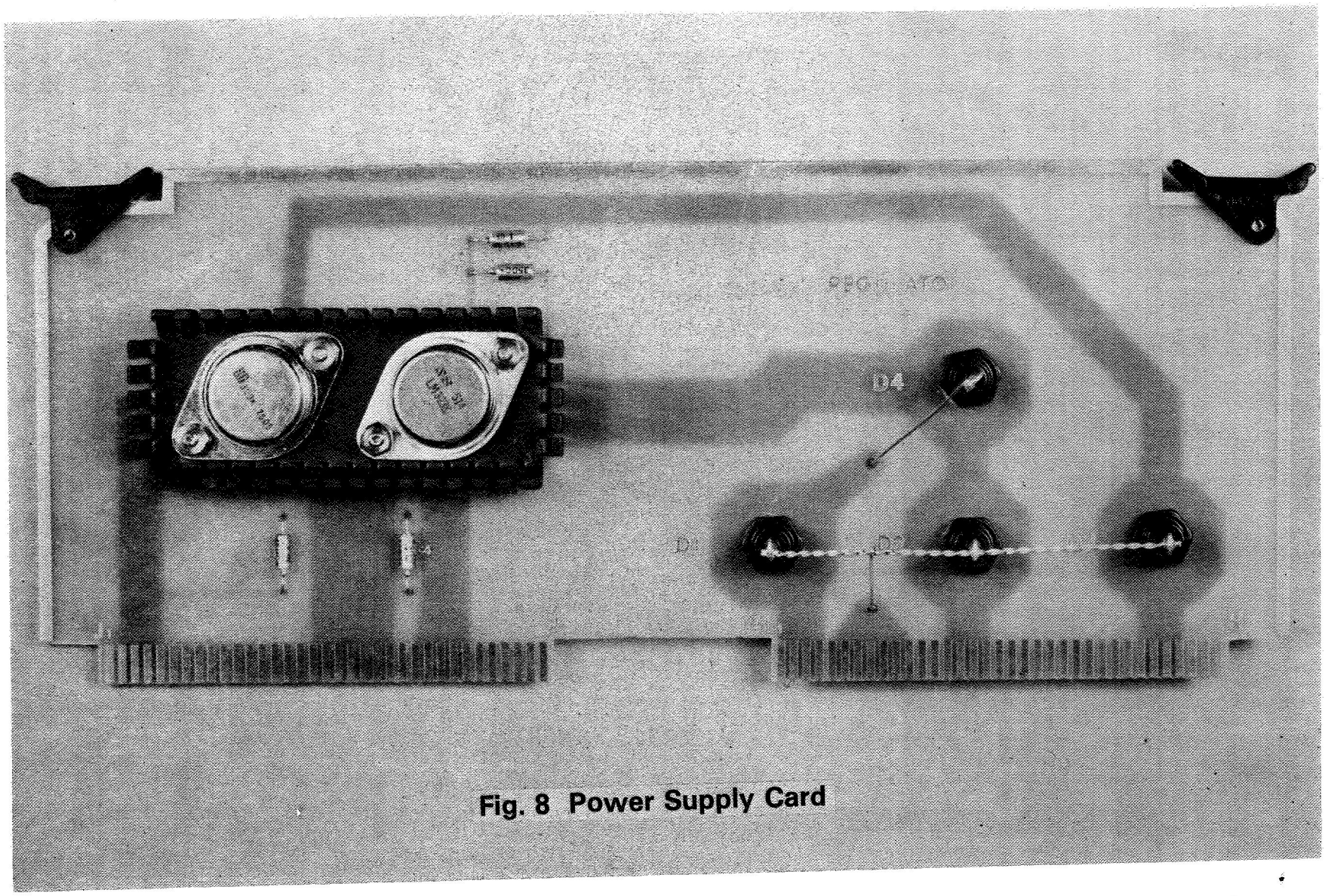
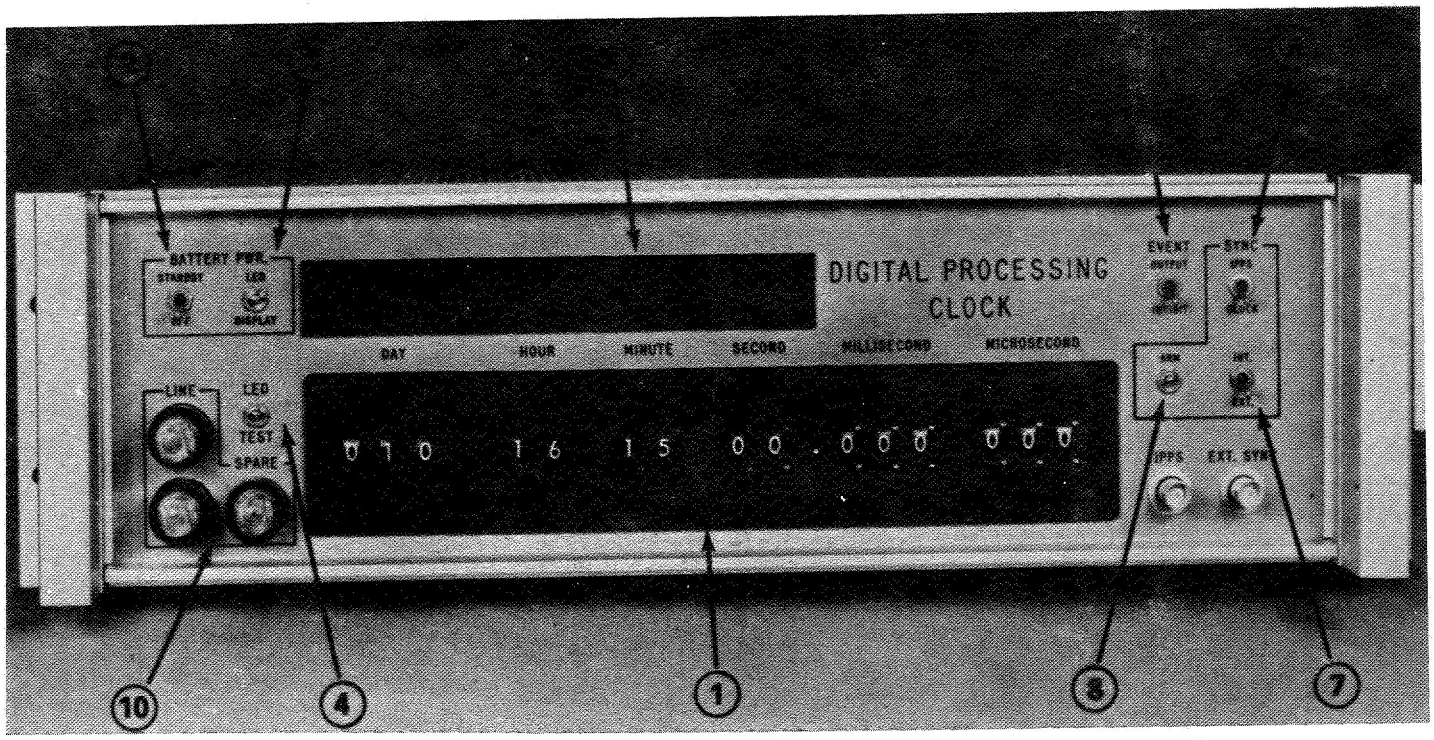


Fig. 8 Power Supply Card



1. Thumbwheel Switches—15 unit decade used for time setting, delay insertion, and time of event operations.
2. Battery Standby/Off Switch—in Standby postion supplies backup power for clock for ½ hour; in Off position battery is taken out of circuit to prevent discharging during shipping or storage.
3. LED Display—when on battery power, push to get display of day of year and time of day.
4. LED Test—when pushed display shows all 8s and decimal points lit.
5. Event Output/Inhibit—Time of Event outputs on back of clock are enabled in Output position.
6. Sync 1 PPS/Clock—in Clock position sets clock to time on thumbwheel switches and syncs to within one microsecond with sync signal when it arrives. In 1 PPS position only the subsecond timing is changed.
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10. Fuses—two 1.5A Line fuses and one spare.

Fig. 9 Operator Controls

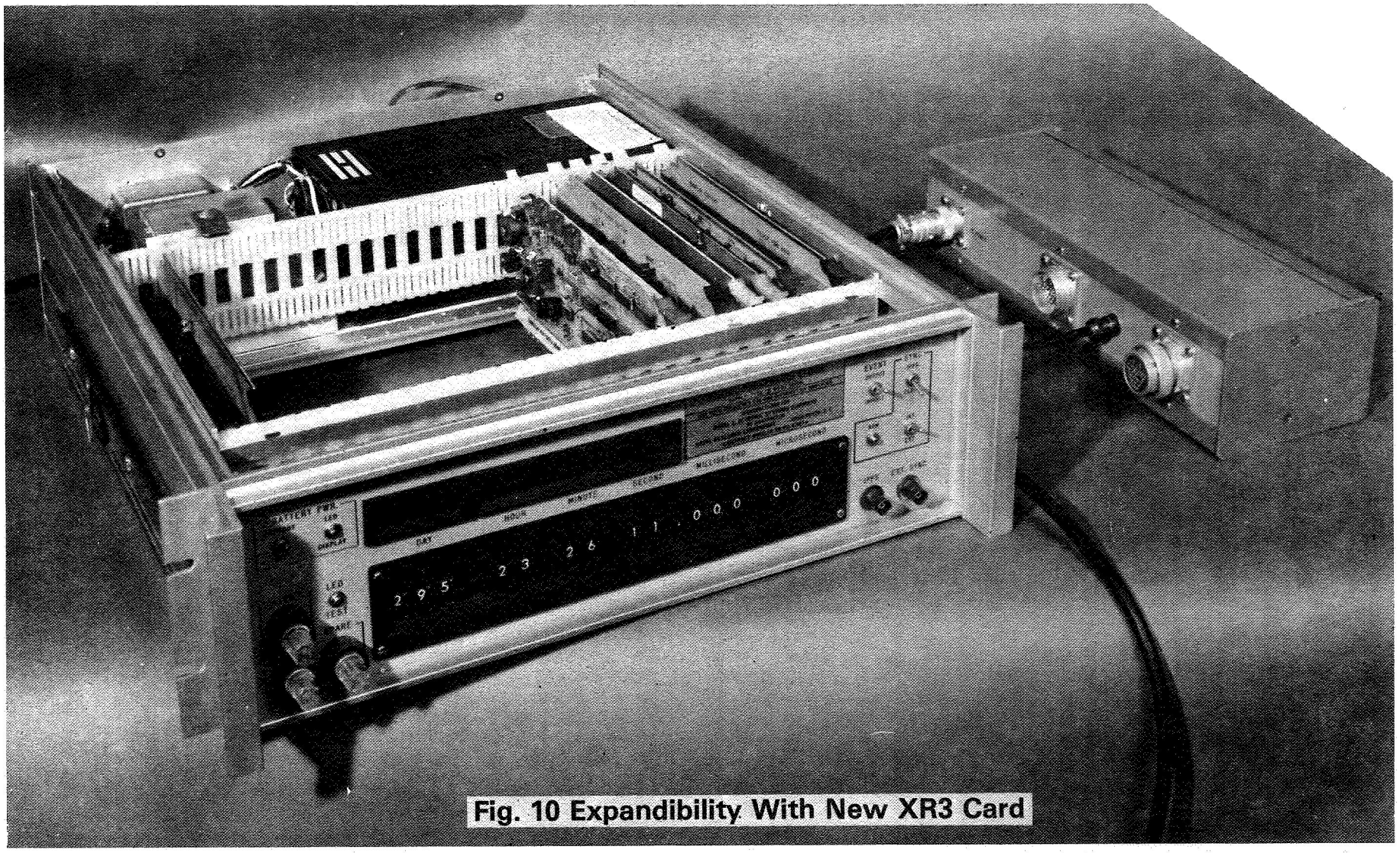


Fig. 10 Expandibility With New XR3 Card

Fig. 11 Spare Output and Batteries

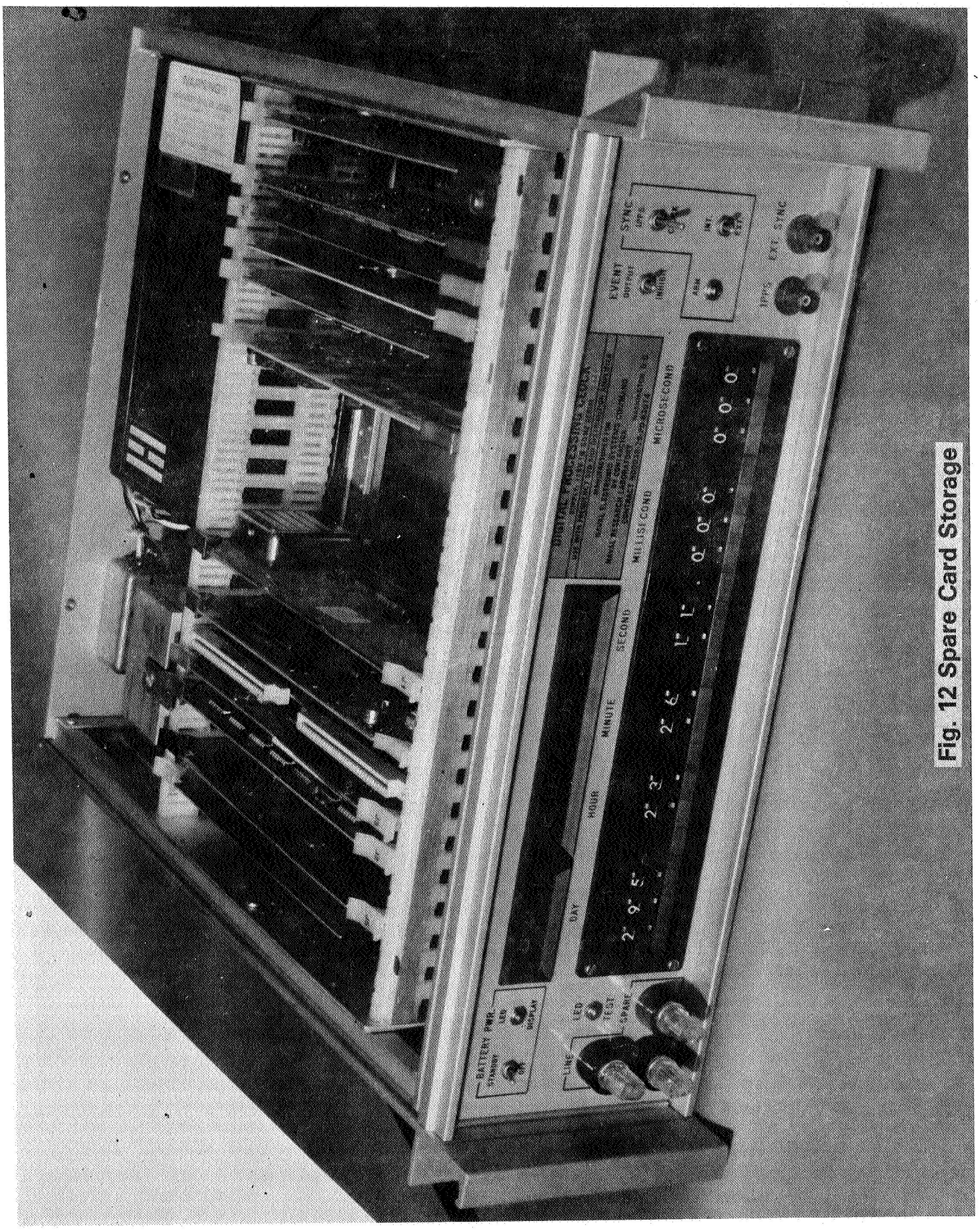
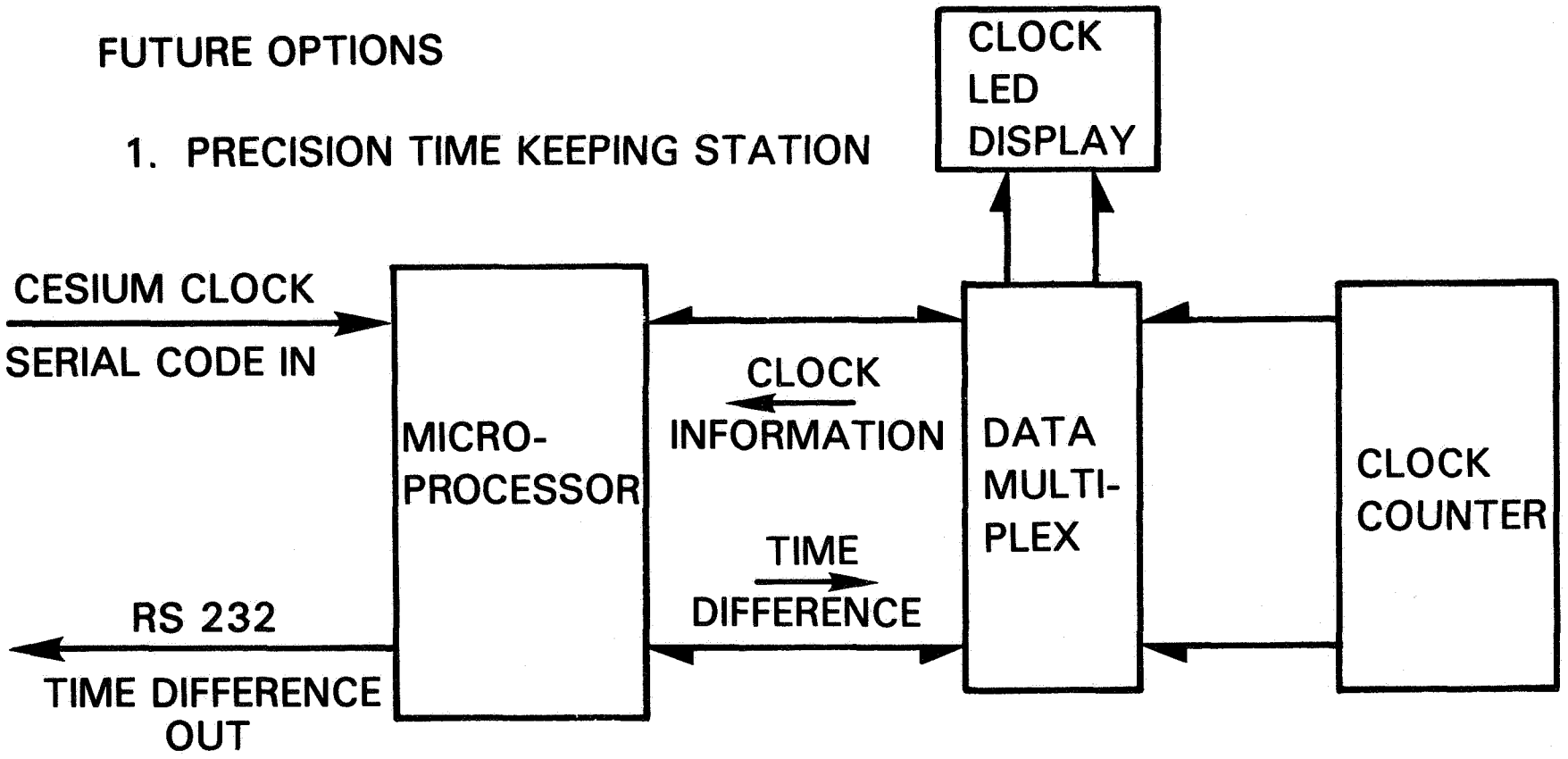


Fig. 12 Spare Card Storage

FUTURE OPTIONS

1. PRECISION TIME KEEPING STATION



2. UPGRADE TO 100 n SEC SYNCHRONIZATION CAPABILITY

3. HIGH SPEED RECORDER CAPABILITY

Fig. 13 Future Options