THE SPS INTERFERENCE PROBLEM - ELECTRONIC SYSTEM EFFECTS AND MITIGATION TECHNIQUES

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The potential for interference between SPS and various electronic systems is examined in this talk. The talk begins by briefly reviewing some of the causes of interference and their cures. Next estimates are presented of the various interference levels that can be expected from SPS. A significant portion of the remainder of the talk is then devoted to describing interference problems and protection requirements for satellite systems. The talk concludes by describing interference problems to other electronic devices such as integrated circuits.

One of the problems encountered during the analysis was the lack of estimates on the magnitude of the SPS microwave field at frequencies other than the fundamental. The characteristics of the transmission system at harmonics and frequency bands adjacent to the ISM band are currently unknown. For the analysis we have assumed out of band radiation levels as shown in figure 1 and 2. These values are representative of current technology. The interference levels are shown for both 4 kHz and 1 MHz reference bandwidths. The narrower bandwidths are of interest in interference studies with narrow band communications systems such as single channel per carrier satellite systems. The 1 MHz reference bandwidth is applicable to wideband systems such as the digital, pcm, multiple access systems.

The conclusions of the study are that interference is likely in the 2500 MHz to 2690 MHz direct broadcast satellite band adjacent to SPS. Estimates of the adjacent channel noise from SPS in this band are as high as -124 dBc/4 kHz and -100 dBc/MHz, where dBc represents decibels relative to the total power in the fundamental. A second potential problem is the 7350 MHz, 3d harmonic from SPS that falls within the 7300 MHz to 7450 MHz space-to-earth, government, satellite assignment. The talk will also discuss the separations required between SPS and other satellites in geosynchronous orbit.

A second example of the EMC study is the potential reaction of integrated circuits to microwave fields. Catastrophic failures can be produced in integrated circuits when the microwave power levels coupled into inputs and power leads reach 1 to 100 watts. The failures are typically due to bonding wire melting, metallization failures, and junction shorting. Non destructive interaction or interference, however, generally occurs with coupled power levels of the order of 10 milliwatts. This interaction is due to the rectification of microwave energy by the numerous pn junctions within these circuits. Table 3 shows estimates of the susceptability of 3 representative integrated circuits in an SPS microwave field. Values in the table represent the difference between the maximum power coupled into the device and the interference threshold. Thus a postive number denotes a potential interference problem while a negative numer indicates no interference. The table was prepared for worst case conditions of no shielding around the integrated circuit and a worst case alignment of the circuit and connecting leads in the microwave field.

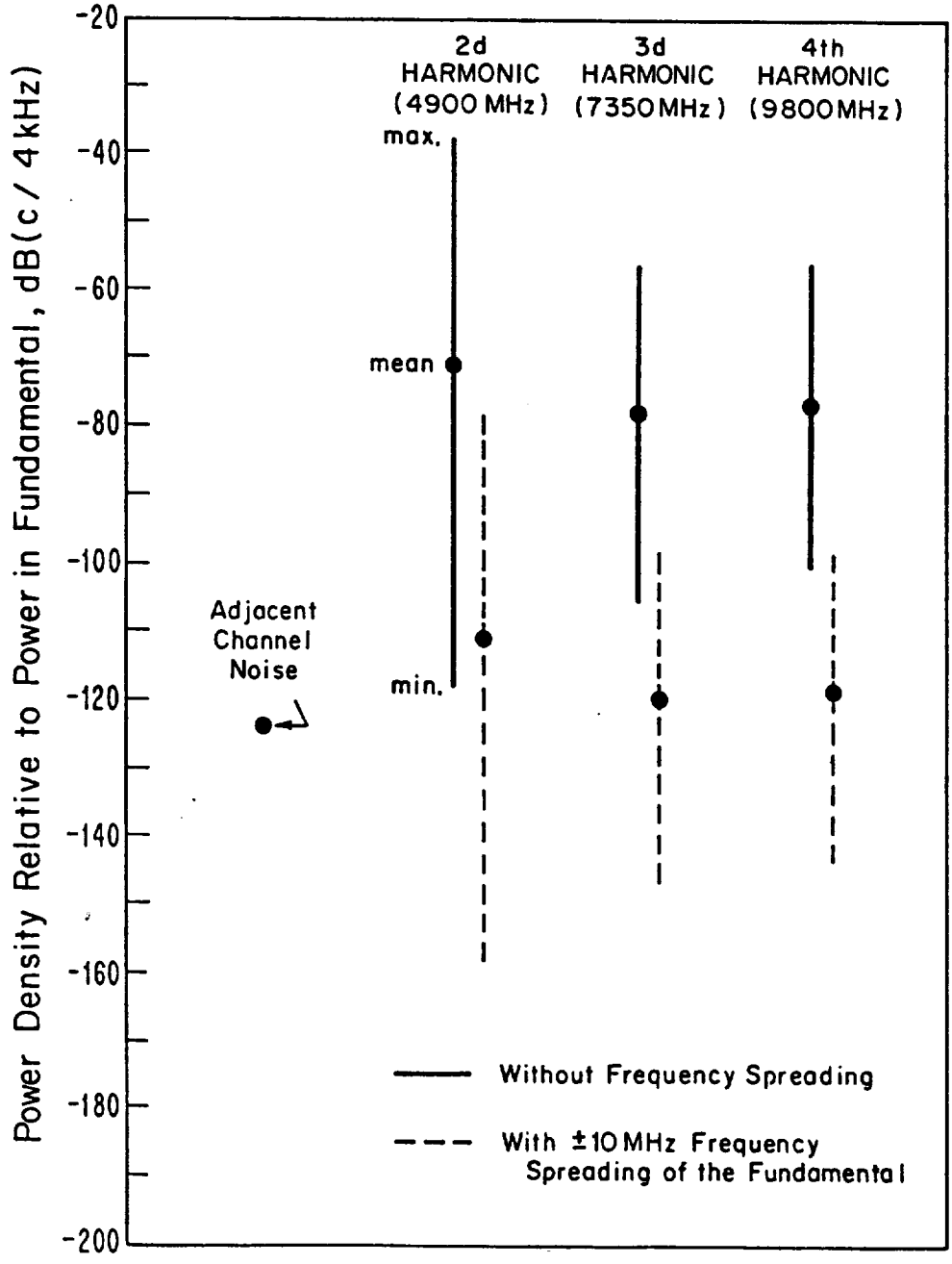

Figure 1. Estimates of interference levels in a 4 kHz bandwidth.

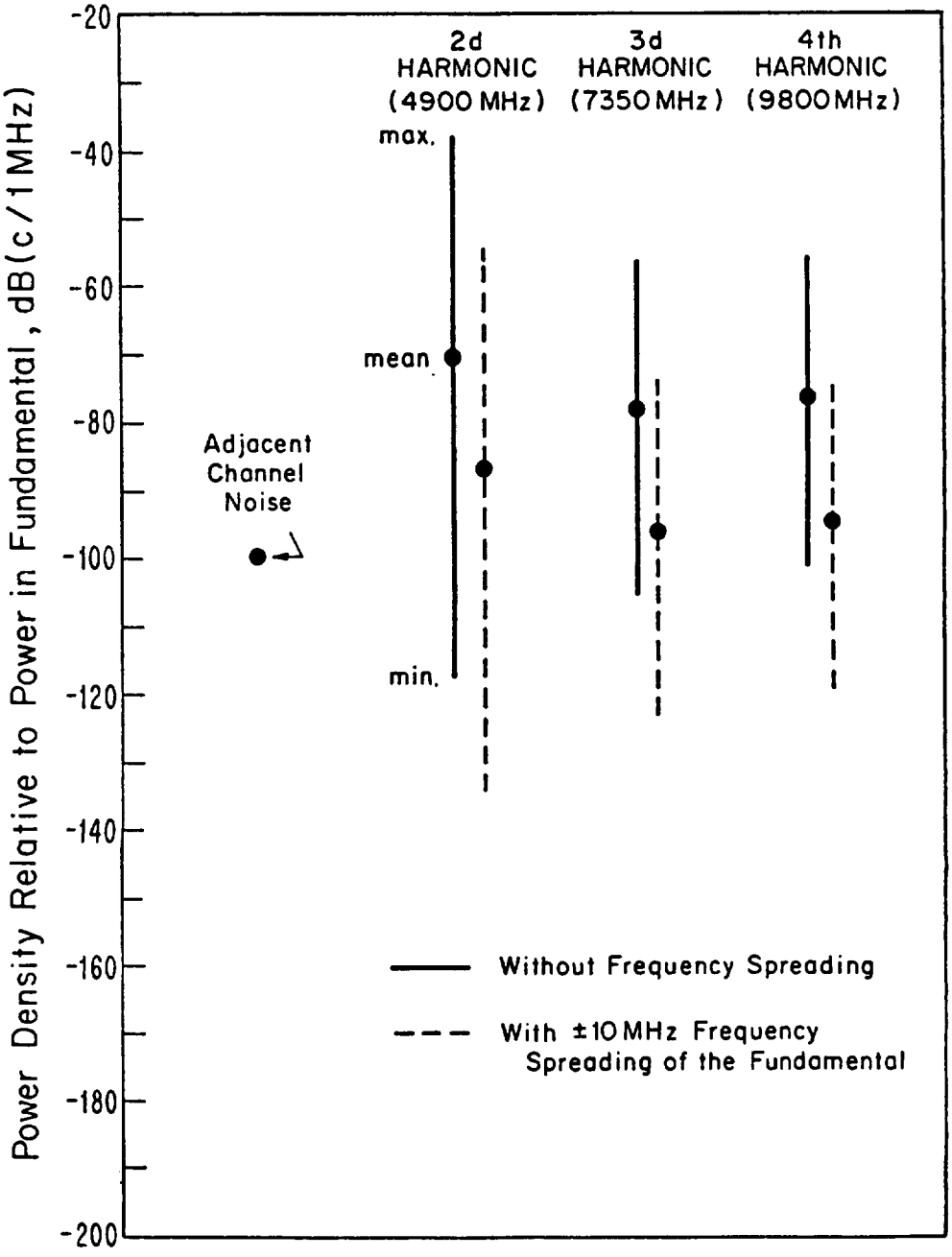

Figure 2. Estimates of interference levels in a 1 MHz bandwidth.

TABLE 3.

Difference between the maximum power coupled into three types of integrated circuits and interference threshold.

LOCATION	7400 NAND GATE	4011 NAND GATE	5474 FLIP FLOP
Center of Rectenna	+ 15.0 dB	+ 18.2 dB	+ 15.3 dB
Edge of Rectenna 5 km from Center	+ 1.3	+ 4.5	+ 1.6
Exclusion Fence 5.7 km from Center	-8.7	-5.4	-8.4
First Sidelobe 9.0 km from Center	- 9.6	-6.4	-9.3
Second Sidelobe 13.0 km from Center	-13.9	-10.7	-13.6
Third Sidelobe 17.0 km from Center	-18.6	-15.4	-18.3