PRE AND POST ANNEALING OF MECHANICAL DAMAGE IN SILICON WAFERS

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ABSTRACT

Shaping operations of silicon, such as sawing, grinding, and lapping introduce micro-cracks and abrasion damage into silicon. The crystallographic nature of such defects in wafer surfaces before and after annealing is discussed. It is shown that dislocations and stacking faults are the annealing product of micro-cracks. Abrasion damage consists of shear loops. Frequently, such shear loops introduce sub-micron cracks due to dislocation pile-ups. Sub-micron cracks lead to stacking faults in the silicon surface during high temperature annealing. The electrical properties of such defects are discussed. It is shown that their presence reduces minority carrier lifetime in silicon. The effectiveness of damage removal techniques on silicon surfaces is also reviewed. Measurements are presented that indicate that silicon dioxide polishing of silicon removes damage with a minimum of damage propagation.

INTRODUCTION

Silicon wafers are produced from cylindrical single crystal ingots through mechanical shaping operations, such as grinding, sawing, lapping and polishing. The semiconductor industry has expanded considerable effort on the subject of producing damage free wafer surfaces. This has lead to numerous studies by many workers dealing with damage removal techniques, depth of damage measurements, crystallographic nature of damage, annealing properties of damage, electrical properties of mechanical damage and others.[1-10] Some of the highlights of such studies are reviewed in this paper.

INFLUENCE OF MECHANICAL DAMAGE ON ELECTRICAL PROPERTIES

Mechanical damage on silicon surfaces has significant influence on minority carrier lifetime and surface recombination velocities of carriers. This is illustrated in Figs. 1a and 1b for minority carrier lifetime. Both figures represent MOS C-t generation lifetime maps of silicon wafers. Figure 1a shows generation lifetime distributions for a "state of the art" silicon dioxide polished wafer. Average lifetime for this wafer is 400 μsec. The results shown in Fig. 1b were obtained by first

lightly abrading half of a polished wafer surface and subsequently removing 10 μm of the abraded surface by chemical etching before MOS processing. The average lifetime in the damaged wafer half is 0.07 μsec as compared to 300 μsec obtained in the undamaged part of the wafer. This 4 order of magnitude decrease in lifetime in the damaged part of the wafer is due to dislocations and stacking faults.[10] Such defects are the annealing product of mechanical damage in silicon.[4,10] This subject is discussed in the next section of this review.

CRYSTALLOGRAPHIC STUDIES OF MECHANICAL DAMAGE

Detailed analytical studies of mechanical damage in silicon wafers are primarily hindered by the complexity of the defect state in the wafer surface encountered after conventional shaping procedures such as sawing and grinding.[4] The problem of damage complexity can be avoided by introducing mechanical damage into crystal surfaces in a controlled manner. This can be done most effectively using Impact Sound Stressing (ISS).[11] ISS of silicon wafers can reproduce the two basic features of mechanical damage in silicon such as micro-cracks and abrasion damage.[4] Using ISS a detailed study of mechanical damage in silicon surfaces was made and the pre- and post-annealing properties of cracks and abrasion on silicon surfaces were determined.[10] Some highlights of these studies are summarized in the following.

PRE-ANNEALING STUDIES OF CRACKS

A micro-crack in a silicon surface causes three different types of lattice distortion: (1) A rotation of both surface parts of the fractured wafer surface around an axis perpendicular to the surface, (2) A rotation of both surface parts of the fractured wafer surface around an axis parallel to the surface and parallel to the crack (bending), (3) Translation of the split crystal parts by a vector R mainly in (011) or (101) type directions for (001) surfaces in (111) or (011) planes (block slip).[10,12]

In general all three effects are present simultaneously. Thus the lattice distortions overlap and produce a rather complicated Moire pattern if observed in the transmission electron microscope (TEM). Simple patterns are seen for cracks lying in cleavage planes. Such Moires consists of pure translational fringes and the crack image looks very much like a stacking fault. This similarity is very striking if "closure" of the crack has taken place. This is always the case for areas close to the crack tip. Examples are given in the micrographs of Figs. 2.

TEM Moire patterns of crack tips can reveal many interesting facts about the crystallographic nature of cracks in silicon. For instance it can be shown that cleavage at room temperature does not introduce dislocations into the silicon because stresses

around the crack tips are not plastically relieved. Consequently, crack tips in silicon represent stress centers which anneal out at high temperature. The annealing behavior of cracks is discussed in the next section.

POST-ANNEALING STUDIES OF CRACKS

Typical strain fields associated with crack tips before annealing are shown in Fig. 3. High temperature annealing of such cracks causes the formation of dislocations outside the crack area. An example is shown in the micrographs of Fig. 4 and reveals dislocation formation around a crack tip after annealing in nitrogen. Similar results are obtained for annealing in oxygen.

The simple equation $\theta = N.b/D$ can be used to estimate the number of dislocations necessary to relieve the strain connected with a crack in the lattice (θ = lattice tilt due to crack, N = number of dislocations, b = Burgers vector of dislocation, D = spacing between dislocations). The lattice tilt θ can be measured using the Kikuchi technique. For a tilt of approximately 0.15 degrees, it is calculated that only 6 dislocations are necessary to relieve the strain field connected with a micro-crack in silicon. This value is in good agreement with the experimental findings (Fig. 4).

Microcracks can be annealed out, specifically, if such splits are located in {111} planes. Assuming that "block slip"[12] governs crack formation it appears plausible that bonding between the silicon atoms in the vicinity of the crack tip is re-established through high temperature relaxation. Thus fairly large crack areas (micron range) can heal and 60° - and 90° - dislocations are the healing product of this process. Sub-micron cracks cause a much smaller displacement between the split crystal parts and stacking fault nucleation may occur directly through rebonding of the silicon atoms if the displacement "R" of the free crystal surfaces is of the right order of magnitude. This is shown very clearly in the TEM - micrograph of Fig. 5 and is an important mechanism for the annealing of abrasion damage as discussed in the next section.

PRE-ANNEALING STUDIES OF ABRASION DAMAGE

Abrasion of silicon surfaces introduces dislocation bands into the crystal. A typical example is given in Fig. 6. Such dislocation bands are composed of dislocation loops and appear in rows oriented along <100>, <110> or <120> directions. However, the intersections of all loops with the (001) surface is always a <110> direction indicating that the loops are located on {111} glide planes.

To understand the annealing properties of such dislocation bands Burgers vector determination of the dislocations were made before annealing. Accordingly, the Burgers vector of the loops is

contained in the (111) or ($\bar{1}\bar{1}1$) plane with Burgers vector (a/2) [011] or (a/2) [101]. Consequently, these dislocations are mixed dislocation loops which lie and expand in the {111} slip planes. Thus the loops are not prismatic dislocations, as generally assumed,[13] but are of the shear type.

POST-ANNEALING STUDIES OF ABRASION

Experimental evidence indicates that annealing of abraded silicon surfaces generates stacking faults (Fig. 7). The most frequently studied nucleation model for stacking faults relies on a dislocation reaction first pointed out by Hirsch[13] and assumes that mechanical damage produces prismatic dislocations which form stacking faults according to the reaction: (a/2) $[1\bar{1}0] \rightarrow (a/3)[1\bar{1}1] + (a/6)[1\bar{1}2]$. However, our measurements indicate that dislocation loops introduced through abrasive damage are shear loops. A shear loop cannot dissociate as required by the Hirsch reaction. Consequently, the generally accepted prismatic loop nucleation mechanism for oxidation induced stacking faults cannot explain stacking fault nucleation.[10]

An additional result from our abrasion studies is the finding that the dislocation bands due to abrasion contain dislocation pile-ups, on neighboring slip planes, which are separated by only 200A. The corresponding dislocation density can be estimated to be 10^{5} [10] $/cm^2$ or higher. Based on the work of Fujita[14], Cottrell[15], and specifically of Abrahams and Ekstrom[16] such dense dislocation pile-ups favor micro-crack formation. Consequently, we must assume that abrasive type of damage produces microcracks.

The contention that microsplits in the silicon surface--caused by dislocation pile-ups -- act as sources for stacking fault generation during oxidation, is supported by experimental evidence (Fig. 8). We have observed many examples of small Moire patterns connected with high density dislocation clusters. Such patterns are only 2000A in size or even smaller[10] and grow into stacking faults during oxidation.

DAMAGE REMOVAL

It is interesting to note that the agreement between differently measured values of saw damage depth published in the literature[2,7] is quite poor, indicating certain difficulties with such measurements primarily related to the different measurement techniques. In this context it is also noteworthy to observe that polishing techniques are generally assumed to be equal in terms of "effectiveness" of damage removal. Actually, large variations in damage removal and damage propagation are characteristic for different polishing techniques. This is discussed in the following.

Three polishing techniques are compared: (1) Chemical polishing using nitric, acetic and hydrofluoric acid mixtures

(fast and slow), (2) Chem-mech cupric ion polishing, (3) Chem-mech silicon dioxide polishing.

The comparison is based on the idea that first mechanical damage is introduced into highly perfect silicon surfaces in a controlled manner. Subsequently, the damage removal effectiveness of a polishing technique is measured as the amount of material necessary to be removed to again obtain a "perfect" surface. The damage is introduced through the technique of Impact Sound Stressing (ISS). The damage removal is monitored through generation lifetime measurements.[10]

The experimental findings that relate the effectiveness of damage removal to the polishing agents are summarized in Fig. 9.

It is evident that the more mechanical acting polishing technique - silicon-dioxide - is the most effective one for damage removal. The least effective polish is the slow chemical etch. This difference in damage removal rate between chemical and mechanical acting agents relates to crack propagation during polishing. Chemical etching requires removal of at least four times the original damage depth as a result of crack propagation during etching. Generation lifetime of the original surface is not recovered through chemical etching.[10]

SUMMARY

Basic properties of mechanical damage in silicon consisting of cracks and abrasion were studied using transmission electron microscopy. The crystallographic structure of mechanical damage was determined before and after high temperature annealing. The main findings include that stresses in silicon around crack tips are not plastically relieved at room temperature and that abrasion at room temperature introduces shear loops into the silicon. It was also found that cracks of micron size can be annealed out, specifically, if cleavage occurs on {111} planes. The healing products of such cracks are 60° and 90° dislocations. Sub-micron cracks transform into stacking faults during annealing. Likewise high concentrations of shear loops due to abrasion were found to anneal into stacking faults. No direct evidence of the stacking fault nucleation process was obtained. However, a one to one correlation between surface areas containing small cracks and stacking faults was made.

Measurements of damage removal on silicon surfaces through chemical-mechanical etching techniques are presented. It is shown that silicon dioxide repolishes damaged silicon surfaces most effectively.

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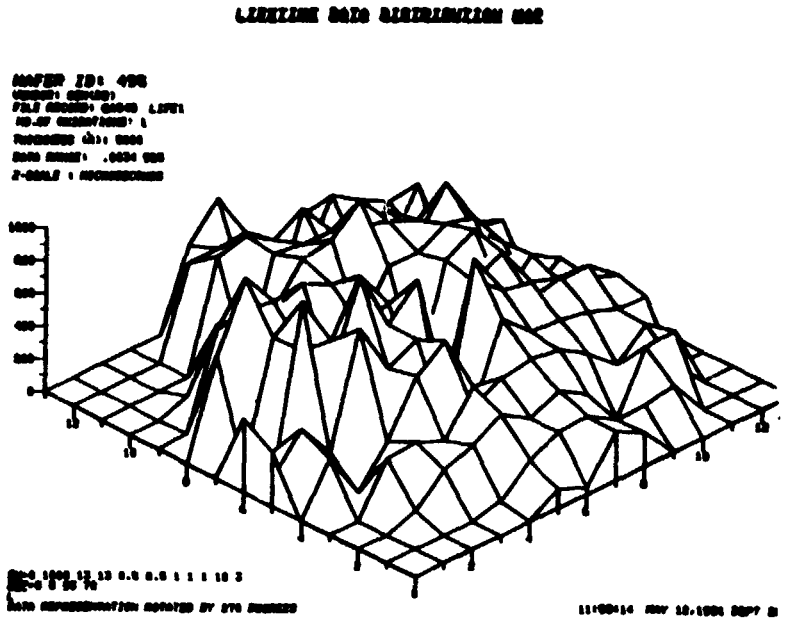

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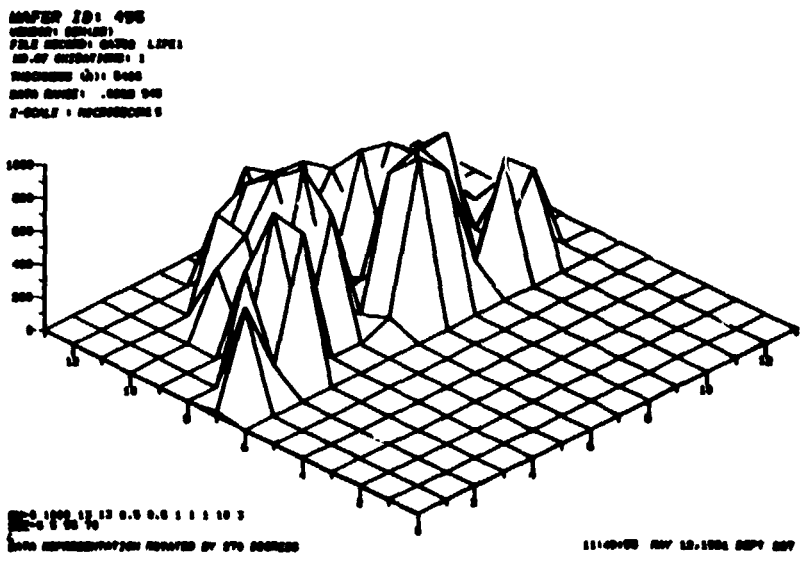

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Fig. 1. Generation lifetime maps of silicon wafers. (a) Standard wafer after silicon dioxide polishing. (b) Same as (a) only one half of wafer surface contains residual mechanical damage. Note decrease of lifetime by 4 orders of magnitude in this part.

Fig. 2 Transmission electron micrograph of crack in silicon.

Fig. 3 Transmission electron micrograph of strain field associated with crack in silicon.

Fig. 4. Transmission electron micrograph of annealed crack showing dislocations

Fig. 5. Transmission electron micrograph of stacking fault nucleation through annealing of microcrack.

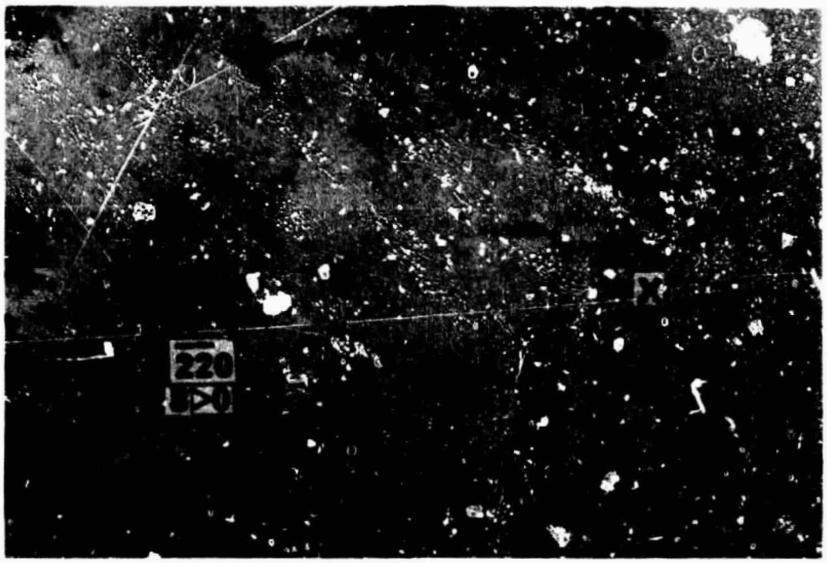

Fig. 6 Transmission electron micrograph of abrasion damage showing dislocation shear loops.

Fig. 7 Transmission electron micrograph of annealed abrasion damage showing stacking faults.

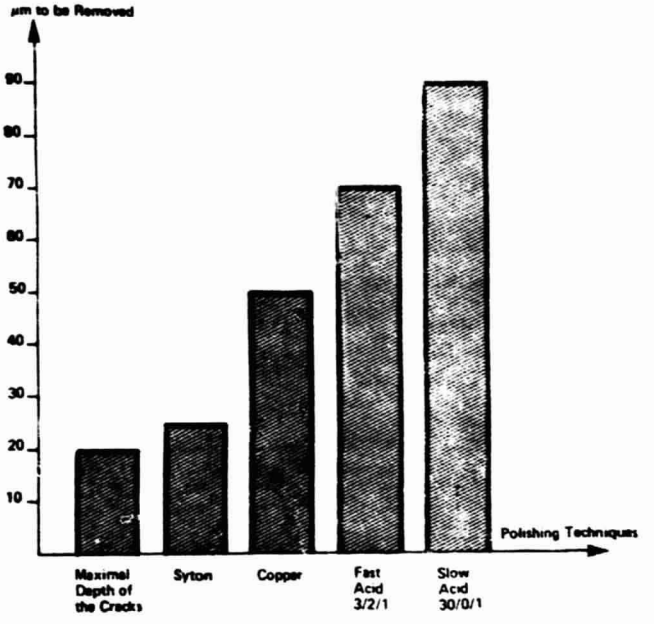

Fig. 8 Summary of damage removal effectiveness of different polishing techniques.

DISCUSSION:

KOLIWAD: One of the objectives we had in the work we did three years ago on the nature and the effect of damage on solar-cell efficiencies in the multiblade-sliced wafers was to verify whether, in fact, that damage has microsplits, and secondly of course to verify the effect of damage itself on efficiency. We did not look extensively into the existence of microcracks, but one of the ways we tried to identify them was doing exactly what he showed in the last viewgraph. We did remove the damage by Syton polish as well as by chemical etching. One of our conclusions was that for certain removal of damage, there was no difference at all on the efficiency of the cells from the polished wafers and the efficiency of the cells from the chemically removed wafers. So what we concluded was that maybe there were no microsplits in the multiblade-sliced wafers and of course depth of damage itself had an effect. We also concluded from the study that the efficiency increased up to the point where we had removed all damage, and then remained stable after that. So I would like to know if you have any thoughts on whether the simulation by ISS is general or is particular for the plunge cutting kind of technique?

SCHWUTTKE: I think the ISS allows you to do some real basic studies. It does not relate to any particular slicing or sawing technique. It allows me to put abrasion in a controlled manner into a surface, and I can do this before processing. It really doesn't matter what kind of device you use. It also allows me to put splits into the silicon surface, and since we know the annealing properties of this type of damage, you can make a prediction of what effect it might have on your device characteristics. I'd like to address what you said in your comment. When you did these measurements, you did not find any influence on solar-cell efficiency. I believe as long as you are satisfied with a 10% to 12% solar-cell efficiency, you are not addressing the key problem. If you are after a better than 15% solar cell, then the solar cell is much more lifetime-dependent. At higher efficiencies, this will be very important.

KOLIWAD: Of course we are comparing the wafers where the damage was removed first chemically and then polished. But the question I had was: are we right in assuming, since our efficiency did not change with respect to how we removed the damage, that there are no microsplits?

SCHWUTTKE: Multiblade slicing I would say, if done properly, and in a controlled way, is a gentler technique than ID slicing. Based on this I would say you have a better chance to end up with a good surface. A wire saw is basically a very gentle technique. I get concerned if I listen to comments like the last two days, that everybody puts his effort into speeding up multiblade cutting, multi-wire cutting, many miles per hour faster. So actually, you may approach an out-of-control process again, and then you will have other problems.

ROUTBORT: Does the formation of these shear loops depend on the dopant level of the silicon?

SCHWUTTKE: Not so much. We have investigated a wide range of doping, n-type and p-type, and in all cases, we find similar damage. Very much alike.

ROUTBORT: You know, these abrasion experiments are really nice because in the old days, in the late '50s, Hausner and Alexander deformed silicon at high temperatures, and they found precisely that the deformation characteristics depend on the surface finish at room temperature, because they are, of course, the source of all the dislocations.

SCHWUTTKE: I think it's a very neat way of studying damage in silicon. The intent of our experiments was to simulate, to get a handle on residual damage. We have two damage modes if you address ID saw damage. One is a uniform damage, which indicates that you have the controlled ID slicing process. Now if you find superimposed a nonhomogeneous damage mode, then you know that the process is out of control, and you are dealing with blade vibrations. The blade vibrations we found are highly undesirable because they are responsible for that tremendous variation in damage depths. This is based on cracking of the material. If you prepare your wafer surface, you remove the original saw damage, you are left with such splits. Originally you knew the semiconductor industry would deliver slices, and you had split concentration of 10^6 per square centimeter. It's unbelievable. Subsequently, we learned how to do a better job. Out-of-plane vibration is something that can be eliminated. Then you should be left with a very uniform damage depth, and so you are in a much better shape from the beginning. And this is how I interpret Kris Koliwad's experiment. He had a much better-controlled slicing process.

WOLF: I have two other questions . First, we heard from Larry Dyer earlier this morning about the split propagation in the (100) cutting direction. Would we be better off if we would be cutting the (111) direction, where the crack propagation is more in line with the saw normal force? Would we get less penetration sideways off these microcracks? The second part is, if we go to ductile deformation rather than to brittle erosion, where we deal more with plastic deformation, would we also get less damage in the wafers?

SCHWUTTKE: I think the application of lubricants of the type discussed in the first two papers on Monday is an important aspect of the slicing. Particularly if you want to go faster. These things will become very important. Orientation dependence in terms of hardness: silicon is a non-isotropic material, and is softest in the (111) plane. There are tradeoffs from that point of view.

DYER: Both your paper and the one preceding are fundamental to this field. They help us understand how to cut the silicon; everybody should appreciate that. From one of the statements of Jules (Routbort) and statements of yours, a person could get the impression that the plastic deformation or the formation of the shear loops is beneficial to removing silicon. In my view, that might be an incorrect way of looking at it, i.e., if we could prevent that, it would probably be better. Thus, we want the direct application of the stress to form the cracks, and all that any plastic deformation does is to absorb some of the energy temporarily and make it necessary to build up more stresses before the thing finally does the cracking that we want. Any plasticity will actually hurt.

"Would it better to have ductile behavior?" I doubt it very much. I think we want it to stay brittle.

SCHWUTTKE: You will have a trade-off. If you stay too brittle and you go too fast, you knock the hell out of silicon and that is no good either. If you want to go fast, you will be forced to use lubricants.

DYER: To me, if you try to cut fast through something and you try to make it ductile, you get through it all right, but the thing gets bogged down by grabbing onto the sides.

SCHWUTTKE: I'm not so much concerned about the ID saw. I think the guys have made a lot of progress in ID slicing. If I look at the equipment we threw out several years ago, and take a look at the equipment we are using today, it's like day and night. You probably find the same thing. You never would make a 100-millimeter slice and show your lifetime distribution is an average of 400. It's not exactly a plateau, but it's coming close to that. I think that is progress in technology. That was unthinkable just a few years ago. So slicing and combined chem-mech polishing has made a tremendous leap forward. Using these two techniques, the first a very tough one, the second the polishing technique, we can reestablish and bring back a basically perfect silicon surface. It's amazing that this can be done.

DYER: I make a distinction between the beneficial nature of having it brittle and having the very many, many cracks, very small in depth, and the type of brittle you're talking about, where you have big cracks going all the way through something. So we can actually use the brittle nature of it to our benefit.

SCHWUTTKE: Deformation at room temperature of brittle materials like silicon is advantageous because we were able to develop polishing techniques that will remove this type of damage. Your concern is if we go now to plastic deformation at room temperature, by the use of lubricants, we may lose that particular benefit. We may not be able to bring back a perfect surface, because the plastic deformation process will be out of control. If it is a brittle material, we seem to be able to control the plastic deformation to the contact point, and that is where the advantage is right now.

DYER: You show this difference between polishing by removal of the damage layer with the acid and with the polisher. Have you any idea why that is? Why that tremendous difference? Can you give us some physical insight?

SCHWUTTKE: Yes. I think it relates to the chemical potential around the crack tip. And if you use chemistry, then you lower the chemical potential and the crack continues to run ahead of the etching front. If you do a more mechanical polishing you don't encounter this problem; you don't propagate the crack. So Syton is just fantastic. Syton seems to be able to recover the crystal without crack propagations. We are just lucky.

UNO: We have the same problem. We do our chemical etching. Now what do you consider slow and fast? Is 25 microns per minute fast or slow?

SCHWUTTKE: That is fast. Slow, I'm talking about 2 microns per minute.

SCHWUTTKE: By the way, Peter (Iles), looking at your picture yesterday: you indicated that you had an uneven surface where you were cutting chemically through the water. You indicated that you thought that this may be related to internal defects present in the material. It is my experience, and I have seen such surfaces as you showed, it is due to bubble formation. And you also indicated that you have violent action of hydrogen. All that happens is that the hydrogen seems to form bubbles on the internal surfaces, and that's where you get your uneven etching.

CHEN: You have a beautiful TEM picture of the crack on the sample. Can you address, a little bit, the TEM sample preparation--what are the thicknesses of the samples you prepared?

SCHWUTTKE: We are fortunate, we have a 200 kilowatt electron microscope, so I can penetrate more silicon than with a 100 kV. It makes it simpler to display these cracks.

CHEN: Do you have any other simple method in use for crack examination?

SCHWUTTKE: I have shown you some pictures, but this is really tedious work, as the SEM pictures I showed you where those splits opened up. They are very tedious. It's very tough. The best way to find cracks is really the transmission electron microscope. Because you have two crystal faces, no bonding between, so you just chase the thing down till you see a Moire pattern, and you know you have a crack. To find these things--it took us weeks and months the first time, when we attacked the problem, to see this tiny Moire pattern--but once you know what to look for they suddenly pop out all over the place. As I said, we even come up with a million per square centimeter, but we never could find any before that. It's really a matter of knowing what to look for, like everything else, and then you suddenly see it.