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STATUS OF SEMI'S SOLAR-GRADE SUBSTRATE STANDARDS

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The primary purpose of the Semiconductor Equipment and Materials Institute, Inc. (SEMI), was to manage a local equipment and materials trade show that would attract Santa Clara County's semiconductor companies. Since its formation in 1970, however, SEMI has grown into an international organization providing multiple services to its members. It is guided by industry committees staffed by member-company representatives working to develop services beneficial to all.

The first step of SEMI's evolution from a trade-show organization into a full-service trade association occurred in 1973, with the formation of a Standards Committee. The committee explored the possibilities of an institute-organized industry effort to standarize specifications for materials, equipment and processes used in semiconductor manufacturing. The first Book of SEMI Standards (BOSS) was published in 1978.

The original Standards Committee evolved into seven major divisions:

(1) Chemical Division
(2) Equipment Division
(3) Packaging Division
(4) Photomask Division
(5) European Liaison
(6) Government Liaison
(7) Materials Division

Because participants in the wafering workshop are interested in solar-grade substrate standards, a breakdown of the areas of interest to that subcommittee in the Materials Division is given:

(1) Silicon Wafer
(2) Silicon on Sapphire
(3) Epitaxial Substrate
(4) Gadolinium Gallium Garnet Substrate
(5) Solar-Grade Substrates

The subcommittee approved the General Requirements document on the solar-grade substrate standards for balloting by industry on May 18, 1981. It now stands as an addition to the BOSS. This standard specification covers requirements for silicon slices (wafers) used in solar cell manufacture. Dimensional characteristics and crystal-structure defects are the only standardized

properties set forth. Three classes of material are defined: polycrystalline, substantially monocrystalline and monocrystalline. These are defined as:

(1) Polycrystalline: does not meet requirements of another class. Minimum grain size of N times the slice thickness.
(2) Substantially Monocrystalline: not more than X grain boundaries per slice or Y mm total length of grain boundaries, or having no crystallites smaller than 0.Z of the width of the slice.*
(3) Monocrystalline: free of grain boundaries.

A complete purchase specification requires that additional physical properties be defined. These properties are listed with test methods suitable for determining their magnitude.

The Standards format consists of two specific documents: the first describes the general requirements of the specification that is applicable to all of the SEMI Standards. The second, which will be the SEMI Standard specification for that particular substrate, will describe the specific dimensional characteristics and crystalline structure.

A breakdown of the specific paragraphs of the general requirements specification and a statement of content follows:

(1) Preface: contains the general information as given above.
(2) Applicable Documents: the applicable ASTM Standards and DIN Standards that are required to measure specific properties, and statistical documents for test sampling, are listed.
(3) Definitions: the required definitions are stated specifically (e.g., define a "lot").
(4) Ordering Information.
(5) Dimensions and Permissible Variations.
(6) Materials and Manufacture: defines the structural class or growth method.
(7) Physical Parameters.
(8) Sampling.
(9) Test Methods.
(10) Certification.
(11) Packaging and Marking.

A specific example of a proposed slice specification, in this case for a square slice, is given in Table 1 and Figure 1.

In conclusion, the general requirements for a SEMI Specification for solar-grade silicon slices has been approved for balloting by industry. The results are expected to be published at the next meeting to be held in September. The definition of specific dimension and tolerance requirements for individual slices is still in committee.

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*Numerical Values of N, X, Y and Z are to be established in committee.

Table 1. Example of Proposed Square Cell Specification

I. Crystallographic	II Electrical	III Mechanical*		IV Visual
No limit for dislocation EPD, slip, limeage, or swirl Surface orientation on <100> ± 3° Crystal orientation to growth lines 45° ± 8°	Boron dopant 0.5 to 2.0 ohm-cm.	Cell width, Cell diagonal, Flat length, Adjacent sides, Thickness, TTV, Warp,	100 ± 0.5 mm 125 ± 3 mm <74.9 mm 90° ± 0°20' .37 ± 0.10 mm 50 μm maximum 60 μm maximum	Front and back surfaces, sawn. Saw marks, none on one side. Roughness, 1 micrometer RMS maximum Cracks, none. Chips, conchoidal, up to 6 each with a maximum length or radial penetration of 1.6 mm. Chips with both dimensions less than 0.25 mm are exempt. No conchoidal chips are permitted. No fracture or pointed apex chips of any size. Saw exit defects permitted on 5 percent of cells. No foreign matter visible to unaided eye permitted.

*See Figure 1.

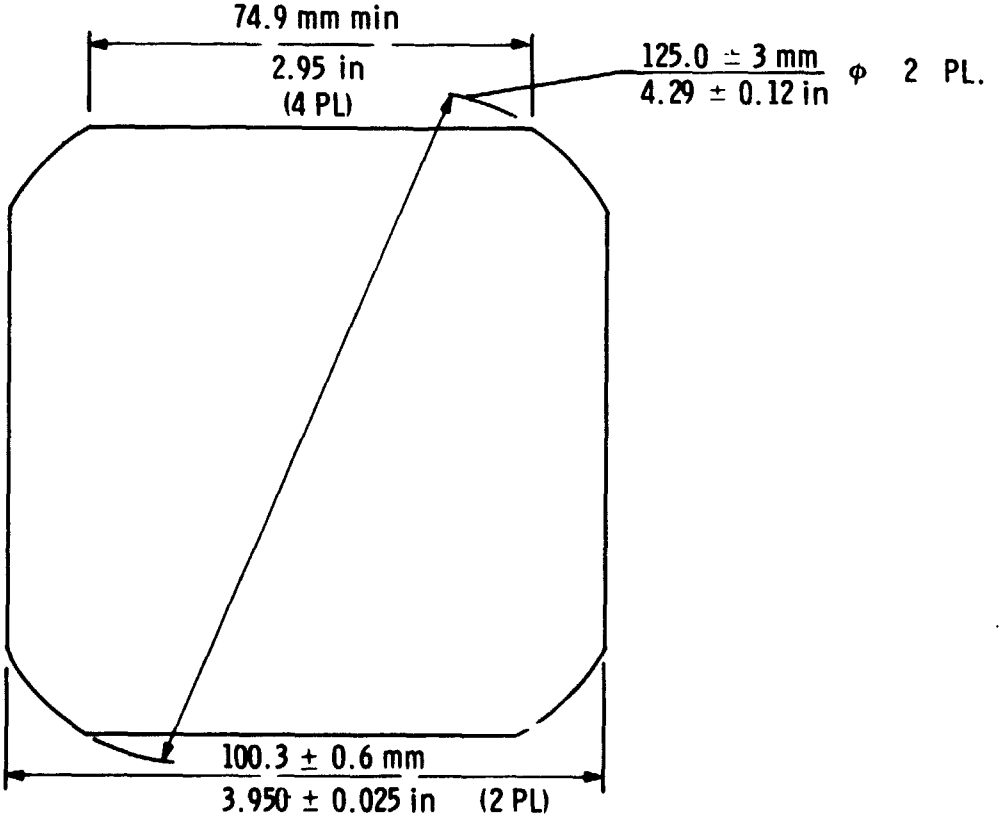

Fig. 1. Example of Proposed Square Cell Specification

DISCUSSION:

GALLAGHER: Remember that this is a strictly voluntary type participation and we definitely need more participation than we have now. There are usually three meetings a year. San Mateo, Boston, and the third one is usually held in Anaheim, in conjunction with the Nepcon show.

ILES: I should mention for the people in wafering, as a means of self-defense, you should keep an eye on these things. Once these specs get slipped in on you, you'll find they haven't heard your input and they don't know that some things are very difficult to do altogether.

It was interesting that many people came thinking they were going to hear all sorts of wonderful numbers on slicing speeds and wafers you can see through and things like that. It was very interesting that we were guided gradually and rather expertly into the microscopic aspects, and people may be going away thinking more about what's really happening in the process rather than cursing about the machine that rocks or bumps too much.

I think we even strayed into philosophy last night. I was listening to Tom (Lewandowski) from STC, and he was talking about the problem if you had 10 machines and there's a noise on one but no operator. Sounded like that old business about the tree falling in the forest and whether there's really a noise or not, depending on whether there's a human ear to hear it. I guess we can be satisfied that we can say "if we see a lot of chips on the floor, then we can tell the philosophers something happened." I think the ID people go away feeling that "Thank God that the blade, saw, wire people have some problems" and vice versa, so I think we've at least shared our problems and everyone feels a little better to know that the other guy has a different set of insurmountable problems, mainly based on low cost. I had a comment from someone who'd not been to any of the PIMs or any of the JPL meetings. He said he particularly appreciated the fact that there were so many disciplines presented here. I think the original fear of the steering committee was that we might find that some people would sit around bored to death while other people talked about stuff that they'd been hearing a lot of, but I think it is very good to have different viewpoints on all the questions. I'm sure JPL is going to focus all this work, and upgrade all this wafering thing, and I'll just finish by saying the success of this conference can be traced very accurately by just watching how well the ribbons do. If the ribbon people take over from us, then we haven't done our job in wafering.