

# Mark IVA Microprocessor Support

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*This report discusses the requirements and plans for the maintenance support of microprocessor-based controllers in the Deep Space Network Mark IVA System. Additional new interfaces and 16-bit processors have introduced problems not present in the Mark III System. This report also points out the need for continuous training of maintenance personnel to maintain a level of expertise consistent with the sophistication of the required tools.*

## I. Introduction

The Mark IVA System makes extensive use of microprocessor-based controllers. Much of the equipment is in areas remote to the complex control room environment and difficult to access, e.g., high places on antennas (see Figs. 1 and 2). These subsystem controllers will require lightweight, highly portable test equipment for maintenance. Easily accessible controllers within the complex control room may be tested with more sophisticated analyzers. This equipment will be resident in a rollaround maintenance cart, thus providing greater flexibility and in-depth testing.

While technological advances have increased data throughput, these same advances have introduced new maintenance problems, namely, poor visibility into the system. Test equipment, such as data analyzers and in-circuit emulators, will be available to help solve these problems.

## II. Maintenance Philosophy

The Mark III microprocessor controllers implemented in the Deep Space Network were not compatible with existing

automatic test equipment. This and other factors forced a maintenance practice that often resulted in diagnosing a problem to the chip level in an operations environment. This approach has been generally successful primarily due to the test equipment supplied and the skill level of the technicians involved.

The availability requirements placed on the Mark IVA System require conformance to the DSN maintenance philosophy which establishes boundaries for various levels of maintenance. Briefly stated, Level 1 is "failure detection"; Level 2 is "failure identification and replacement (to the least replaceable element)"; Level 3 is "off-line repair" (normally depot repair). These boundaries are not to be considered "law"; emergency situations will dictate Level 3 repair at a Level 2 location. Faced with this possibility, capability must be provided in a maintenance and operations environment to perform Level 3 repair.

## III. Mark III Support

The backbone of the current microprocessor support for 8-bit processors includes the Micro/Sys DS22 and the Millen-

nium Microsystem Analyzer, Ref. 1. The DS22 uses the CPM operating system and has been used for development of diagnostics for the Mark III System controllers. The DS22 interfaces with the Millennium Microsystem Analyzer (an in-circuit emulator) and the Data I/O System 19 PROM (Programmable Read Only Memory) programmer; in addition, it can be connected to a modem for communication with other computers (Fig. 3). The unit has been used extensively for on-the-job-training of on-site personnel; this has been a valuable contribution. Because of its portability and flexibility, the Millennium analyzer will continue to be used in the Mark IVA era. The DS22 will continue to support the Millennium for diagnostic development.

No field support presently exists for 16-bit processors. The only support for 16-bit processors (the digitally controlled oscillator is the only one in the Mark III System) has been from the Development Engineering Group. This requires returning the boards to engineering for repair in a prototype mockup.

#### **IV. Requirements for Mark IVA Support**

With the advent of 16-bit microprocessors in the network it is obvious that additional requirements beyond the capabilities of the DS22 and the Millennium Microsystem Analyzer are needed. Only recently have portable testers for 16-bit microprocessors become available from industry. Various instruments are currently being investigated for their suitability to the Mark IVA requirements for supporting Level 2 and Level 3 maintenance (see Fig. 4). Level 3 requirements include complete software compatibility, with the development system used to develop the controllers, thus eliminating situations that require lengthy workaround solutions. The prominent development system used at JPL is the INTEL Microprocessor Development System. To satisfy future requirements an INTEL Development System and in-circuit emulation for 16-bit processors will be needed at each complex.

#### **V. Test Equipment Requirements**

The following paragraphs provide a review of the test equipment requirements for supporting microprocessor maintenance in the Mark IVA System.

- (1) The 8-bit processors are adequately supported by the Millennium Microsystem Analyzer. Several 16-bit instruments are being investigated for support of the INTEL 8086 microprocessor. A major consideration for Level 2 maintenance is portability.

- (2) The requirement for conventional instruments to support time domain analysis, voltage, and continuity measurements still exists. This would include oscilloscopes, counters, meters, etc.
- (3) Logic analyzers will be required for detailed data domain analysis. Bus adapters are being considered for these instruments to preclude the problem of connecting many probes to the unit under test.
- (4) In-circuit emulators will continue to be used because they essentially provide front panel controls for the unit under test. In addition, these instruments are invaluable for providing digital signature analysis.

### **VI. Digital Interface Testing**

#### **A. General-Purpose Interface Bus**

In the Mark IVA System all of the recently supplied instrumentation have as an interface the IEEE 488 Bus. A planned tester for this interface is the Racal-Dana GPIB-488 analyzer, which includes the following features: (1) Passive Mode, displays the bus activity in real-time; (2) Trace Mode, captures data for later display and analysis; (3) Single Step Mode, allows bus transactions to be single stepped or stopped.

#### **B. Serial Interface**

The standard serial interface used is RS232C. This interface is prevalent wherever serial data is being transferred. An excellent tester for this interface is the "Model 60 EIA interface monitor and breakout panel," manufactured by International Data Sciences, Inc. This device is equipped with switches for breaking any line and jumpers for altering the signal paths. Light emitting diodes are used to display the status of each line.

#### **C. JPL Standard Interface**

The JPL standard interface (sometimes called the 15-line interface) was used extensively in the Mark III System and will be used in the Mark IVA. A switch box and LED (light emitting diode) display is used to test this interface. To provide rapid fault isolation on this bus, a more sophisticated tester will be provided as part of the rollaround cart.

#### **D. Local Area Network**

The DSN version of Ethernet is the Local Area Network used throughout the Signal Processing Center of the Mark IVA System. Because of the Ethernet bus arbitration and bit rates, the testing of this interface poses special problems. An

Ethernet interface will be provided on the rollaround cart and software supplied to verify local operation.

## VII. Analog Interface Testing

Means must be provided to assure the integrity of the analog signal processing associated with the subsystem controllers. In some cases it may be possible to loopback signals between the input and output, thus allowing an internal diagnostic to verify proper operation, or it may be possible to test an internal reference, as in the field interface modules (FIM) (Refs 2 and 3). If proper operation is not verified by this approach, then precision voltage source and measurement instruments must be available.

Pursuant to solving this problem, analog signature analysis will be investigated and a determination made as to its practicality in the Mark IVA environment.

## VIII. Software Requirements

Diagnostics are an indispensable aspect of fault finding in a microprocessor-based controller. Capability for developing diagnostics for both 8- and 16-bit processors must be at each complex or depot repair facility.

Once it has been established that the kernel of the controller is operational, various levels of diagnostics may be invoked. These diagnostics will be available as resident in the UUT, as PROM, as DISK and as TAPE.

- (1) Resident diagnostics will be located in the "Unit Under Test" (UUT). These diagnostics should point to the defective "Lowest Replaceable Element" (LRE), such as a module. It is expected that these diagnostics will isolate the fault in the majority of the failures (Ref. 2).
- (2) Nonresident diagnostics are provided as "Programmable Read Only Memory" (PROM) for use either in

the UUT or the in-circuit emulator (ICE). These diagnostics would be used for special testing of a particular logic element or toggling of data at a specific node for oscilloscope observation.

- (3) Diagnostics will be provided on disk for downloading either into the UUT or the in-circuit emulator tester.
- (4) Diagnostics will be provided on tape for use in the Fluke Troubleshooter (in-circuit emulator).

## IX. Training

Based on DSN maintenance experience the technicians are required to (1) know the functions of the LSI elements, (2) know the logic of the UUT, (3) be able to operate the equipment to assist in maintenance, and (4) be familiar with the hardware and software documentation.

Technician proficiency (relative to training) will affect the required sparing of LREs. If low skill levels exist (for Level 2 maintenance), more spares will be required because more non-defective boards will end up in the repair cycle (increased board float). This complicates testing in the depot environment because all returned boards must be assumed to be defective. The final result is increased operating costs.

For efficient troubleshooting, a thorough knowledge of the instrumentation used in microprocessor fault finding is absolutely essential. Special courses should be developed to raise the level of expertise in this area.

## X. Conclusion

An appropriate maintenance program can be developed to provide rapid fault isolation in the field and repair in the depot of Mark IVA controllers if state-of-the-art analyzers, test equipment and adequate training are provided as outlined in this article.

## References

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2. Baher, F., "Field Interface Module for Antenna Control Assembly," *TDA Progress Report 42-69*, Jet Propulsion Laboratory, Pasadena, Calif., June 15, 1982
3. Valtier, H., "Field Interface Module Software Description," *TDA Progress Report 42-69*, Jet Propulsion Laboratory, Pasadena, Calif., June 15, 1982

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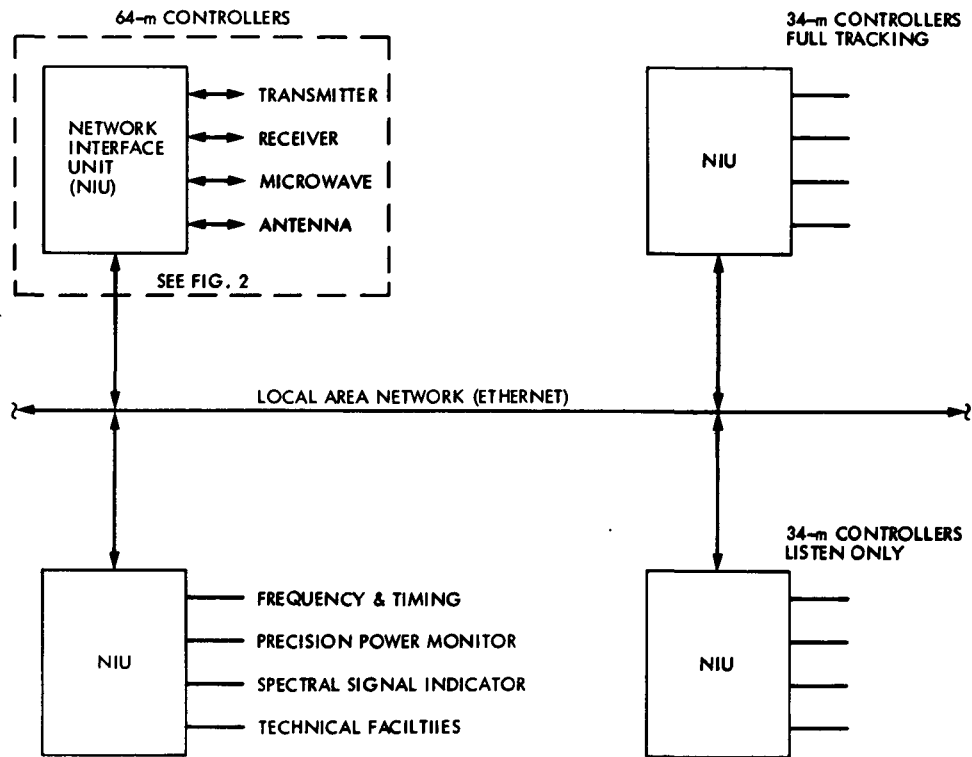


Fig. 1. Mark IVA controller network

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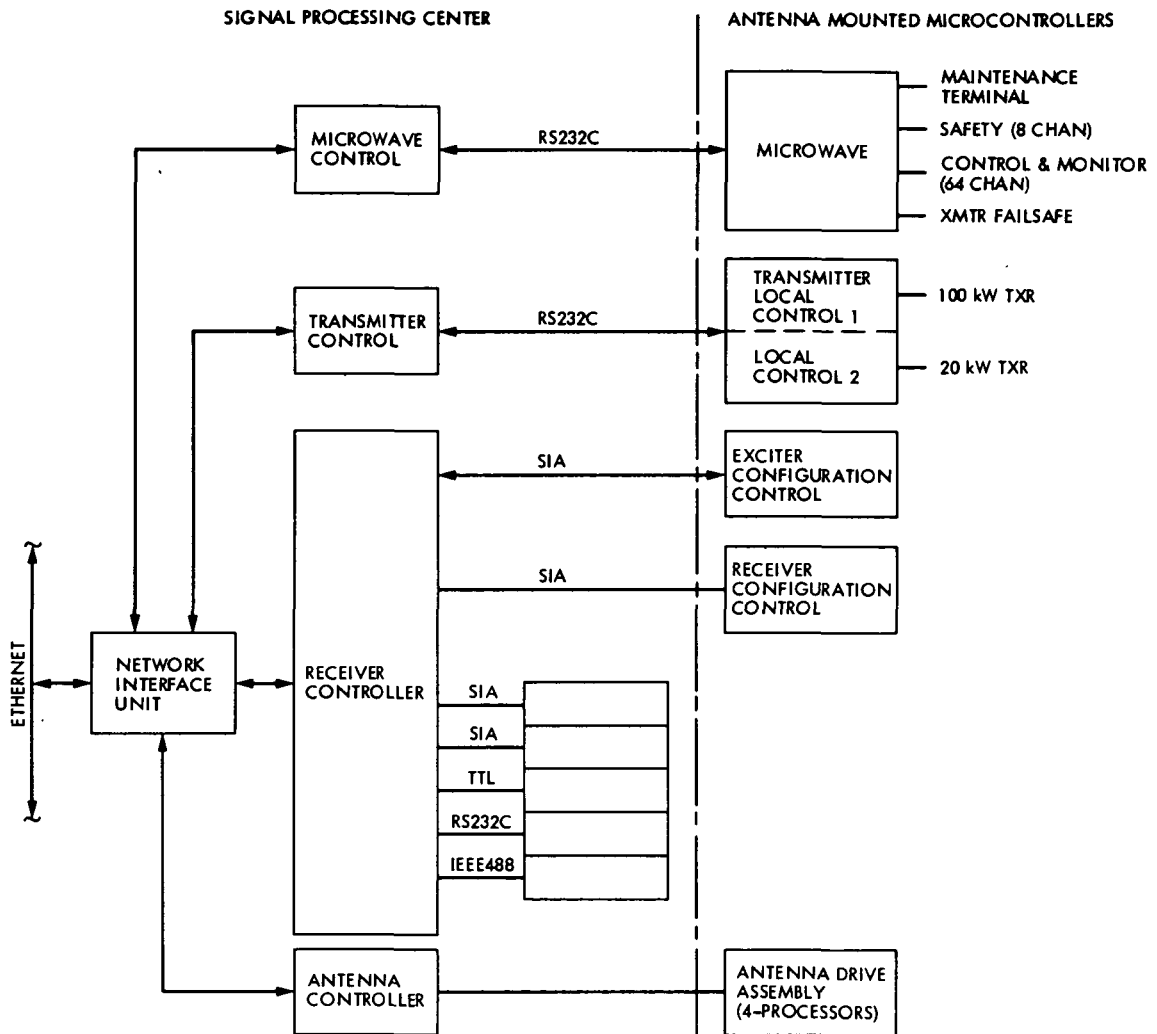


Fig. 2. Microcomputer controller locations

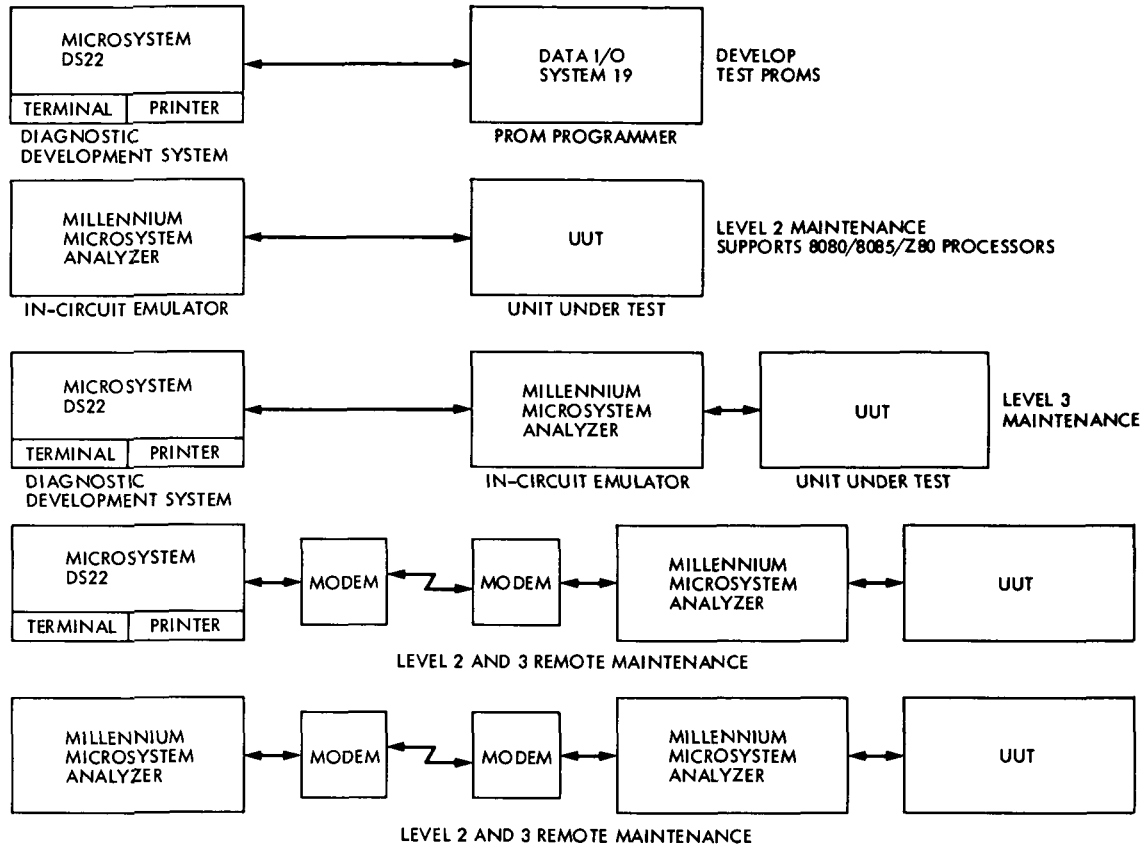


Fig. 3. Mark III 8-bit microprocessor maintenance support equipment

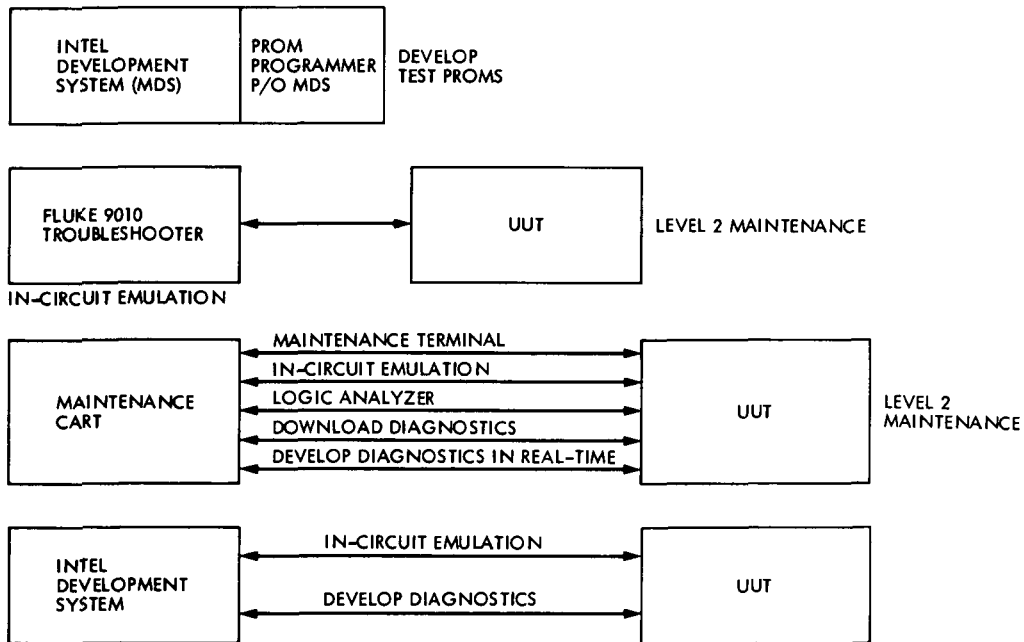


Fig. 4. Mark IVA 16-bit microcomputer maintenance support