LARGE AREA SPACE SOLAR CELL ASSEMBLIES*

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SUMMARY

Development of a large area space solar cell assembly is presented. The assembly consists of an ion implanted silicon cell and glass cover. The important attributes of fabrication are (1) use of a back surface field which is compatible with a back surface reflector, and (2) integration of coverglass application and cell fabrication.

INTRODUCTION

The economic constraints on future large space power systems will require a reduction in cell cost without compromise of cell quality. Certainly innovative cell fabrication techniques are necessary for achievement of this reduction. A further reduction may be possible with the use of low-cost terrestrial solar cell technology (ref. 1).

This paper describes the ongoing development of a low-cost large area (34.3 cm^2) n^+pp^+ solar cell assembly based on ion implantation. Whereas the cost of ion implantation is considered to be a disadvantage at current production levels, future large scale production will require an automated, effluentless, high throughput process. The development of ion implantation anticipates this need. The technical features of ion implantation and its development for terrestrial purposes are discussed in references 2 and 3. Application of the technology to space solar cell fabrication has a particular advantage arising from the ease with which back surface reflectors can be formed on the implanted back surface (ref. 4). This will be discussed more fully in the next section.

An important innovation in cell encapsulation has also been developed. In this new technique, the coverglass is applied before the cell is sawed to final size. The coverglass and cell are then sawed as a unit. In this way, the cost of the coverglass is reduced, since the tolerance on glass size is relaxed, and costly coverglass/cell alignment procedures are eliminated.

CELL DEVELOPMENT

All cell development was based on 2 ohm-cm p-type (100) silicon, with thickness of 250 μm and diameter 7.6 cm. No AR coatings were used during cell development.

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Back Surface Implantation

The implantation of $^{27}Al^+$, $^{11}B^+$ and $^{70}Ga^+$ ions was investigated for $p\text{-}p^+$ BSF formation. Implant and anneal parameters are given in Table 1. After this sequence, front junctions were formed by phosphorus implantation (10 keV, 2.5×10^{15} ions/cm^2) and annealed with a three-step anneal (ref. 3).

Figure 1 shows the resulting doping profiles obtained by spreading resistance analysis. The anomalous Al profile is not understood; however, the B and Ga have the abrupt profile characteristic of the implantation process. Boron yields the highest activation. Table 2 shows the measured cell performance under simulated AMO insolation. Also shown in the table are results obtained without BSF formation. These cells had a slightly different front junction anneal and a different back contact, but were fabricated from the same starting material and are included here to indicate the performance achievable without a back implant. Cells with implanted backs have slightly better FF; this is attributed to an improved electrical back contact. We infer from this data that the Al and Ga implants are not effective in providing BSF enhancement of voltage and current, even though the doping varies over two orders of magnitude at the $p\text{-}p^+$ junction.

One of the major advantages of using ion implantation for back surface field formation is that implantation leaves the physical appearance of the surface unchanged. Thus, a wafer with a polished back can be used for back surface reflector (BSR) formation, without repolishing of the implanted surface. This should be contrasted with Al-paste processes, which require extensive repolishing after BSF formation.

A BSR was formed on surfaces which were boron-implanted as described above. The BSR consisted of evaporated Al-Ti-Pd-Ag and no repolishing was used prior to evaporation. The polished fronts of the samples were AR coated with TiO_2 but had neither front metallization nor front junctions. Table 3 shows the measured values of thermal alpha (courtesy of H. Curtis of NASA-LeRC) for four samples. All samples had thermal alpha values less than 0.70. It can be seen from these data that (1) contact sintering has no measurable effect on thermal alpha, and (2) boron implantation increases thermal alpha slightly.

Emitter Development

Various phosphorus and arsenic implantations were studied in order to achieve very shallow (≤ 0.2 μm) highly doped n^+ layers. Refinements such as oxide passivation and junction tailoring (ref. 5) were not pursued at this stage of the development.

Spreading resistance profiles for three different emitters are shown in Fig. 2. The ion implantation and anneal parameters are listed in Table 4. Also listed are the measured AMO performance data of test cells fabricated with the indicated emitters. Each test cell had a boron-implanted BSF and Ti-Pd-Ag metallization. No antireflection coating was used.

The first two entries in Table 4 compare direct implantation of phosphorus to phosphorus implanted in a surface which is first rendered amorphous by silicon implantation. This "pre-implantation" was investigated because it offers complete elimination of channeling, and should also yield better epitaxial regrowth during the anneal, since the surface layer has no polycrystalline features (ref. 6).

As is evident in Figure 2, this pre-implantation does result in reduced junction depth; however, the Voc of these cells is much lower than that of the directly implanted phosphorus. Since the dark logI-V curves of the predamaged cells show a small increase in saturation current with no change in n-factor, we attribute the reduced Voc to an increase in emitter dark current resulting from a decrease in emitter diffusion length. This decrease of emitter diffusion length is attributed to unsatisfactory annealing of the implantation damage.

We have also examined arsenic implantation and very shallow junctions have been obtained as indicated in Figure 2. Spectral response measurements indicate that the blue response is enhanced, but that the red response is lower than the phosphorus-implanted cells. Various anneal cycles were investigated to determine whether the minority carrier lifetime had been compromised by the one-step anneal, but no improvement was attained. The poor performance of these cells is therefore attributed to low lifetime in the material used for arsenic studies.

Results

Large area cells were fabricated using the boron implantation and anneal as described above and phosphorus implantation (5 keV, 2.5×10^{15} ions/cm^2) followed by a three-step anneal (ref. 3). Patterned Ti-Pd-Ag contacts were applied to the front and full area Al-Ti-Pd-Ag contacts were applied to the back. An evaporated antireflection coating of Ta_2O_5 was applied and cells were sawed to final size (5.9 cm x 5.9 cm). The cell shape and contact configuration were selected so as to be compatible with the encapsulation design (Fig. 3). Total cell area was 34.3 cm^2.

Performance under simulated AM0 insolation at 25°C was measured, and the following average characteristics were obtained for a group of twenty-five cells.

	Average	Standard Deviation
V_{oc} (mV)	605	0.2
J_{sc} (mA/cm^2)	38.1	0.3
FF (%)	75.2	1.1
EFF (%)	12.8	0.2

We attribute the low fill factor in part to a shunt resistance arising at the wafer edge (part of this edge is incorporated in the final cell - see Fig. 3) and in part to contact series resistance. Improvements in cell design and fabrication techniques which will yield a fill factor of 80% without substantial increase in cell cost are being pursued.

ENCAPSULATION

A major reduction in assembly cost is achieved by a new procedure for attaching glass coverslips. Standard practice has been to bond a precisely cut coverslip to a finished cell. The demands on cell and glass tolerance and on precision alignment of coverslip with respect to the cell during assembly add substantially to the assembly cost. To reduce this cost, we have developed a process in which the glass cover is bonded to the wafer before sawing the cell to its final size. In this way, cell and glass are sawed to size as one using a wafer dicing saw. This obviates the need for precision in both coverslip preparation and alignment, without loss of registration, and so results in a major cost saving. We believe that this is the first demonstration of this technology.

Materials and Lamination

An encapsulation procedure was developed for three adhesives: ethylene vinyl acetate (EVA), FEP-Teflon sheet and Dow-Corning 93-500. Two types of glass were used: Corning 0211 (nominally 300 μm thick) and Corning 7070 microsheet (nominally 100 μm thick). The thermal expansion coefficient of Corning 7070 is quite close to that of silicon; it is therefore the best choice for use with lamination sequences involving temperature cycling.

The lamination procedures used for EVA and FEP-Teflon were straightforward. A brief description is provided here. The details can be found in reference 7. An assembly consisting of the glass, adhesive and cell are placed in an evacuated chamber. Pressure is applied (½ atm. for EVA, 2 atm. for FEP-Teflon) and the sample is heated (150°C for EVA, 300°C for FEP-Teflon) to allow the adhesive to flow. The assembly is then cooled slowly to room temperature.

Lamination with DC93-500 was also straightforward. The adhesive is mixed, de-aired and poured onto the center of the cell. The cell is then placed in a bell jar and the DC93-500 is de-aired a second time. A cleaned coverslip is placed over the DC93-500 and the air is pressed out manually. The assembly is then placed in an oven at 150°C for 15 minutes to speed the adhesive cure.

Complete lamination over an area of 45 cm^2 was attained with each adhesive. No delamination occurred after 10 temperature cycles between 77 K and 373 K.

Assembly Configuration

Figure 3 illustrates the contact configuration used in this work. The final cell is square with a connection pad at each corner. Note that the corners would actually extend beyond the edge of the wafer since the diagonal of the square is larger than the wafer diameter. The actual corners are therefore rounded and are formed by the edge of the original wafer. This edge is never removed.

Silver ribbon leads were welded to the connection pads and a glass cover was laminated to the assembly as described in the previous section. The dotted lines in Figure 3 indicate the locations of the saw cut. It is necessary to fold the ribbon leads over either the rounded corner or the edge of the glass so as to remain out of the path of the saw blade. A photograph of an assembly prepared for sawing is shown in Figure 4A. The leads have been taped to the coverglass. The assembly is shown after sawing in Figure 4B.

Assembly Results

Assemblies have been fabricated with each of the adhesives with good results obtained when Corning 7070 microsheet is used. Problems resulting from residual stress when Corning 0211 was used in combination with a thermal lamination process included cell bowing and spontaneous coverglass cracking.

Two wafers were removed prior to sawing from the large area cell process group described in the first section of this paper and were encapsulated with the DC93-500 lamination process and Corning 7070 microsheet. The performance under simulated AM0 insolation is shown below.

Cell	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
31-6	600	37.0	72.8	12.0
34-3	603	37.2	75.9	12.6

There would appear to be a slight decrease in short circuit current (in comparison to the non-encapsulated cells), perhaps owing to a change in the effectiveness of the antireflection coating upon encapsulation. In general, however, the performance does not seem to be degraded by the encapsulation process.

CONCLUSIONS

Cells were fabricated using potentially low-cost ion implantation processing. Average efficiency of large area cells of 12.8% AM0 was achieved. A novel encapsulation technology was investigated and found to simplify encapsulation without sacrifice of cell quality.

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TABLE 1 - BACK SURFACE FIELD PROCESS PARAMETERS

Ion Implantation

Energy	=	50 keV
Fluence	=	5×10^{15} ions/cm

Furnace Anneal

550°C for 2 hours
Ramp to 950°C at 8°C/min
950°C for 2 hours
Ramp to 500°C at 5°C/min.

TABLE 2 - MEASURED PERFORMANCE OF B, Ga AND Al BSF SOLAR CELLS.

BSF (no. of cells)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	EFF (%)
Boron (35)	595 (003)	27.0 (0.4)	78.7 (1.4)	9.37 (0.24)
Gallium (11)	584 (005)	26.0 (0.3)	77.4 (4.0)	8.71 (0.59)
Aluminum (24)	584 (003)	26.2 (0.3)	78.8 (0.8)	9.00 (.14)
None (24)	582 (002)	26.3 (0.3)	76.9 (1.9)	8.7 (0.2)

Notes: Simulated AM0 illumination. Cell area = 4 cm^2, no AR coating. Standard deviation shown in parenthesis. T=25°C.

TABLE 3 - MEASURED VALUES OF THERMAL ALPHA FOR FOUR BSR PROCESSES

Back Implantation	Metallization	Thermal Alpha
None	Not sintered	0.64 + 0.02
None	Sintered, 400°C	0.66 + 0.02
$^{11}B^+$	Not sintered	0.67 ± 0.02
$^{11}B^+$	Sintered, 400°C	0.68 ± 0.02

TABLE 4 - COMPARISON OF SHALLOW JUNCTION CELLS FORMED BY VARIOUS FRONT IMPLANTATION PROCESSES

Implantation	Furnace Anneal Cycle	Junction Depth (μm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	AMO Eff (%)
$^{31}P^+$ 10 keV 2.5 x 10^{15} ions/cm^2 (Direct)	550°C - 2 hours 850°C - 15 min 550°C - 2 hours (flowing N_2)	0.18	582 (001)	26.6 (0.2)	78.1 (1.3)	9.0 (0.1)
$^{31}P^+$ 10 keV 2.5 x 10^{15} ions/cm^2 (Si pre-implanted)	550°C - 2 hours 850°C - 15 min 550°C - 2 hours (flowing N_2)	0.13	555 (002)	26.6 (0.1)	77.2 (2.2)	8.5 (0.3)
$^{75}As^+$ 30 keV 3.5 x 10^{15} ions/cm^2 (Direct)	900°C - 30 min. (flowing O_2)	0.10	567 (001)	24.2 (0.9)	77.3 (0.1)	7.9 (0.4)

Notes: Simulated AMO insolation. Cell area is 4 cm^2. No AR coatings. Standard deviation shown in parenthesis. T = 25°C.

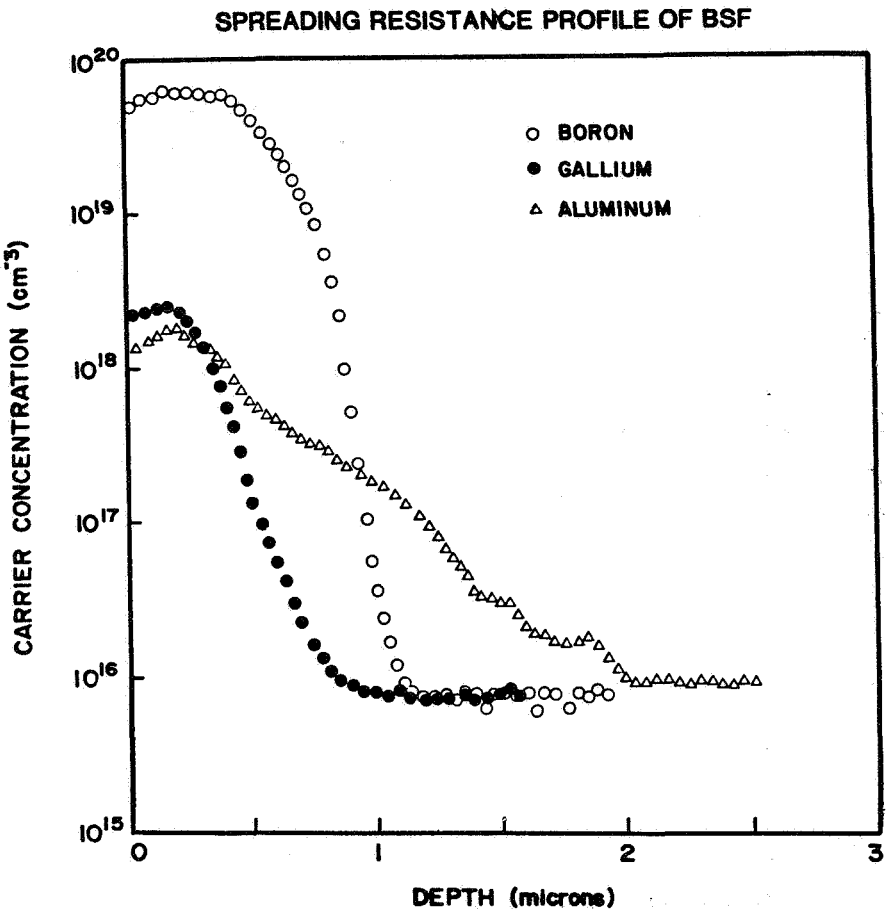

Figure 1: Spreading Resistance Profiles of Boron, Gallium and Aluminum Implants.

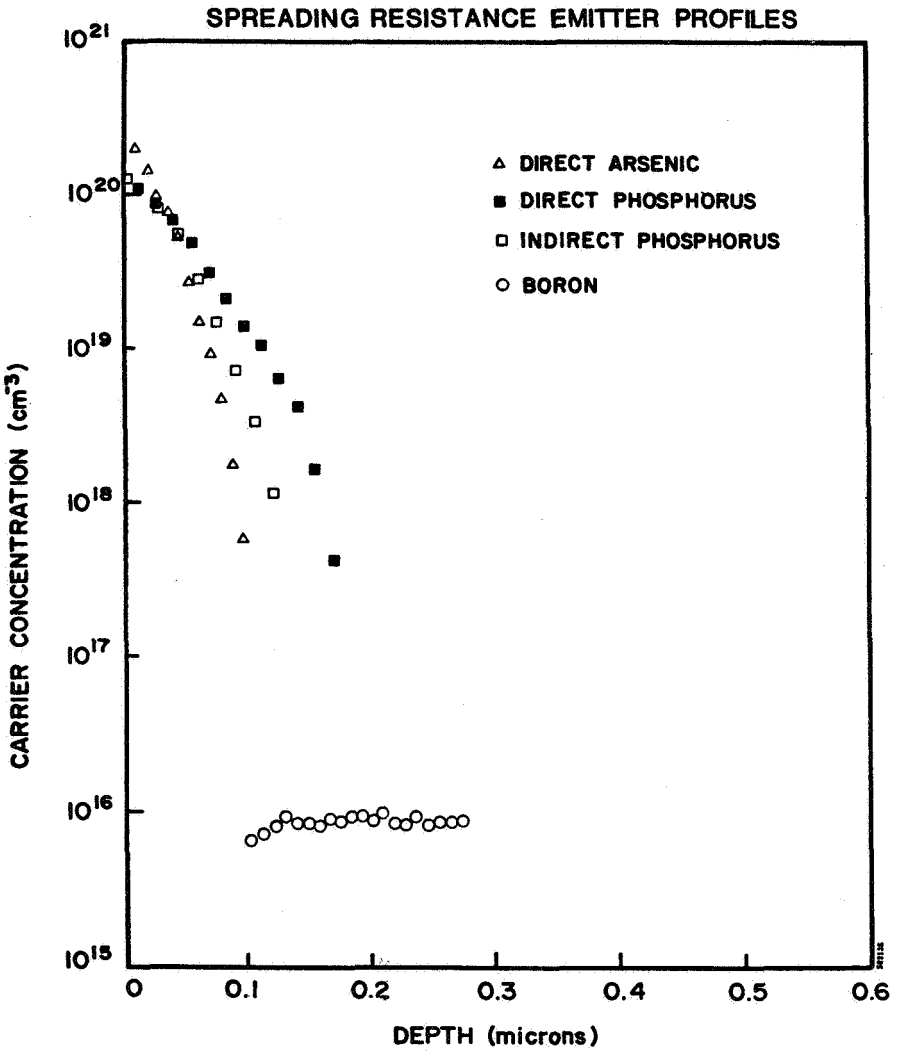

Figure 2: Spreading Resistance Profiles of Direct Arsenic, Direct Phosphorus, and Silicon Followed by Phosphorus Implants.

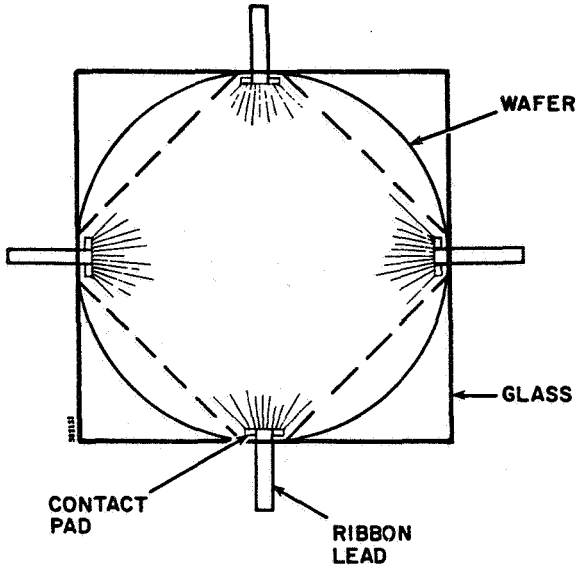

Figure 3: Configuration of Cell and Coverglass Assembly Prior to Sawing. The dotted lines indicate the saw cut positions.

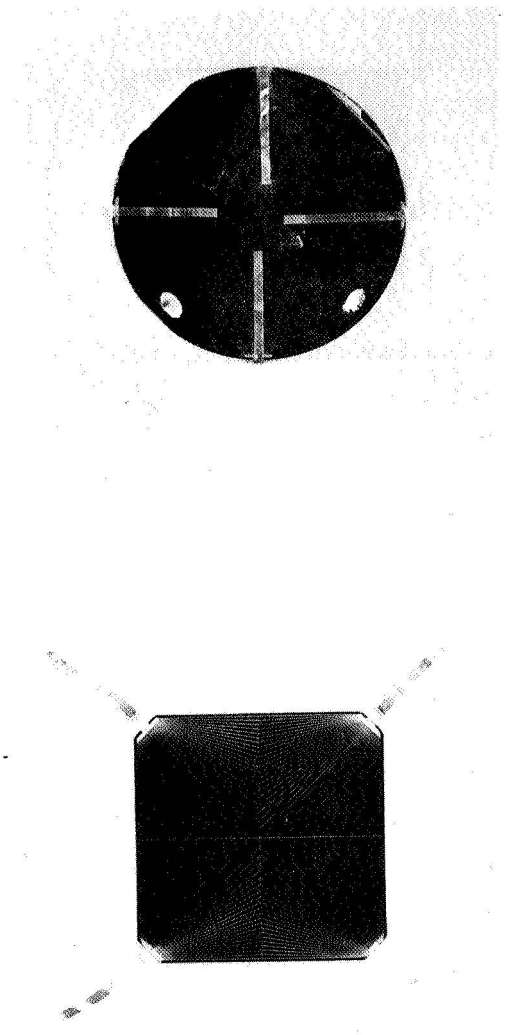

Figure 4: Photograph of the Solar Cell Assembly (a) Before sawing, with the ribbon leads folded over the front surface, and (b) after sawing, with the ribbon leads removed from the front surface.