IR AREA ARRAY STATUS

JON RODE

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AGENDA

- IR FOCAL PLANE OVERVIEW: THE CHOICES
- STATUS OF HCT HYBRID FOCAL PLANES
- AREAS OF DEVELOPMENT

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TRADE-OFFS FOR APPLICATION COMPLEX

- OPERATING TEMPERATURE
- QUANTUM EFFICIENCY
- FILL FACTOR
- WAVELENGTH
- UNIFORMITY (λ_C, η)
- COMPLEXITY
- YIELD
- COST
- CELL SIZE
- ARRAY SIZE
- SPEED OF READOUT
- INTEGRATION TIME
- DYNAMIC RANGE
- POWER
- SIGNAL PROCESSING
- BUTTABILITY

IR ARRAYS BASED ON PHOTON DETECTION

DETECTION

INTRINSIC (PV, MIS, PC)	SCHOTTKY BARRIER	EXTRINSIC
– HgCdTe	– PtSi	Si: As, G, In, S, Zn, ––
– InSb	– PdSi	
– InAsSb		
– PbSnTe		
– PbSSe		
– HgMnTe		

FOCAL PLANE ARCHITECTURE

BACKSIDE ILLUMINATED
(EPITAXY, THINNED)

FRONT-SIDE
ILLUMINATED

MONOLITHIC

CHARGE INJECTION
DEVICE

SPRITE

HYBRID

Z-PLANE

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LEADING ARRAY TECHNOLOGIES

- EPITAXIAL HgCdTe HYBRIDS (EXTEND TO Z PLANE)
- EXTRINSIC (As, Ga, In, S) SILICON (MONOLITHIC AND HYBRID)
- MONOLITHIC AND CID HgCdTe (ALSO InSb)
- SCHOTTKY BARRIER MONOLITHIC DEVICES (Pt AND Pd)

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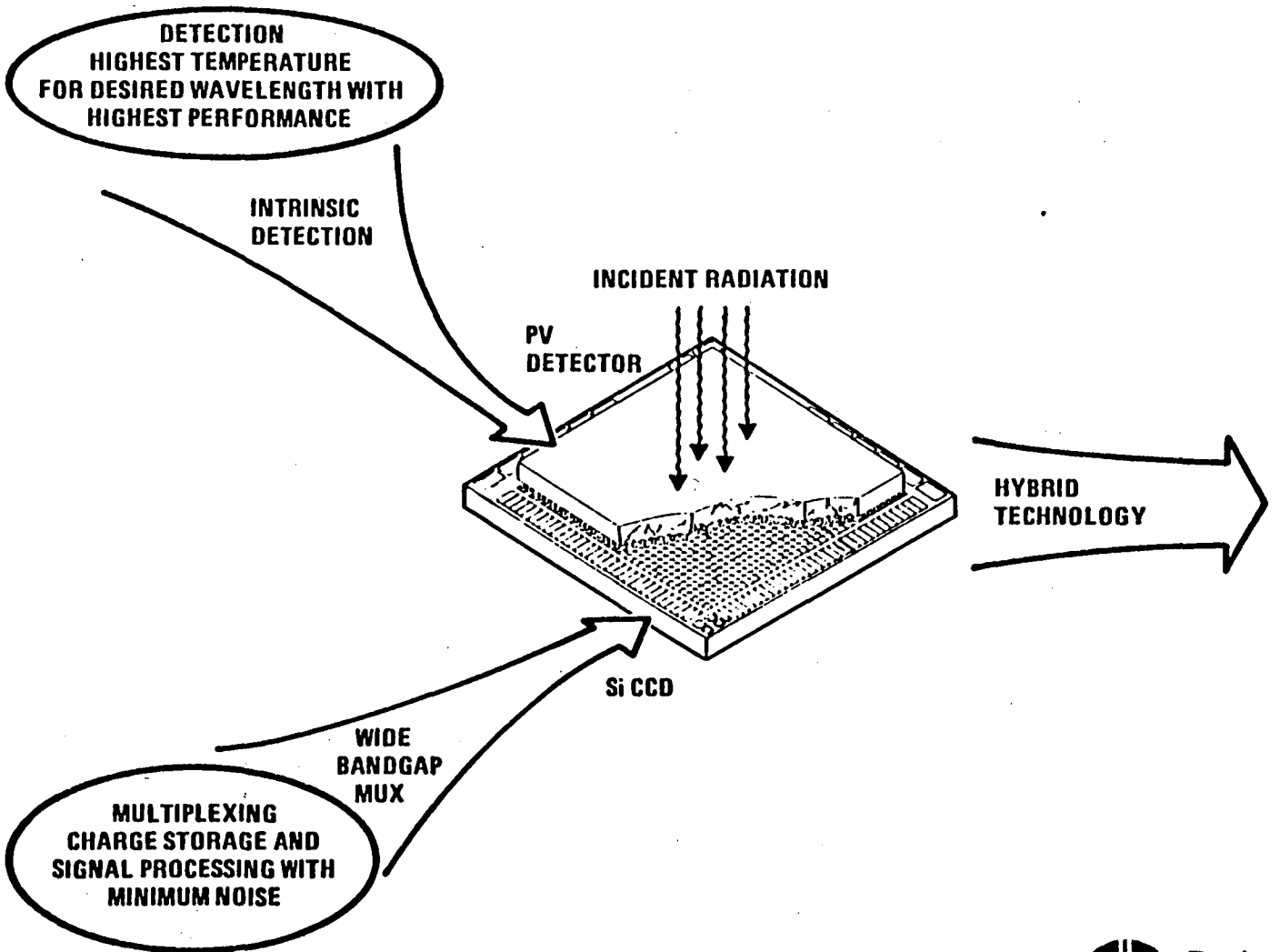
HYBRID TECHNOLOGY

SC80-7335



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EPITAXIAL HgCdTe HYBRID FOCAL PLANE

- SPECTRAL RANGE 1-12 μm
  - 3-5 μm MOST MATURE

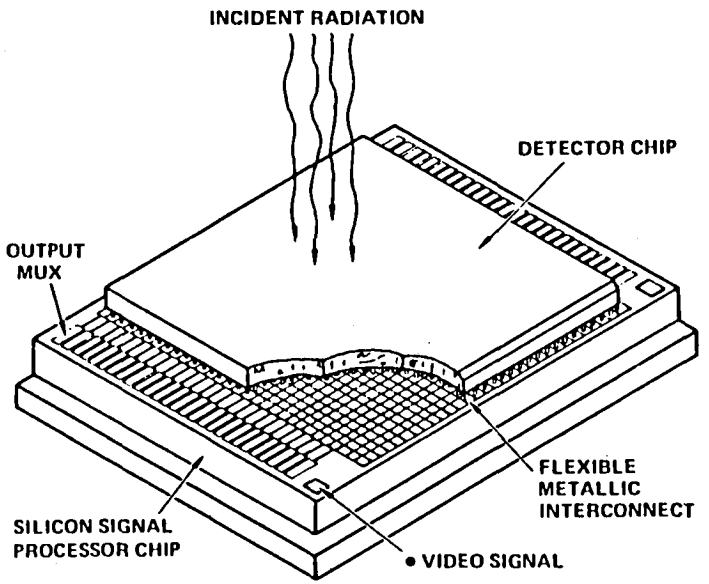
    1-3 μm RIPE FOR DEVELOPMENT
  - 8-12 μm MOST DIFFICULT FOR MATERIALS AND SIGNAL PROCESSING

- ARRAY SIZE
  - 64 x 64 DEMONSTRATED; 128 x 128 FEASIBLE
  - DETECTOR SIZE AT 25 x 25 μm,CAN GO TO 15 μm x 15 μm
  - CELL SIZE AT 50 μm x 50 μm, CAN GO TO 30 μm x 30 μm

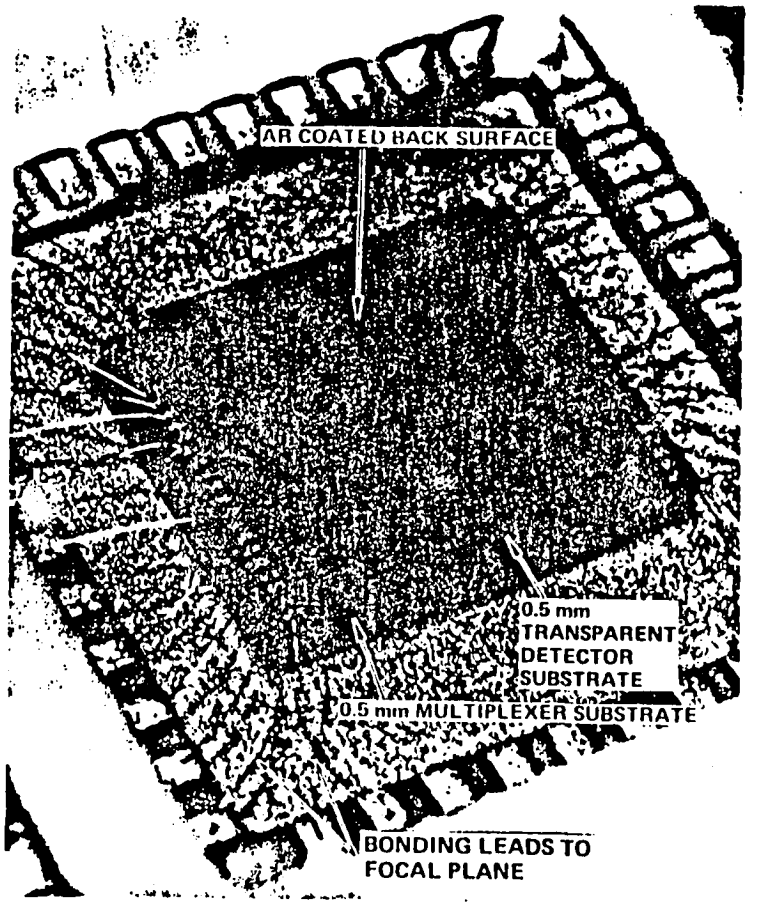
- SIGNAL PROCESSING
  - DIRECT INJECTION WITH DC SUPPRESSION AND GAIN REDUCTION
  - GATE MODULATION (DC SUPPRESSION)
  - AC COUPLED CIRCUITS IN DEVELOPMENT

PLANAR HYBRID FOCAL PLANE

SC81-13051



PERSPECTIVE DRAWING



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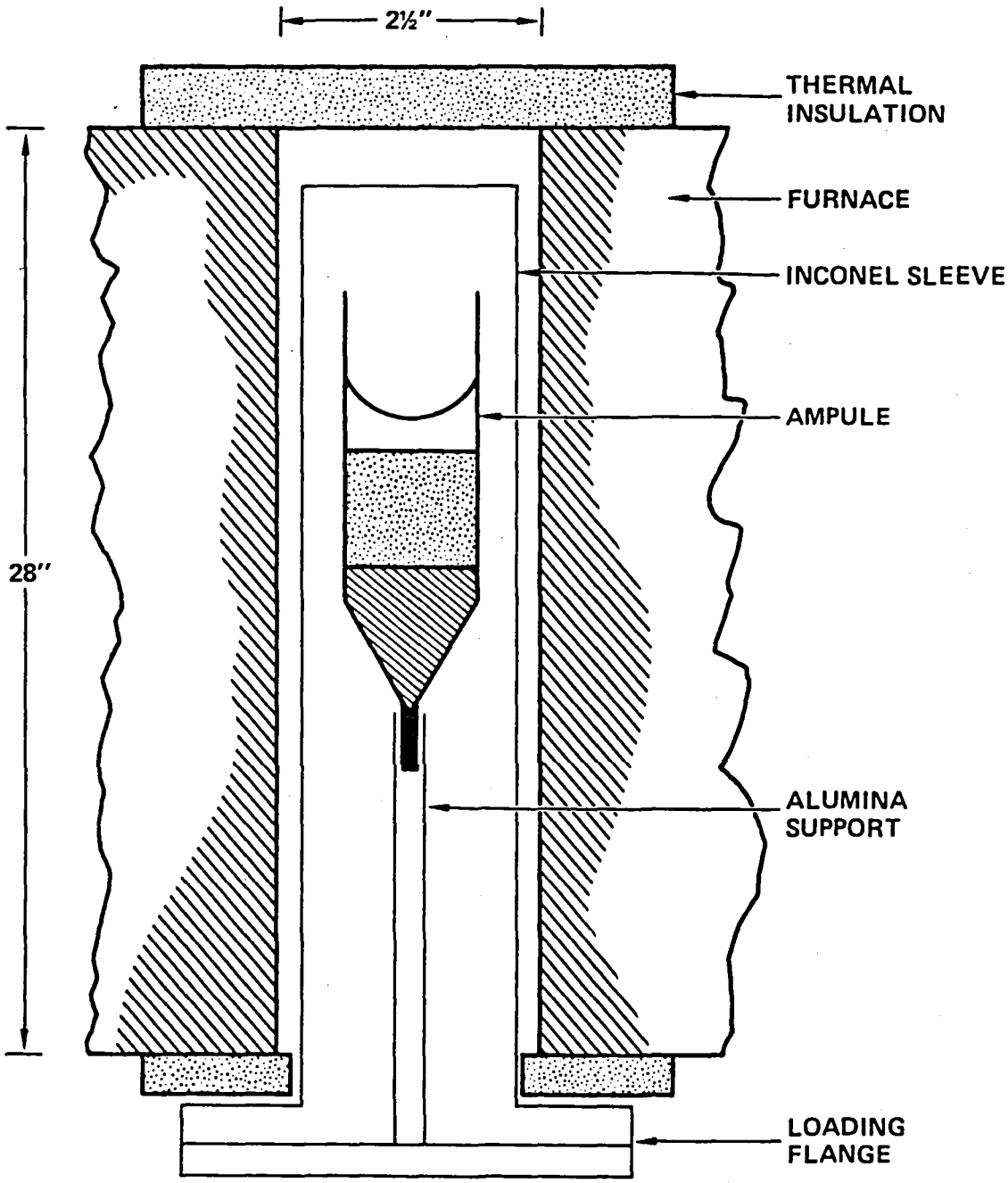
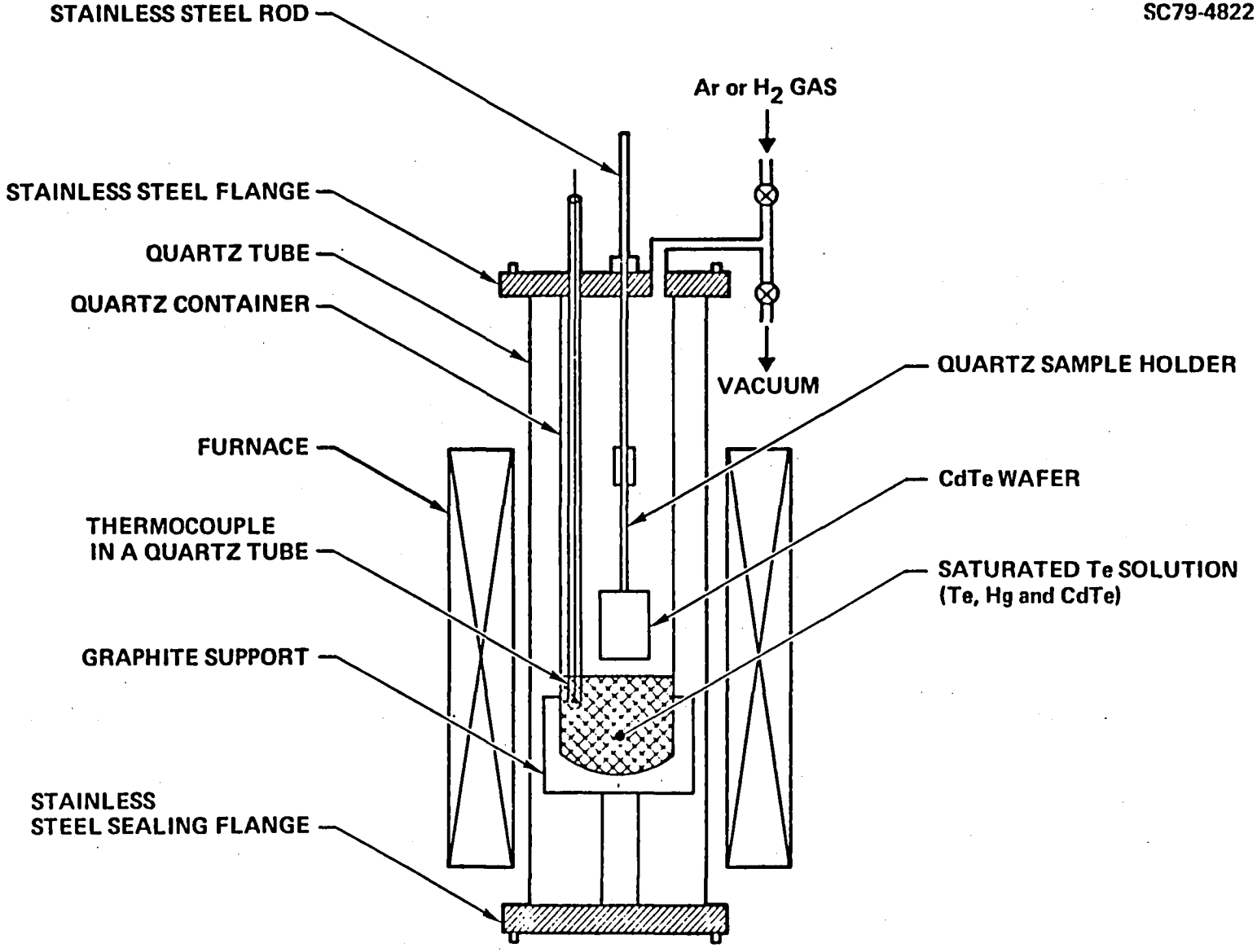
SC81-13778


2½"
THERMAL INSULATION
FURNACE
INCONEL SLEEVE
AMPULE
28"
ALUMINA SUPPORT
LOADING FLANGE

HgCdTe LPE SYSTEM

SC79-4822



24 CM^2 HgCdTe MWIR LPE

GOALS ADDRESSED: LARGE ELEMENT NUMBER, LOW DEAD SPACE
VERSATILITY, PRODUCIBILITY

PARAMETER	TYPICAL VALUE
GROWTH AREA	> 15 CM^2
THICKNESS	15 μm
MORPHOLOGY	SUITABLE FOR DEVICE PROCESSING
λ_c UNIFORMITY (ACROSS WAFER)	σ = 0.035 μm
λ_c REPRODUCIBILITY (FOR > 200 LAYERS)	σ = 0.056 μm
HOLE CONCENTRATION	3×10^{16} cm^{-3}
MOBILITY	300 cm^2/V-sec
DEVICE QUALITY	EXCELLENT

- LPE HgCdTe CAN BE FABRICATED IN SIZES AND GEOMETRIES COMPATIBLE WITH Si PROCESSING
- 35 MEDIUM ARRAYS/WAFER POSSIBLE WITH OPTIMIZATION OF GROWTH

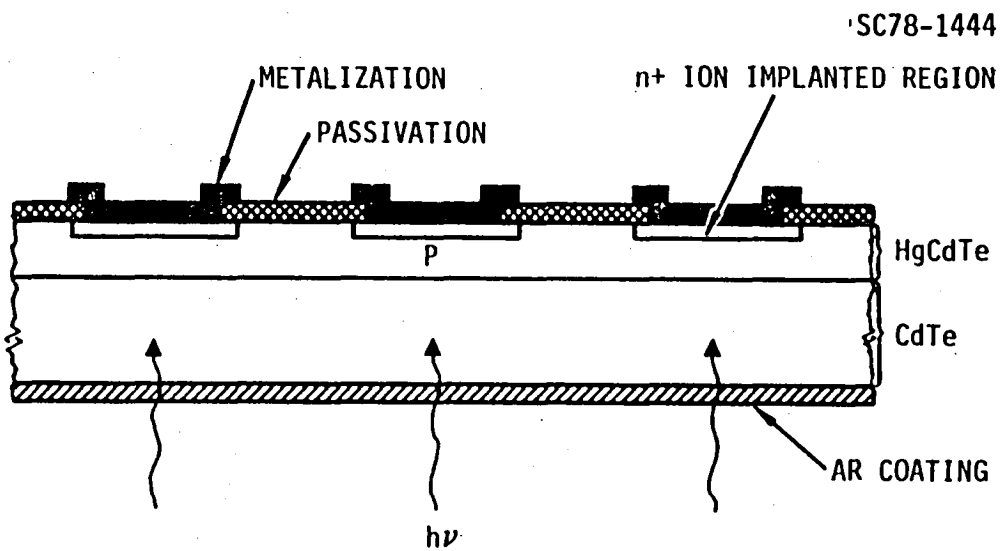
HgCdTe DIODE ARRAYS

GOALS ADDRESSED: COST, LARGE ELEMENT NUMBER,
LOW DEAD SPACE PRODUCIBILITY VERSATILITY

ARRAY CHARACTERISTICS

- PLANAR (MAXIMIZES USEFUL AREA, SIMPLIFIES PROCESSING)
- PROCESS COMPATIBLE WITH Si PROCESSING
- HIGH UNIFORMITY FROM IMPLANT PROCESS
- PROCESS ADAPTABLE TO PRODUCTION FOCAL PLANES

SCHEMATIC VIEW OF HgCdTe/CdTe DETECTOR ARRAY



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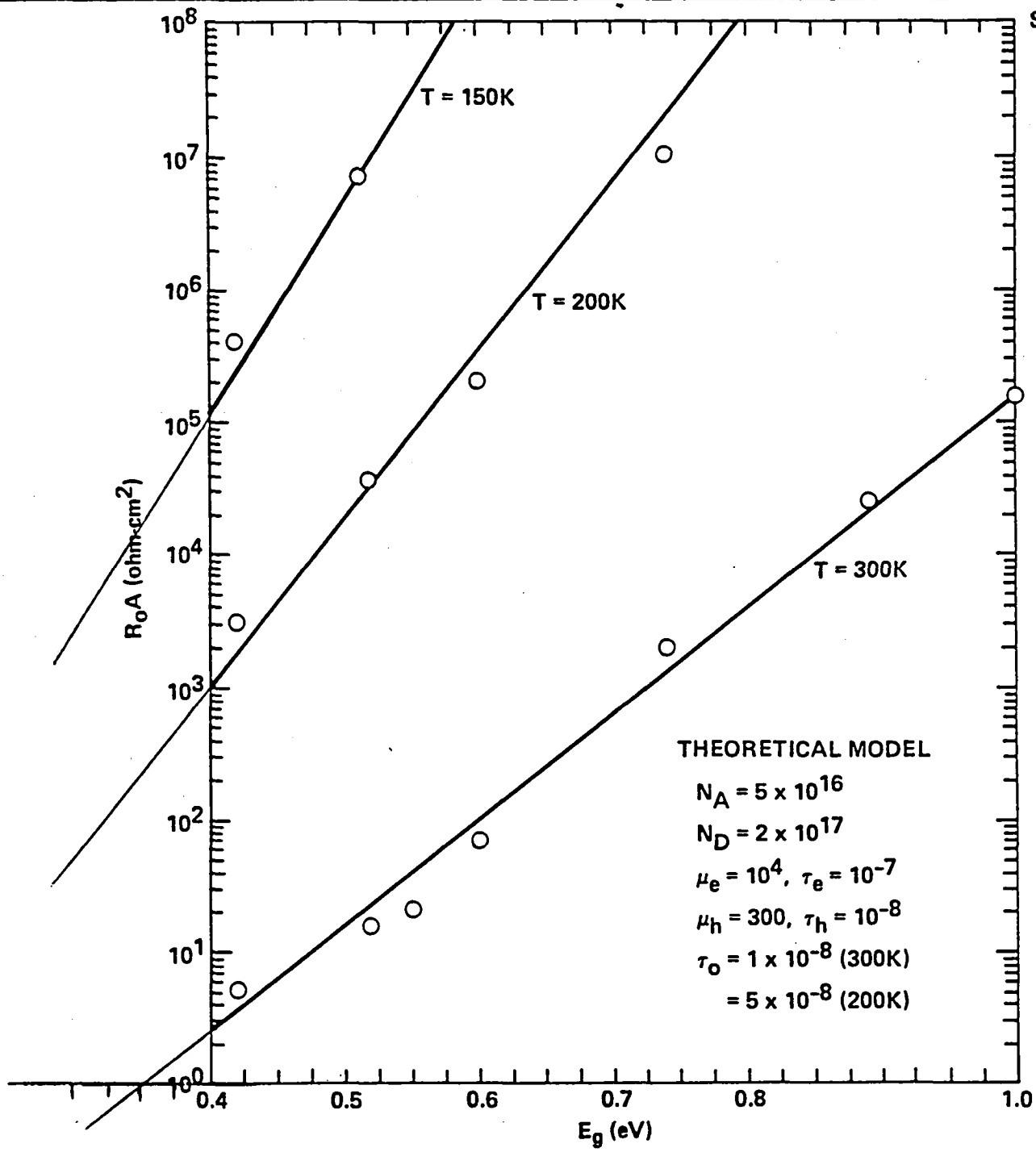
R_oA PRODUCTS OF SWIR PHOTODIODES AS A FUNCTION OF E_g



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SC80-9061A

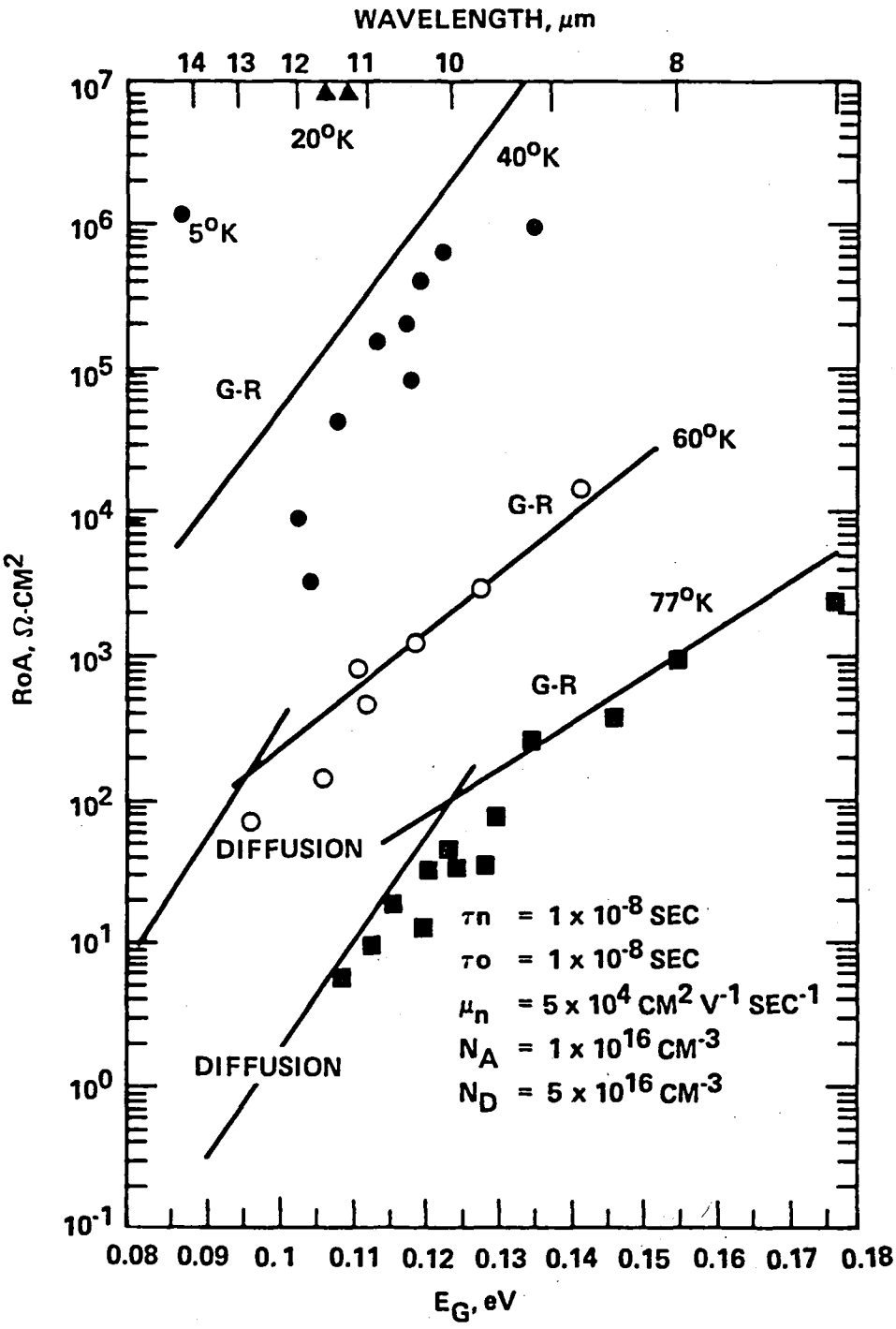
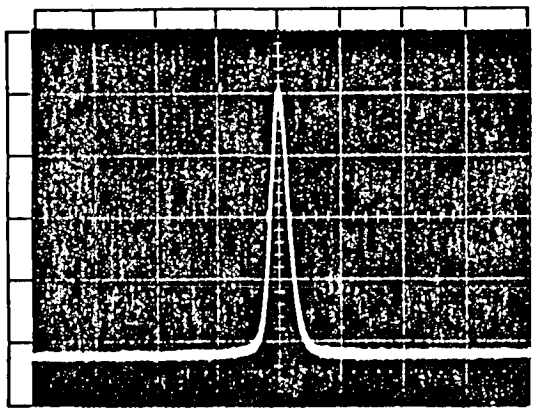


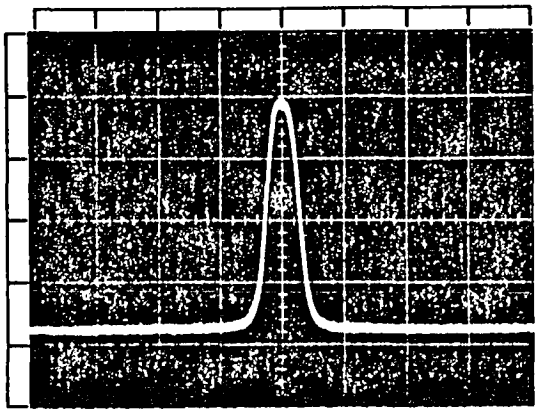
Fig. 3 Calculated and experimental results of R_0A versus energy bandgap for LPE-grown PV HgCdTe devices.

SPOT SCAN OF DIFFERENT AREA HgCdTe DETECTORS

SC81-12755

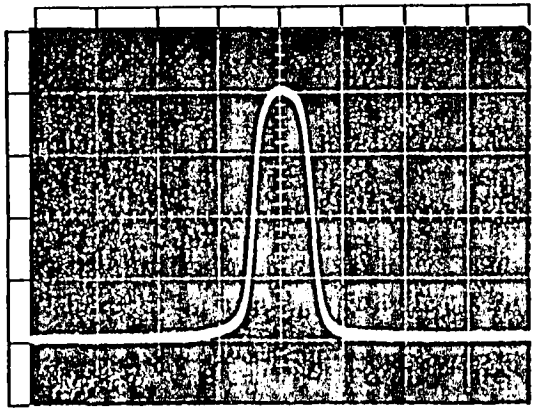


A. (0.5 x 0.5)

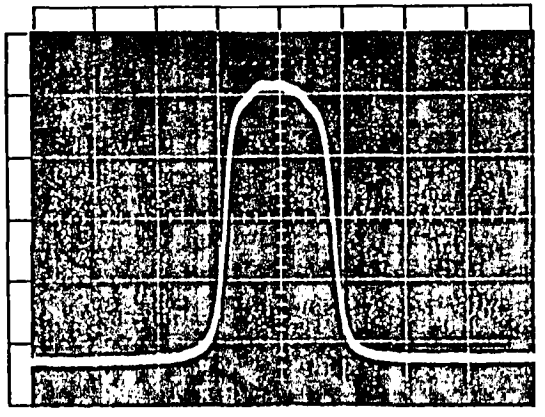


B. (1.0 x 1.0)

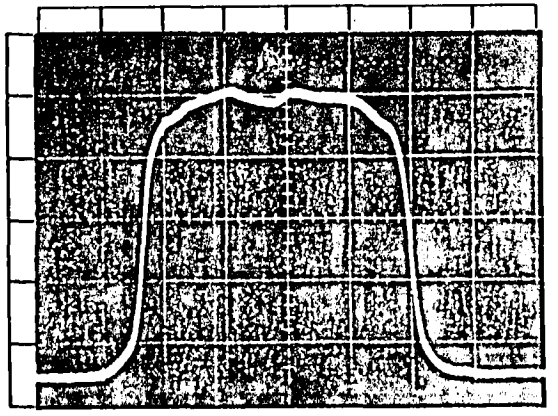
- PLANAR, BACKSIDE ILLUMINATED PV DETECTORS AT 77K
- 1 DIVISION = 2.40 MILS
- IMPLANT AREA (MILS)
  - A. 0.5 x 0.5
  - B. 1.0 x 1.0
  - C. 2.0 x 2.0
  - D. 4.0 x 4.0
  - E. 10.0 x 10.0



C. (2.0 x 2.0)



D. (4.0 x 4.0)



E.(10.0 x 10.0)

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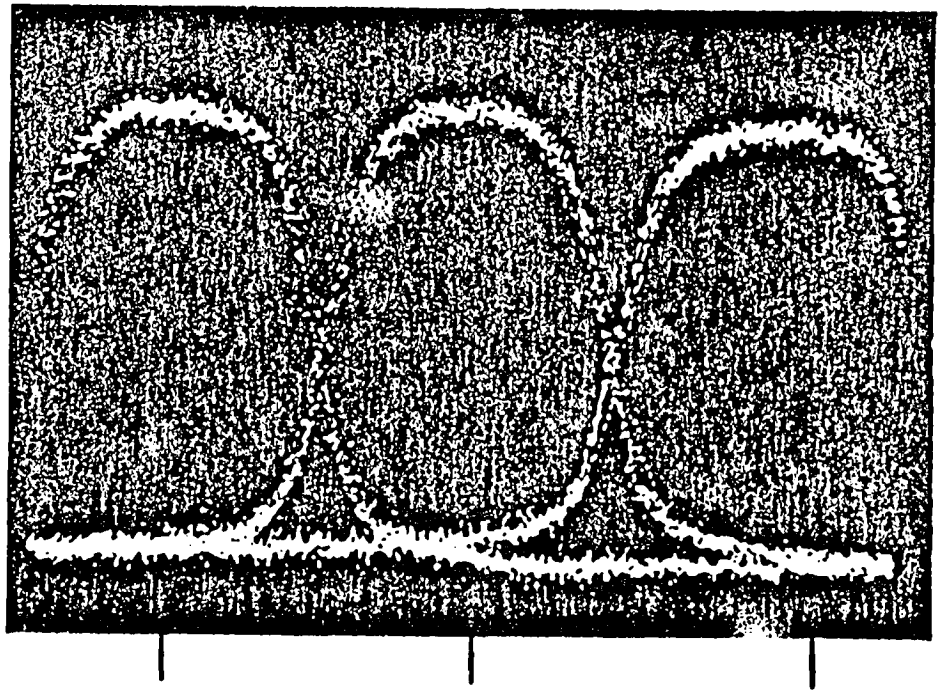
SPOT SCAN OF MWIR DEVICE 149N01-2C5

SC81-12340



68 μm UNIT CELL

DEVICE No. 149N01-2C5
T = 77K
λ_c = 4.7 μm

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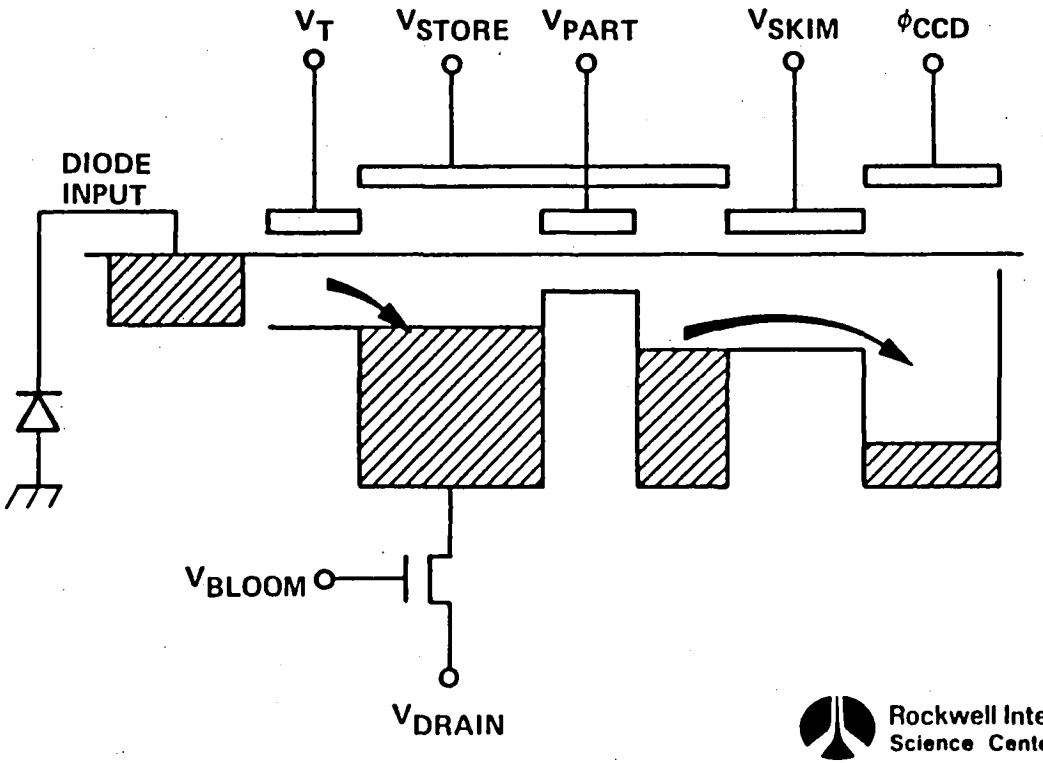
BACKGROUND SUPPRESSION OF DIRECT INJECTION INPUT

SC80-9371A



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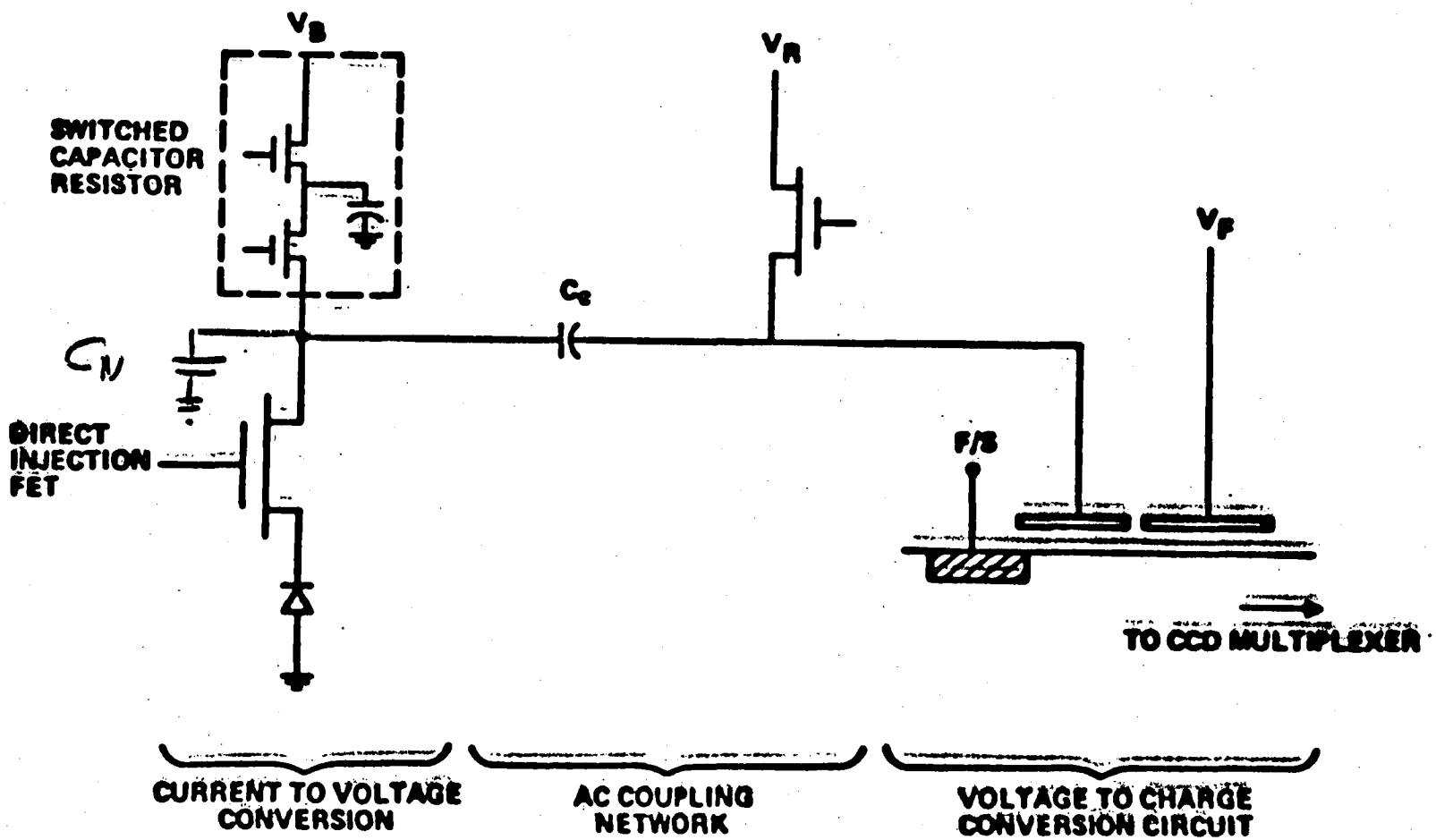
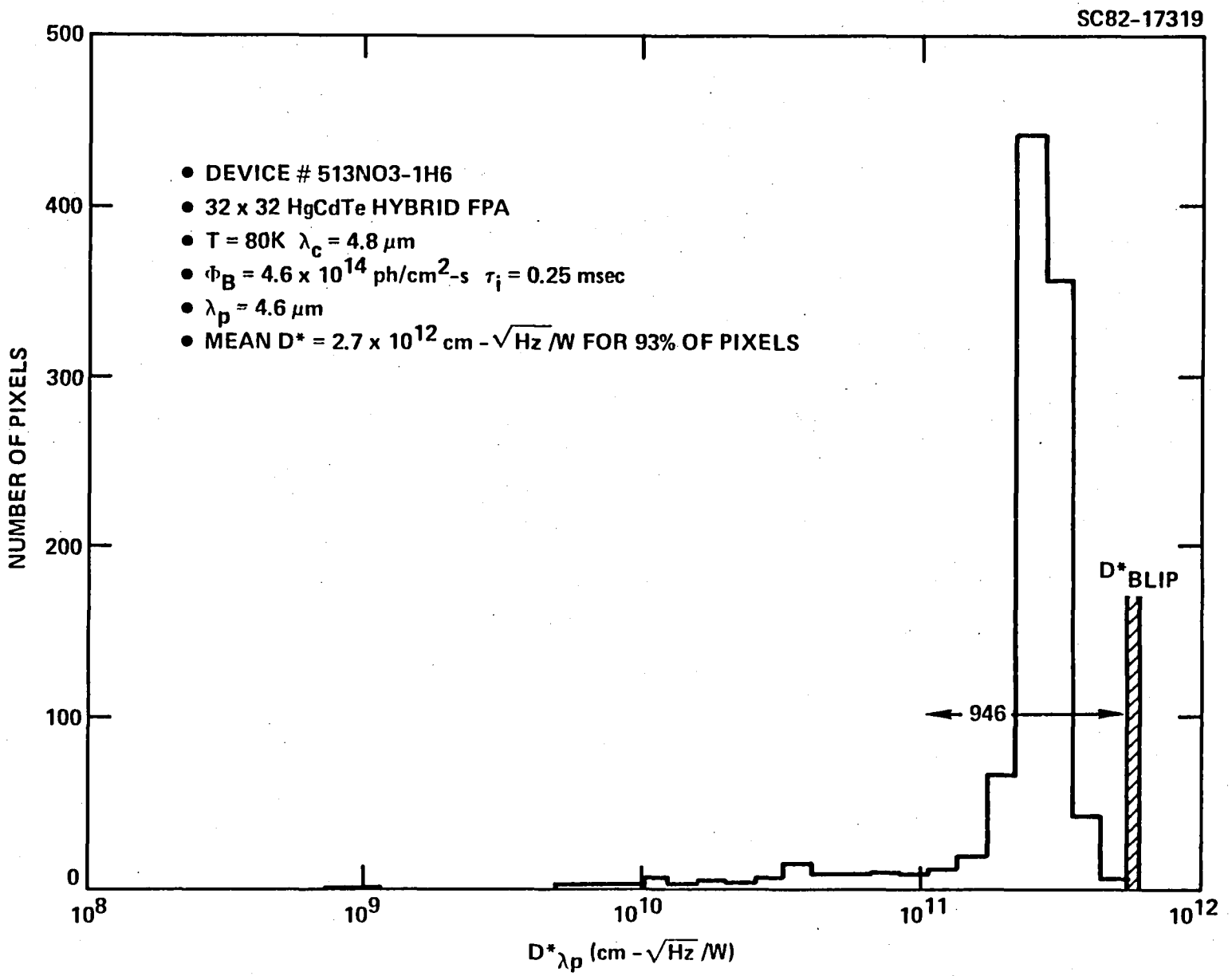
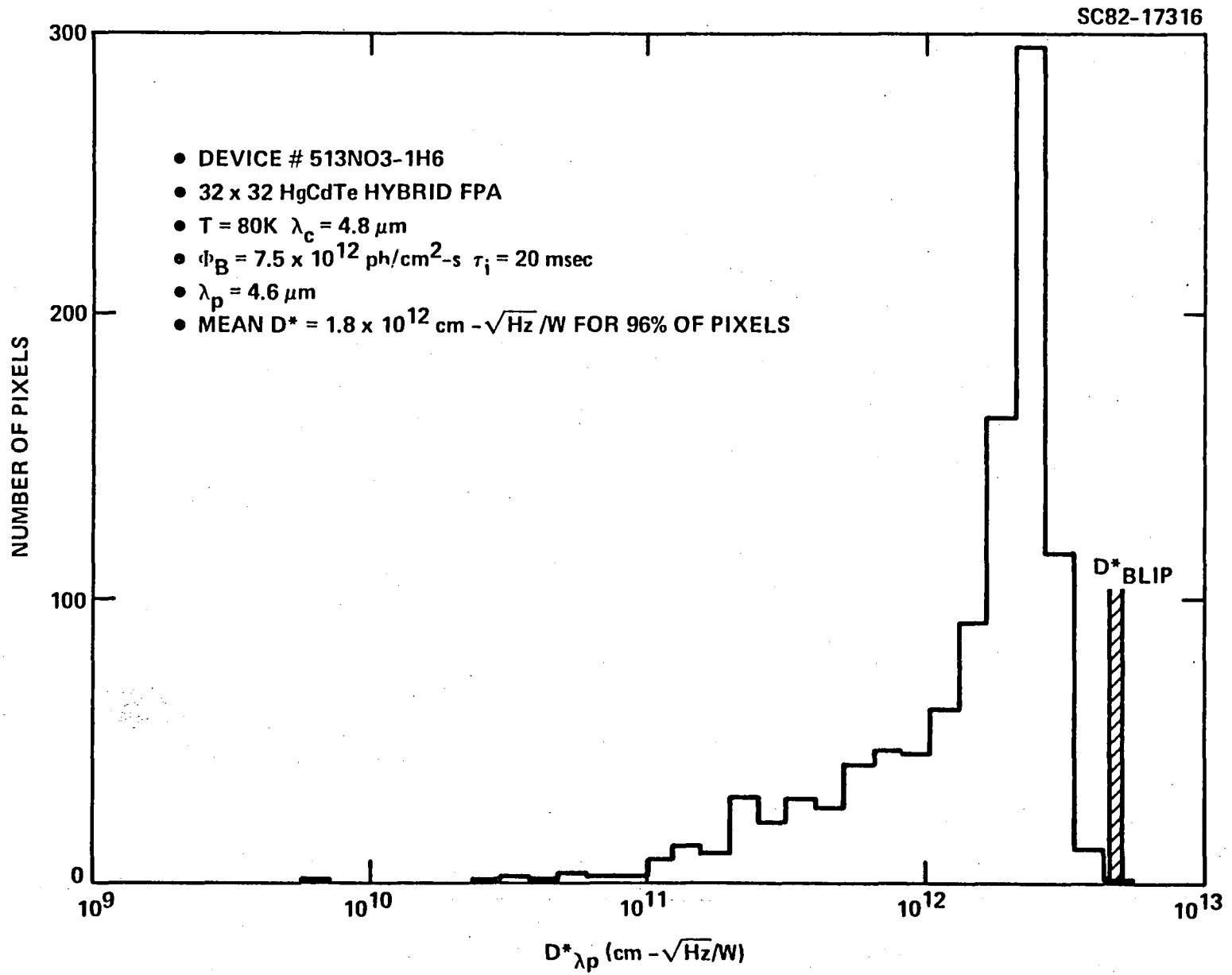
INPUT CIRCUIT DESIGN FOR AC COUPLED MULTIPLEXER



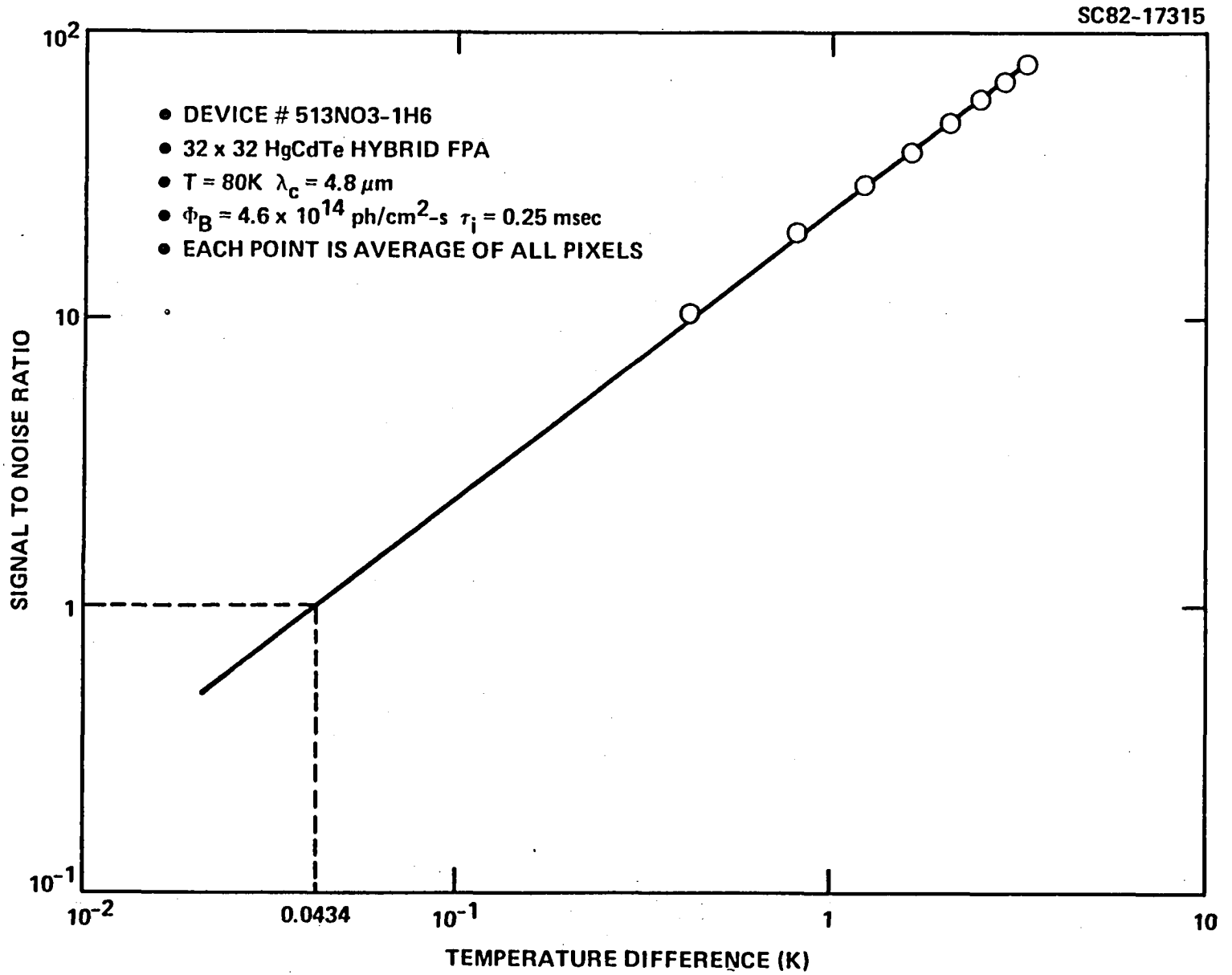
$D^*_{\lambda p}$ HISTOGRAM



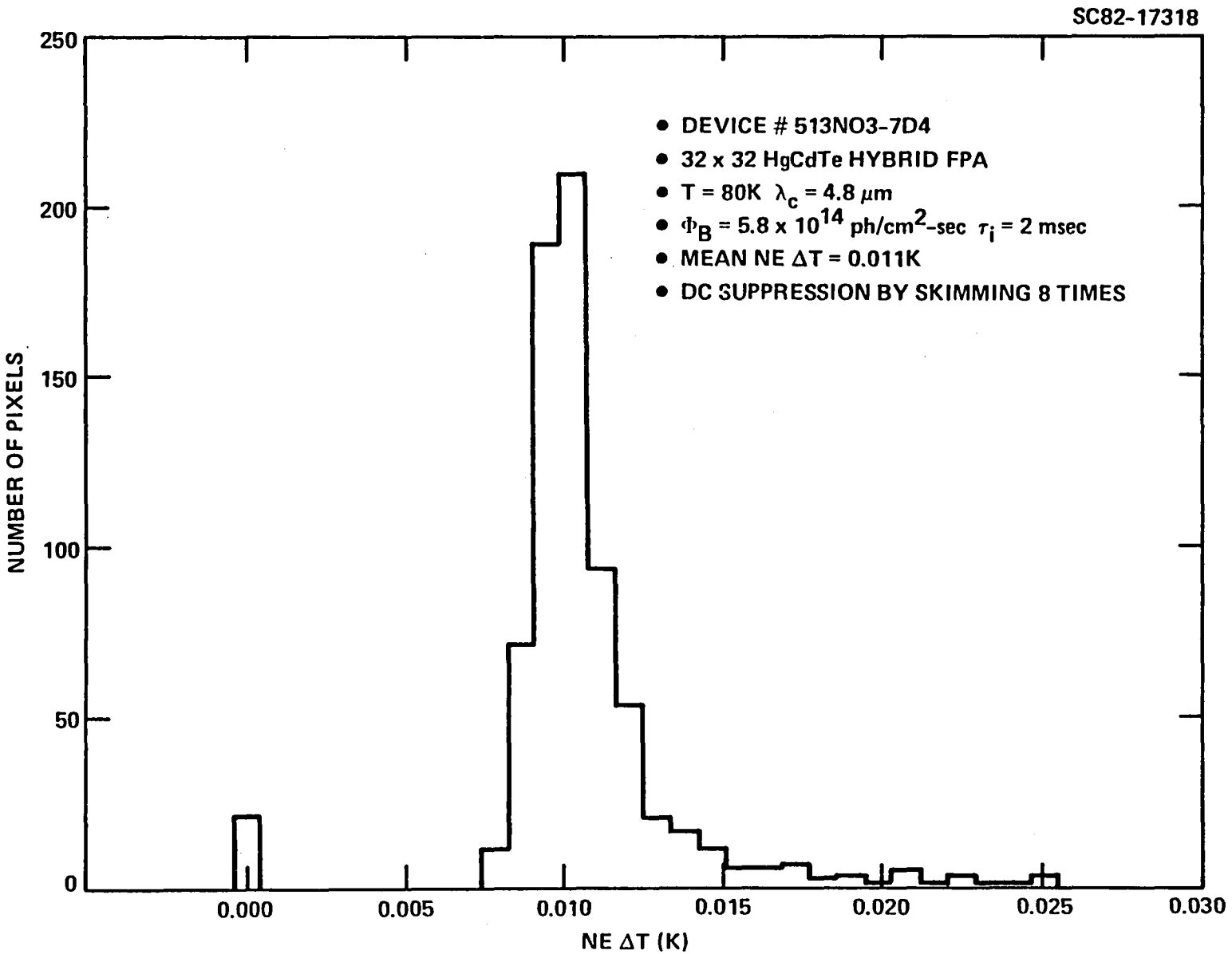
$D^*_{\lambda p}$ HISTOGRAM



NOISE EQUIVALENT TEMPERATURE DIFFERENCE

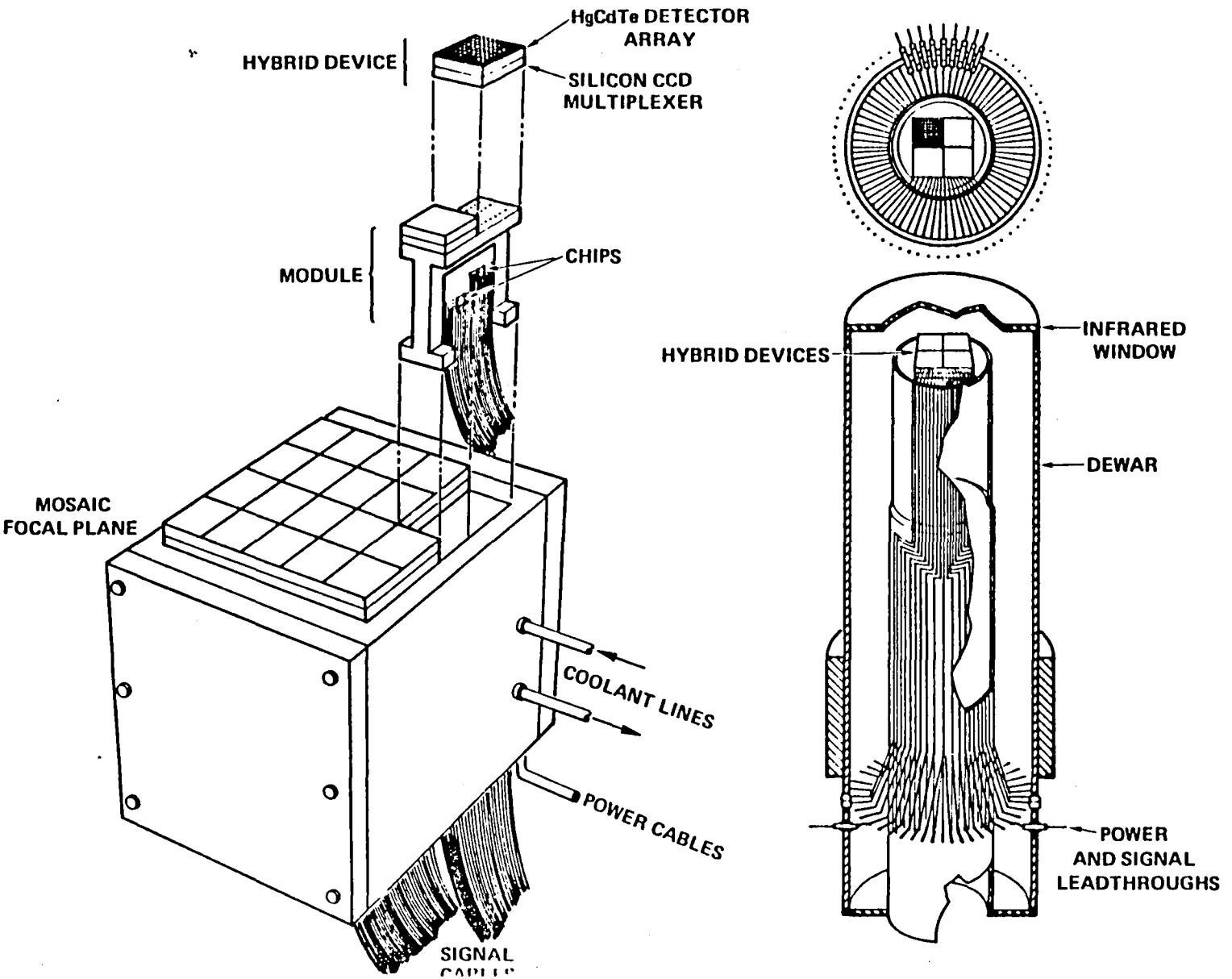


NOISE EQUIVALENT TEMPERATURE DIFFERENCE HISTOGRAM



FOCAL PLANE MODULES

SC80-7286A



DEVELOPMENT OF HgCdTe FOCAL PLANES

MATERIALS

- ALTERNATE SUBSTRATES (CHEAP, STRONG, UNIFORM)
- ALTERNATE GROWTH TECHNIQUES (IMPROVE MORPHOLOGY)

PROCESSING

- PASSIVATION
- YIELD

UNIT CELL

- NEW INPUT STRUCTURES (ESPECIALLY LWIR)
- IMPROVE SIGNAL PROCESSING
- INCREASE DYNAMIC RANGE

FOCAL PLANE ARCHITECTURE

- LOW DEAD SPACE
- Z-PLANE
- MONOLITHIC