N84-18537

UNIVERSITY OF PENNSYLVANIA
The Moore School of Electrical Engineering
Philadelphia, Pa. 19104

FINAL REPORT

Deep Diode Arrays for X-ray Detection

TO

NASA/Goddard Space Flight Center
Code 287
Greenbelt, Maryland 20771

CONTRACT NAS-5-27285

PRINCIPAL INVESTIGATOR: Jay N. Zemel

29 January 1984

ABSTRACT

Temperature Gradient Zone Melting Process (TGZMP) was used to form P-N junctions in bulk of high purity silicon wafers. These diodes were patterned to form arrays for x-ray spectrometers. The whole fabrication processes for these x-ray detectors are reviewed in detail.

The P-N junctions were evaluated by

(i) the dark diode I-V measurements,

(ii) the diode C_T-V measurements,

(iii) the MOS C-V measurements.

The results showed that these junctions were linearly graded in charge distribution with low reverse bias leakage current flowing through them (few nA at -10 volts).

The x-ray detection experiments showed that an FWHM of 500 eV was obtained from these diodes with a small bias of just -5 volts (for x-ray source Fe^{55}). A theoretical model was proposed to explain the extra peaks found in the energy spectra and a very interesting point--cross talk effect was pointed out. This might be a solution to the problem of making really high resolution x-ray spectrometers.

Few additional studies on materials subjected to TGZMP conditions were done. They were

(i) annealing of chemically deposited silicon,

(ii) recrystallization of chemically deposited silicon,

(iii) inspection of defects generated by incoherent radiation annealing.

These provide us with very useful information in understanding the mechanism of radiation heating used in TGZMP.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my thesis supervisor, Dr. Jay N. Zemel for his patient guidance, suggestions and encouragement during the course of the work.

I also wish to thank menbers of the Moore School of Electrical Engineering, especially Dr. Imants R. Lauks, Dr. Jan Van der Spiegel, Dr. Koriyama (visiting scholar of Penn. in 1982), Dr. M. Ogita (visiting scholar of Penn. in 1983), and Dr. D. J. Jaggard for many valuable discussions and also Mr. T. Carrol and Mr. V. Dominko for their technical asistance.

My sincere thanks also go to the knowledgeable and skillful people in NASA Goddard Space Center, especially Dr. George E. Alcorn and Ms. Kathryn A. Kost for many useful discussions and experiments.

In particular, my special thanks must go to my brother, Winston I. Way and his wife, Janney Chen for their constant encouragement.

Finally, my gratitude is also extended to my academic colleagues and friends: S. Azizi, G. C. Chern, J. C. Young, D. Babic, T. Fare, G. Edelson, P. Hesketh, D. S. Lin, and Z. Triester.

DEEP DIODE ARRAYS FOR X-RAY DETECTION

TABLE OF CONTENTS

I Introduction.. 1

II Principles of X-Ray Detection.......................... 2
- II-(a) Preamplifier.................................... 4
- II-(b) Linear Amplifier................................ 8
- II-(c) Multichannel Analyzer........................... 9

III Fabrication Procedures................................ 10
- III-(a) Sample Preparations........................... 10
- III-(b) Substrate Contact by Phosphorous Diffusion.... 10
- III-(c) Thermal Oxidation............................. 12
- III-(d) Aluminum Evaporation.......................... 12
- III-(e) Aluminum Migration by TGZMP................... 14
- III-(f) Potassium Hydroxide (KOH) Preferential Etching.. 23
- III-(g) Wet Thermal Oxidation......................... 25
- III-(h) Shape of the P-N Junction..................... 25
- III-(i) Metallization and Packaging................... 29

IV Experimental Results................................... 31
- IV-(a) Junction Evaluations............................ 31
  - (i) Dark I-V Measurements......................... 31
  - (ii) Diode C_T-V Measurements................... 32
  - (iii) MOS C-V Measurements........................ 41
- IV-(b) X-Ray Detection Experiments..................... 43
- IV-(c) α-Particles Detection Experiments............... 59

V Additional Studies on Materials Subjected to TGZMP Conditions.. 61
- V-(a) Annealing of Chemically Deposited SiO_2......... 61
- V-(b) Recrystallization of Chemically Deposited Silicon.. 64

V-(c) Inspection of Defects Generated by Incoherent Radiation Annealing.......................... 67

VI Conclusions.......................... 73

VII References.......................... 76

Appendix A.......................... 79

Appendix B.......................... 80

Appendix C.......................... 81

Appendix D.......................... 82

Appendix E.......................... 83

I. INTRODUCTION

Pfann (1) was the first one who used the temperature gradient zone melting process (TGZMP) to produce P-N junctions within bulk semiconductors. Later Anthony and Cline demonstrated that droplets of aluminum could be stably migrated through the silicon wafer if the dimension of the zone is sufficiently small (2,3). They first recognized that thermomigration had possibilities in radiation detection (4). The advent of large scale x-ray telescope, such as the Einstein Observatory, has created a need for an x-ray spectrometer with broad energy response. Therefore, the people in National Aeronautics and Space Administration (NASA) undertook the developement of a TGZMP based detector using high purity silicon wafers. Workers at this Laboratory successfully used the TGZMP to fabricate ion controlled diodes (ICD) (5,6). A corperation was initiated between NASA Goddard and the University of Pennsylvania to develope a TGZMP apparatus that then matured into the current contract to make a small x-ray detector array. These diode arrays have been fabricated, tested, and evaluated. The results indicate that it is possible to exercise control over some of the critical processes. The results both here and NASA Goddard indicate that TGZMP diode arrays have attractive features including very good resolution as x-ray spectrometers.

II. PRINCIPLES OF X-RAY DTECTION

When a charged particle or photon passes through a semiconductor like silicon, the overall significant effect is the production of many electron-hole pairs along the track of it (7,8). The production process may be either direct or indirect, in that the particle produces high-energy electrons which subsquently lose their energy in producing more electron-hole pairs. Regardless of the detailed mechanism involved, the quantity of practical interest for detector application is the average energy expended by the primary charged particle or photon to produce one elctron-hole pair. This quantity, often loosely called the "ionization energy" and given the symbol E_i , is experimentally observed to be largely independent of both the energy and the type of the incident radiation (9,10). The ionization energy of silicon is found to be $3.55 \sim 3.60$ eV at room temperature (9,10,11, 12). At lower temperatures, the energy gap between conduction band and valence band of silicon increases. Thus, the energy required to produce an electron-hole pair in silicon increases a little bit to $3.75 \sim 3.80$ eV for temperature region between 77°K and 90°K (13,14).

From the theory of P-N junction (15), a depletion region almost completely depleted of carriers is formed between P and N type materials when a reverse bias is applied on the junction. Across this depletion region there is a large electrical field due to charge redistribution. When charge particles or photons are incident on this depletion region, many electron-hole pairs will be generated. These generated carriers are then immediately swept by the eledtric field to the appropriate electrode of the diode where they are collectd.

When a diode is reverse biased across its junction, it can be treated as a parallel plate capacitor with junction capacitance

$$C_j = \epsilon_{Si} \cdot \frac{A}{d} \qquad (1)$$

where ϵ_{Si} is the permitivity of silicon, A is the area of the junction, and d is the width of the depletion region (15).

For an step graded P^+-N junction, the width of the depletion region can be written as

$$d = \left(\frac{2 \cdot \epsilon_{Si}}{q \cdot N_D} \right)^{1/2} = (2 \cdot \epsilon_{Si} \cdot \rho_N \cdot \mu_N \cdot (V_R + \phi_B))^{1/2} \qquad (2)$$

where q is the charge of an electron, N_D is the doping concentration of the N type material, ρ_N is the resistivity of the N type material, μ_N is the mobility of the electron, and V_R is the reverse bias across the junction (15). (ϕ_B is the built-in voltage across the junction.)

From Eq. (1) and (2),

$$C_j = A \cdot \left(\frac{q \cdot \epsilon_{Si} \cdot N_D}{2 \cdot (V_R + \phi_B)} \right)^{1/2} \qquad (3)$$

When V_R is large compared to ϕ_B, we obtain

$$d \propto (\rho_N \cdot V_R)^{1/2} \qquad (4)$$

Similarly, for a linearly graded P-N junction (15),

$$C_j \propto (V_R)^{-1/3} \qquad (5)$$

$$d \propto (\rho_N \cdot V_R)^{1/3} \qquad (6)$$

The energies of x-rays range from 5 KeV to about 1 MeV.

With these kinds of photons incident on the reverse biased P-N junction, the number of electron-hole pairs generated by each photon in the depletion region (If this photon fully stops in this region.) is

$$N = f \cdot \frac{E_{x\text{-ray}}\ (eV)}{E_i\ (eV)} \qquad (7)$$

where $E_{x\text{-ray}}$ is the energy of the x-ray photon, E_i is the ionization energy discussed before, and f is a factor related to the collection efficiency of the diode (16).

The charge collected by the diode for each photon is

$$Q = f \cdot N \propto E_{x\text{-ray}} \qquad (8)$$

Therefore, the charge generated is proportional to the energy of the incident photons. By measuring the amount of charge collected by the diode due to x-ray the energy of the corresponding x-ray can then be determined.

The whole radiation detection system is shown in Figure 1. (7).

Besides the detector, the system consists of three main parts:

(a) Preamplifier

The fast charge pulses generated in radiation detectors will first be collected by a following charge sensitive preamplifier. In order to assure that complete charge collection occurs, this preamplifier is normally adjusted to provide a decay time for the pulse which is quite long (typically 50 to 100 µs). The leading edge of the output pulse from the preamplifier corresponds to the time over which the charge produced by the detector is integrated across the capacitance of the collection circuit. Therefore, the time characteristics of the leading edge are determined exclusively by the charge collection

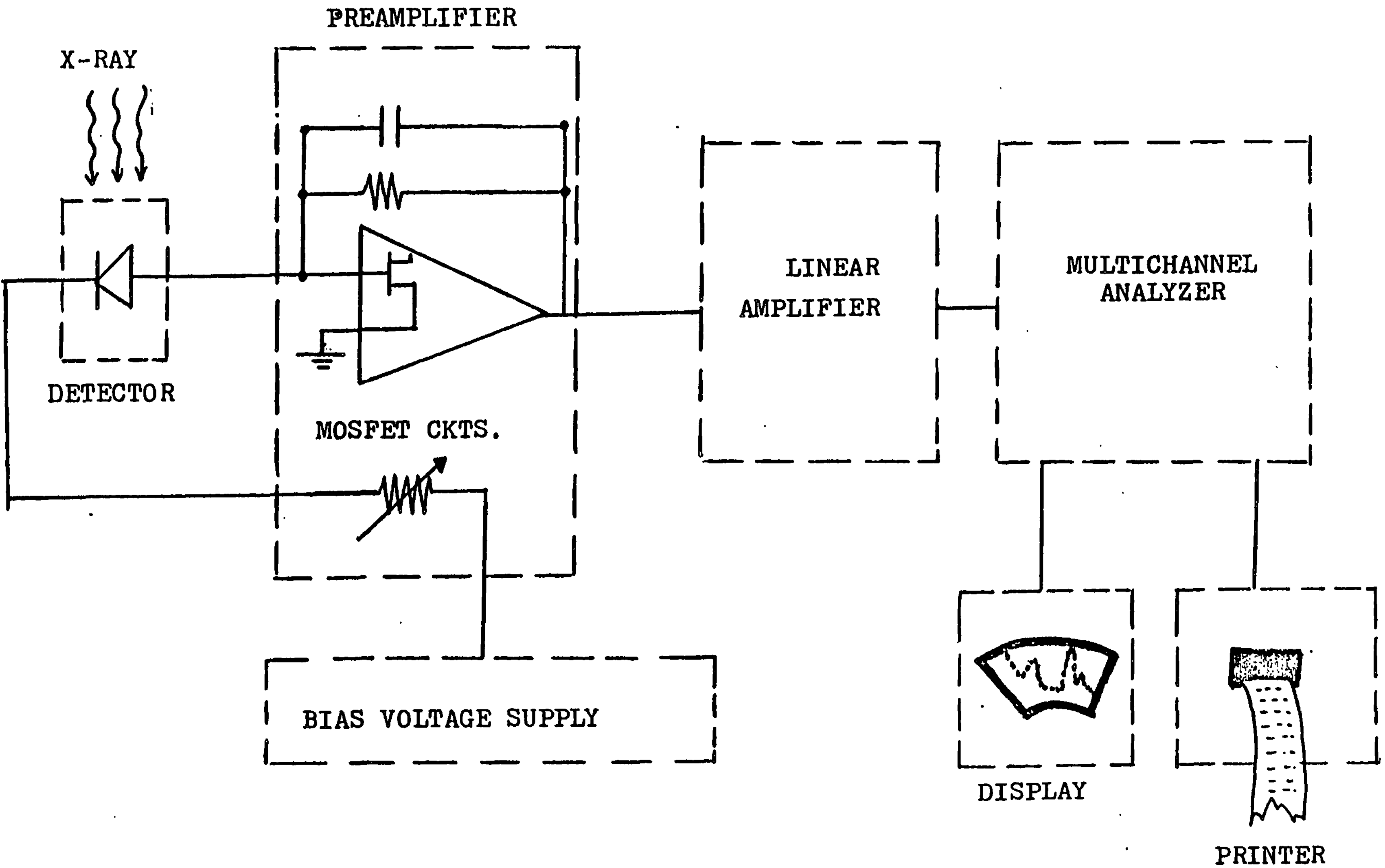


FIGURE 1. Block Diagram Of Radiation Detection System.

time within the detector. But the decay or return to zero of the pulse is determined by the time constant of the collection circuit in the preamplifier. This time constant must be large compared with the detector charge collection time, which might be a function of the device geometry, so that full collection of the charge from detectors with widely different collection times can occur before significant decay of the pulse sets in. Therefore, such pulses generated from the preamplifier as shown in Figure 2. (a) have a long tail compared with their leading edge, giving rise to the name "tail pulse". The preamplifier has a high impedance MOSFET as its input stage to reduce the noise level. It is cooled down to liquid temperature together with the detector in the detection experiment, which will be discussed in section IV.

If the rate of interaction in the detector is not small, thses pulses will tend to overlap one another and give rese to a pulse train which has the apperance shown in Figure 2.(b). Because it is the amplitude that carries the basic information (the charge Q deposited in the detector), the "pile-up" of pulses on the tails of preceeding pulses which have not fully decayed to zero can be a serious problem. Because the time spacing between nuclear pulses is random, each pulse can be superimposed on a different residual tail and the resulting amplitude no longer is a good measure of Q from that event. The method used to solve this problem is to shape the pulses in such a way to produce a pulse train similar to that shown in Figure 2.(c) by using CR differentiator - RC integrator shaping networks (7,8), which is part of the next circuits-linear amplifier. In Figure 2.(c), all the long tails have been eliminated but the information carried by the

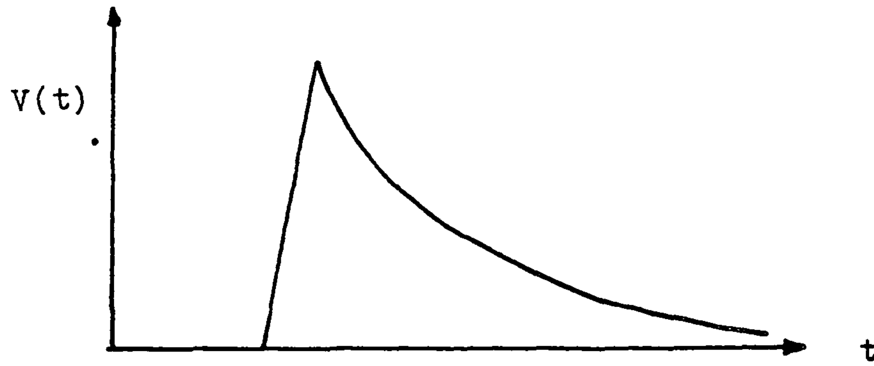
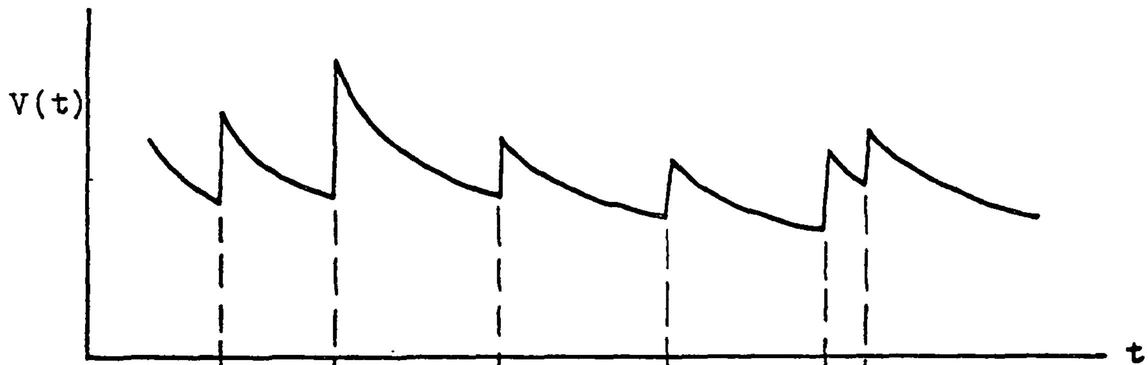
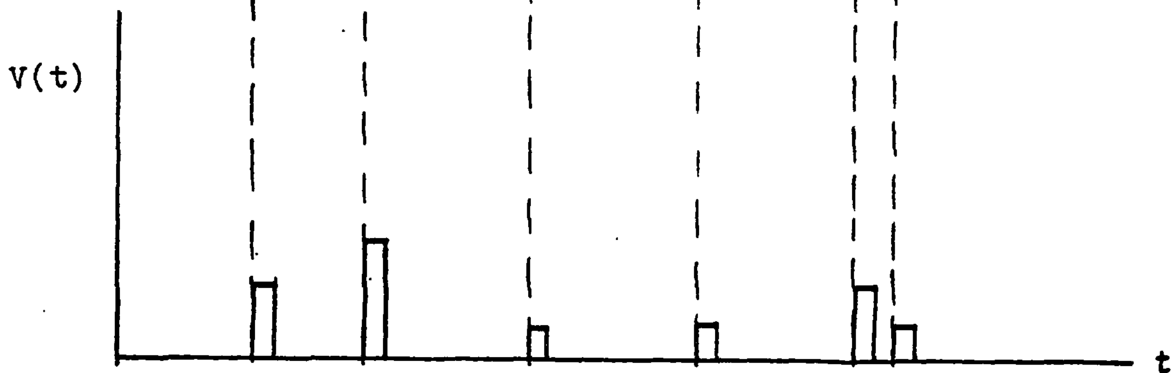


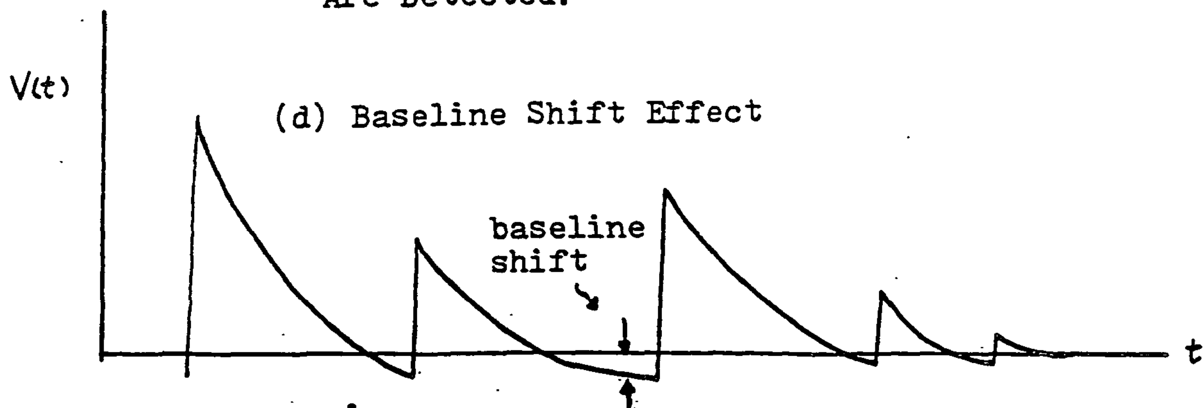
FIGURE 2. (a) Output Tail Pulse from the Preamplifier.



(b) the Pile-Up Effect of the tail pulses



(c) Only the Relative Amplitudes of the Voltages Are Detected.



(d) Baseline Shift Effect

maximum amplitude of the pulse has been preserved. The pulses have been shaped in the sense that their total length has been drastically reduced but in a way that does not affect the maximum amplitude. "Pile-up" problem also introduces the shift of the baseline as shown in Figure 2.(d). This can be solved by using baseline restorer, which will not be discussed here.

(b) Linear amplifier

The proper choice for the time constant of the shapping circuits mentioned above depends primarily on the charge collection time in the detector being used. In the interest of reducing pile-up, one would like to keep these time constants short so that the shaped waveform can return to the baseline as quickly as possible. On the other hand, once the shaping time constants become comparable with the rise time of the pulse from the preamplifier, the input to the network no longer appears as a step voltage and some of its amplitude is lost. This loss is called the ballistic deficit and can be avoided by keeping the time constants long compared with the charge collection time in the detector. Typical values for the time constants of CR-RC circuits vary from a few tenths of a microsecond for use with very fast semiconductor diode detectors, to tens of micorseconds, more suitable for some types of proportional counters in which the charge collection time can also improve the signal-to-noise ratio by limiting the response of the instrumentation to those frequency ranges in which the signal has useful components.

Besides pulse shaping, linear amplifier has another function of providing enough amplification to match the input span for which the multichannel analyzer

has been designed. Here a voltage gain of 1000 or more can be provided so that the shaped pulse at its output can easily cover a span of 0-10 volts. It is the shaping function of the linear amplifier that often dominates the performance of the pulse processing system.

(c) <u>Multichannel analyzer</u>

Two sets of circuits are included in the analyzer:

(1) <u>Discriminator</u>

In order to count the generated pulses properly, the shaped linear pulses must be converted into logic pulses. A defferential discriminater with two discrimination levels produce a logic output pulse only if the input pulse (from linear amplifier) amplitude lies between the two levels. By using a series of this circuit the bands of amplitudes or "windows" can be selected in one of which the input amplitude must fall in order to to produce an output pulse.

(2) <u>Counter</u>

As the final step in a counting system the logic pulses must be accumulated and their number recorded over a fixed period of time. The device used for this purpose is a digital counter. The counter system is preset to a specified number. The counting period is terminated when the number of accumulated pulses has reached this value. By designing like this a given statistical precision can be specified before the start of the measurement and the duration of counting will be prolonged until enough counts have been accumulated to guarantee the desired statistical precision.

Finally, the collected data are displayed on a oscilloscope screen and can also be printed out from a printer.

III. FABRICATION PROCEDURES

Temperature Gradient Zone Melting Process (TGZMP) has been successfully used for making ion controlled diodes (5,6). Some of the processes involved in the fabrication were not well enough controlled. In making x-ray detedtors, essentially the same procedures were followed for fabricating ICD, but better control was exercised over each individual process step.

(a) Sample preperations

Three kinds of wafers were prepared as shown in Table 1. N-type silicon was chosen because aluminum doping would form P-N junctions. (100) orientation was chosen for potasium hydroxide (KOH) preferential etching. The high purity silicon (1550 Ω-cm) wafers were provided by NASA. They proved to be very suitable for x-ray detectors because of their wide depletion region width, long lifetime, and high breakdown voltage. Also it was found that with wafers having both sides polished, better P-N junctions could be more readily obtained.

Each wafer was given an initial and basic cleaning (Appendix A). Considerable care was exercised in these processes because any thermal stress or scratch during cleaning would kill the lifetime of the devices.

(b) Substrate contact by phosphorous diffusion

N^+ ohmic contacts were made to the substrate material by phosphorous diffusion. The spin-on phosphorous dopant solution used is called Accuspin P-120 and is made by Allied Chemical Company. First, 7-9 drops of P-120 were spun on to the backside of each wafer to form a source film. The thickness of this film was about 2500 Å when spin speeds of 3000 r.p.m. were used. A 30 minute prebake at 120°C followed in order to drive off the excess solvent vechicle and harden the film. Upon completion, the same precedures were repeated on the

TABLE 1

RESISTIVITY (Ω-cm)	DOPANT TYPE	DOPONT CONCENTRATION (cm^{-3})	ORIENTATION	THICKNESS (mil)	SURFACE CONDITION
6	N	$7.4 \cdot 10^{15}$	(100)	10	one side polished
12	N	$3.7 \cdot 10^{15}$	(100)	10	one side polished
1550	N	$3 \cdot 10^{12}$	(100)	15	both side polished

front surface.

The diffusion was done in an open system flushed with N_2 and O_2. The diffusion temperature was 1100°C and the time was 50 minutes. The conditions for gas flow were

N_2 (1.5 liters/min) for the first 40 minutes
N_2 (1.5 liters/min) 5% O_2 (75 c.c./min) for the last 10 minutes

After diffusion the wafers were dipped in buffered hydrofluoric acid (BHF) solution for 5 minutes to remove the glass film. The four point probe technique was used to measure the sheet resistance and the results are listed in Table 2.

The data listed in Table 2. is in agreement with those provided by the company. The thickness of this diffused layer is about 2 um, so the surface impurity concentration is approximately 6×10^{20} atoms/cm^3.

(c) Thermal oxidation

Following the diffusion an oxide layer is grown. The dry oxidation was done at 1080°C for one hour and forty-five minutes. After oxidation, the interference color of the oxide film was metallic blue. This oxide layer is used to mask the KOH preferential etching of the silicon, so therefore its electrical quality is not very important. However, the thickness range which gives the optimal condition is from 1200 Å to 1500 Å.

(d) Aluminum evaporation

The evaporation was done in a vacumn evaporator at a pressure of 6×10^{-7} torr. The aluminum slugs were melted in boron nitride boats by a tungston coated heater. The thickness of the aluminum is a very important parameter in thermal migration. Usually, the thinner the aluminum is, the longer it

RESISTIVITY OF WAFER (Ω- cm)	SHEET RESISTANCE ($\Omega/\square$)
6	4.7
12	5
1550	7

TABLE 2.

takes to penetrate through the wafer. The longer thermal processing time might be bad for devices especially like our radiation detectors because the radiation keeps on damaging the surface. Conversely, if the aluminum is too thick, it will migrate through the silicon very quickly usually causing a smearing-out effect which will cause large leakage current through the junctions. The optimal condition is to evaporate aluminum dots 5 to 6 μm in thickness.

In order not to contaminate the aluminum after it is evaporated on to the wafer, mechanical masks were used to define the pattern directly. Molybdenum sheets with dimensions 2" by 2" by 0.003" were covered by KODAK negative photoresist and then etched by molybdenum etchant at room temperature to get the patterns (Appendix B). The Al patterns have twenty-five 2 by 2 diode arrays on a two inch wafer. The area of each Al dot is $(150 \mu m)^2$.

(e) Aluminum migration by T.G.Z.M.P.

The TGZMP is a process in which a liquid zone in the form of a sheet, rod, or droplet migrates through a solid in a temperature gradient. The migration of the liquid zone is caused by three spatially sequential process: dissolution of the solid on the hot forward side of the zone; diffusion transport of the dissolved silicon to the cold rear side of the liquid zone; deposition of the silicon-aluminum alloy on the cold rear surface.

The experimental apparatus used in TGZMP is shown in Figure 3. It consists of two major parts: the light source and the heat sink. The light source consists of a water cooled reflector main cavity which houses six QHI 1200T3/CL quartz infrared lamps (General Electric) in parallel. The lamps are cooled by flushing air through the cavity. The cavity is covered by a piece of quartz. The heat sink is a water cooled copper chamber whose surface is covered by a layer of carbon paint to avoid reflection. The surface of the heat sink is 2 cm directly under the light source. On top of the sur-

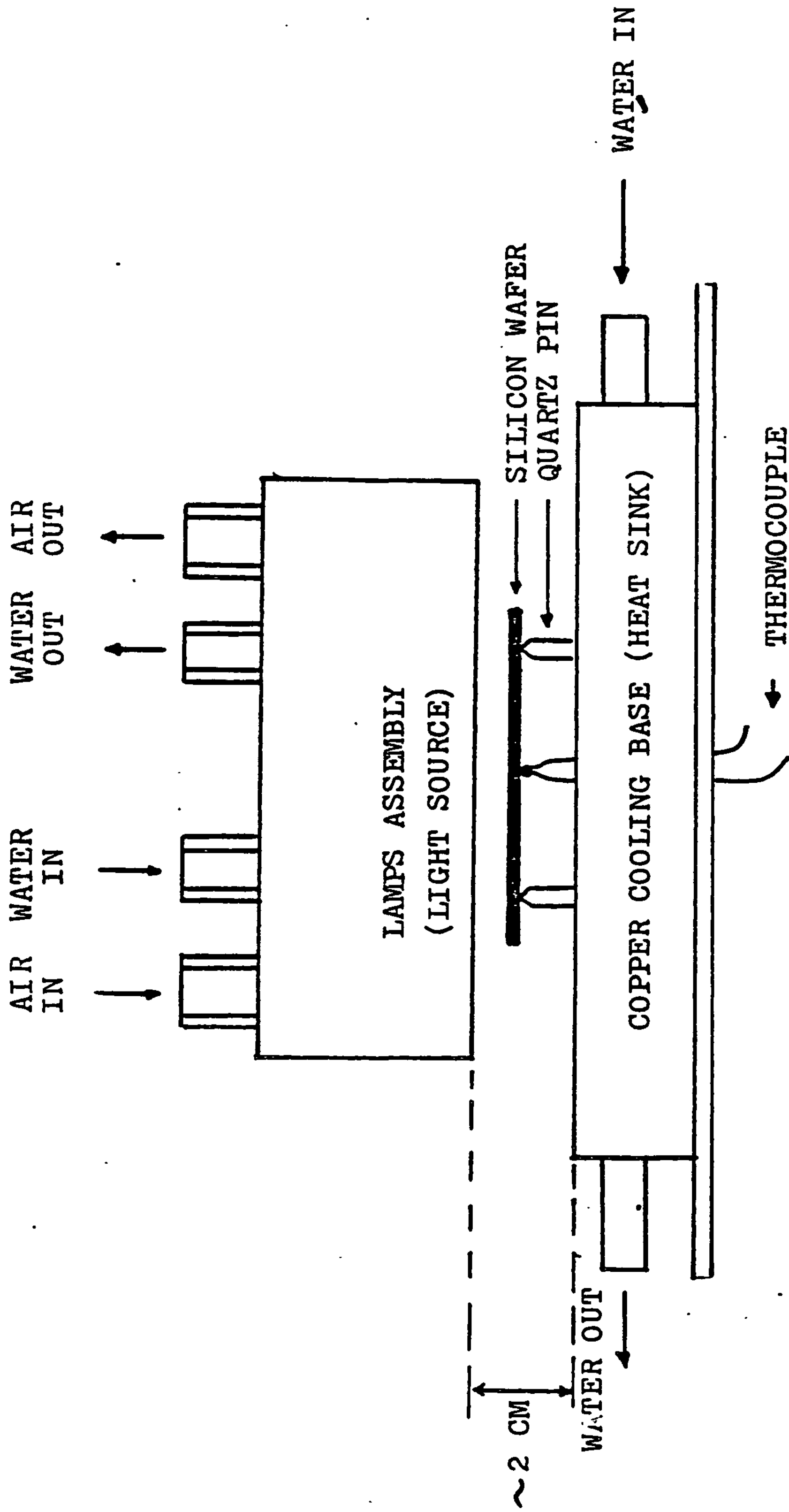


FIGURE 3. APPARATUS FOR TEMPERATURE GRADIENT ZONE MELTING PROCESS (TGZMP)

face, thin quartz pins 1.5 cm long are used as supports for the silicon wafer, which is placed directly on top of them. The surface of the silicon with aluminum pattern is placed face down to the cooling base. The temperature was measured by a chromel-alumel thermocouple (usable range: -180°C to 1260°C) directly contacting to the back surface of the wafer.

The electrical circuit of the TGZMP facility is shown in Figure 4. The three phase AC voltage is controlled by a three phase variac driven by a synchronous. The output of the variac is rectified by a diode bridge as shown in the figure. The DC voltage is then supplied to the lamps.

The temperature gradient across the silicon wafer is about 200°C/cm. The 150 μm wide aluminum dots can be stably migrated through the silicon wafer in eighteen minutes and fifteen seconds including 4'50" rise time and 5'15" fall time. The slow rise and fall times were necessary to avoid warping of the wafer and the consequent introduction of defects which would reduce the lifetime. The fall time began when most of the aluminum dots had migrated through the wafer.

The temperature-time and power density-time profiles are shown in Figure 5. (a) and (b). When logarithm of power density versus temperature is plotted, a linear relationship is obtained for both rise and fall periods as shown in Figure 6. This relationship can be expressed as

$$\text{Power Density} = \text{constant} \times 10^{k\cdot(\text{temperature})} \quad (9)$$

where k is a constant ranging from 0.52 to 0.57. This expression satisfies the differential equation

$$\frac{dP}{dT} = k \cdot P \quad \text{or} \quad \frac{dT}{dP} \cdot P = \frac{1}{k} \quad (10)$$

where P is the power density and T is the temperature of the

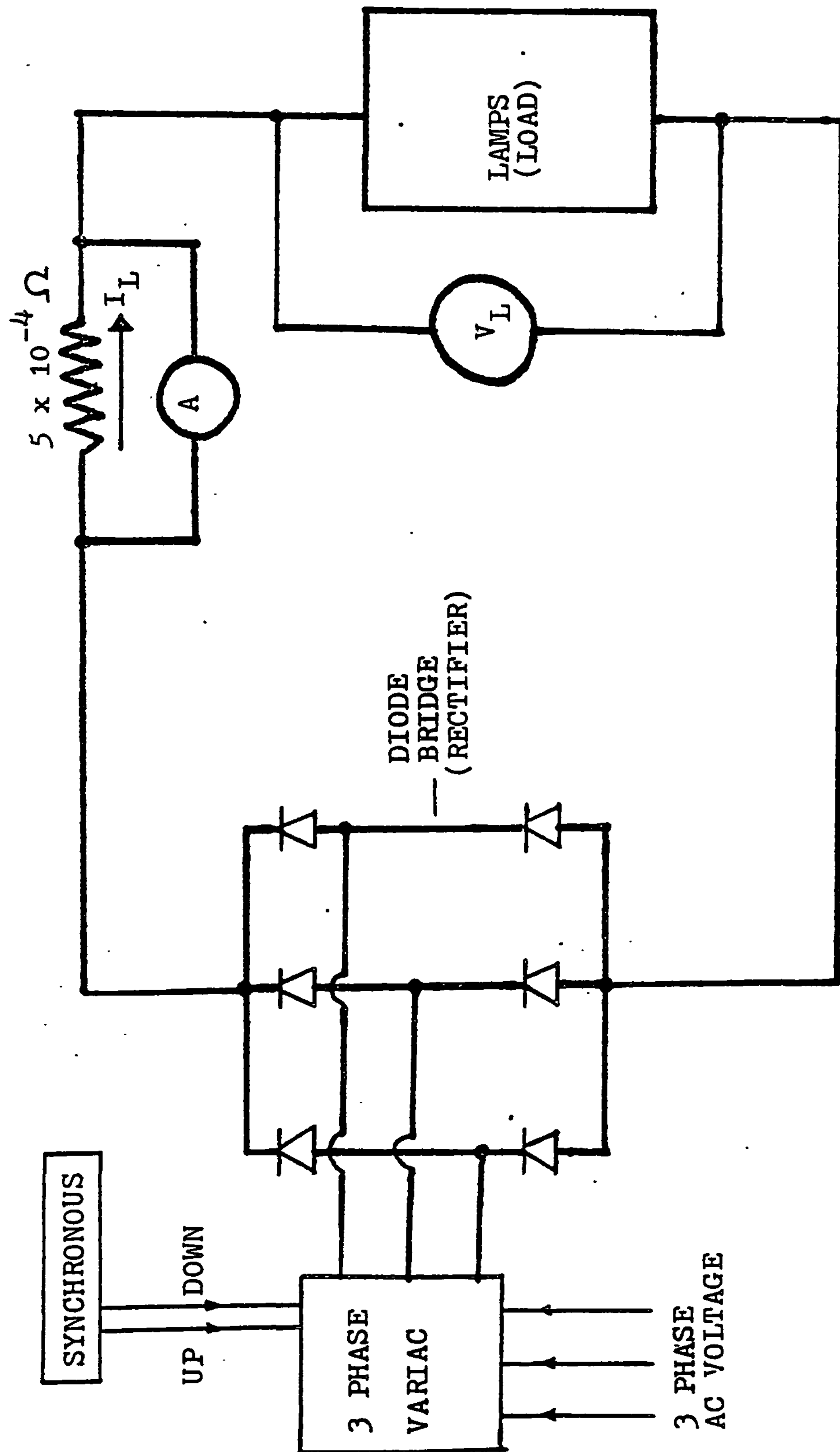
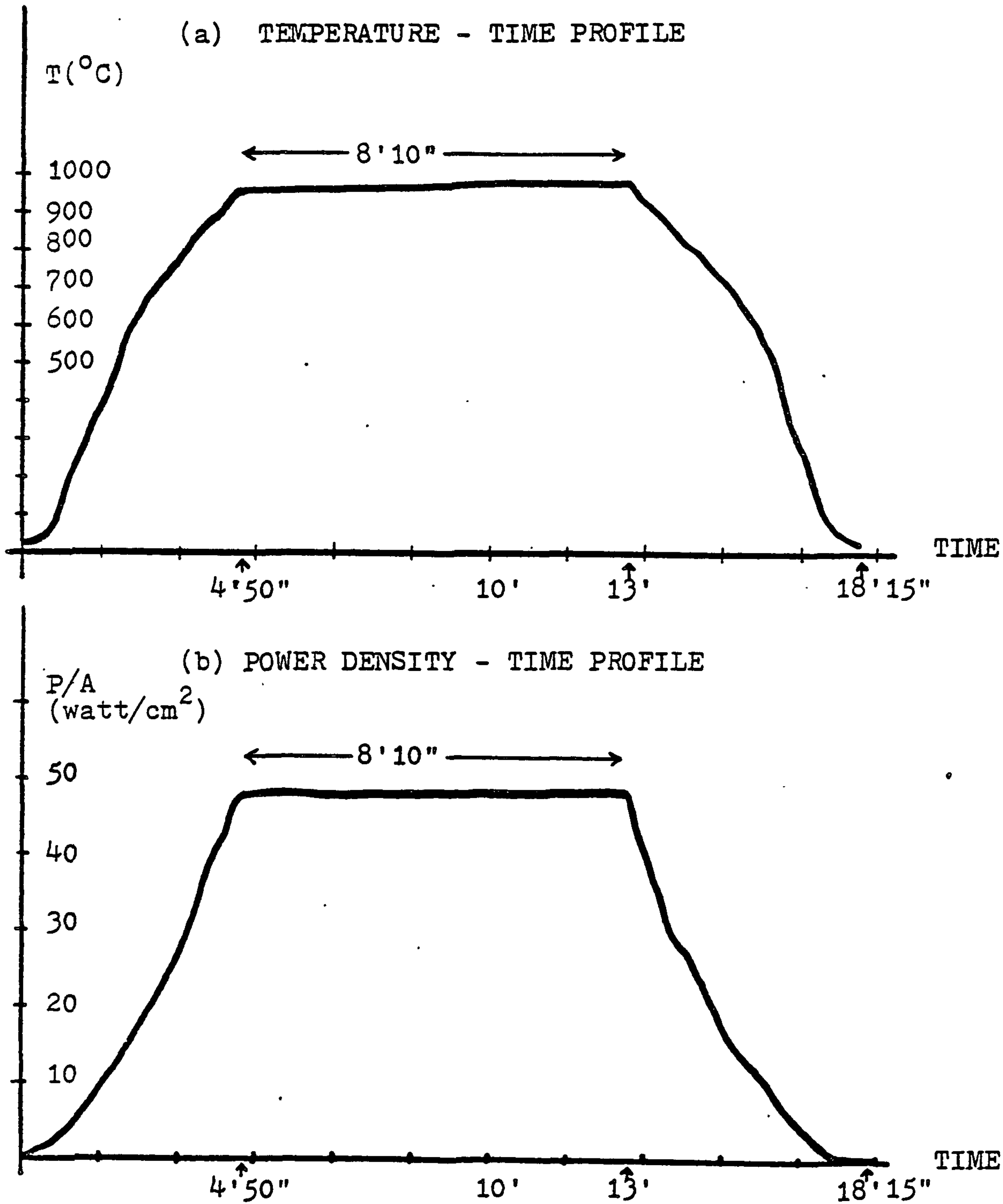


FIGURE 4. Electrical Circuit of the Apparatus for TGZMP

FIGURE 5.



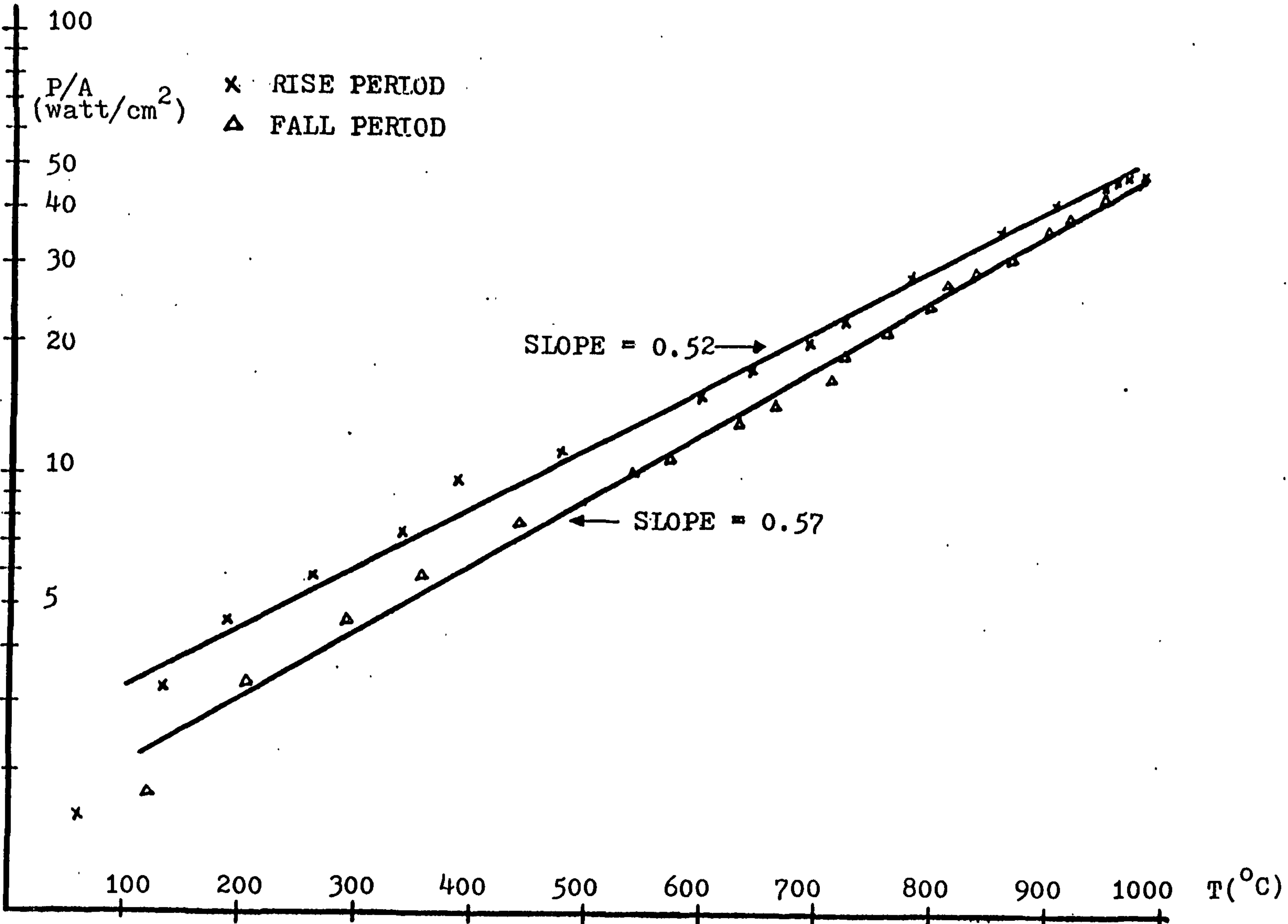


FIGURE 6. LOGARITHM OF POWER DENSITY VS. TEMPERATURE

wafer. The input power will have to be one hundred times larger in order to double the temperature of the sample.

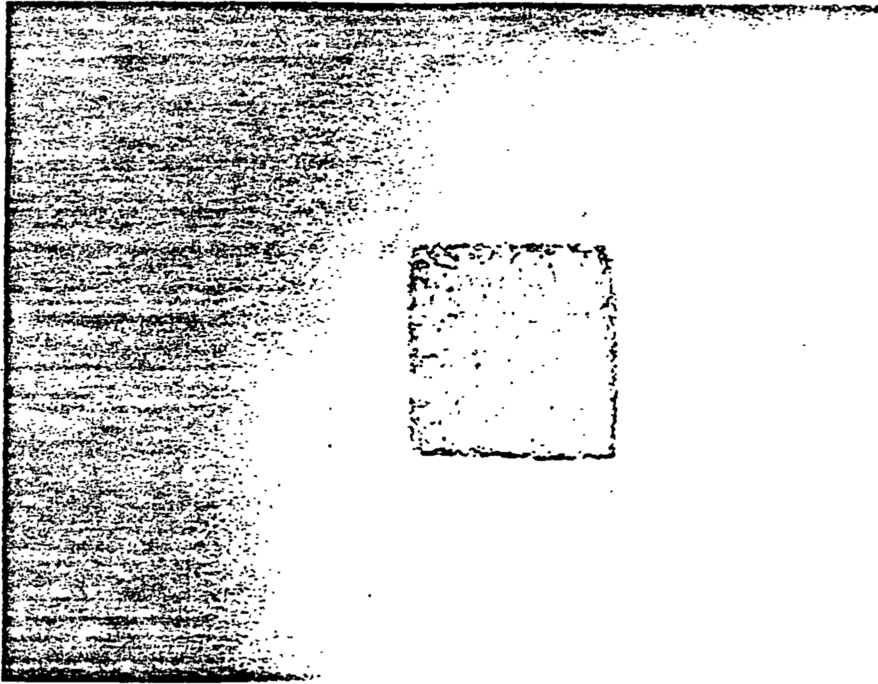
During the thermal migration, the aluminum dot continues to travel in the wafer along the direction of maximum thermal gradient . Its concentration keeps on decreasing along the path. When the migration is completed, the zone near the back surface is filled with aluminum-enriched silicon while the zone near the front surface is filled with silicon-enriched aluminum. This is why the KOH etchant can etch the back zone of the P^+ region even when there is no window opened on SiO_2 layer at the back surface. We can see some mullite covering the P^+ region on both surfaces after thermomigration. This might be due to the contamination from the environment.

The pictures preceeding and following the migration of an aluminum dot through silicon are shown in Figure 7. (a) and (b), respectively. The cross section views of the P-N junction after migration are shown in Figure 8. (a) and (b). These pictures were taken by Siamak Azizi who was a graduate student here.

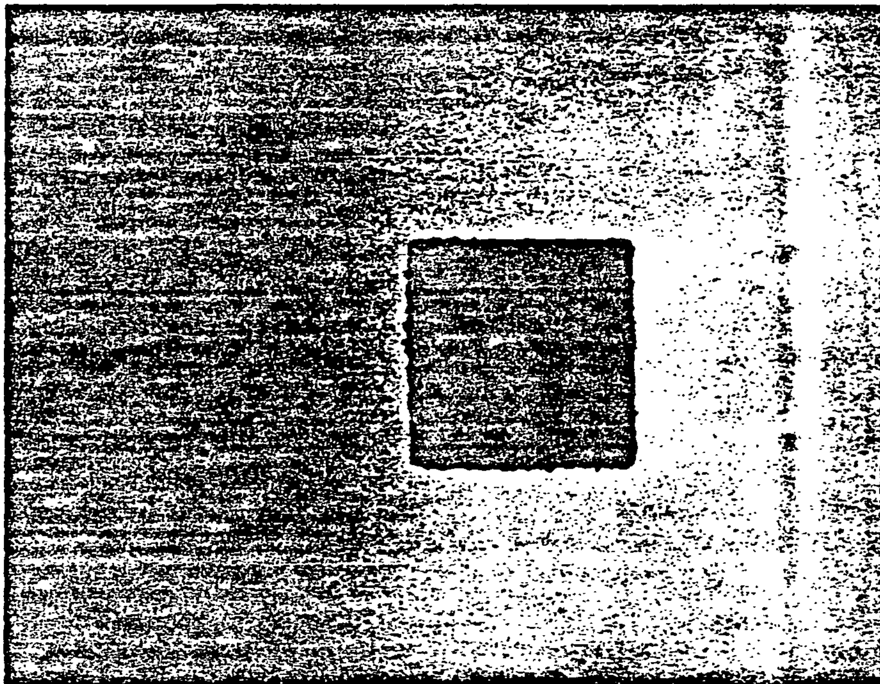
TGZMP is the most critical process step for the fabrication of x-ray detectors. Because of the nature of the heat source, this is also the hardest step over which to get control. The reasons are:

(i) The thermomigration was done at atmospheric pressure and the convective heat loss can be quite variable. Also because of this, the surface region near the P-N junctions was undoubtedly contaminated. The extent of this contamination was not studied in this work.

(ii) Since the temperature distribution was not uniform, thermal stress was introduced and lateral migration occurred in the wafer. This has been experienced

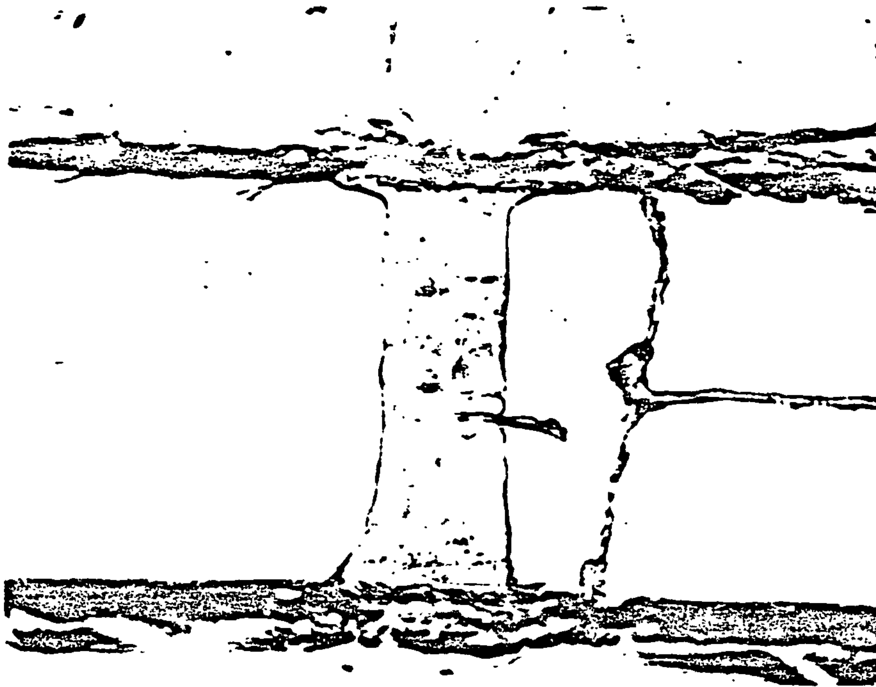


(a) Aluminum Dot Before Thermal Migration

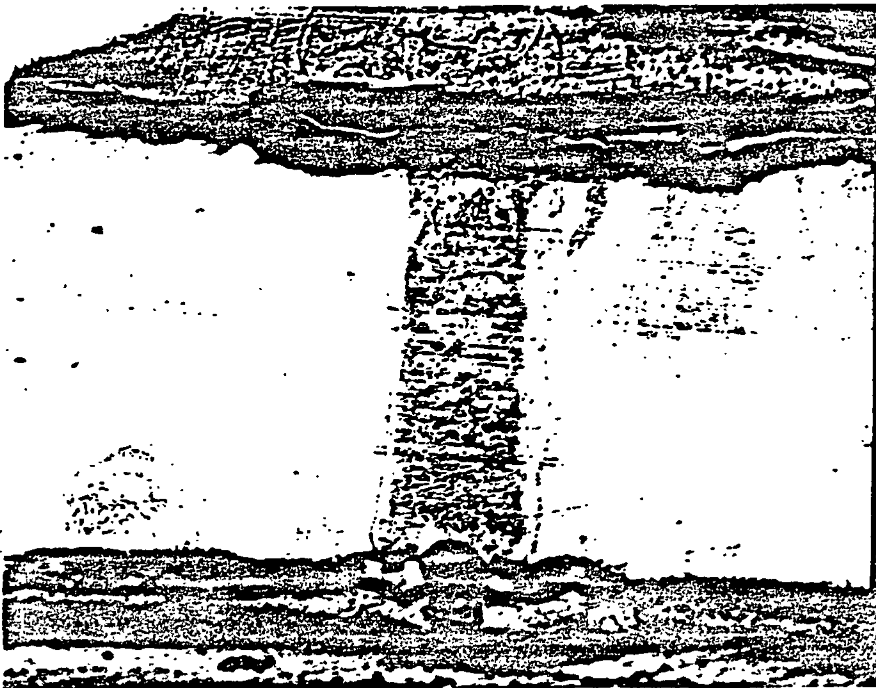


(b) Aluminum Dot After Thermal Migration
(The background is the silicon wafer.)

FIGURE 7.



(a) Lateral View of the P^+ Region
(The "T" shape lines are due to the crack of the sample holder.)



(b) Cross Section View of the P^+ Region
(We can see a little lateral diffusion from the P^+ region.)

DIRECTION OF THERMOMIGRATION →

FIGURE 8.

from the warping of the wafer after migration and seen from the shape of the junction as shown in Figure 8. To solve for the warping problem, thicker wafers (14 to 16 mils) are recommended for processing.

(f) Potassium hydroxide (KOH) preferential etching

Before etching the silicon we first defined windows (750 µm) on both surfaces surrounding the P^+ region by using negative photoresist and buffered hydrofluoric acid.

There are two reasons why we have to etch the silicon itself:

(i) The mullite covering on the P^+ region has to be removed for better ohmic contact and smaller diode leakage current due to surface contamination.

(ii) The N^+ layer beneath the SiO_2 layer has to be removed in order not to short the junction.

Different kinds of etching solutions such as aluminum etchant (Appendix C), isotropic silicon etchant (Appencix D) (17), and anisotropic silicon etchant (Appendix E) (18) were tried and all failed to remove the mullite. Finally, a KOH (25 %) solution in a 4 : 1 ratio with isopropyl alcohol (IPA) was tried at 60°C and the mullite was removed completely in one hour and thirty minutes. In this etchant, KOH has been employed as the oxidant and IPA as a complexing agent. From our experience, it seems as though IPA does not play an important role in the etching because the KOH solution does not mix with IPA. KOH solution etches the 100 surface much faster than it does the (111) surface. The ratio of the etching rates of these two surfaces is about 25 : 1 at 60°C as shown in Figure 9. The etching rate of the (100) surface is about 0.5 µm/min. During the etching process, stirring was used, this was an important factor in getting good P-N junctions. Upon

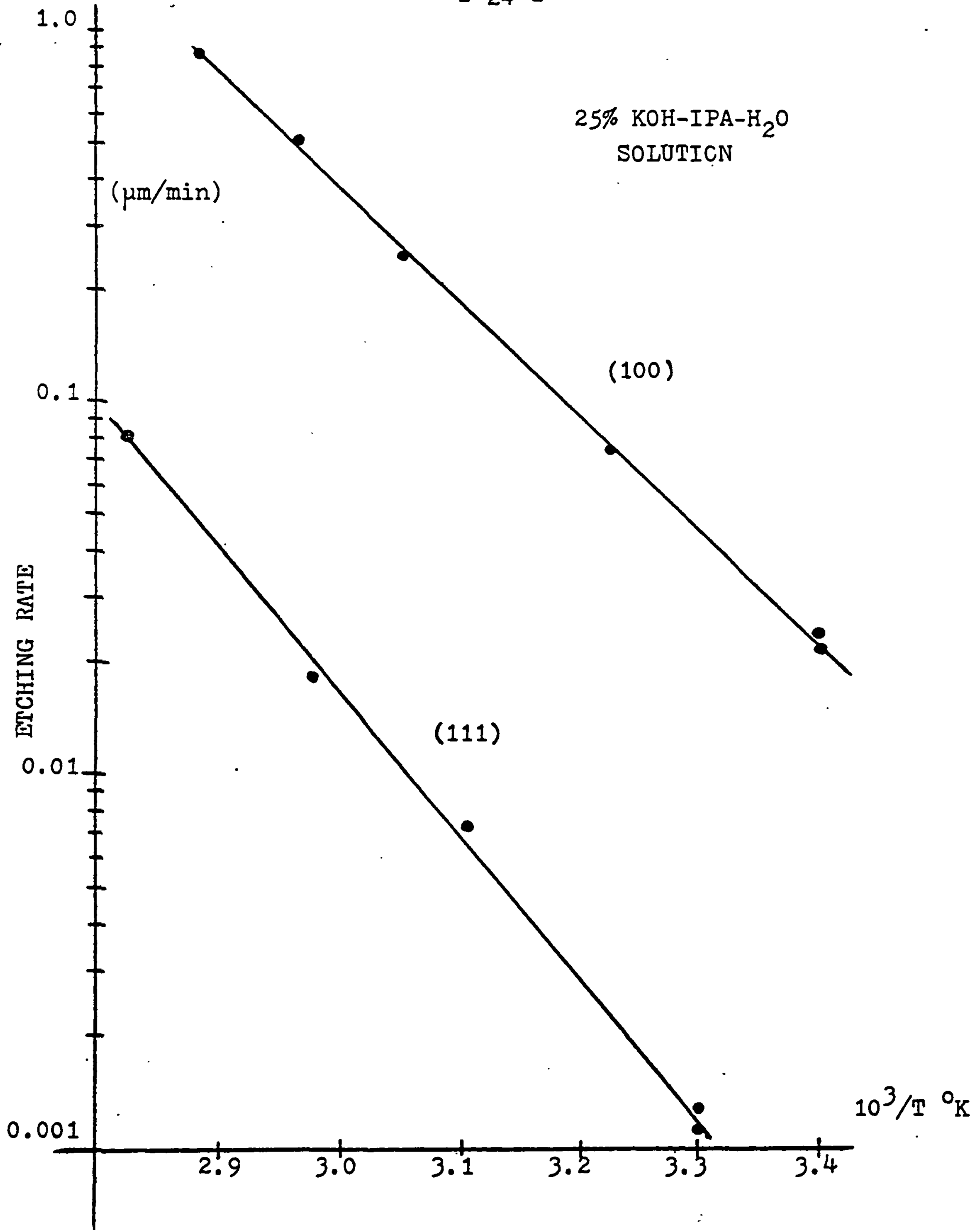


FIGURE 9. Temperature Dependence of the Etching Rate for (100) and (111) Orientations of Silicon (19).

completion of the etching, a very clean and shining P^+ region was left as shown in Figure10. for the front surface and in Figure11. for the back surface. The cross section views are shown in Figure 12.

(g) Wet thermal oxidation

After preferential etching, the SiO_2 layer was removed and the samples went through basic cleaning again (Appendix A). Experience has shown that to passivate the silicon surface an oxide layer of suitable thickness is needed. The purpose of surface passivation is to reduce the leakage current through the surfaces of the junction. Because the aluminum-rich region may melt at high temperature, we should minimize the oxidation temperature and shorten the oxidation time as much as possible. It is because of this that we adopted a low temperature (950°C) wet oxidation process to minimize the lateral diffusion. A 1700 Å thick oxide layer was obtained in an oxidation time of sixty minutes (20).

(h) Shape of the P-N junction

Aluminum is a substitutional dopant in silicon. The temperature dependence of its diffusion constant is

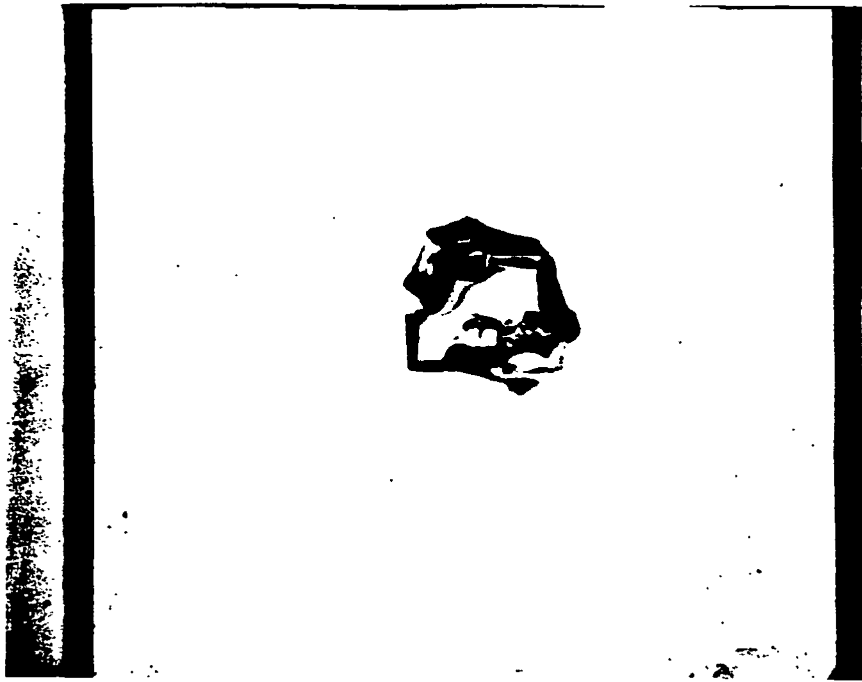
$$D_{Al} = D_{\infty} \cdot \mathrm{Exp}\,(-E_a / k_B \cdot T) \tag{11}$$

where $D_{\infty} = 4.8\ cm^2/sec$ is the diffusion constant of aluminum in silicon at infinitely high temperature, and $E_a = 3.36$ eV is its activation energy (21).

Therefore, for the oxidation temperature and time used the diffusion length is approximately

$$L = \sqrt{D_{Al} \cdot \mathrm{Time}} = 0.16\ \mu m \tag{12}$$

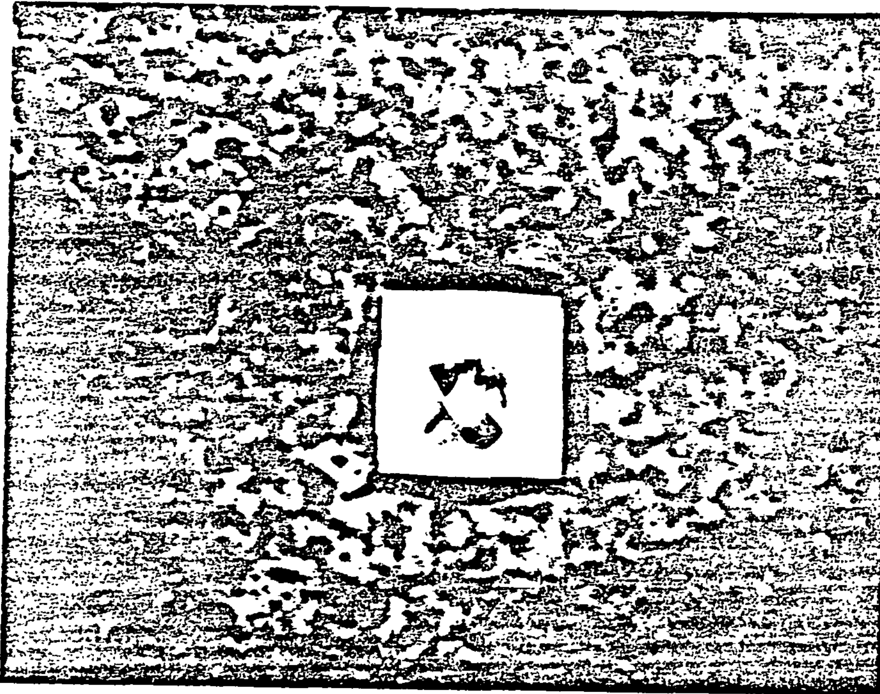
This indicates that the aluminum diffused out to produce a linearly graded junction rather than an abrupt junction.



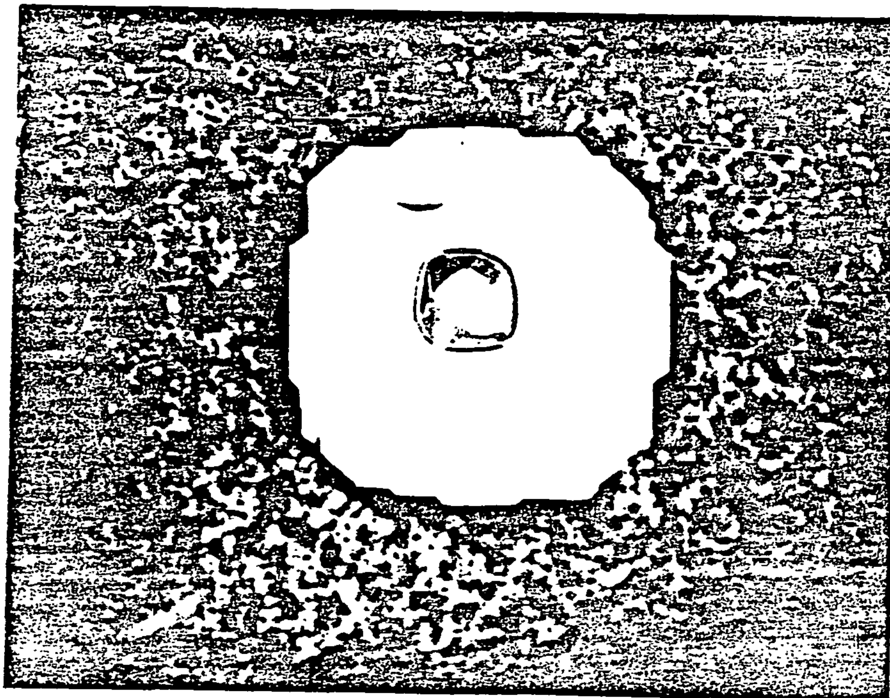
(a)

(b)

FIGURE 10. Top View of P^+ Region After KOH Preferential Etching.



(a)

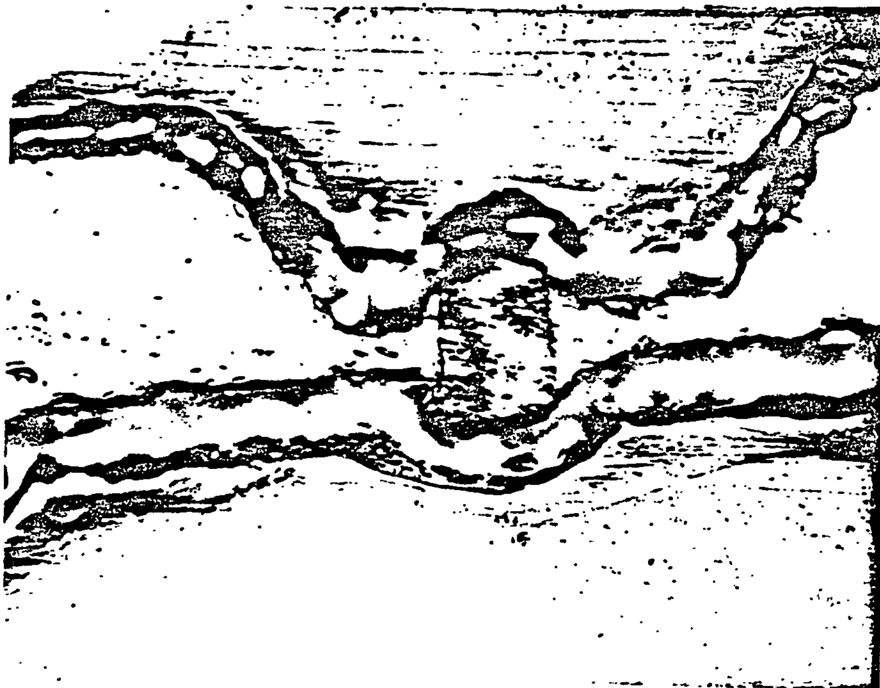


(b)

<u>FIGURE 11.</u> The Views of Back Surface of Silicon Wafers After Preferential Etching. (P+ regions are at the center.)

(a)

DIRECTION OF THERMOMIGRATION



(b) (larger magnification)

FIGURE 12. Lateral Views of P^+ Region After Preferential Etching.

This will be discussed further in Section IV. (b).

(i) Metallization and packaging

The electrical contacts were made to both the substrate and the P^+ region by evaporating thin aluminum layer (about 5000 Å) on to the wafers. An anneal process for aluminum at 435°C for 30 minutes in forming gas (92% N_2 and 8% H_2) is needed to improve the adhesion.

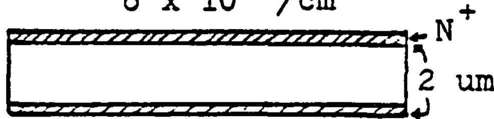
Finally, these two by two diode array chips were scribed and mounted onto ceramic substrates with epoxy. Five gold pads cut from a piece of gold foil were glued on the ceramic substrate. Four of them were connected to the four P^+ regions and the fifth one to the substrate (the N^+ layer). This completes the assembling of the devices.

The whole fabrication process is shown schematically in Figure 11.

(1) Wafer Preparation and Cleaning

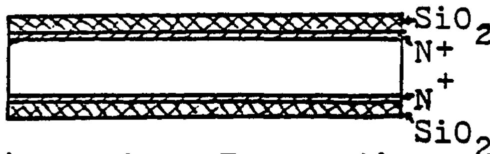
<100>, bothside polished
N type, 1550 Ω-cm

(2) Phosphorous Diffusion
$6 \times 10^{20}/cm^3$



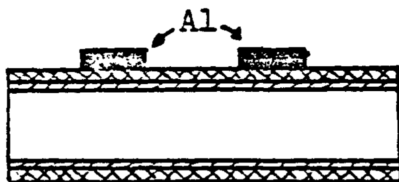
(3) Thermal Oxidation

1500 Å SiO_2

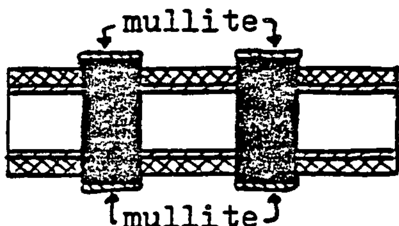


(4) Aluminum Evaporation

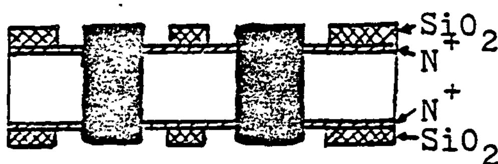
Aluminum: 5~6 um



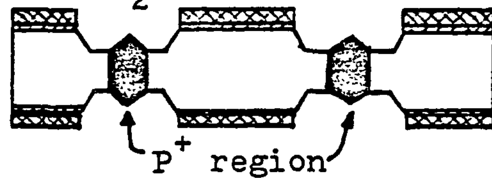
(5) Thermomigration



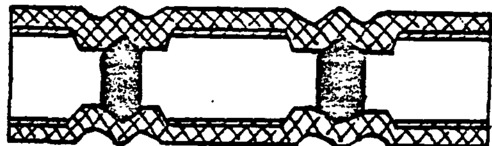
(6) SiO_2 Etching (HF or BHF)



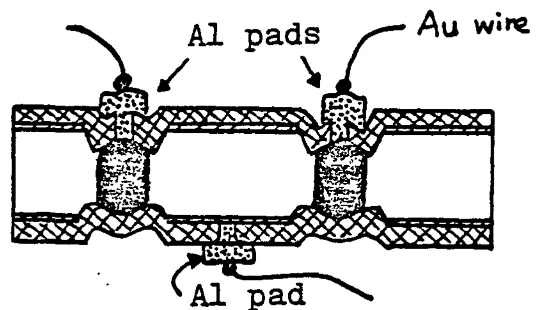
(7) KOH Preferential Etching
25% KOH + IPA, 60°C
$1\frac{1}{2}$ hours



(8) SiO_2 Etching and Wet Oxidation
950°C, 50~60 min
⟹ 1700Å



(9) Metallization and Gold Wire Bonding



(10) Packaging

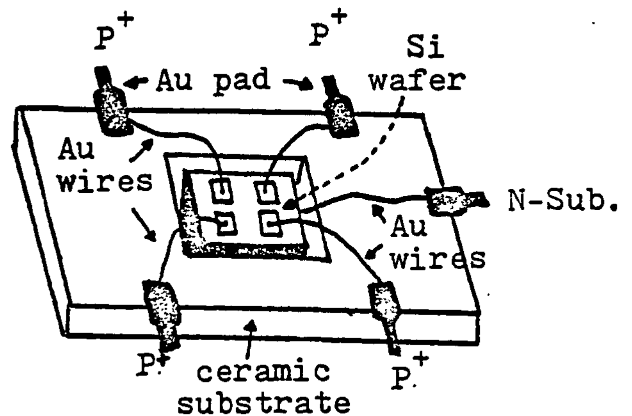


FIGURE 13. Fabrication Procedures For X-Ray Detectors

IV. EXPERIMENTAL RESULTS

(a) Junction evaluations

Different methods are used to evaluate the diode junctions including diode I-V measurements, diode C_T-V measurements, and Metal Oxide Semiconductor (MOS) capacitor measurements.

(i) Dark I-V measurements

The dark current flowing through a reverse biased diode is composed of three separate parts:

(1) saturation current due to diffusion of the minority carriers:

Minority carriers of both P and N type materials near the boundaries of the depletion region can diffuse into the depletion region. They are then swept through this region by the strong electric field. This current can not be controlled by the process and is proportional to the square of impurity concentration of the substrate for both abrupt and linearly graded junctions. So, the higher the resistivity is, the lower this current will be.

(2) generation current in the depletion region: (22)

The generation current is related to the existence of recombination centers, which are due to the impurity atoms or structural imperfections. This current is quite process-dependent because

$$I_{generation} \propto n_i \cdot (\rho \cdot V_R)^{1/3} / \tau \qquad (13)$$

for a linearly graded junction. ρ and τ are the resistivity and lifetime of the substrate and V_R is the reverse bias. If V_R is increased or τ is decreased due to the process, this current

will be increased.

(3) surface leakage current:

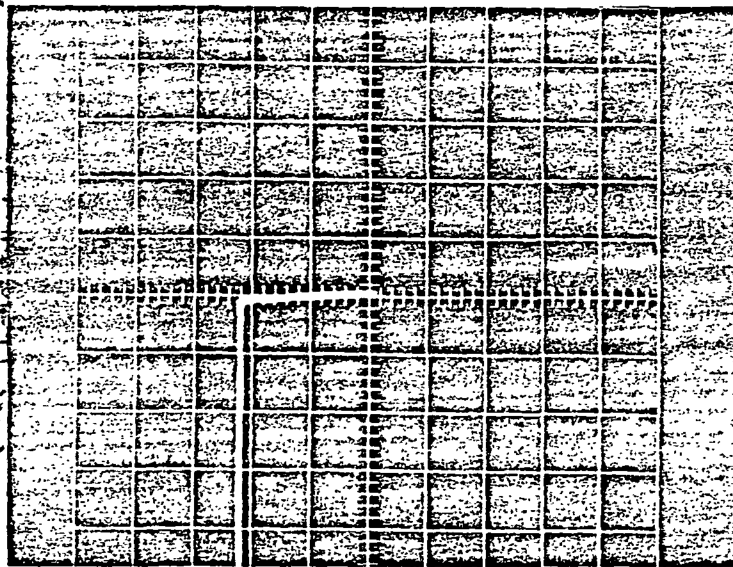
This current is induced by the interface centers near the intersection of the junction and the surface. It is quite process-dependent. Because of the nature of the etching solution used, it is expected that this current would be the dominant factor among all different current contributions. This is one of the reasons why we have to passivate the surface by oxidation.

The reverse bias I-V characteristics of these diodes had been taken before the surface was passivated. They are shown in Figure 14. for three different kinds of wafers. The same characteristics were also measured after the surface had been passivated, metallized, and packaged as shown in Figure 15. for comparisons. For the latter case, the leakage current is always in the nano-ampere region if the bias is not too large.

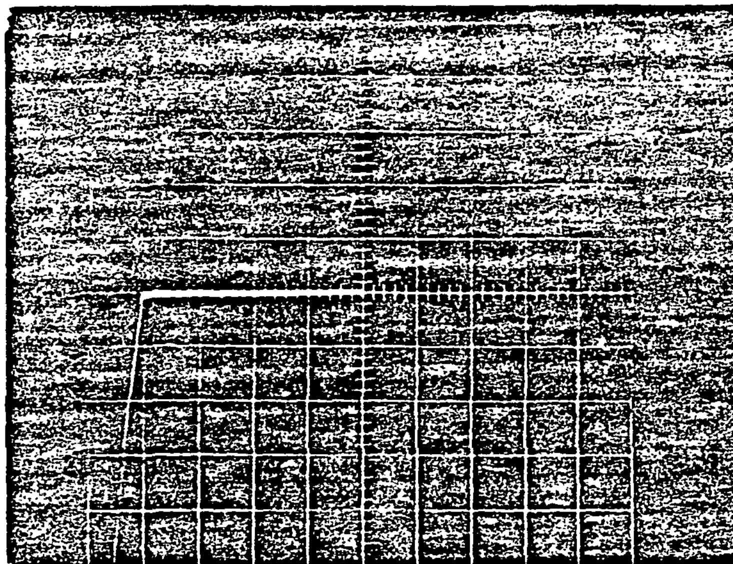
The informations shown in Figure 14. and 15. are again summarized in Table 3. Also listed in the table are the corresponding depletion region widths at the approximate breakdown voltages calculated from Equation (2). (page 3)

(ii) Diode C_T-V measurements:

The trasition capacitances (or space charge capacitances) of diodes under reverse biases were measured after surface passivation. Because of the thermal process involved, such as thermomigration and oxidation, we expect the P-N junction to be linearly graded rather than of the ideally step graded type. Figure 16. (a) shows the C_T-V curve for a diode on

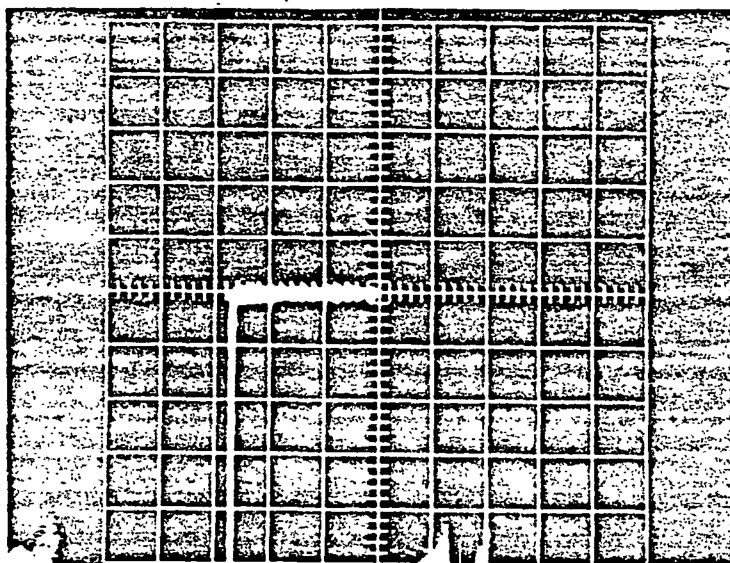


(a) Wafer: 8 Ω-cm.
Breakdown Voltage: -120 volts..
Current Scale: 50 μA/Division.
Voltage Scale: 50 volts/Division.



(b) Wafer: 12 Ω-cm.
Breakdown Voltage: -200 volts.
Current Scale: 100 μA/Division.
Voltage Scale: 50 volts/Division.

FIGURE 14. P - N Junction Characteristics Measured Before Surface Passivation.



(c) Wafer: 1550 Ω-cm.
Breakdown Voltage: -270 volts.
Current Scale: 100 μA/Division.
Voltage Scale: 100 volts/Division.

RESISTIVITY (Ω-cm)	BREAKDOWN VOLTAGE(V) (from Fig. 14.)	DARK LEAKAGE CURRENT(nA) (from Fig. 15.)	DEPLETION REGION WIDTH (μm)
6	120	3.4 at -13 v.	4.6
12	200	0.54 at -13 v.	8.4
1550	270~300	15. at -30 v.	343.4

TABLE 3.

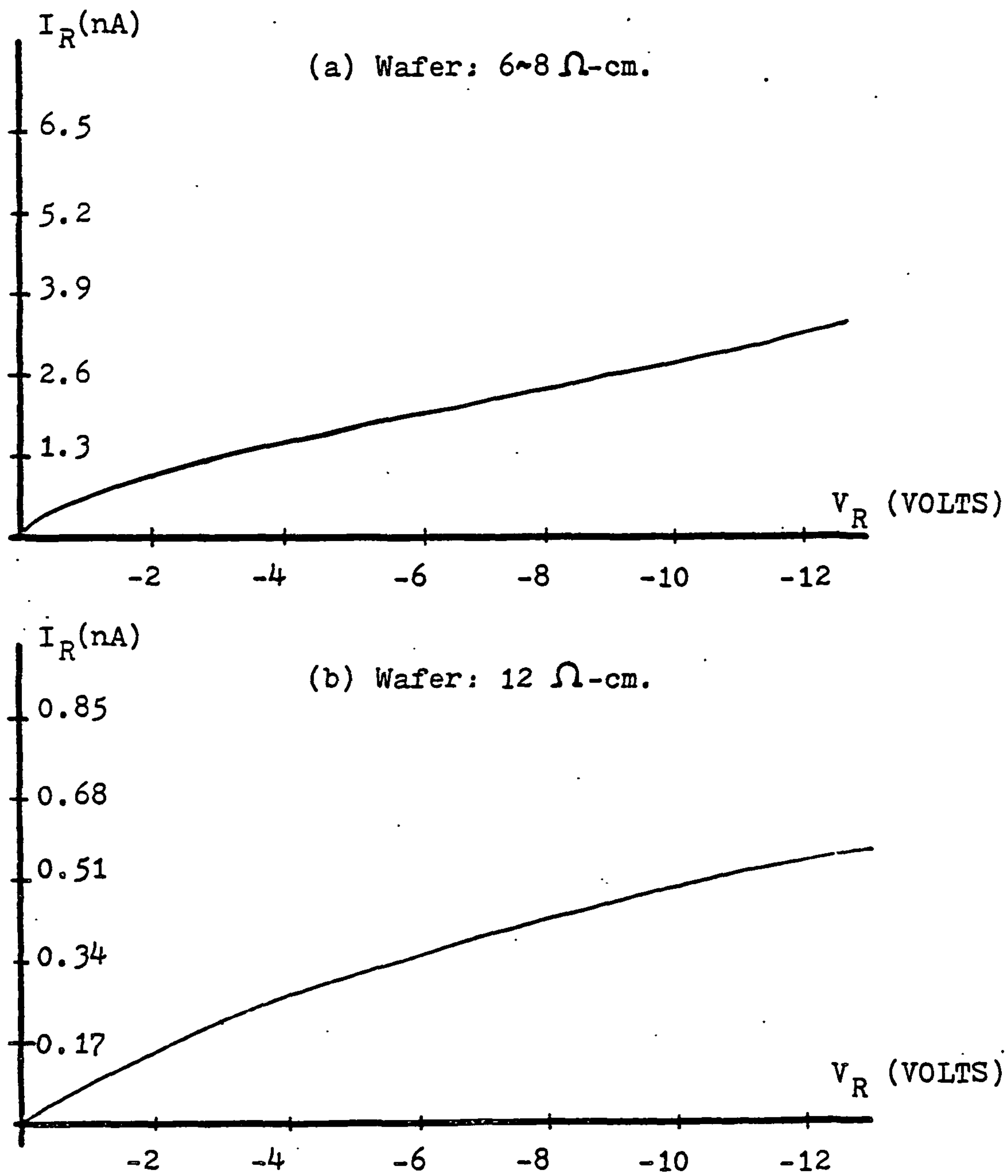
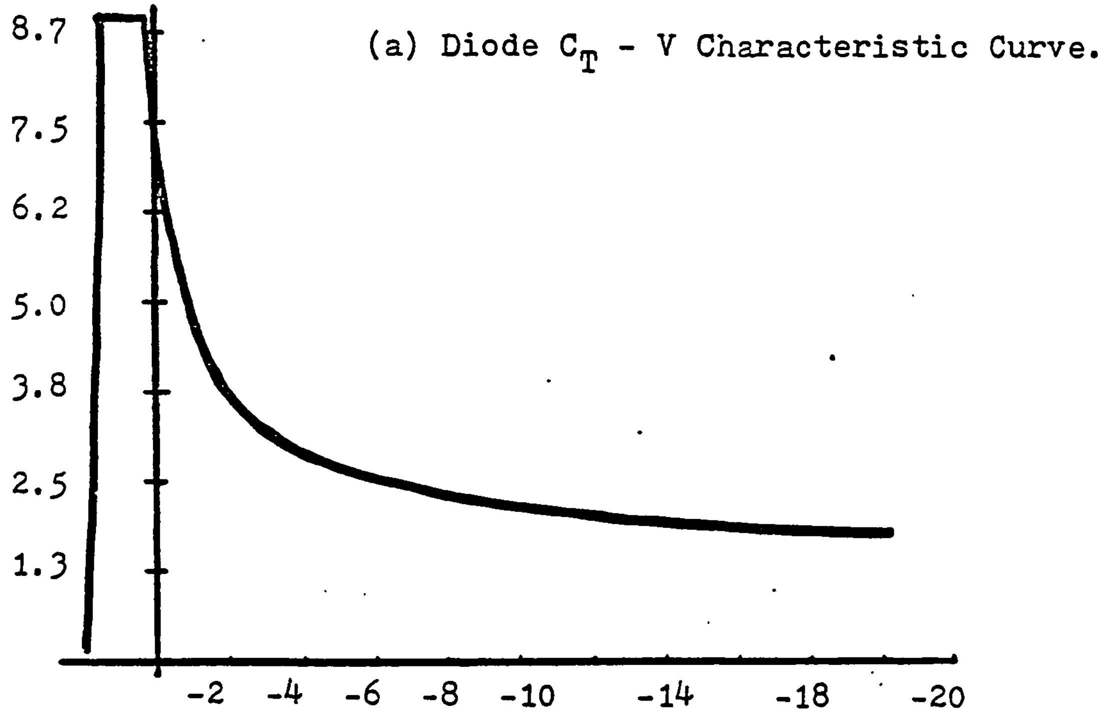


FIGURE 15. P - N Junction Characteristics After Surface Passivation.



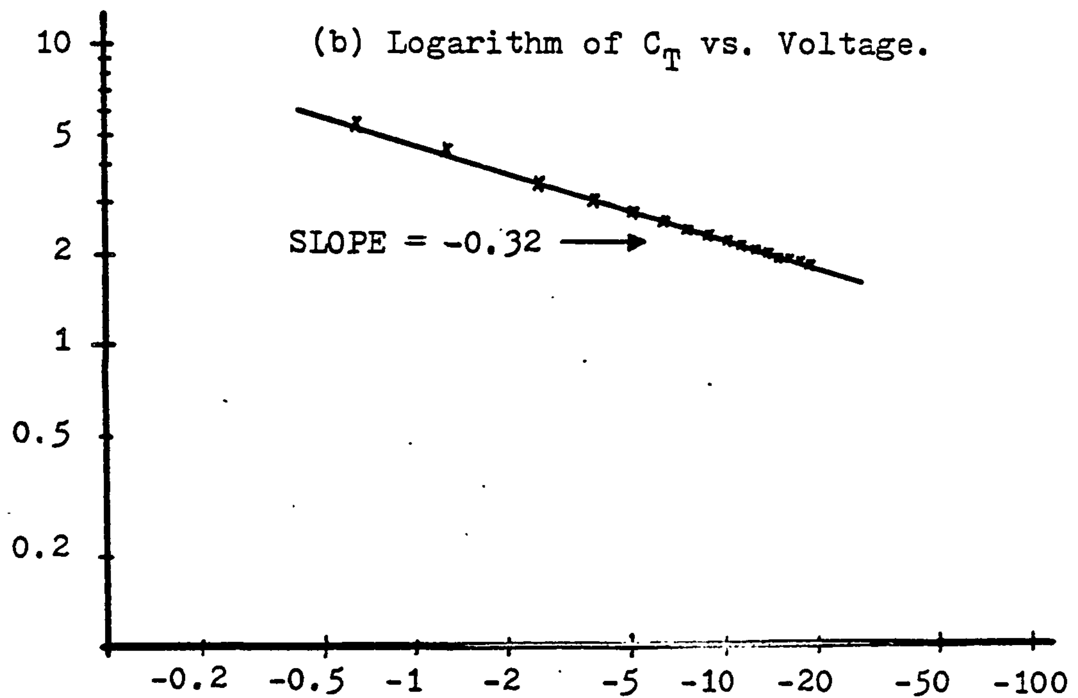


FIGURE 16. C_T - V and Log (C_T) - V Characteristic Curves for the Case of 12 Ω-cm Wafer.

the 12 Ω-cm wafer. The Logarithm (C_T) - Logarithm (V_R) curve is shown in Figure 16.(b) which shows a linear relationship with slope

$$\frac{\text{Logarithm }(C_T)}{\text{Logarithm }(V_R)} = -0.32 = -1/3 \qquad (14)$$

This established that the junctions are linearly graded rather than abrupt. The C_T-V curves for other two kinds of wafers are shown in Figure 17.(a) and (b).

The following model for calculating the space charge capacitance is proposed:

cylindrical capacitor model

Because during thermomigration the aluminum square dots are rounded off in the silicon wafer, the actual shape of the P^+ region is cylindrical but not square as shown in Figure 18. From the equation for calculating the capacitance between two concentric cylindrical plates, we have (23)

$$C_{junction} = \frac{2 \cdot \pi \cdot \epsilon_{Si} \cdot \epsilon_o \cdot t}{\ln\left((A+d) / A \right)} \qquad (15)$$

where 2 . A = 150 µm is the dimension of the aluminum dot,

d is the depletion width,

and t is the thickness of the wafer.

t is very difficult to determine precisely due to the preferential etching, so estimation is used. Table 4. shows the comparisons between the calculated values and the experimental data. The data was all obtained at V_R equal to -20 volts.

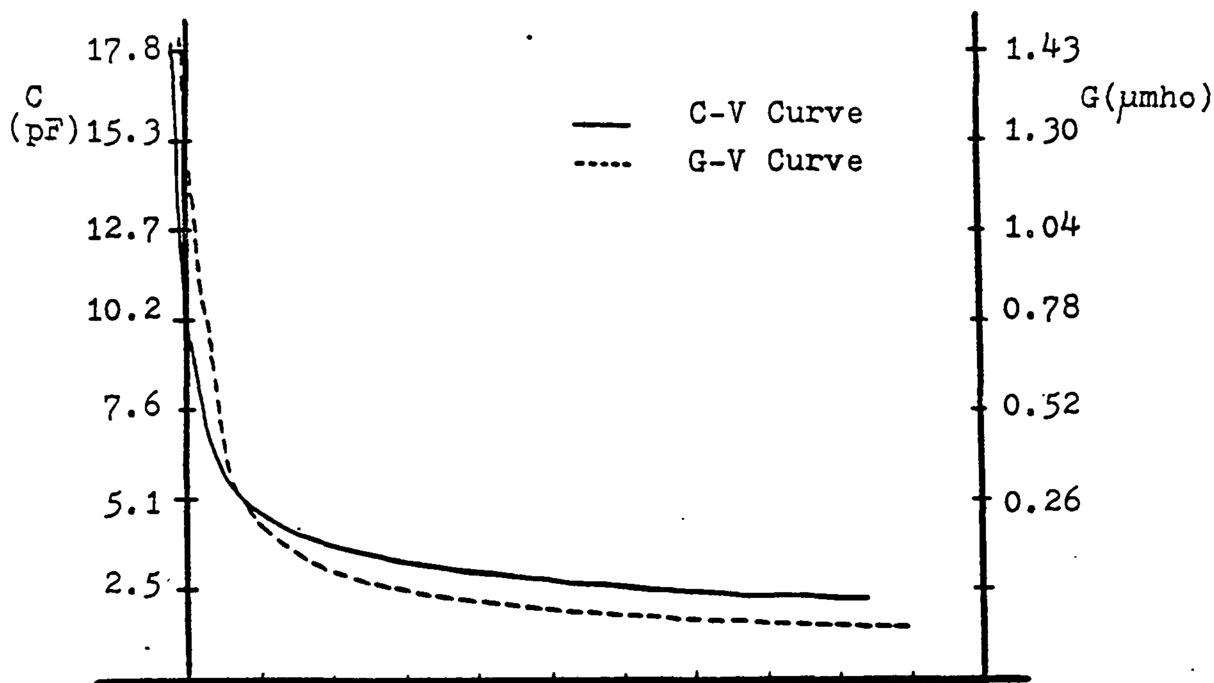
The discrepancies might be due to:

(1) the over-simplified model.

(2) the error of measurements.

(3) the rough estimation about t.

(a) C - V and G - V Curves for 6 Ω-cm Wafer.



(b) C - V and G - V Curves for 1550 Ω-cm Wafer

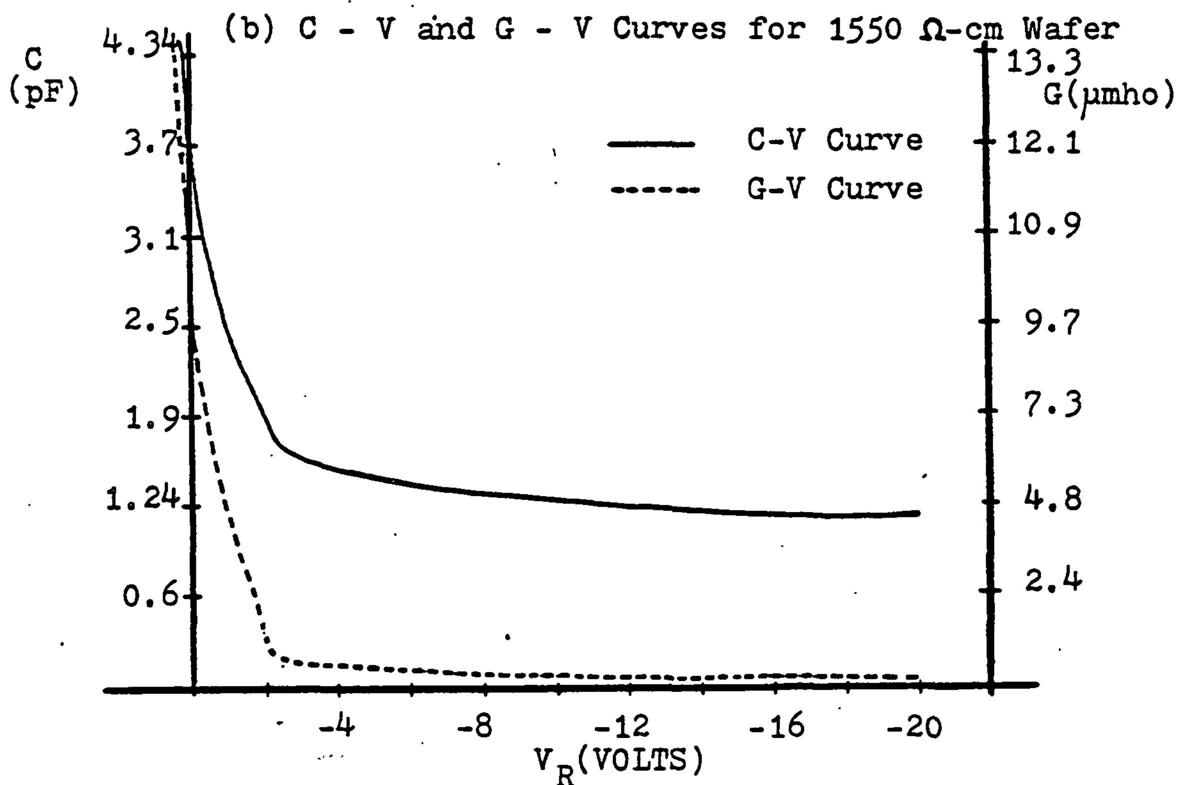


FIGURE 17. C - V and G (Conductance)- V Curves for 6 and 1550 Ω-cm wafers.

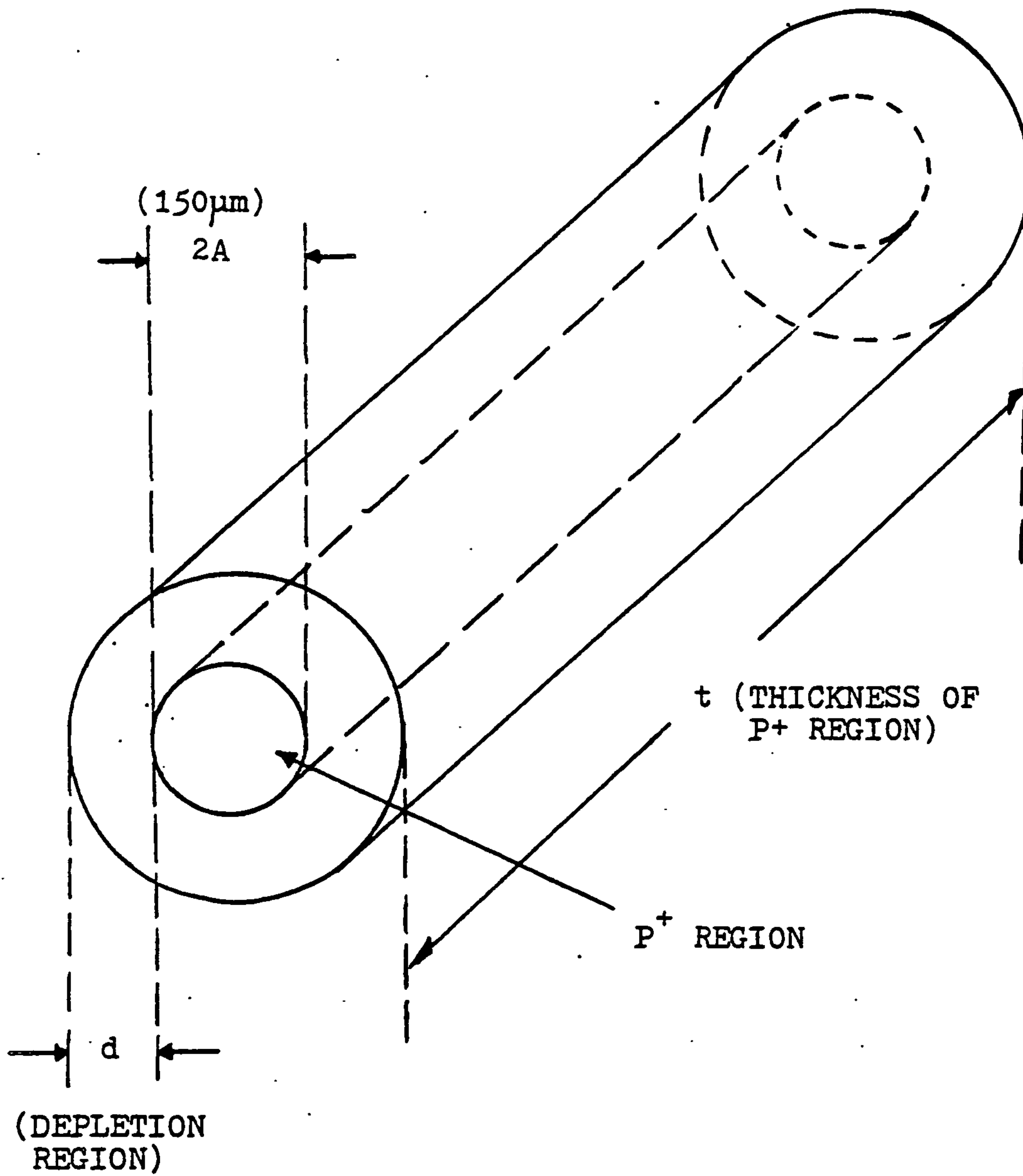


FIGURE 18. Simplified Geometry Of The Diode Used For Cylindrical Capacitor Model.

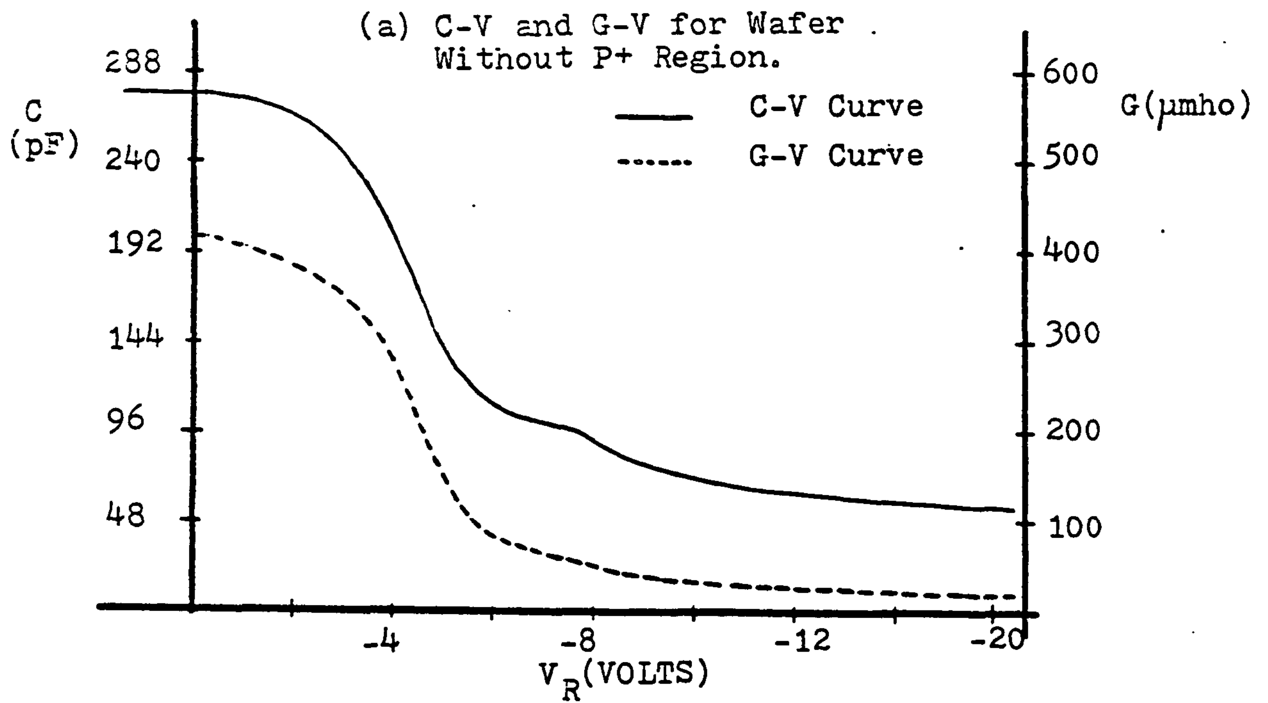
RESISTIVITY (Ω-cm)	THICKNESS "t" (μm)	CYLINDRICAL CAPACITANCE (pF)	EXPERIMENTAL DATA(pF)
6	200	3.55	2.2
12	200	3.29	1.95
1550	330	0.33	1.15

TABLE 4.

(iii) MOS C-V measurements:

When the 6 Ω-cm wafers were processed for x-ray detectors, three other wafers of the same resistivity were processed together with them. However, the aluminum migration process was skipped for these three wafers. After KOH preferential etching and basic cleaning, very clean dry oxide films were grown on both kinds of wafers-the wafers with P^+ region and those without. Chromium film (100 Å) and gold film (500Å) were then evaporated on to these wafers in sequence for MOS gate.

After completion, the C-V characteristic curves were taken for both cases as shown in Figure 19. The shapes of these two curves are very similar. The G-V curves are also shown in Figure 19. The shoulders on both the C-V and G-V curves correspond to turn-on of the (111) region at higher voltages (as expected due to their higher interfacial state density). The (111) surface arises because of the KOH preferential etching. No additional bumps that might be associated with the P^+ region were found in Figure 19.(b). This indicates that the P^+ region has no influence on the C-V curve of a regular MOS capacitor. However, the problem of growing good quality oxide on top of the P^+ region remains. Problems like large leakage current through the oxide or low dielectric strength appears. The lower dielectric constant also influences the reverse bias dielectric breakdown. Since the leakage problem occurrs in both cases of Figure 19 when positive bias was applied, this might be due to the microcracks in the oxide. These microcracks might be introduced by the roughness of the etched surface of the wafers.



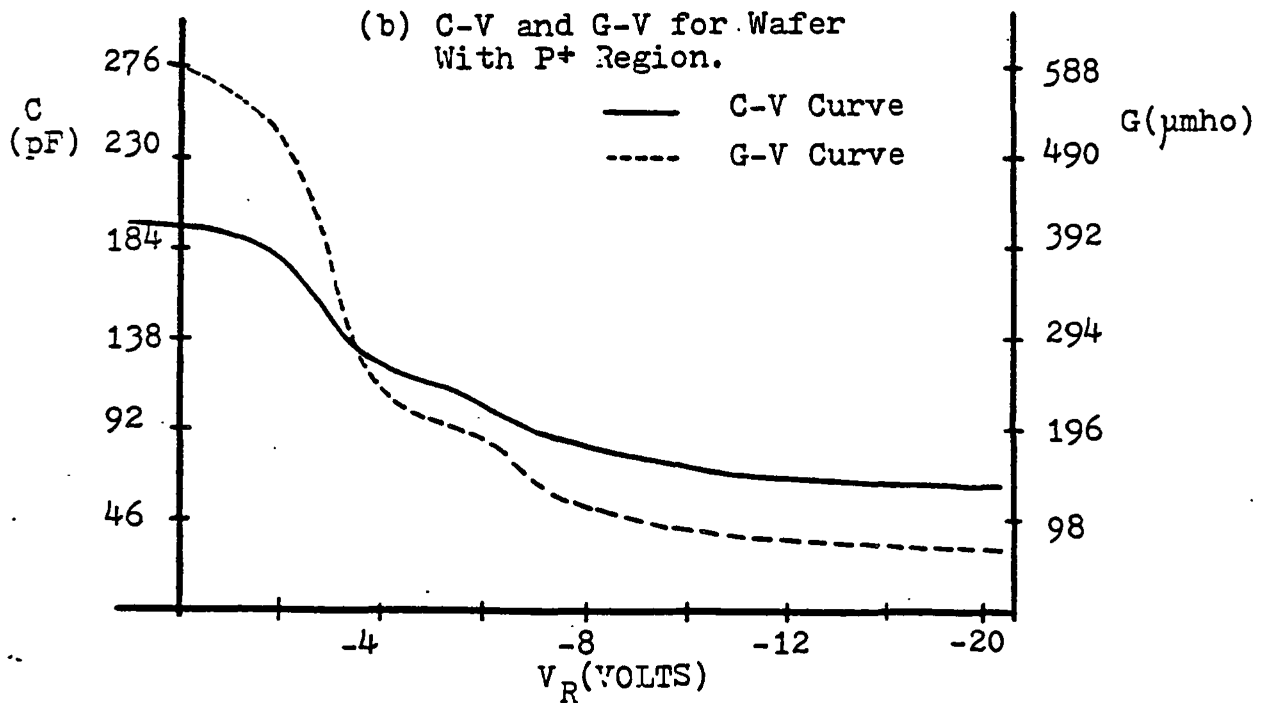


FIGURE 19. C -V and G - V for Wafers (a) Without (b) With P^+ Region. (6 Ω-cm wafer)

(b) X-RAY DETECTION EXPERIMENTS

The diode arrays on 1550 Ω-cm wafers were sent to NASA for test. The cryostat system for detection experiment is shown in Figure 20. The sample was thermally contacted with a copper tube, which could be cooled down to liquid nitrogen temperature ($77^{\circ}K$). The preamplifier containing a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) circuit was also cooled down to this temperature. The importance of the MOSFET circuit will be discussed later. The temperature was measured by a standard silicon diode contacting to the device and a voltmeter. The usable temperature region of this diode is from $4^{\circ}K$ to $400^{\circ}K$. The pressure during measurements was about $10^{-4} \sim 10^{-5}$ torr obtained by an absorption pump. The devices and circuits were shielded by thin Be foils and the whole cryostat system was covered with black cloth.

The x-ray energy of interest is from 5 KeV to 50 KeV. The x-ray source used in this work was Fe^{55} with characteristic energies as follows:

$$K_{\alpha} = 5.895 \text{ KeV}$$
$$K_{\beta} = 6.492 \text{ KeV}$$

Since the difference between K_{α} and K_{β} is only 597 eV, we really need a detector with Full Width at Half Maximum (FWHM) less than this difference in order to identify the two peaks. During the experiment the devices were reduced to about $86^{\circ}K$ to reduce the noise background. The energy spectra obtained from the detection system for different bias conditions and operating temperatures are shown from Figure 21.(a) to (e). In the right halves of these photographs we can see two peaks, one bigger and the other one smaller. The big peak corresponds to the energy level k_{α} of Fe^{55} while the small one corresponds to k_{β}. Also observed from these pictures is that the positions of those two peaks in the energy spectrum stay invariant through

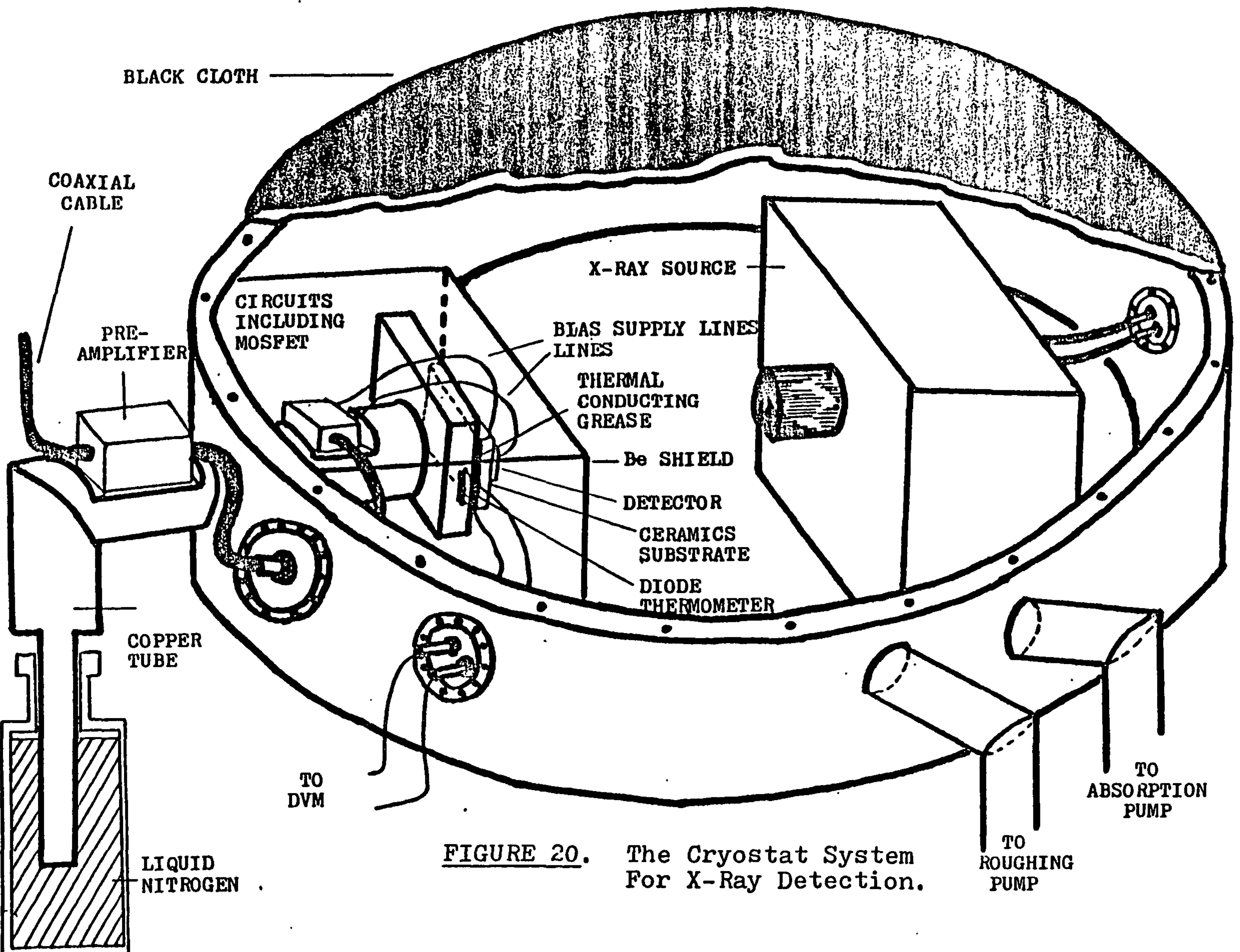
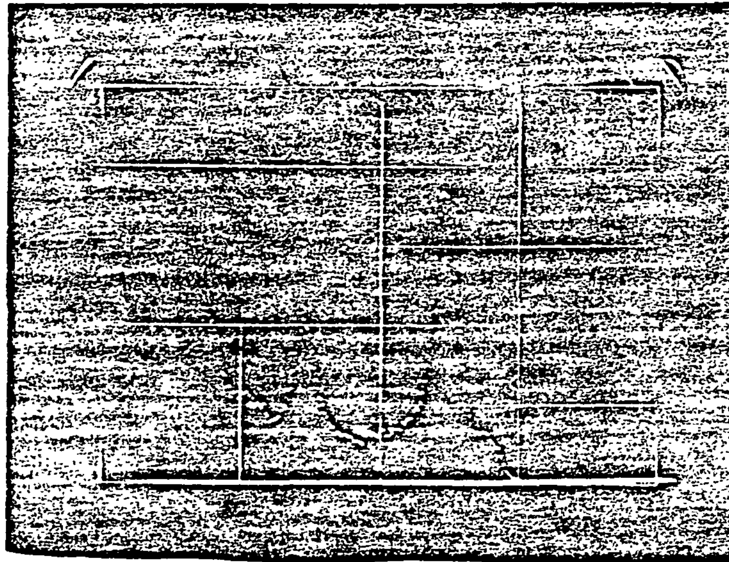
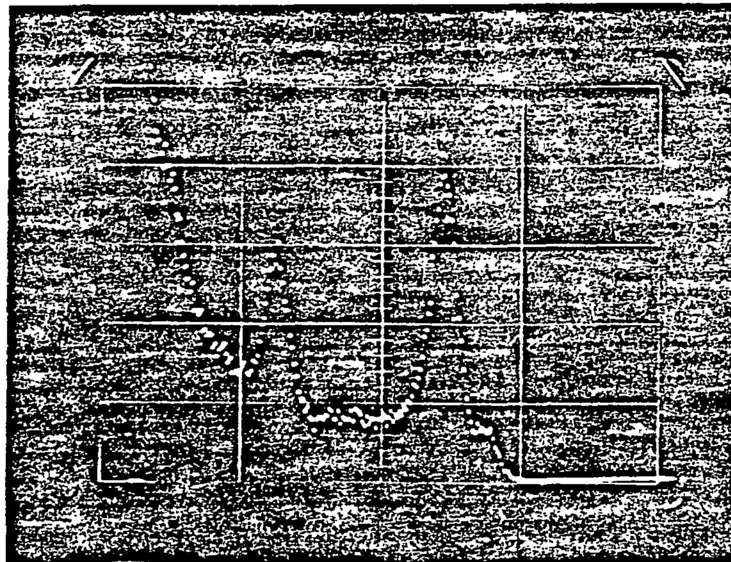


FIGURE 20. The Cryostat System For X-Ray Detection.

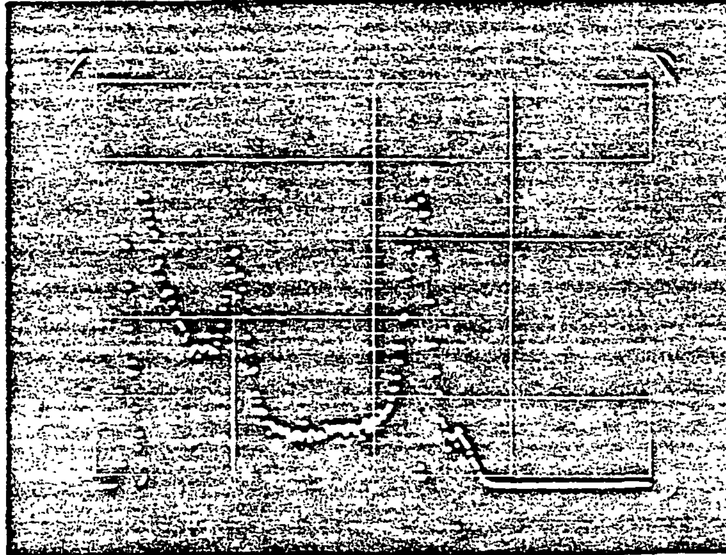


(a) BIAS: -100 VOLTS.
TEMP. : 115°K.
FWHM (K_α): 593 eV.

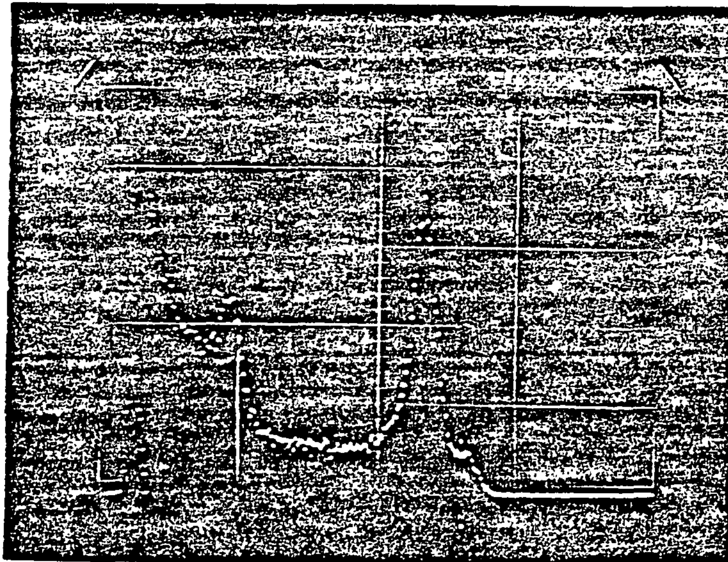


(b) BIAS: -40 VOLTS
TEMP. : 87°K.
FWHM (K_α): 613 eV.

FIGURE 21. Energy Spectra Obtained From Detection System Under Different Operating Conditions.

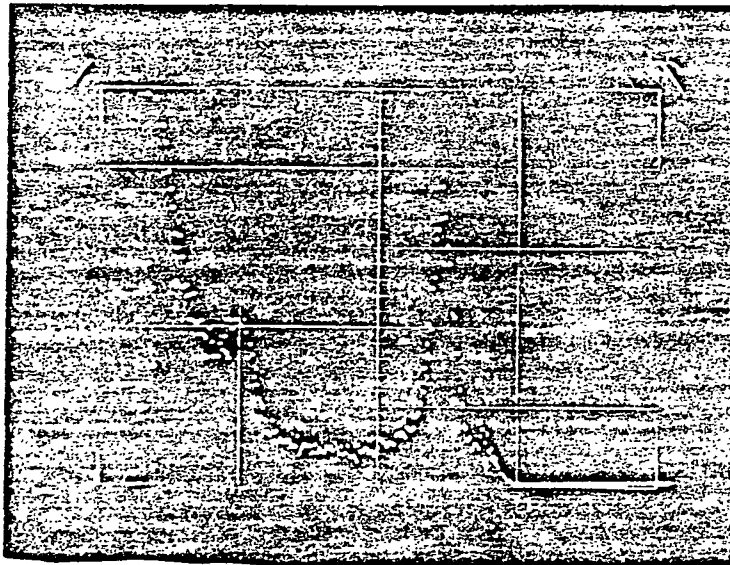


(c) BIAS: -20VOLTS.
TEMP. : 86°K.
FWHM: 534 eV.

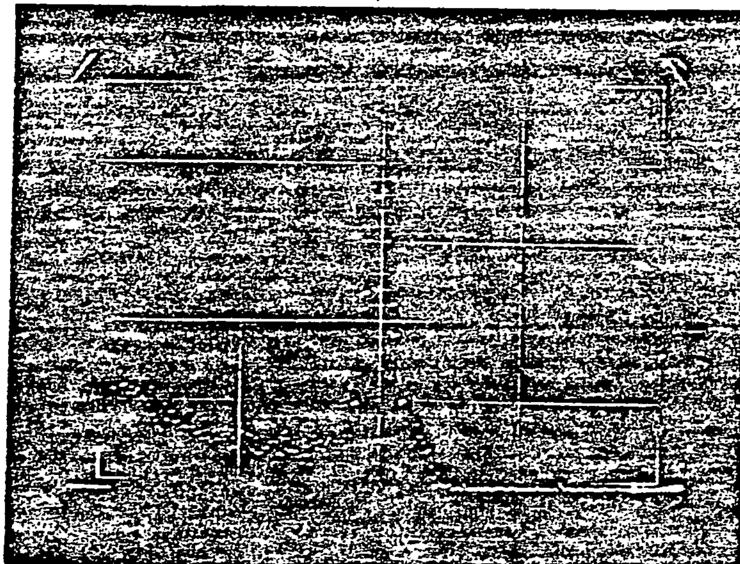


(d) BIAS: -10 VOLTS.
TEMP. : 85°K.
FWHM: 514 eV.

FIGURE 21. (CONTINUED)



(e) BIAS: -5 VOLTS.
TEMP. : 89°K.
FWHM: 514 eV.



(f) BIAS: -20 VOLTS.
TEMP. : 130°K.
FWHM: 480 ~ 500 eV. (estimated)
(NASA Chip)

FIGURE 21. (CONTINUED)

different bias conditions. The results indicates that these diode detectors are suitable for soft x-ray detection. The full width at half maximum (FWHM) was also measured for each case and the results are listed in Table 5. The best condition found is sample "PENN 5" where -5 volts and 89°K were used. Its FWHM is around 500 eV. This result is good because the preamplifier, which used resistive rather than opto-feedback, had a FWHM of about 400 eV with a Si(Li) radiation detector.

Figure 22 shows the comparison of these results in the same spectrum. The counts of peaks K_α and K_β were plotted as a function of bias voltages in full logarithm scale as shown in Figure 23. and 24. Two linear relationships with solpes 0.38 and 0.37 for K_α and K_β were obtained, respectively. This means that

$$\text{(Counts of } K_\alpha \text{ or } K_\beta \text{ peak)} \propto V_R^{0.37 \sim 0.38} \qquad (16)$$

From Eq. (14) in Section II, we know that

$$d \propto (V_R)^{1/3}$$

Therefore, We conclude that

$$\text{(Counts of } K_\alpha \text{ or } K_\beta \text{ peak)} \propto \text{Depletion Region Width} \qquad (17)$$

This is reasonable because the wider the depletion region, the more charge be collected.

In Table 5. and Figure 21.(f) also show the data and spectra obtained from one of NASA's device operated at similar condition except that 130°K was used in stead. Similar results to ours were obtained. The reason for this higher operating temperature will be clear in the last part of this section.

In the left halves of the photographs from Figure 21.(a) to (e), we see another peak in the spectrum in each case which is unexpected. Two phenomena are observed from this. First, the energy positions of these extra peaks are dependent on the applied biases. The energy increases with the bias. Secondly, the peak corresponding to -100 volts case

TABLE 5

SAMPLE	REVERSE BIAS (VOLTS)	OPERATING TEMPERATURE (K°)	COUNTS OF PEAK Kα	COUNTS OF PEAK Kβ	POSITION OF THE EXTRA PEAKS (eV)	F.W.H.M. (eV)
PENN 1	100	115	1932	349	3165.6, 1385	593.7
PENN 2	40	87	1324	234	2769.9	613.5
PENN 3	20	36	1060	181	2492.9	534.3
PENN 4	10	85	979	141	2295.1	514.5
PENN 5	5	89	601	110	2176.4	514.5
NASA chip	20	130	- -	-	-	480.0 (estimated)

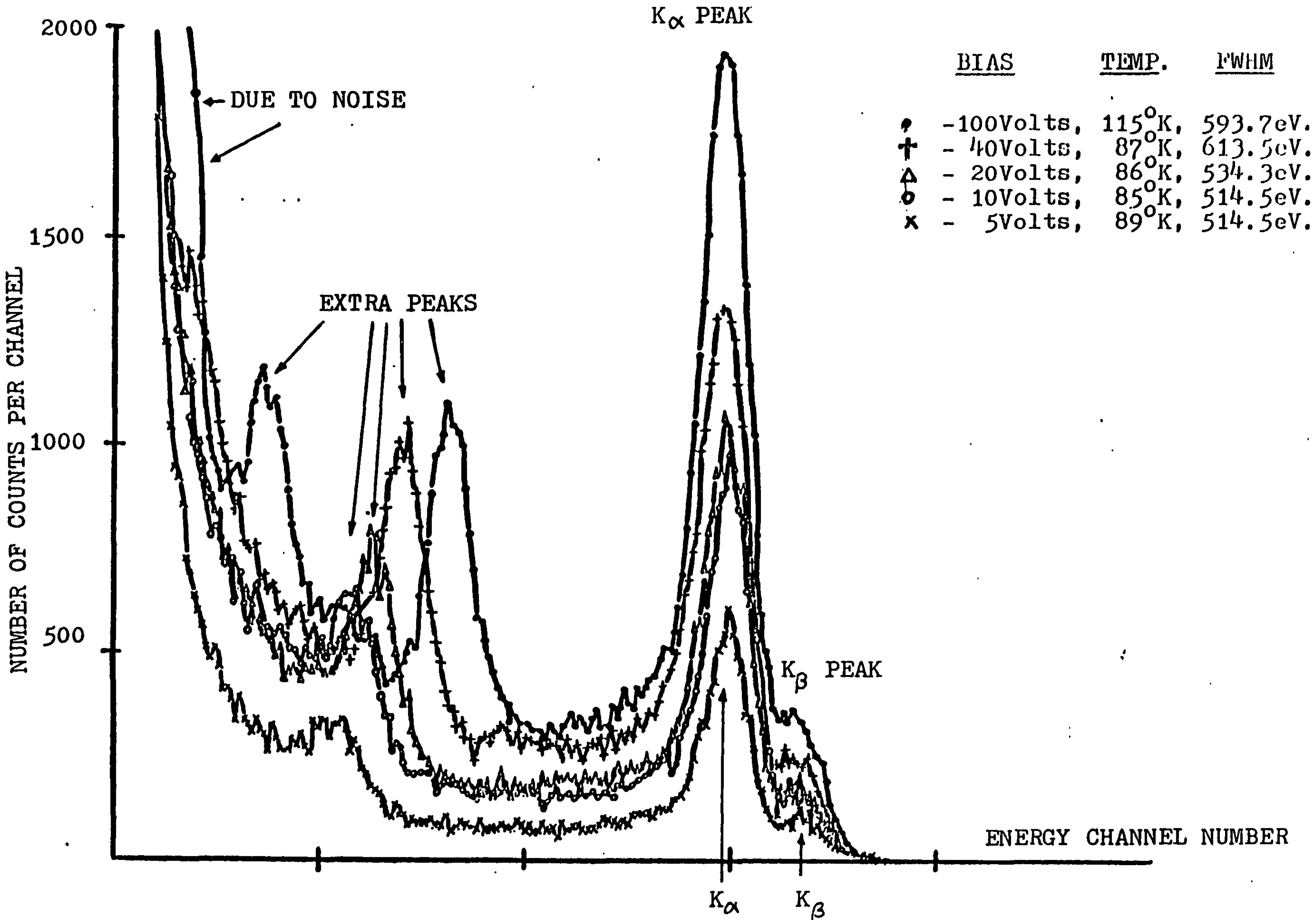


FIGURE 22. Comparison Of The Energy Spectra.

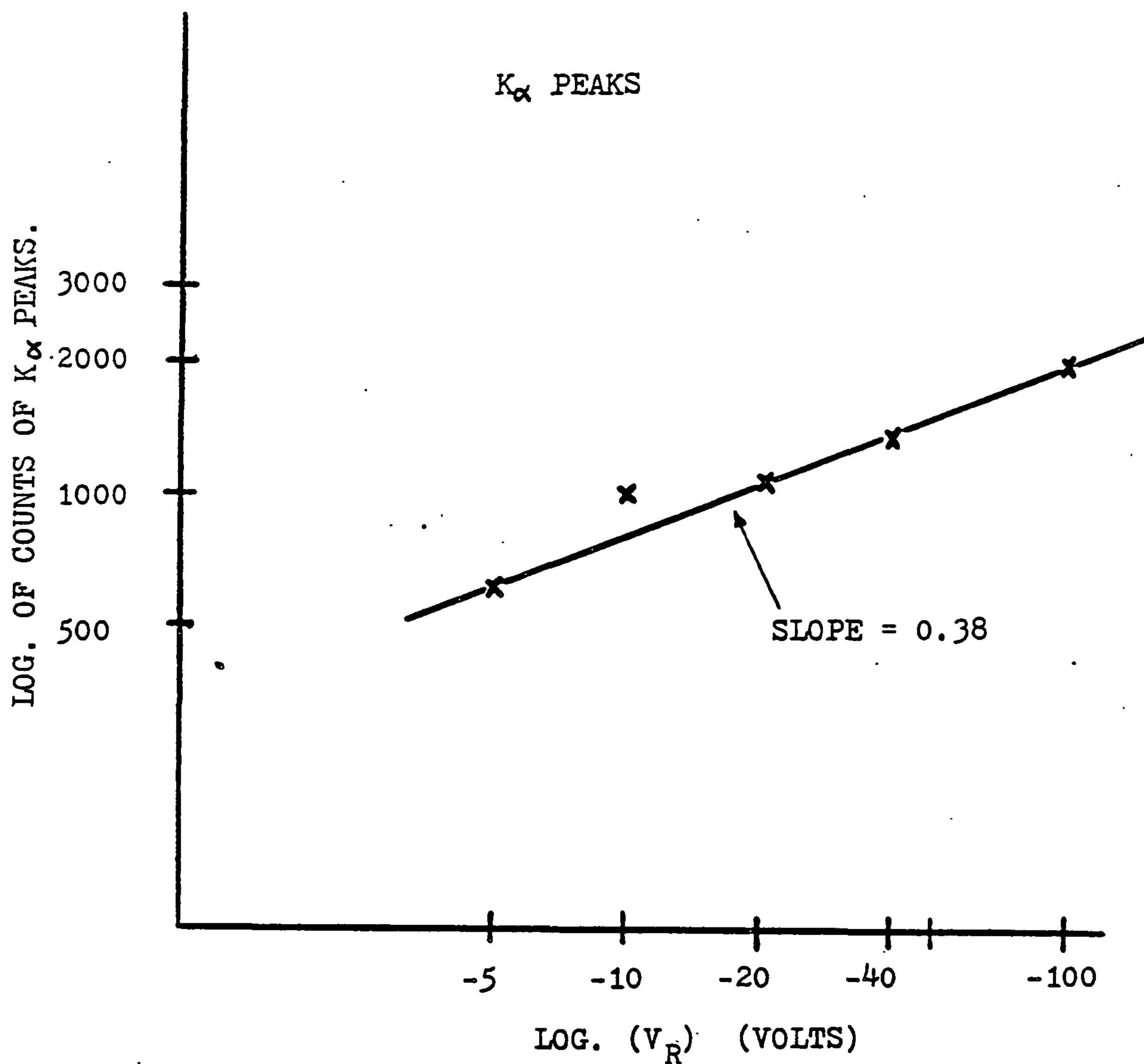


FIGURE 23. Logarithm Of K_α Peak Counts vs. Bias Voltage.

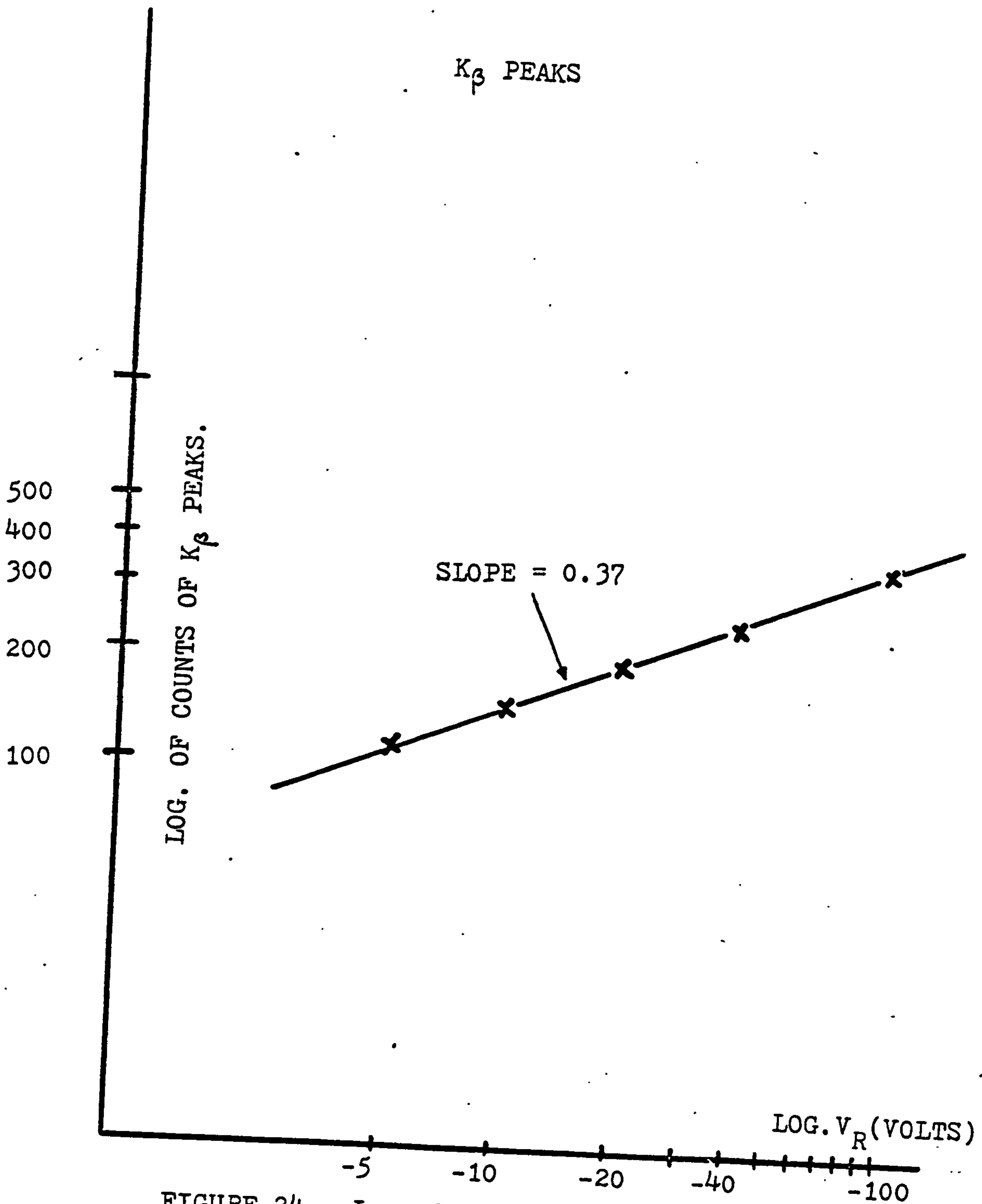


FIGURE 24. Logarithm Of K_β Peak Counts vs. Bias Voltage.

split into two. We propose the following model to explain these interesting phenomena.

In the array pattern there are four P^+ regions sitting at the four corners of a $(1000\ \mu m)^2$ cubic. When one of these four diodes is reverse biased at very low temperature, its depletion region can extend to about 300 to 400 micrometers away from the central P^+ region. This is schematically shown in Figure 25.(a). The corresponding energy band diagram is shown in Figure 25.(b). Holes are generated by radiation in the neighbors of the three floating diodes. But only the holes in the regions of these neighborhoods that are closer to the biased diode have a chance to diffuse into the depletion region. From a rough calculation, if the temperature is 87°K and the lifetime of the holes in the bulk material is in the range of 100 μs, which is reasonable for this high purity (1550 Ω-cm) material and low temperature condition, we obtain the diffuion length as

$$L_D = \sqrt{D_P \cdot \tau_P} = 500 \sim 1000\ \mu m \qquad (18)$$

which shows that there is indeed a probability for the holes from those energy band valleys to diffuse into the depletion region.

If we use a very simple diffusion model assuming that the probabilityof a hole not being recombined or scattered during its diffusion process is exponentially decaying as shown in Figure 25.(c). Therefore, the charge collected by the biased diode from the nearest neighboring diodes is

$$\begin{aligned} q_{survived} &= q - \frac{q}{L_D}\left[\int_{\cong 0}^{1000-d} e^{-\frac{x}{L_D}}\, dx\right] \\ &= q + q \cdot \left(e^{-\frac{x}{L_D}}\right)\Big|_{\cong 0}^{1000-d} = q \cdot e^{-\frac{1000-d}{L_D}} \\ &= K_1 \cdot e^{d/L_D} \qquad (19) \end{aligned}$$

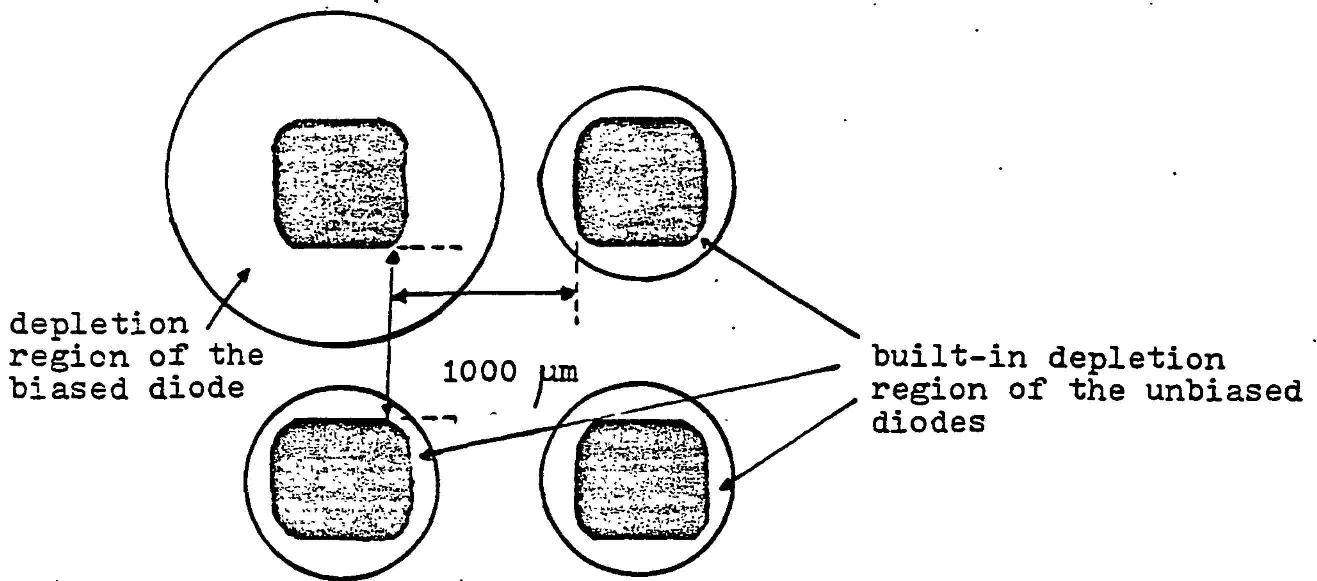
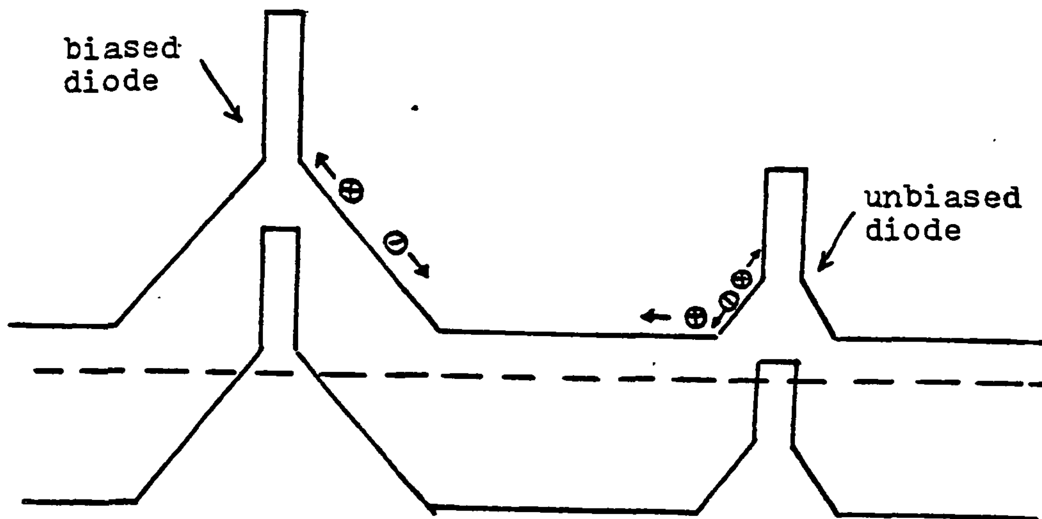
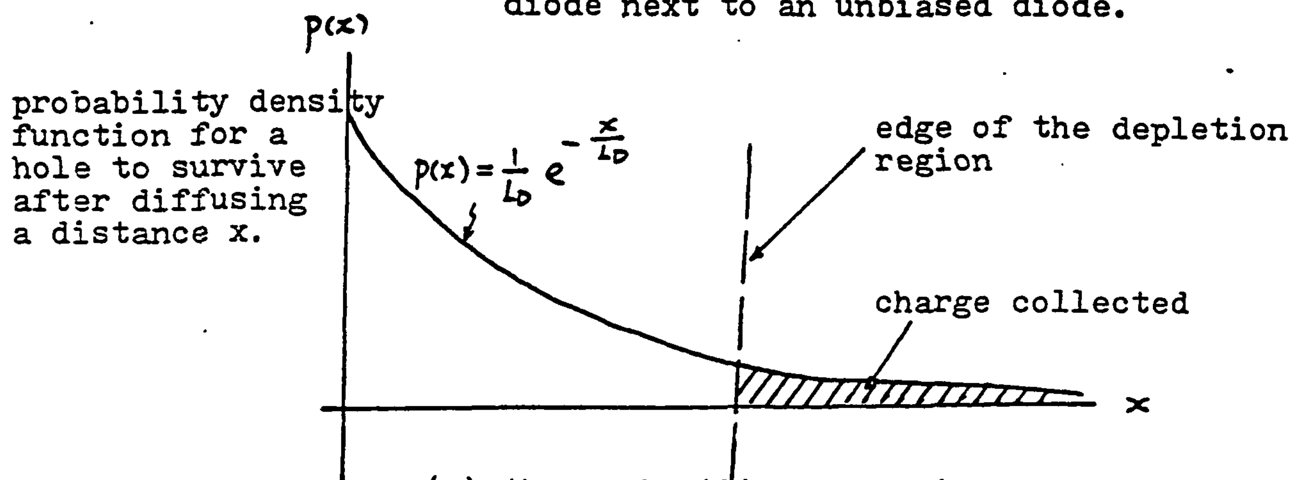


FIGURE 25. (a) the diode pattern when one of them is reverse biased.



(b) the energy bands diagram for a biased diode next to an unbiased diode.



(c) the probability function of collecting charge from the neighboring unbiased diodes.

where k_1 is a constant.

Since from Eq. (8) we know that the energy in the energy spectrum is proportional to the amount of generated charge in the depletion region. These diffused charges have suffered a distortion in amount before they are collected. This explains why the extra peak came out in lower energy region. When the reverse bias is increased, the depletion region is wider which can then collect generated charge more completely from the three floating diodes. The holes in the next nearest neighboring diode can be collected in a detectable amount only when the depletion region is wide enough. This explains why the second extra peak came out in even lower energy region for the case of bias equal to -100 volts.

The ratio between the charges collected from the next nearest and nearest neighbors is

$$\frac{e^{-\frac{1000\cdot\sqrt{2}-d}{L_D}}}{e^{-\frac{1000-d}{L_D}}} = e^{\frac{1000(\sqrt{2}-1)}{L_D}} \underset{L_D \cong 500}{\cong} e^{-\frac{414}{500}} = 43.7\% \quad (20)$$

This is very close to the ratio between the energies of the two unexpected peaks for -100 volts case, which is

$$\frac{35}{80} \equiv 43.8\ \% \quad (21)$$

When the logarithm of the energy position corresponding to the extra peak for each case is plotted as a function of $V_R^{1/3}$, a linear relationship is obtained, which means

$$\text{Log (energy position)} \propto V_R^{1/3} \quad (22)$$

or

$$\text{energy position} \propto \text{amount of charge} \propto e^{k_2 \cdot V_R^{1/3}} \propto e^{K_3 \cdot d} \quad (23)$$

This relationship is shown in Figure 26.

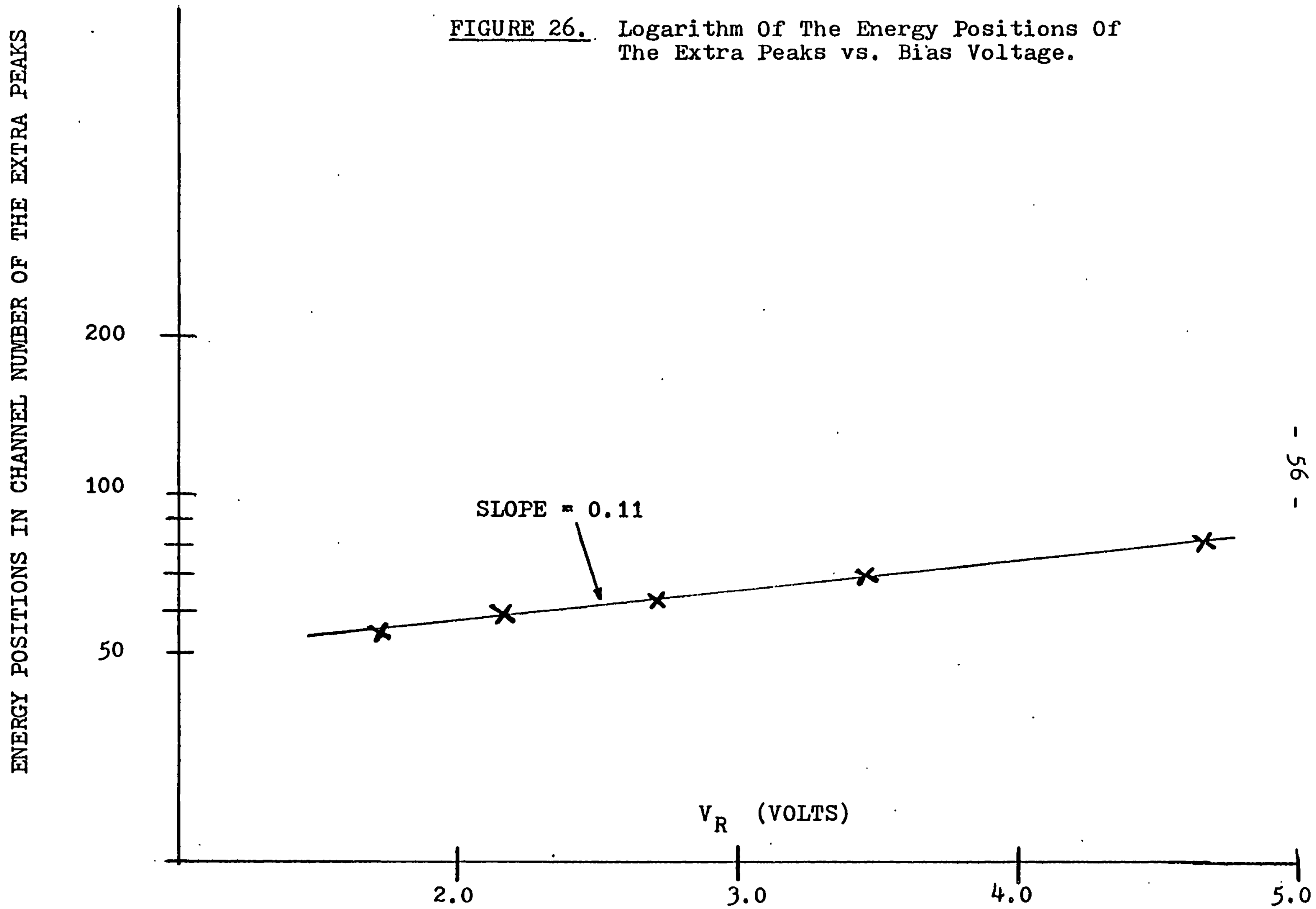


FIGURE 26. Logarithm Of The Energy Positions Of The Extra Peaks vs. Bias Voltage.

This proves our proposed model. The importance of this result is that really good spacial resolution spectrometer arrays to the dimension of diffusion length of holes in silicon at low temperature can be available.

Noise

The noise in the energy spectrum comes from several sources:

(1) any drift of the operating characteristics of the detector during the course of the measurements, e.g., the leakage current. This current produces a high level of low frequency noise. Such noise can dominate in low-energy x-ray spectrometer systems.

(2) sources of random noise within the detector, e.g., the thermal noise. This will be reduced at lower temperature.

(3) random noise of the instrumentation system. The important sources of noise occur near the beginning of the signal chain where the signal level is at minimum. Noise generated at this point undergoes the same amplification as the signal, whereas noise generated further along the singal chain is usually much smaller than the signal. Therefore, discussions of electronic noise sources generally center on the preamplifier, and, most important, its input stage. This is why we choose to use MOSFETs as the input stage. MOSFETs have low leakage current and high input impedance.

If we define the equivalent noise charge (ENC) as the amount of charge which, if applied suddenly to the input terminals of the system, would give rise to an output voltage equal to the RMS level of the output due only to noise. ENC is translated into the equivalent energy deposition by a charged particle in the detector. This explains the pile-up of counts at the very low end of the energy spectrum.

For MOSFET, it can be obtained that (24)

$$ENC \propto \frac{1}{g_m} \tag{24}$$

where g_m is the transconductance of the channel of MOSFET. g_m is temperature-dependent and has a maximum between 110°K and 140°K for silicon as shown in Figure 27. When g_m is at its maximum, the ENC will be at its minimum. This is why 115°K to 130°K was used for some of the experiments.

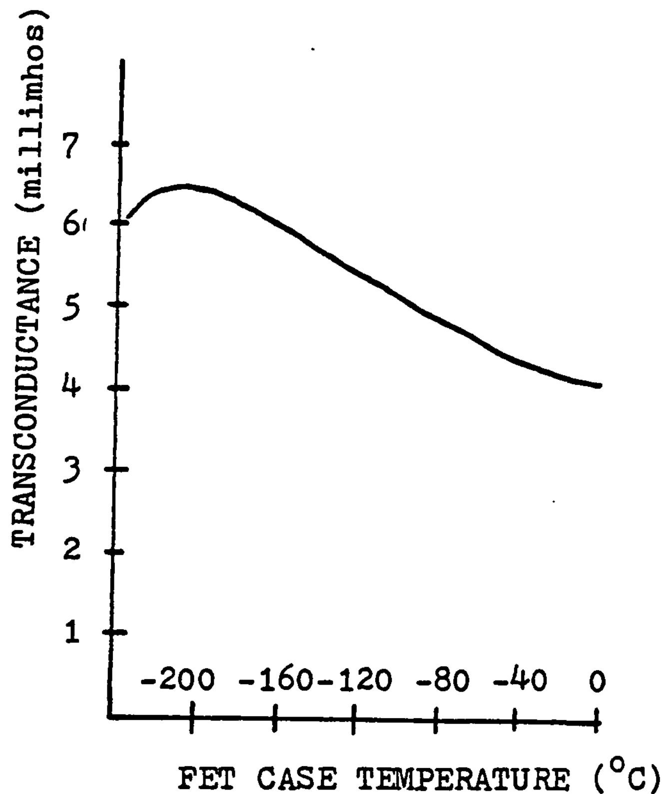


FIGURE 27. Temperature Dependence Of The Transconductance Of An MOSFET. (25)

(c) α-particles detection experiment:

This experiment was done in Physics Department, University of Pennsylvania. The detection facility was very similar to the one described before. The source of α-particles was Am^{241} whose peak energy is at 5.48 MeV. The operating temperature was higher than liquid nitrogen temperature. The results of the test are listed in Table 6.

For comparison the data obtained from an ion implanted detector is also enclosed in the table. From the comparison the deep diode arrays are found not suitable for α-particle detections. The reasons for this might be that

(i) the penetration depth of α-particles is too short.
(ii) the passivation film (SiO_2) acts as a dead layer for α-particles.
(iii) the junction area of the ion implanted diode is large in this case (25 mm^2).

TABLE 6

SAMPLE	REVERSE BIAS (V)	OPERATING TEMP (^{o}C)	REVERSE CURRENT (nA)	F.W.H.M. (keV)
Penn.	-20	-45	8	12.2
Penn	-50	-45	9	16.5
Penn.	-100	-45	10	24.4
ion implanted detector (26, 27)	-100	25	1	10.6

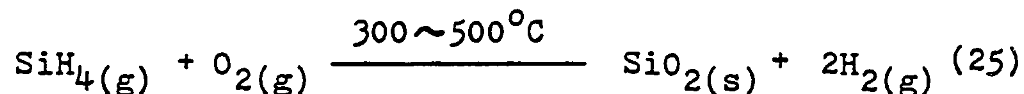
V. ADDITIONAL STUDIES ON MATERIALS SUBJECTED TO TGZMP CONDITIONS

A series of additional intense incoherent radiation studies were conduted on the Si wafers in order to obtain greater insight into the effect of this processing. They are:

(a) Annealing of chemical vapor deposited SiO_2.
(b) Recrystallization of chemical vapor deposited SiO_2.
(c) Inspection of defects generated by thermal radiation.

(a) Annealing of chemically deposited SiO_2

Using the results of N. Goldsmith and W. Kern (28, 29) Chemical Vapor Deposited (CVD) SiO_2 system was designed as shown in Figure 28.
Silane (SiH_4) gas (2.1 % balanced with Ar) was flushed into the system to react with oxygen gas just above the surface of the sample in a surface reaction. The reaction temperature ranged from 300 to 500°C. The reaction equation is

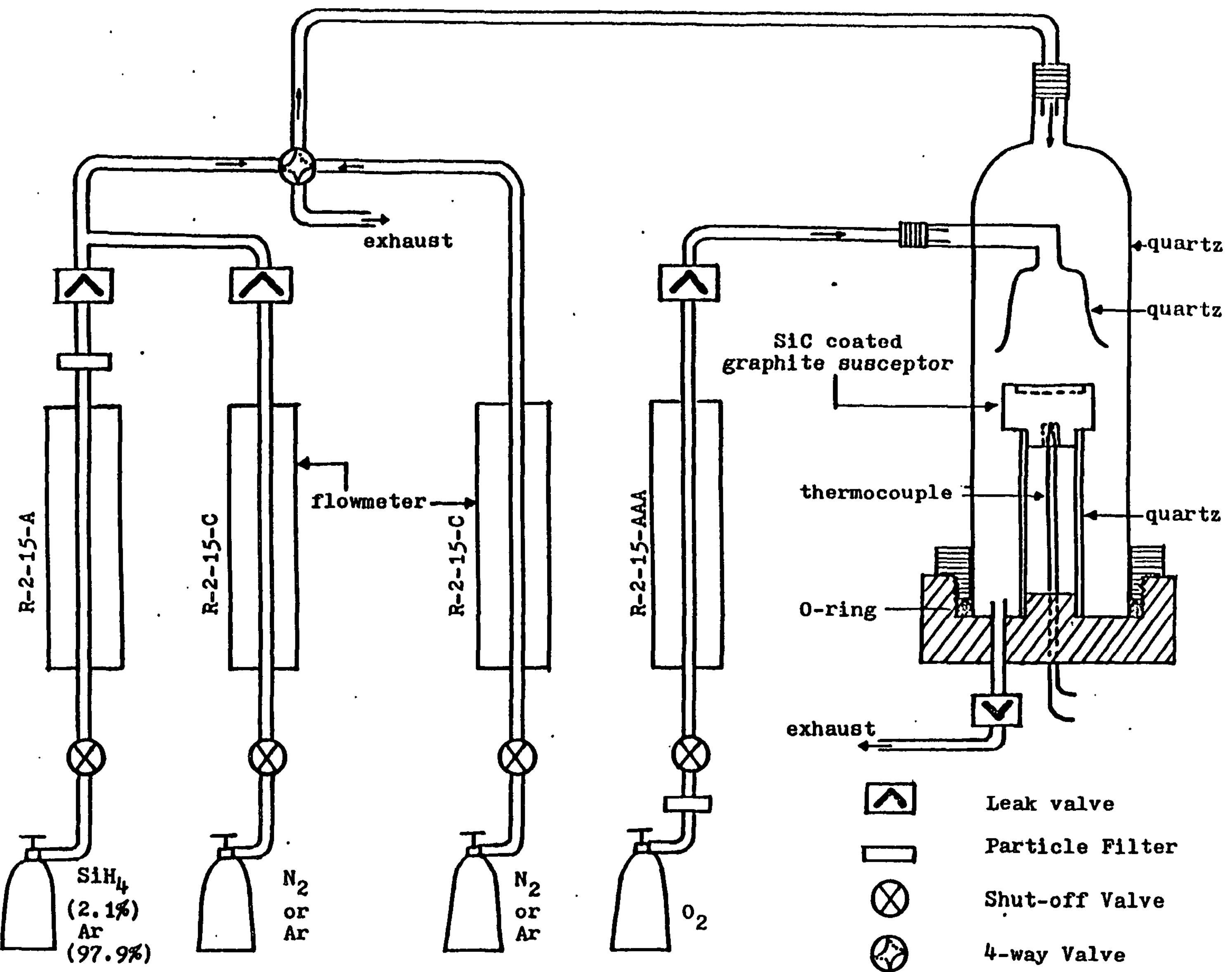


$$SiH_{4(g)} + O_{2(g)} \xrightarrow{300 \sim 500^{\circ}C} SiO_{2(s)} + 2H_{2(g)} \quad (25)$$

Argon or nitrgen was used as the carrier. The flow rate for each gas species is shown in Table 7.
The optimal ratio between O_2 flow and SiH_4

$$O_2 : SiH_4 = 13 : 1 \quad (26)$$

and the optimal growth temperature was between 320°C and 350°C. Even for the optimal conditions, it was difficult to obtain uniform films from this single wafer system. The SiO_2 growth rate was from 400 Å/min to 500 Å/min. The resulting film could be etched by hydrofluoric acid (10%) or buffered HF. In order to study the effect of incoherent radiation



<u>FIGURE 28</u>. CVD System Designed For Deposition Of Both Silicon And Silicon Oxide.

GAS SPECIES	FLOW RATE
O_2	112.5 c.c./min.
SiH_4	8.6 c.c./min.
Ar (balanced with SiH_4)	357.1 c.c./min.
Ar or N_2	7.1 litter/min.

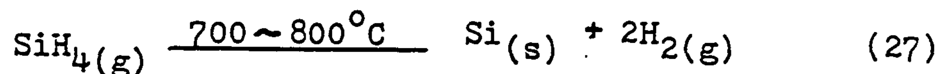
TABLE 7.

annealing, a two inch wafer with a relatively uniform SiO_2 thin film (about 3000 Å) cut into four quarters was used. It was placed in the annealing facility (already shown in Figure 3.). The temperature was measured as described in section III.(e). The SiO_2 films were placed to face directly the radiation source . Different annealing periods were used for three samples, as shown in Table 8. After the annealing, thicknesses were measured by an -step machine and the infrared spectra were taken from these four samples. The results are shown in Table 8. and Figure 29.

The thickness of the oxide film decreased with annealing time. Wafer 4 is peculiar on its thickness. There might be some oxide growing during the annealing because of the high temperature and long anneal-time used on this wafer. Th infrared spectra show an increase in the absorption peaks at wavelength 1075 cm^{-1} and 813 cm^{-1}. These two peaks correspond to the vibrational energies of the bonding between Si and O. This suggests that the number of Si-O bonds increased and that the films became denser with time. From the spectra we also see the change in the peak height at wavelength 2330 cm^{-1}. This peak position is very close to the bonding between Si and H (2240~2300 cm^{-1}) (30).

(b) Recrystallization of chemically deposited silicon

The system for polycrystalline silicon (poli-Si) is exactly the same as the one used for SiO_2 deposition. The reaction used is the pyrolytic deposition of silane (SiH_4).



$$SiH_{4(g)} \xrightarrow{700 \sim 800^{\circ}C} Si_{(s)} + 2H_{2(g)} \qquad (27)$$

Different growth temperatures (700, 750, and 800°C)

SAMPLE NO.	ANNEALING CONDITION	COLOR OF SiO_2	THICKNESS(Å)	% TRANSMISSION OF PEAK AT 1075 CM^{-1}
1	as-deposited	Violet-blue	2900	23
2	30" from 25°C to 800°C 30" annealing at 800°C 30" from 800°C to 100°C	Orange to melon	2750	20.5
3.	30" from 25°C to 800°C 1' annealing at 800°C 30" from 800°C to 100°C	Orange to melon	2500	19.5
4.	30" from 25°C to 800°C 2' annealing at 800°C 30" from 800°C to 100°C	red-violet	2850	17

TABLE 8.

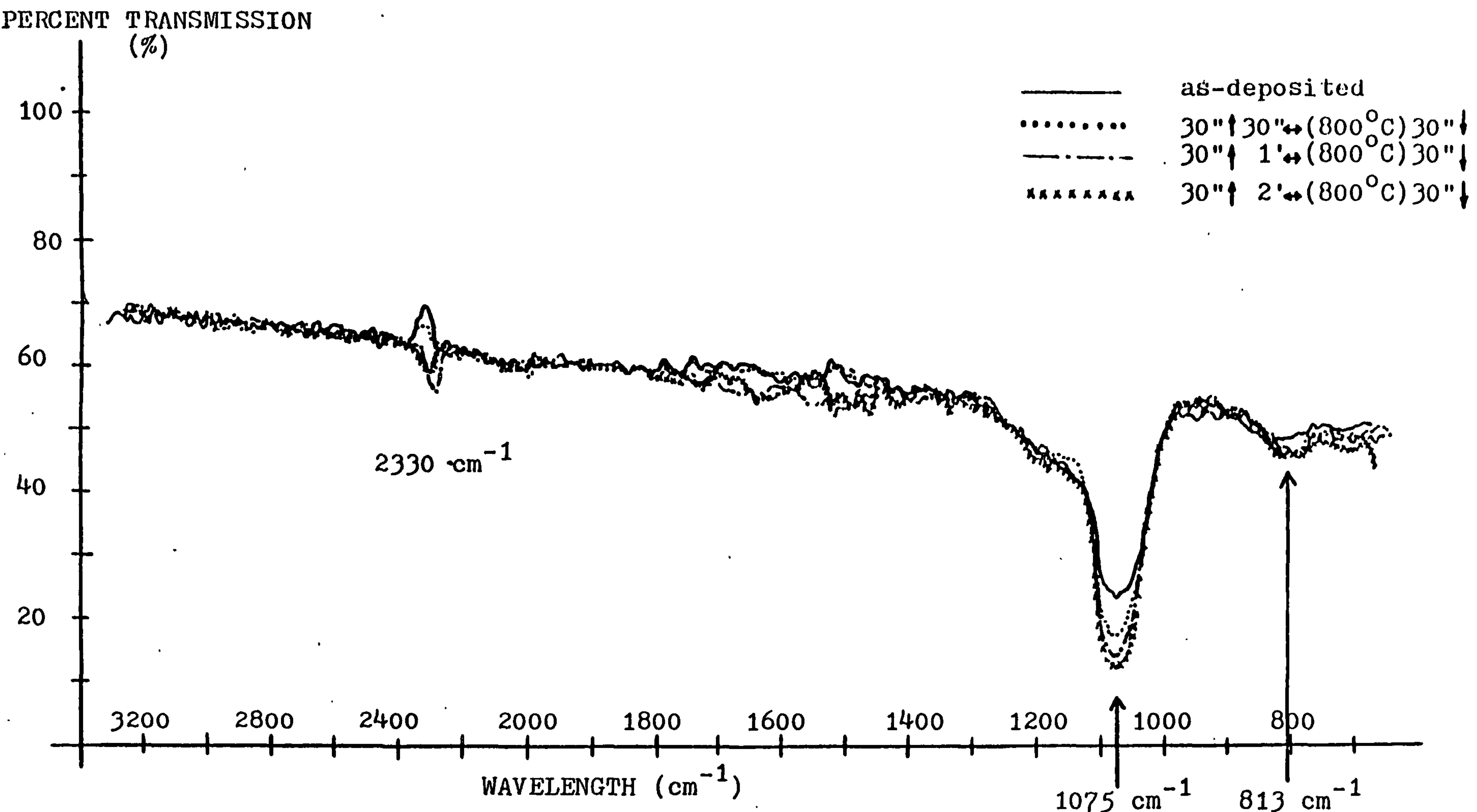


FIGURE 29. Infrared Spectra Of CVD SiO_2 Obtained From Different Annealing Conditions.

were used. X-ray diffraction spectra were taken from these samples. When the temperature was lower than 700°C, the silicon film was "armophous" because no crystallization peak came out in the spectrum. When the temperature was from 700 to 750°C, the film was polycrystalline and it favored the (111) orientation growth rather than (110). However, when the temperature went higher than 750°C, the growth of crystal along (110) was preferred. These results are in agreement with those obtained by Kamins and Cass (31).

The sample grown at 700°C was cut into three parts and two of them were further annealed by the radiation source. The x-ray diffraction spectra were taken again. The results and annealing condition used are shown in Table 9 and Figure 30. We see that during the annealing the films had gone from armophous status to polycrystalline status mainly along the (111) direction. In a very short annealing period of 30 seconds at 730°C poli-Si with crystallization peaks even higher than those grown at 730°C for 10 minutes has been obtained.

(c) <u>Inspection of defects generated by incoherent radiation annealing</u>

The procedures shown in Figure 31. were conducted on silicon wafers in order to study surface defects generated by Incoherent Radiation Annealing (IRA).

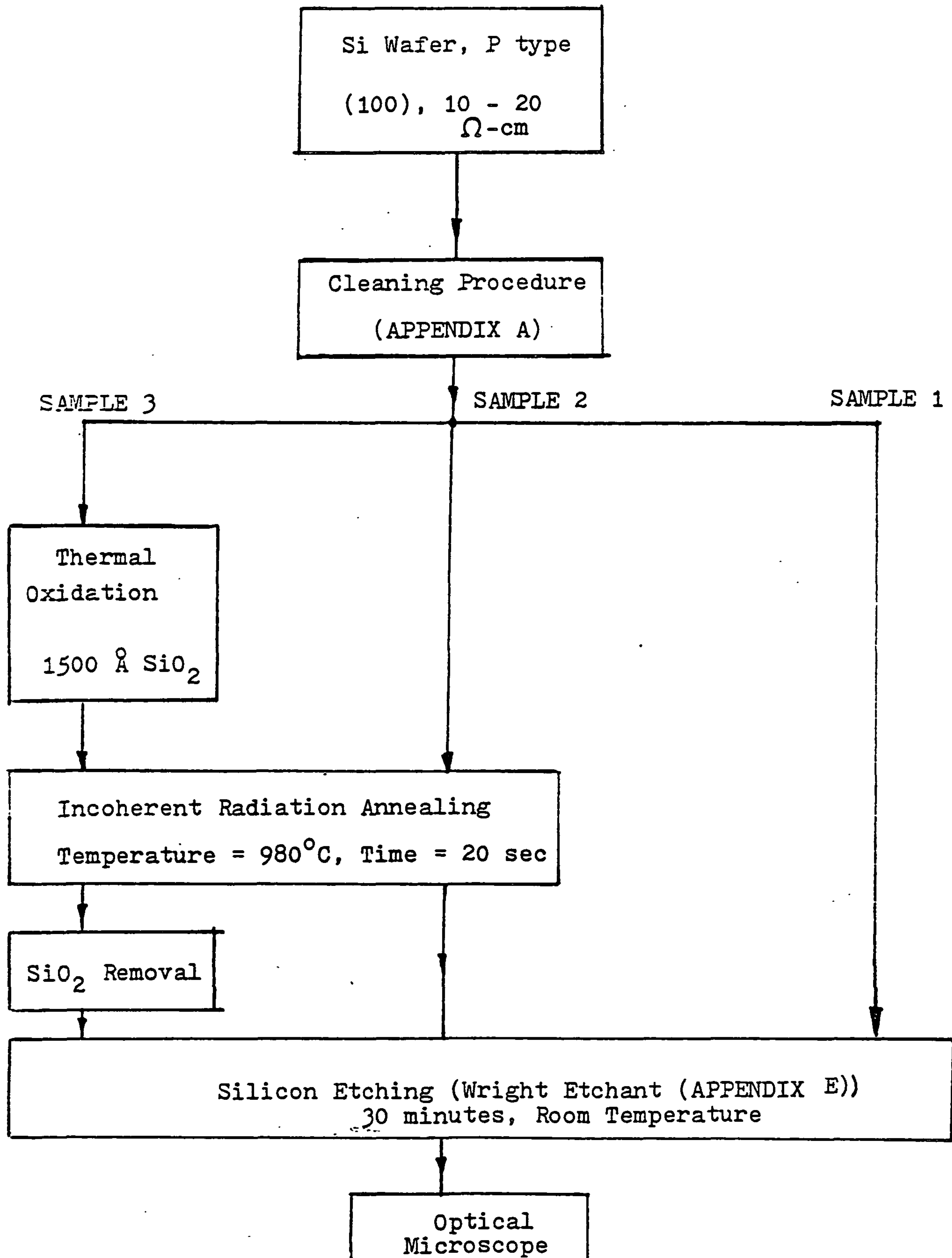
After completion of the three different processes, photographs were taken on the surface of the silicon wafers. They are shown in Figure 32.

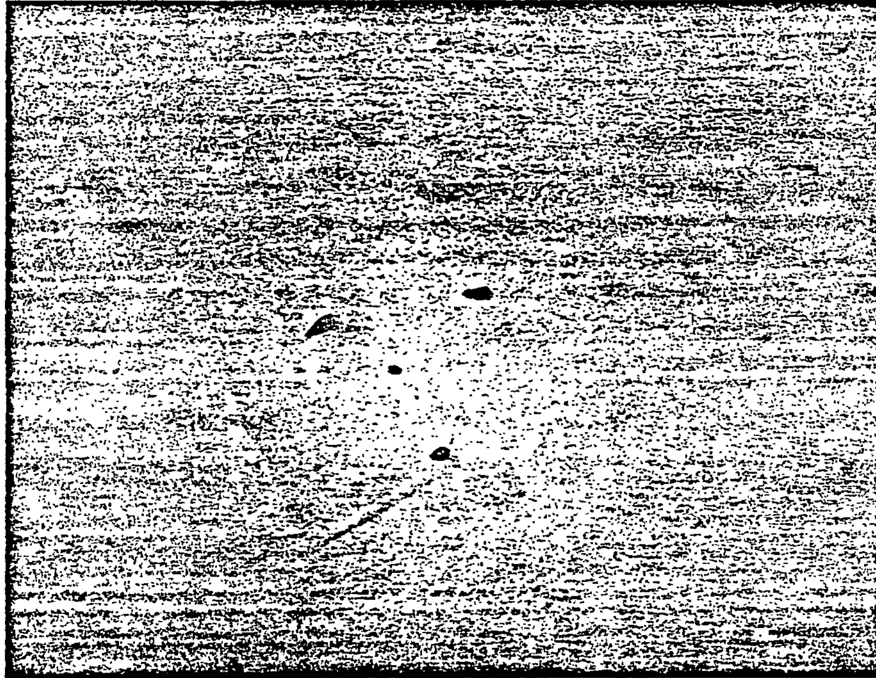
The results indicate that the SiO_2 film actually protects the surface of the silicon wafers from some aspect of radiation damage. This coincides

TABLE 9

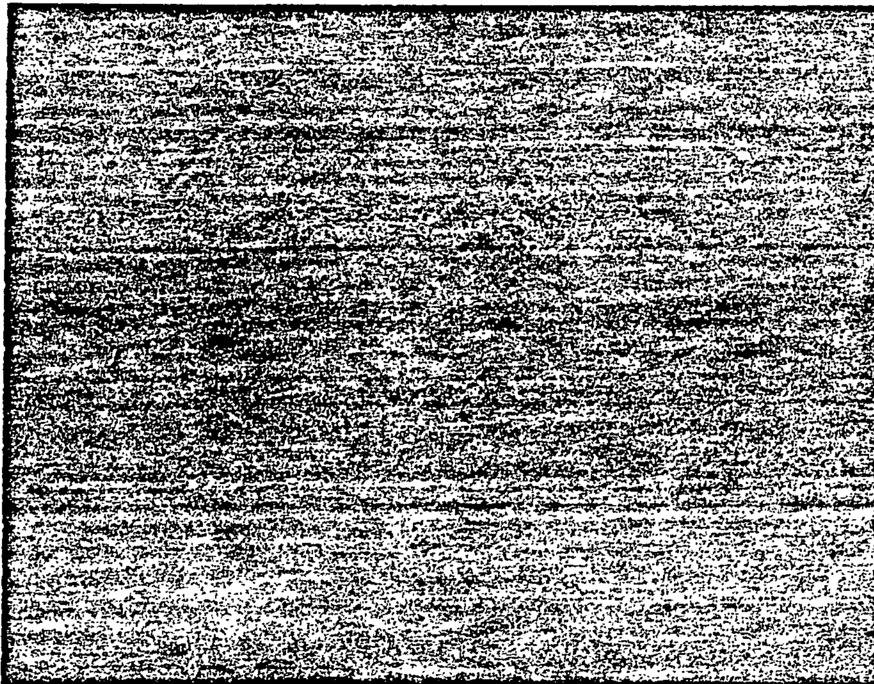
SAMPLE NO.	GROWTH CONDITION	INTENSITY OF (111) PEAK	INTENSITY OF (110) PEAK
1	700^oC 10 min. in CVD furnace	14	9
2	750^oC 10 min. in CVD furnace	35	13
3	[1] 700^oC 10 min. in CVD furnace [2] 30" from 25^oC to 730^oC 30" annealing at 730^oC 30" from 730^oC to 100^oC	39	14
4	[1] 700^oC 10 min in CVD furnace [2] 30" from 25^oC to 730^oC 1' annealing at 730^oC 30" from 730° to 100^oC	42	10
5	800^oC 10 min. in CVD furnace	28	over scale

FIGURE 31.





(a) SAMPLE 1.



(b) SAMPLE 2.

FIGURE 32. Surface Defects Inspection On Silicon Wafers.

(c) SAMPLE 3.

FIGURE 32. (CONTINUED)

with our experience that migration of aluminum dots through silicon wafers with oxide always gives us P-N junctions with lower leakage current. This is because there are more surface defects generated by the radiation in the unoxidized case.

VI. CONCLUSIONS

The deep diode arrays fabricated by TGZMP have proved to be very suitable for x-ray detection. A 500 eV FWHM energy resolution has been obtained by biasing the device to -5 volts. We believe that better results would have been possible if more suitable masks and packages were available.

TGZMP has proved to be a very reproducible process for fabricating the deep diode arrays. Some key points about the fabrication process are:

(1) to use both side polished high purity wafer for processing.

(2) to use thick wafer (14 to 16 mils).

(3) to grow 1200 Å to 1500 Å SiO_2 for both radiation shield and etching mask for the silicon wafer.

(4) to use mechanical mask to define the aluminum pattern on the silicon wafer directly.

(5) to use long rise and fall time (3 min to 4 min) to keep the lifetime longer, and also to migrate aluminum in controlled atmosphere.

(6) to grow a low temperature wet oxide for surface passivation.

Thermal migration offers solutions toward extending x-ray detectors to the 5 to 50 KeV range and still obtaining good energy and spatial resolution. Some strong features of these x-ray detectors are:

(1) ability to produce detectors with good energy and spacial resolution.
If those extra energy peaks in the spectrum can be proved to be the crosstalk between diodes in the same array in further experiment, the dimension of these arrays can be shrinked to within the diffusion length of the carriers in the bulk.

(2) ability to detect high energy x-rays using moderate

bias voltages and moderate resistivity material.

(3) Variable pixel size from the order of tens of microns to hundreds of microns can be obtained.

TABLE 10

TYPE OF DETECTOR	ADVANTAGES	DISADVANTAGES
Diffused junctions	1. Easy to make. 2. Less radiation damage. 3. Less sensitive to contamination.	1. Less sensitive to radiation (dead layer effect).
Surface barriers	1. Sensitive to radiation. 2. Larger collection area. 3. Room temperature operation.	1. Poor spatial resolution. 2. Not easy to make. 3. Sensitive to radiation damage. 4. Sensitive to contaminations. 5. Larger leakage current.
Charge coupled device	1. Good spatial resolution.	1. Poor collection efficiency
Ion-implanted junctions	1. Smaller leakage current 2. Sensitive to radiation 3. Large collection area 4. Room temperature operation	1. Low temperature operation for low energy radiation or particles.
Thermally migrated junctions	1. Good spatial resolution. 2. Smaller leakage current 3. Less sensitive to contamination.	1. Fair collection efficiency (small junction area) 2. Low temperature operation

VII. REFERENCES

(1) W. G. Pfann, "Zone Melting", John Wiley & Sons, N.Y., (1966)

(2) H. E. Cline and T. R. Anthony, J. Appl. Phys., 43, p.10, (1972)

(3) T. R. Anthony and H. E. Cline, J. Appl. Phys., 47, p.2325, (1976)

(4) T. R. Anthony and H. E. Cline, J. Appl. Phys., 47, P.2316, (1976)

(5) C. C. Wen, Ph.d. Dissertation, (1979)

(6) G. C. Chern, Master Thesis, (1981)

(7) G. F. Knoll, "Radiation Detection and Measurement", John Wiley & Sons, N.Y., Chap. 11, (1983)

(8) G. Bertolini, and A. Coche, "Semiconductor Detectors", John Wiley & Sons, N.Y., Chap. 1, (1968)

(9) G. L. Miller, W. L. Brown, P. F. Donovan, and I. M. Mackintosh, IRE Trans. Nucl. Sci. NS7, P.185, (1960)

(10) W. M. Gibson, G. L. Miller, and P. F. Donovan, "Alpha, beta-, and gamma-ray spectroscopy", ed. K. Siegbahn, North-Holland Publ. Co., Amsterdam, p.348, (1965)

(11) K. G. McKay, and K. B. McAfee, Phys. Rev. 91, p.1079, (1953)

(12) L. M. Halbert, and J. L. Blankenship, Nucl. Instr. Meth. 8, p.106,(1960)

(13) C. W. Fabjan, M. Kenawy, and H. Rauch, Z. Physik 188, p.378, (1965)

(14) R. H. Pehl, F. S. Goulding, D. A. Landis, and M. Lenzlinger, Nucl. Instr. Meth. 59, p.45, (1968)

(15) A. S. Grove, "Physics and Technology of Semiconductor Devices", Chap. 6.

(16) the same as (9).

(17) B. Schwartz, and H. Robbins, "Chemical Etching of Silicon", J. Electrochem. Soc., 123, p.1903, (1976)

(18) R. M. Finne, and D. L. Klein, "A Water-Amine-Complexing Agent System for Etching Silicon", J. Electrochem. Soc., 114, p.965, (1967)

(19) J. B. Price, Report of Motorola Semiconductor Product Division.

(20) R. M. Burger, and R. P. Donovan, "Fundamentals of Silicon Integrated Device Technology", Vol. I., Prentice-Hall Inc., Chap. 2, (1967)

(21) H. F. Wolf, "Silicon Semiconductor Data", Pergamon Press, p.138.

(22) the same as (8), p.111.

(23) L. C. Shen, and J. A. Kong, "Applied Electromagnetism", Brooks/Cole Engineering Division, p.304, (1983)

(24) the same as (8), Chapter 3.

(25) T. V. Blalock, IEEE Trans. Nucl. Sci. NS-13, p.457, (1966)

(26) J. Kemmer, Nucl. Inst. and Meth., 169, p.499, (1980)

(27) J. Kemmer, P. Burger, R. Henck, and E. Heijne, " "Performance and Application of Passivated Ion-Implanted Silicon Detectors", IEEE Trans. Nucl. Sci., p.733, (1982)

(28) W. Kern, "Apparatus for Chemical Vapor Deposition of Oxide and Glass Film", RCA Review, Dec., p.525, (1968)

(29) N. Goldsmith, and W. Kern, "the Deposition of Vitreous Silicon Dioxide Films from Silane", RCA Review, March, p.153, (1967)

(30) W. A. Pliskin, and H. S. Lehman, "Structural Evaluation of Silicon Oxide Films", J. Electrochem. Soc., Vol. 112, p.1013, Oct., (1965)

(31) T. J. Kamins, and T. R. Cass, "Structure of Chemically Deposited Poly Crystalline-Silicon Films", Thin Solid Films, 16, p.147, (1973)

APPENDIX A

I. Initial cleaning:

(a) Boil wafer in mixture of H_2SO_4/H_2O_2 (4/1) for 10 minutes.

(b) Rinse in deionized H_2O.

(c) Etch wafer in 10% HF for 1 minute.

(d) Rinse in deionized H_2O.

II. Basic cleaning:

(a) $NH_4OH/H_2O_2/H_2O$ (1/1/5) at temperature 75 ∿ 85°C for 10 minutes.

(b) Rinse in deionized H_2O.

(c) $HCl/H_2O_2/H_2O$ (1/1/5) at temperature 75 ∿ 85°C for 10 minutes.

(d) Rinse in deionized H_2O.

(e) Spin dry the wafers.

APPENDIX B

Molybdenum etchant:

(a) H_3PO_4 : 38 parts (by volume)

(b) HNO_3 : 15 parts

(c) CH_3COOH: 30 parts

(d) H_2O : 75 parts

APPENDIX C

Aluminum etchant:

(a) H_3PO_4	150 ml
(b) HNO_3	5 ml
(c) CH_3COOH	5 ml
(d) H_2O	10 ml

APPENDIX D

Anisotropic silicon etchant:

(a) $C_6H_4(OH)_2$	4.0 m/o
(b) $NH_2(CH_2)_2NH_2$	46.4 m/o
(c) H_2O	49.6 m/o

APPENDIX E

Wright etchant:

(a)	HF	60 ml
(b)	HNO_3	30 ml
(c)	CrO_3 (5M)	30 ml
(d)	$Cu(NO_3)_2 \cdot 3H_2O$	2 g
(e)	CH_3COOH	60 ml
(f)	H_2O	60 ml