5.6A COMPLEMENTARY CODE AND DIGITAL FILTERING FOR DETECTION OF WEAK VHF RADAR SIGNALS FROM THE MESOSPHERE

G. Schmidt, R. Ruster and P. Czechowsky

Max-Planck-Institut fur Aeronomie
D-3411 Katlenburg-Lindau 3, Germany

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THE SOUSY RADAR FACILITY

The SOUSY-VHF-Radar operates at a frequency of 53.5 MHz in a valley in the Harz mountains, Germany, 90km from Hanover. Figure 1 presents a block diagram of the radar facility with the main system parameters. The radar controller, which is programmed by a 16-bit computer, is the central unit. It holds 1024 program steps in core and controls, via 8 channels, the whole radar system: in particular the master oscillator, the transmitter, the transmit-receive-switch, the receiver, the analog to digital converter, and the hardware adder.

The transmitter operates as a linear amplifier with a bandwidth of 2.5 MHz. The peak pulse power is 600 kW and the duty cycle 4 percent. The pulse length can be varied from 0.8 to 100 μs. The maximum height resolution is somewhat larger than 120 m because the receiver bandwidth is 1 MHz. Pulse length, pulse coding, and pulse repetition frequency are easily adjustable to the requirements of the different observational programs by software instructions.

The transmitter, the receiver, and the antenna are connected to a high-speed transmit-receive switch with a recovery time of less than 5 μs, corresponding to a minimum radar range of about 750 m. The transmitting antenna consists or a system of 196 four-element Yagis with a total gain of 31 dB and a half-power beamwidth of 5°. To reduce interference with commercial TV stations and to reduce the influence of ground clutter from the surrounding mountains, the suppression of the first side lobes of the antenna pattern is about 20 dB and the antenna response far off-axis (which corresponds to low elevation angles) is approximately 40 dB. At present the antenna beam is directed to the zenith. By means of a system of 4-bit phase shifters, which are computer controlled, the extended version of this array will be steerable continuously in any direction within a cone of 30° vertex angle centered on the vertical. The high-sensitivity receiver has a dynamic range of 70 dB and a video bandwidth of 1 MHz. The complex signals at the receiver output are digitized by an analog-to-digital converter. The maximum sample frequency is 2 megawords/s, with a word length of 10 bits, corresponding to a dynamic range of 57 dB. These digitized complex signals can be coherently added by a hardware adder with a maximum core for 1024 complex values. The adder also is used for coding techniques. Phase coding schemes are applied, in particular for investigations at mesospheric heights, in order to carry out measurements with the maximum duty cycle and the maximum height resolution. The computer takes the data from the adder to store it in magnetic tape or disc.

The central unit of the radar facility is the radar controller, which synchronously controls the whole system. The radar controller is programmed by the computer using simple Fortran IV statements. After the program has been loaded and the computer has started the radar controller, it runs automatically, stopping at the program end. In case of errors or failures occurring during the radar operation, the radar controller is shut off caused either by a

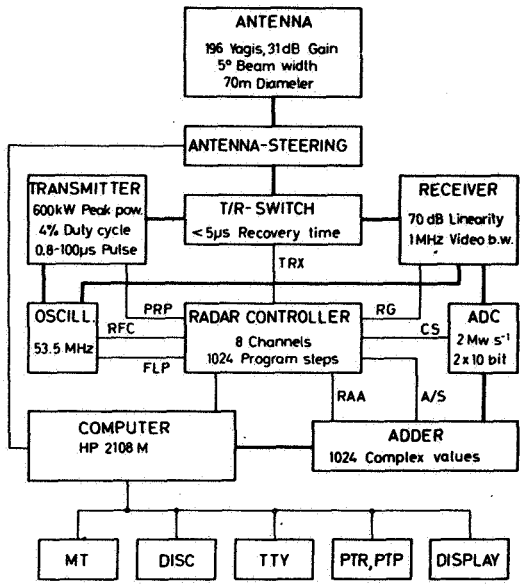

Figure 1. Block diagram of the SOUSY-VHF-Radar facility. (MT-magnetic tape, DSC-moving head disc, TTY- eletype, PTR, PTP-paper tape read/punch, DISPLAY-storage oscilloscope.

safety circuit from the transmitter and the transmit-receive-switch or by a power failure circuit or by a parity check system in the radar controller. The response time of a shutdown in only 50 ns.

Figure 2 shows the block diagram of the radar controller. Its program, generated by the computer, is stored in two different memories and two latches. The core size of each memory is 1024 storage locations of 8-bit length. An additional bit is used for parity check. The first memory (program memory) contains the various commands and the second (rate memory) the respective time intervals for which the commands have to be carried out. These execution times are counted in clock periods, which can be chosen to be 0.5, 1, 2, or 4 µs each. Since a storage location in the rate memory consists of 8 bits, the maximum length to be stored is 255 clock periods. If, however, a program step longer than 255 clock periods is required, this command is divided into several

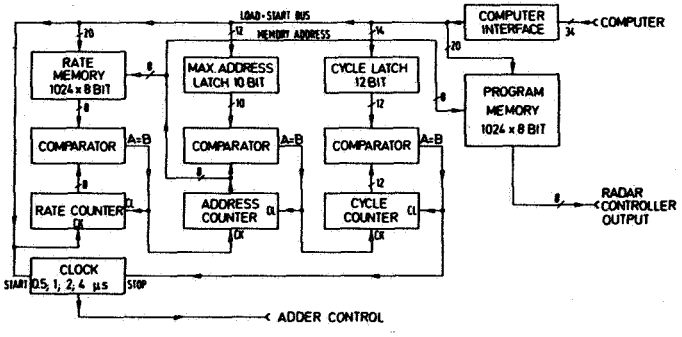

Figure 2. Block diagram of the radar controller.

sequential program steps. The two latches contains the number of repetitions of the radar cycle (cycle latch) and the maximum address for the program in the rate and program memory (maximum address latch). Three cascaded counters with comparators for reset are used as address counter, rate counter, and cycle counter.

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