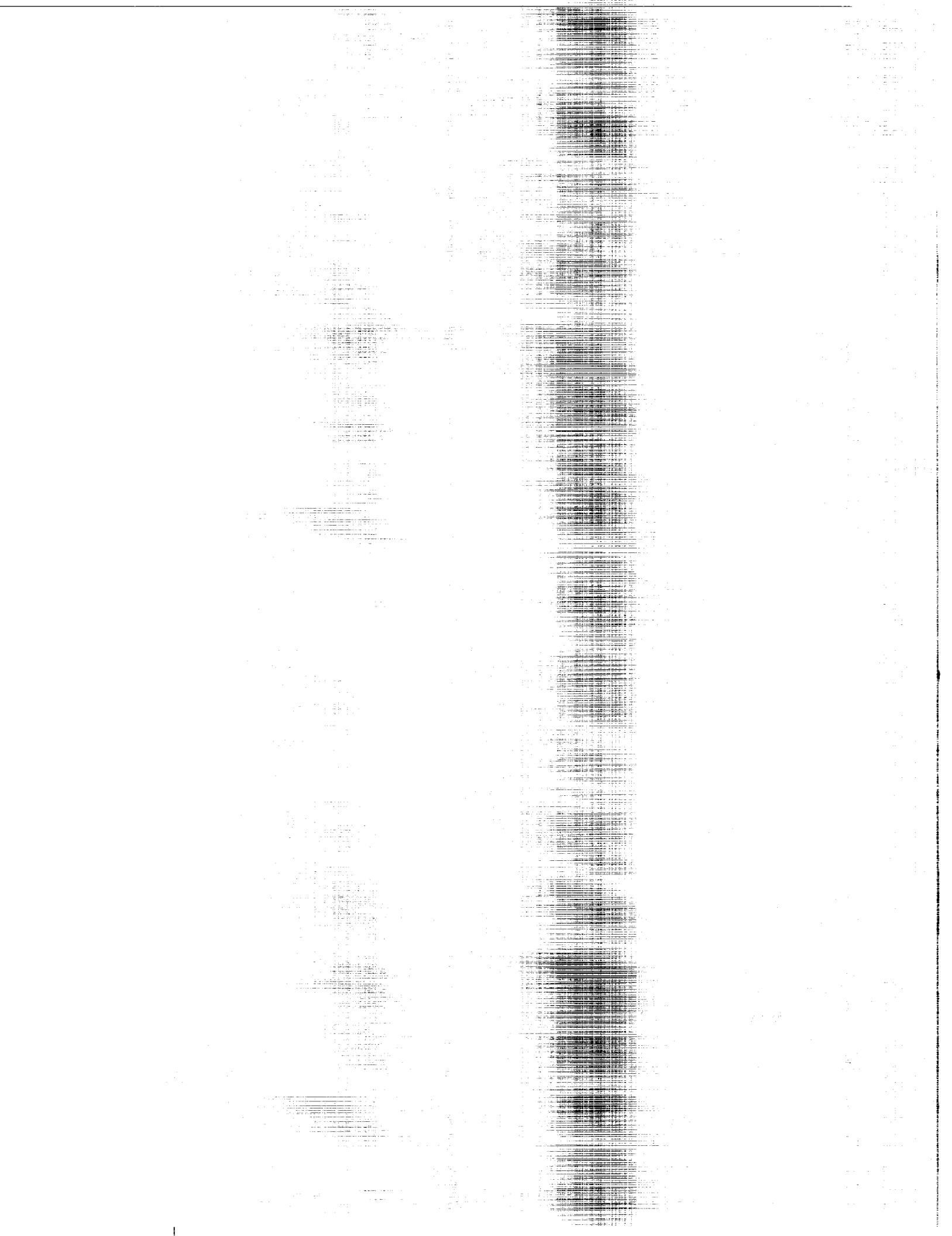
NASA Conference Publication 2356
Supplement to NADC-84104-20

International Aerospace and Ground Conference on Lightning and Static Electricity

1984 Technical Papers

Supplement to the proceedings
of a conference held in
Orlando, Florida
June 26-28, 1984

NASA



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PREFACE

This publication is a supplement to the proceedings of the 1984 International Aerospace and Ground Conference on Lightning and Static Electricity held on June 26-28, 1984, in Orlando, Florida. The conference proceedings are reported in "International Aerospace and Ground Conference on Lightning and Static Electricity - 1984 Technical Papers," which is available as NADC-84104-20. This conference was sponsored by the National Interagency Coordination Group (NICG) on Lightning and Static Electricity consisting of members from NASA, the Federal Aviation Administration, and the United States Air Force, Army, and Navy. NICG sponsored the conference in concert with the Florida Institute of Technology and in association with the Institute of Electrical and Electronic Engineers, SAE-AE4 Committee, the United Kingdom Civil Aviation Authority, the United Kingdom Royal Aircraft Establishment Farnsborough, and Culham Laboratory.

This supplement contains papers that were presented at the conference but were unavailable for printing at the time of publication of the proceedings. The papers are numbered as they were for the conference. The papers were submitted for publication in camera-ready form. The material was taken from a variety of sources; therefore, various units of measure are used.

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CONTENTS

UPSET SUSCEPTIBILITY STUDY EMPLOYING CIRCUIT ANALYSIS AND DIGITAL SIMULATION

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ABSTRACT

This paper describes an approach to predicting the susceptibility of digital systems to signal disturbances. Electrical disturbances on a digital system's input and output lines can be induced by activities and conditions including static electricity, lightning discharge, Electromagnetic Interference (EMI) and Electromagnetic Pulsation (EMP). The electrical signal disturbances employed for the susceptibility study were limited to nondestructive levels, i.e., the system does not sustain partial or total physical damage and reset and/or reload will bring the system to an operational status. The front-end transition from the electrical disturbances to the equivalent digital signals was accomplished by computer-aided circuit analysis. The SCEPTRE (system for circuit evaluation of transient radiation effects) program was used. Gate models were developed according to manufacturers' performance specifications and parameters resulting from construction processes characteristic of the technology. Digital simulation at the gate and functional level was employed to determine the impact of the abnormal signals on system performance and to study the propagation characteristics of these signals through the system architecture. Example results are included for an Intel 8080 processor configuration.

INTRODUCTION

The use of digital electronic systems onboard aircraft is increasing and these systems are eventually expected to perform flight-critical functions on new generation aircraft, thus creating the necessity for ultrareliable digital systems. Various approaches are being taken to achieve ultrareliable fault-tolerant systems that will survive the occurrence of component/subsystem failure. A different threat to digital systems comes from internal state changes caused by external disturbances such as lightning. Aircraft flying in adverse weather conditions can be subjected to lightning discharge which will produce transients on system lines, data buses, etc. Work has been conducted to establish the interaction between the lightning-produced electromagnetic environment and the aircraft (ref. 1). This work is expected to determine the induced voltage energy spectrum and levels inside the aircraft as a result of lightning discharge and the effects of various parameters (electronic system location, cable length, cable type, shielding, etc.) on the induced voltages.

The inherent characteristics of digital systems make these induced transients a major threat since, unlike analog computational systems, a transient on a digital system can cause a logic state change preventing the machine from performing as intended after the transient. In most cases after the machine has entered into an erroneous operation, a reset and (or) a reload are necessary to bring it to normal operation. This erroneous operation is called an upset mode and no component or subsystem failure exists.

Studies of possible changes in program flow (due to upset) and its relation to program structure have been under way for several years (ref. 2). The purpose of the work described in this paper is to develop a methodology through which the susceptibility of a digital system to induced transients can be evaluated. A possible by-product is the identification of system design procedures that increase or decrease the vulnerability of the system to threats as described above. Since the susceptibility study deals with nondestructive transient levels, investigation and tests of component failures caused by excess voltage levels were performed. Upper bounds were established for transient voltage level to avoid failure of the system under test.

The study is divided into two parts: (1) translation of transients into digital equivalents using component-level circuit analysis by associating logic levels with the transient disturbance, and (2) functional-level digital system simulation and transient injection using "digital equivalent transients" produced by this circuit analysis. Figure 1 illustrates the methodology described in this paper.

CIRCUIT ANALYSIS

The waveshapes used for transient injection are shown in figure 2. These waveshapes are recommended by SAE subcommittee AE4L (ref. 3) for lightning-induced transient studies. They are representative of the form of voltages and currents that may be present in cables in a lightning-produced electromagnetic environment. The waveshapes are intended for direct injection on system pins and lines, and levels of the waveshapes are restricted to nondestructive levels.

When analog transients are injected on digital system lines or pins they reach the interfacing circuitry in the system devices. A prediction of the behavior of the interfacing digital circuitry when driven with the analog transient was performed by analyzing the circuitry at the component level using the SCEPTRE (system for circuit evaluation of transient radiation effects) program. Circuit topology is converted to an equivalent SCEPTRE circuit description to be used as input data for the SCEPTRE program. Transistors and diodes are modeled using the basic elements necessary for the SCEPTRE equivalent circuits, including resistors, capacitors, inductors, current and voltage sources. Values for the Ebers-Moll transistor model and the diode model were obtained from manufacturers' data and from information of typical fabrication processes for monolithic integrated circuits. A family of component-level logic models for use in SCEPTRE analysis including gates, flip-flops, and tri-state devices has been developed for this study for transistor-transistor logic (TTL) and complementary metal oxide semiconductor (CMOS) technology.

A typical transient injection circuit used to generate transients coupled to digital devices and shown in figure 3 was designed, breadboarded and tested to compare its operation with SCEPTRE analysis of such a circuitry. The tank circuit is connected to the injection point through a parallel RC circuit for isolation. Since the injection point of the circuit under test has a nonlinear input impedance, the waveshape at the injection point is clipped, nonsinusoidal, and thus unlike the sinusoidal tank output. The SCEPTRE code accurately models this circuit as shown in figures 4 and 5. To achieve the nonclipped SAE recommended waveshape at the injection point, an idealized injection circuit was defined for use with SCEPTRE in the upset

susceptibility study. The idealized circuit is accomplished in the SCEPTRE code via a mathematical function and has a low impedance source, perfect switches, and very high frequency response.

Figures 6 and 7 are examples of the response of a D-type flip-flop used in a latch circuit to the modeled injection circuit and the idealized transient signal. The transient was injected on the data input line while the flip-flop was disabled and in a high state. In the first example, using the oscillating tank injection circuit, the flip-flop state was changed from a high to low state. In the second example, using the ideal injection source, the flip-flop does not experience a state change. Thus, the injected signal harmonic content as well as the coupling circuit has an impact on the circuit analysis results.

SYSTEM SIMULATION

An 8080 microprocessor-based computer system was simulated in the functional-level simulation study. This system was chosen to provide comparison with a similar hardware-based study (ref. 4). Functional-level simulation was accomplished with the General Simulation Program (GSP) (ref. 5) running on a CDC Cyber 170-730 computer. This program has the capability for 16 functional models such as counters, microprocessors, latches, etc. The modeling is performed with a microcode instruction set. Variable propagation delay and internal registers can be implemented in the simulation. An example of a flip-flop model described with the microcode is listed in table 1.

Figure 8 shows the system block diagram used in the upset susceptibility study. An extra module was designed and added to the model system to access the system lines for injection purposes. The injection module is inserted in the line on which injection is intended. Under normal operation, the system signal propagates through the injection module unaltered with no time delay. Therefore, this module, when disabled, is completely transparent to the remaining modules. When the injection module is enabled, the affected line signal is controlled by the user running the simulation. The digital equivalent signal, derived from the SCEPTRE circuit analysis using the idealized transient signal, was used to control the affected line. State changes of latches at either end of the affected line are used to introduce logic errors into the digital signals transmitted over the line according to the results of the circuit analysis.

The program executed during injection studies is in table 2. The program loads a byte from memory into the accumulator, stores the accumulator into memory and jumps to the first instruction at memory location $(1000)_{16}$ in a continuous loop. This program exercises three of a possible ten machine cycles (table 3) and is intended to provide a correlation of the machine cycles with the upset conditions. The first set of hardware tests was performed and reported in reference 4 using this program.

The program is loaded in RAM starting at memory location ROM location $(1000)_{16}$. When the simulation starts, the microprocessor is initialized equivalent to a power on reset. It loads and executes a jump instruction in $(0000)_{16}$ and after 6500 nanoseconds the microprocessor starts executing the program in RAM address $(1000)_{16}$.

The time of the transient injection into the system was determined by selecting a random number between 0 and 15000 and adding it to 6500. The time required by the microprocessor to execute the program in RAM once is 15000 nanoseconds. Therefore, the injection can occur with equal probability at any point in the program. The random numbers were obtained from a table of random numbers (ref. 6) and normalized to meet the boundary requirement.

TEST RESULTS

During initial upset test runs, operation codes (op-codes) that are undefined in the microprocessor instruction set were loaded in the instruction register as a result of the injected transients. The simulation microprocessor model treated these undefined op-codes as "no operation" instructions. A program that makes use of the undefined op-codes was written and executed in hardware to determine the response of the microprocessor to such codes, and modifications were made to the microprocessor model accordingly. Of the 12 undefined codes 7 acted as one byte instruction and execution continued with the next immediate byte and 5 acted as control instructions with the next two bytes as part of the instruction. No attempt was made to reproduce with the microprocessor model the control output signals generated when the hardware microprocessor is executing the undefined op-codes.

Sixty-six transient injections were performed during program execution. Each transient injection was performed on a single line at a time and in all 66 cases the injected signal was the digital equivalent of a 1 MHz damped sinusoid. The points of the injections in the system were MDI_0, MDI_3, and MDI_7 of the input data bus, DB_0 of the output data bus, D_0 of the bidirectional data bus, and MAD_0 of the memory address bus.

During execution, the microprocessor bidirectional data bus, high and low address bus, system output data bus, and chip selection control lines were monitored, as well as the pins and internal registers of the microprocessor model. Locations in memory that were not used for the program were loaded with zero $(00)_{16}$ in the simulation as opposed to the hardware test (ref. 4) where unused memory locations had random content. Therefore, when program control was transferred to a memory location out of the defined program, the no-operation instruction NOP $(00)_{16}$ was loaded and no undefined status word was observed during any of the transient injection runs. Forty-one system anomalies were registered including 24 errors and 17 upsets. System anomalies, errors and upsets for each injection line are summarized in table 4. In the error case, the microprocessor stored or loaded erroneous data, stored data in a non-specified location or skipped an instruction but went back to the normal program loop. In the upset case, the microprocessor went out of the program loop to empty or nonexistent memory locations. Simulation test results on system errors and upsets as a function of injection lines were comparable with hardware results with the exception of the memory address line (MAD) where no errors or upsets were registered in 346 injections in the hardware test and seven errors and four upsets were recorded in 11 injections in the simulation test. Further tests are presently being performed to resolve the difference between hardware and simulation upsets caused by injections on the MAD_0 line. Of 17 upsets, 13 were caused when the injection was performed during the jump instruction. These results point to an apparent higher susceptibility to upset of the program control instruction. Table 5 shows the classification of upsets and errors when the injections were performed during load (MVIA), store (STA) and jump (JMP).

SUMMARY AND CONCLUSIONS

The simplicity of the program executed during transient runs permitted observation of the patterns that led to the upset condition. The upset susceptibility is highly dependent on program structure (ref. 2). When 1 bit of a 3-byte instruction is changed, the instruction could become a 1-byte instruction, and the two next immediate data bytes are then loaded as instructions. This condition was observed 12 times during the 66 upset test runs and three of those cases led to upset. In total, 29 data bytes were read as instructions and the effect on the program flow depended on the data value, its location in the program, and the instruction immediately after the data byte or bytes.

Although none of the test runs caused the original program in RAM to be partially or totally overwriting, the potential for overwritten program was identified in the error cases when the microprocessor stored data in memory locations different from those specified.

Results of the study can be used to obtain the parameters necessary for a stochastic model, similar to the stochastic model in reference 4, to compute susceptibility of the system. The methodology described provides the capability of performing upset tests and establishing an upset susceptibility level for a system using models developed during design stages.

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4. Celeste M. Belcastro, "Digital System Upset - The Effects of Simulated Lightning-Induced Transients on a General-Purpose Microprocessor," NASA TM 84652, 1983.

5. Donald E. Devlin, "A Chip Level, Multimode Logic Simulator," M.S. Thesis, Virginia Polytechnic Institute and State University, 1981.

6. William H. Beyer, ed., "Handbook of Tables for Probability and Statistics," Second Ed., CRC Press, 1976.

TABLE 1 - FLIP-FLOP MODEL WITH GSP MICROCODE

```
; MODEL J K
;
;DECLARATION OF INTERNAL REGISTERS
;NO INTERNAL REGISTERS ARE NEEDED IN J K MODEL
;
   REG(1)  DUMMY
;
;DECLARATION OF ALL EXTERNAL CONNECTIONS
;PIN EX(150) FOR SIMULATION CONTROL PURPOSES
;
   PIN   J(1),K(2),Q(3),QBAR(4),CLK(5),EX(150)
;
;PROPAGATION DELAY SPECIFICATION
;
   EVW   OUT(15)
;
       BEQ  CLK,LATCH   ;   IF CLK EQUAL ZERO JUMP TO LATCH
       BEQ  J,K,INT     ;    IF J EQUAL K JUMP TO INT
       MOV(OUT)  J,Q    ;  GIVE Q THE VALUE OF J AFTER A 15
                        ;  NANOSECOND DELAY
       MOV(OUT) K,QBAR  ;  GIVE QBAR THE VALUE OF K AFTER A 15
                        ;  NANOSECOND DELAY
       MOV    #0,EX     ;  TERMINATE THE EXECUTION OF
                        ;  THIS MODULE
INT:   BEQ  J,LATCH
       COM(OUT)  Q      ;  COMPLEMENT THE VALUE OF Q
                        ;  INSTRUCTION IS EXECUTED WHEN J=K
       COM(OUT)  QBAR   ;  COMPLEMENT THE VALUE OF QBAR.  THIS
                        ;  INSTRUCTION IS EXECUTED WHEN J=K
LATCH:  MOV   #0,EX
   END
```

TABLE 2 - PROGRAM CODE EXECUTED DURING INJECTION STUDIES

CLOCK CYCLES	ADDRESS	INSTRUCTION	MNEMONIC
7	10 00	3E	MVIA
	01	CB	
13	02	32	STA
	03	19	
	04	10	
10	05	C3	JMP
	06	00	
	07	10	

TABLE 3 - 8080 MACHINE CYCLES AND CORRESPONDING 8-BIT STATUS SIGNALS IN HEXADECIMAL FORMAT

MACHINE CYCLE	STATUS SIGNAL
INSTRUCTION FETCH	A2
MEMORY READ	82
MEMORY WRITE	00
STACK READ	86
STACK WRITE	04
INPUT	42
OUTPUT	10
INTERRUPT	23
HALT	8A
INTERRUPT WHILE HALT	2B

TABLE 4 - SYSTEM ANOMALIES AT EACH INPUT POINT ON THE SIMULATED SYSTEM UNDER TEST

INPUT POINTS	INJECTIONS	SYSTEM ANOMALIES	ERRORS	UPSETS
MDI_0	11 (11)	6 (11)	2 (3)	4 (8)
MDI_3	11 (11)	4 (11)	2 (0)	2 (11)
MDI_7	11 (11)	10 (11)	7 (1)	3 (10)
D_0	11 (2)	11 (2)	6 (1)	5 (1)
MAD_0	11 (346)	11 (0)	7 (0)	4 (0)
DB_0	11 (720)	1 (0)	1 (0)	0 (0)
	66	43	25	18

( ) Hardware test results.

TABLE 5 - UPSETS AND ERRORS FOR TRANSIENT INJECTIONS DURING INSTRUCTION CYCLE

	MVIA	STA	JMP	TOTAL
NO UPSET	11	10	4	25
ERRORS	14	10	0	24
UPSET	1	3	13	17
TOTAL	26	23	17	66

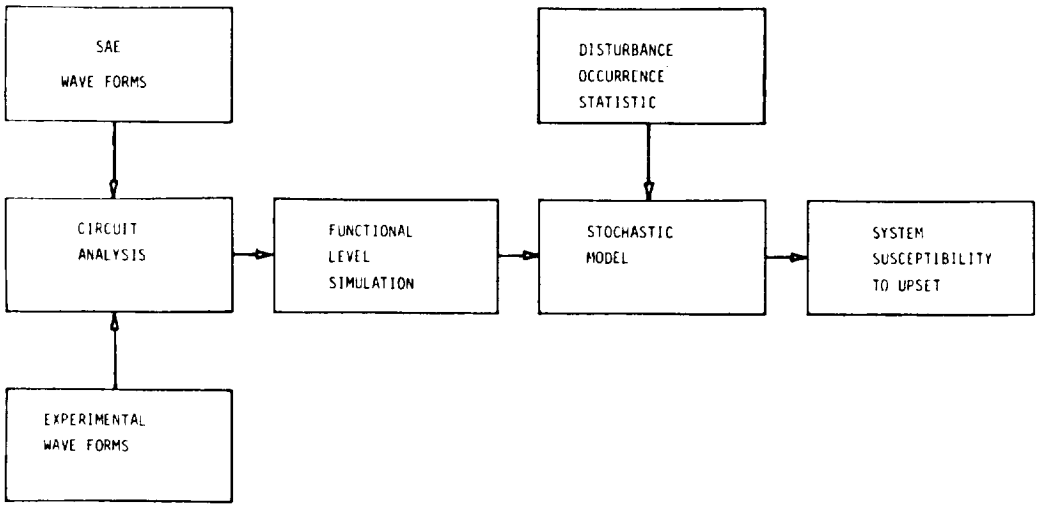

Figure 1. Methodology for susceptibility study.

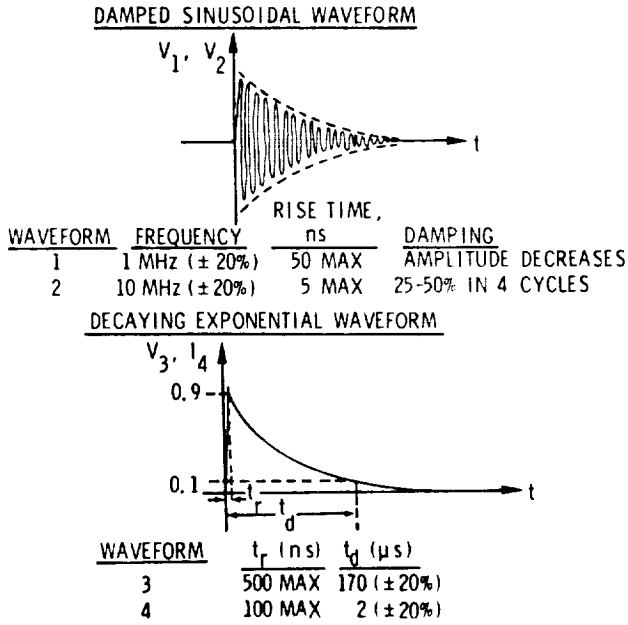

Figure 2. SAE waveforms recommended for lightning-induced testing.

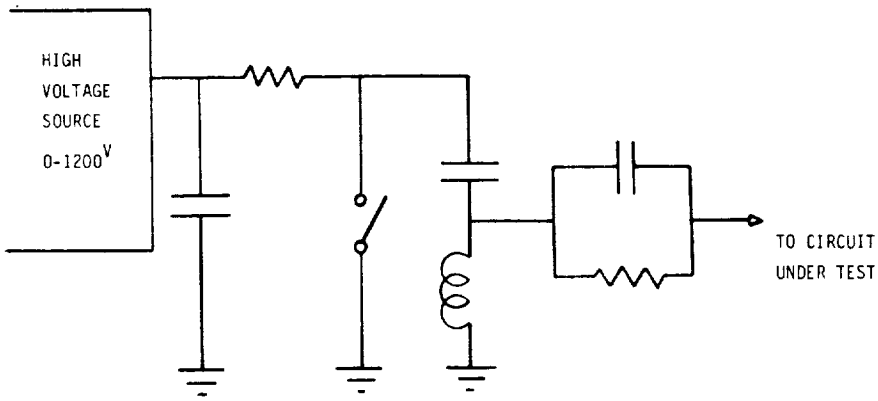

Figure 3. Transient generator circuit.

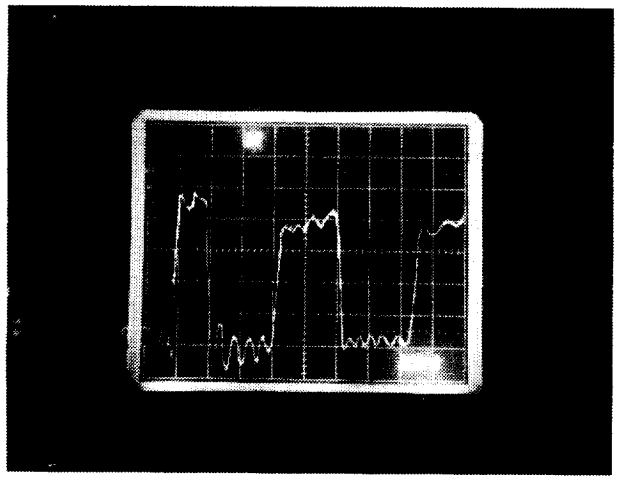

Figure 4. Transient input signal on the flip-flop D line of a hardware setup using a tank injection circuit (1 V, 200 ns).

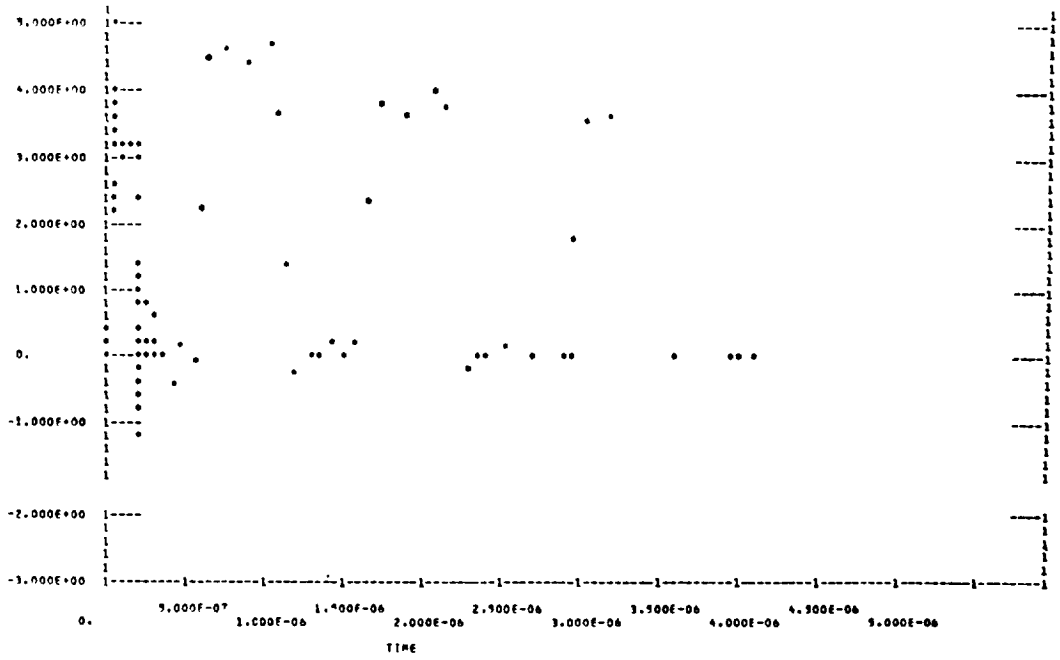

Figure 5. Transient input signal on the flip-flop D line of a modeled configuration using a modeled tank injection circuit.

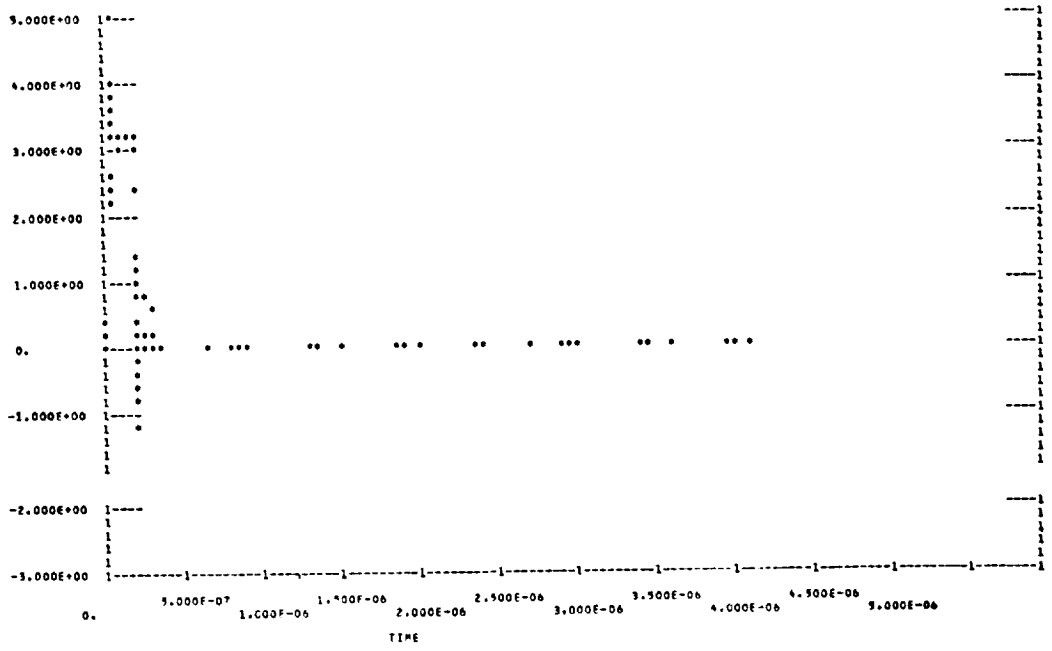

Figure 6. Flip-flop response to the modeled transient injection circuit.

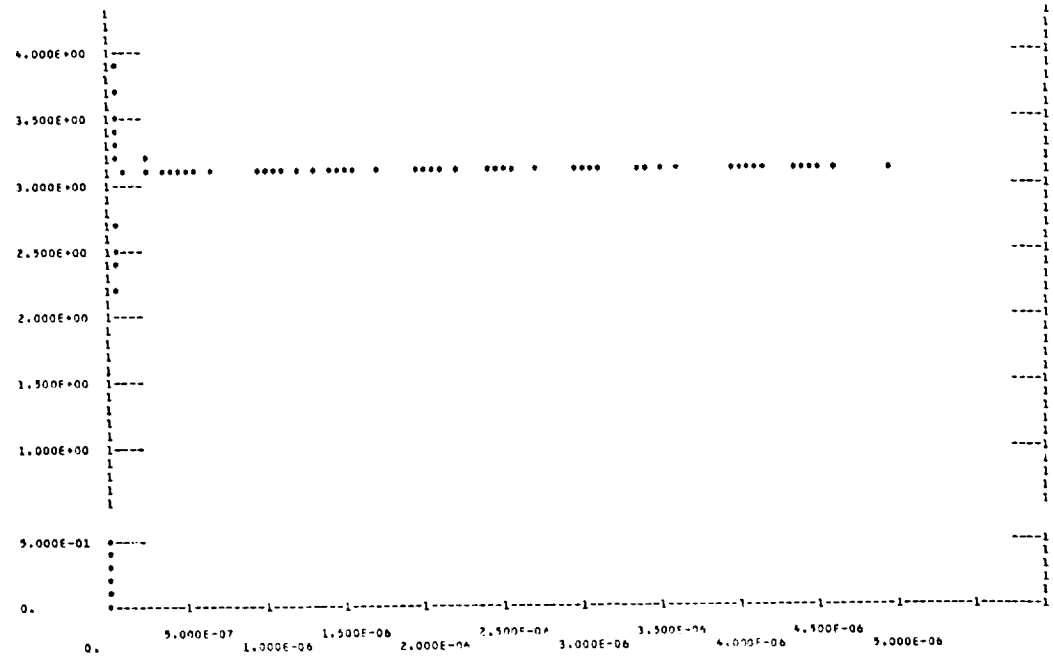

Figure 7. Flip-flop response to the idealized transient signal.

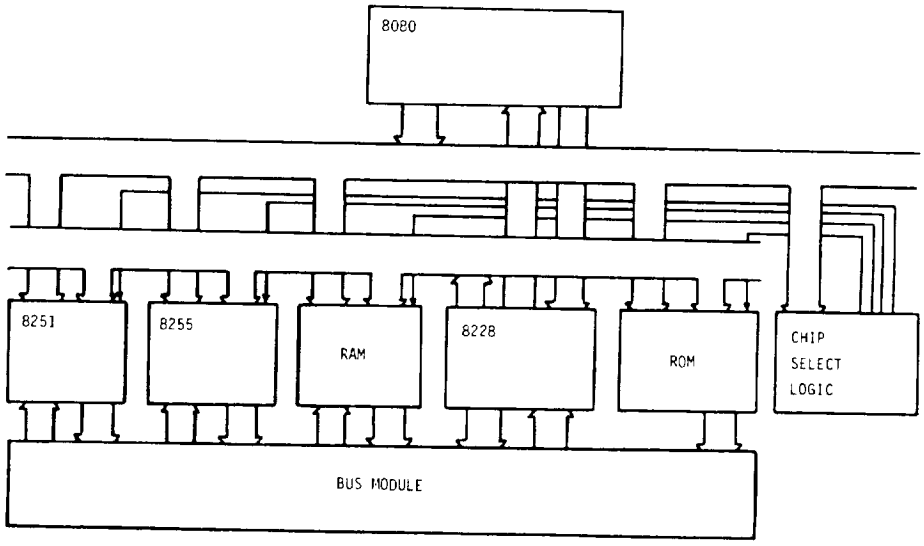

Figure 8. System under test.

DATA AND RESULTS OF A LABORATORY INVESTIGATION OF MICROPROCESSOR UPSET CAUSED BY SIMULATED LIGHTNING-INDUCED ANALOG TRANSIENTS

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ABSTRACT

Advanced composite aircraft designs will include fault-tolerant computer-based digital control systems with high reliability requirements for adverse as well as optimum operating environments. Since aircraft penetrate intense electromagnetic fields during thunderstorms, onboard computer systems may be subjected to field-induced transient voltages and currents resulting in functional error modes which are collectively referred to as digital system upset. A methodology has been developed for assessing the upset susceptibility of a computer system onboard an aircraft flying through a lightning environment. Laboratory tests were performed to study upset error modes in a general-purpose microprocessor. The upset tests performed involved the random input of analog transients which model lightning-induced signals onto interface lines of an 8080-based microcomputer from which upset error data were recorded. The program code being executed on the microprocessor during tests was designed to exercise all of the machine cycles and memory addressing techniques implemented in the 8080 central processing unit. For specific processing states and operations, correlations are established between upset occurrence and transient signal inputs. The application of Markov modeling to upset susceptibility estimation is discussed and a stochastic upset susceptibility model for the 8080 microprocessor is presented to demonstrate stochastic model development.

INTRODUCTION

Lightning strikes to aircraft cause transient voltages and currents to be induced on internal electrical cables throughout the aircraft. These transient signals can propagate to interface circuitry, power lines, etc., of onboard electronic equipment despite shielding and protection devices. Advanced composite aircraft provide less shielding than all-metal aircraft and will utilize computer-based digital control systems that are inherently sensitive to transient voltages and currents. Since these digital systems will be performing flight-critical functions, highly reliable performance must be maintained in adverse environments such as thunderstorms. Therefore, techniques for assessing the susceptibility, performance, and reliability of digital systems when subjected to analog electrical transients must be developed.

Digital system upset collectively refers to functional error modes without component damage in digital computer-based systems and can be caused by lightning-induced electrical transients. An upset test methodology was developed and described in detail in (1)* along with initial data and results. In this paper, more extensive data and results of upset tests performed using this methodology are presented. The purpose of these tests is to statistically investigate the upset susceptibility of a general-purpose microcomputer executing an application program in a simulated lightning environment. The objective of the statistical analysis is to identify correlations between the occurrence of upset and the processing activity of the system (which includes software as well as hardware) that is in progress when input of an analog transient signal occurs. In addition, the analysis serves to demonstrate the application of upset susceptibility assessment techniques. These techniques could be used as an aid in identifying system weaknesses that could be hardened to upset but may be especially useful during the design phase of system development. The application of Markov modeling to upset susceptibility prediction for an upset tolerant system is discussed viewing upset caused by lightning as a random process and using test observations as a basis to demonstrate the development of an upset susceptibility model for the general-purpose microcomputer.

* Numbers in parentheses designate references at end of paper.

UPSET TEST METHODOLOGY

The upset test methodology is based on the comparison monitoring of two synchronized Intel Intellec 8/Mod 80 microcomputers (μCs) executing identical program code concurrently. The Intellec 8 Mod/80 is a modular system based on the 8080 microprocessor (μP) and is configured for 8K bytes of random access memory (RAM), 4K bytes of programmable read-only memory (PROM), 4 input ports, and 4 output ports. The comparison monitor compares the 8-bit data bus, 16-bit address bus, and 8 control lines from each Intellec 8 microcomputer and indicates that an error has occurred if a difference on any line is detected. One of the microcomputers is designated as the μC under test (μC UT) and the other microcomputer serves as a reference (REF μC) on which the comparison is made. A third microcomputer provides input data to the μC UT and REF μC, initiates interrupt requests, and is referred to as the I/O μC. The upset test hardware configuration is shown in figure 1.

The μC UT is perturbed by an analog transient signal. The analog electrical transient is a 1 MHz damped sinusoid of negative polarity, and was designed to model an electrical signal that could be induced by electromagnetic fields associated with lightning discharges. The waveshape of the transient signal is an approximation of a waveform recommended for lightning-induced effects testing (2). The analog transient is directly coupled through a normally open relay onto a single line within the μC UT and its amplitude, therefore, is restricted to the damage threshold of components within the test unit. Input of the transient signal occurs pseudo-randomly in that it is controlled using the output of a counter that is initialized with a pseudo-random number generator. Randomness is desired so that the transient signal input is not synchronized with processing activity of the test unit. This establishes a more realistic laboratory simulation of the random process that might take place in the actual lightning environment than inputting transient signals during a processing activity that is established a priori. Therefore, data recorded from upset tests in which transient signal inputs occurred randomly during program execution, rather than by an a priori determination, should provide the best solution to a Markov upset susceptibility model.

Two types of data are obtained during each upset test--error data and the error detection time. Bit patterns from the data bus, address bus, and control lines of the μC UT are acquired with a Tektronix 9103 Digital Analysis System (DAS), which is triggered when the analog transient is input to the μC UT. If the comparison monitor indicates that an error occurred, the acquired error data is

stored on magnetic tape. The DAS is then reset for another data acquisition. The error detection time is determined by counting the number of clock cycles that occur in the Intellec μC's from the input of the transient signal to the detection of an error. Since the Intellec μC's have a 2 MHz clock, the number of clock cycles is multiplied by 500 ns to obtain the error detection time. The error detection time is a function of the processing delay times within the system under test as well as the speed and efficiency of the comparison monitor, or error detector. Although there is very little literature on upset testing, work has recently been done on the development of monitors for upset detection (3).

UPSET TEST DESCRIPTION AND DATA SUMMARY

The program being executed on the μC UT and REF μC during upset tests was stored in PROM and a flow chart of this program and that of the I/OμC is shown in figure 2. The μC UT and REF μC set the stack pointer, initialize variables, output a preset constant to an I/O port, and input an 8-bit data word from the I/O μC. This 8-bit word is checked to see if it lies within a certain range. If the data word is not within the range, it is stored in memory and another 8-bit word is input to be checked. If the 8-bit word is in the range, it is divided by a constant and stored in memory. During these upset tests, the 8-bit data word was a constant within the desired range. The μC UT and REF μC then output another preset constant to an I/O port, retrieve from memory the 8-bit word resulting from the division, subtract a constant from it, and store this final value in memory. A loop in which no operations are performed is then executed until the I/O μC initiates an interrupt request which causes an RST 6 instruction (single-byte jump to memory location 0030) to be executed. The interrupt routine causes the final 8-bit value to be output to an I/O port. Once this is done, the μC UT and REF μC halt until the I/O μC initiates a second interrupt request which causes an RST 7 (single-byte jump to location 0038) to be executed. The second interrupt routine causes the μC UT and REF μC to reexecute the test program which, therefore, operates in a continuous loop. This test program was not written for efficiency or to perform some real application but to be representative of a typical application program and include instructions from all five 8080 instruction groups (table 1) that collectively require all ten 8080 machine cycles (table 2) and utilize all four memory addressing modes available in the 8080 (table 3).

The analog transient signal was input to the memory data input bus of the μC UT a total of 120 times--30 times each on the four least significant lines of the input data bus from memory (MDI0, MDI1, MDI2, MDI3). The memory data input bus is multiplexed onto the bidirectional data bus of the 8080 CPU (along with input data from the I/O ports and interrupt instructions from a peripheral device) and was chosen as the transient signal input site because transient signal inputs on this bus resulted in a large number of errors during the upset tests reported in (1). The specific lines within the bus as well as the number of transient signal injections per line were arbitrarily selected. Each of the 120 transient signal injections to the μC UT produced either upset or benign errors. Benign errors caused no divergence from correct flow between the main program and subroutines but included incorrect values read from or written into memory and repeated or erroneous states within an instruction cycle, and could be a potentially serious anomaly. For these tests, any divergence from correct program flow was classed as upset whether or not correct program execution was reestablished. Upsets recorded during testing occurred as a result of program execution returning from a subroutine to the wrong memory location, which in some cases was the second or third byte of a multibyte instruction. In some instances, program execution continued to the location at which the return should have occurred, and correct program flow resumed with or without benign errors for the duration of the data acquisition. In other cases, program execution went back and forth between two routines in an erroneous loop that was not exited within the time frame of the data acquisition. These findings are consistent with the upset characterization described in (4). The number of upsets and benign errors that occurred as a result of transient signal inputs at each of the four injection points is shown in table 4. Tables 5-7 show the number of upsets and benign errors that resulted from transient signal inputs during processing of the various instructions within each of the instruction groups, the various memory addressing modes, and the various 8080 machine cycles, respectively.

STATISTICAL ANALYSIS

A statistical analysis was performed to identify processing modes of the 8080 μP that contain some types of activity which may be more critical than other types to the overall susceptibility of the μC system to upset caused by analog transients. A hypothesis test for each processing mode was performed in which the hypothesis being tested was that upset and benign errors occur with equal probability regardless of the processing activity underway when the transient signal is input to the μC UT. This hypothesis is tested by arranging in tabular form the number of

observed upsets and benign errors resulting from transient inputs during each processing activity under consideration. A calculation of the expected value for each entry, assuming the hypothesis is true, is then performed, which enables the chi-square statistic of the sample population to be calculated. If the calculated chi-square statistic is less than the actual value of an appropropriate chi-square distribution, then the hypothesis is true. Otherwise, the hypothesis is not true and must be rejected.

Tables 8-10 show the observation tables, associated joint probabilities and conditional probabilities, and chi-square statistics for several instruction groups, addressing types, and machine cycles, respectively. Since, in each of these tables, the calculated chi-square statistic exceeds the value of the chi-square distribution, the hypothesis being tested in each of these cases must be rejected. This means that differences in the indicated probabilities are statistically significant rather than being due to chance. That is, it cannot be assumed that upset and benign error occurrences are equiprobable for transient signal inputs during execution of the various instruction type, addressing modes, or machine cycles. The data base accrued during these tests is insufficient to identify which instruction groups, addressing modes, and machine cycles are most critical to upset vulnerability. This is because of the diversity in the relative frequency with which activities in each processing mode occurred during execution of the test program. There were activities in each processing mode that occurred so infrequently that they were under way few or no times when the transient signal was input to the μC UT. Identification of critical activities in each mode could be accomplished by additional tests using one or more specially written programs in which the relative frequencies of occurrence are more uniform.

To test the hypothesis that upset and benign error occurrences are equiprobable for transient signals injected on each of the four least significant lines of the memory data input bus, the chi-square statistic shown in Table 11 was calculated. Since the calculated chi-square statistic is less than the value of the chi-square distribution, the hypothesis cannot be rejected. That is, upset and benign error occurrences are equally probable regardless of the line (among the four least significant bits of the input data bus from memory) on which the transient signal is injected.

The overall performance of the 8080-based microcomputer can be conveniently summarized in a Markov chain of discrete states as shown in figure 3. The state transition probabilities θ_{ij} are defined as

$$\theta_{ij} = P(i \rightarrow j \,|\, \text{state } i) = \frac{N_{ij}}{N_i} \qquad \langle 1 \rangle$$

where N_{ij} is the number of observed transitions from state i to state j and N_i is the number of times state i was observed. The quantities θ_{ij} represent the probability of transition along the indicated path and do not represent state probabilities or provide information regarding transition sequence.

STOCHASTIC MODELING

In order to obtain a probabilistic time history of the 8080-based system response to the analog transient, a stochastic Markov model could be constructed consisting of discrete states in continuous time. The states and transition paths would be the same as those shown in figure 3. However, the transition paths would be defined in terms of transition rates λ_{ij} rather than probabilities θ_{ij}. If constant transition rates were assumed, λ_{ij} would be the inverse of the mean transition time from state i to state j, which would have to be determined experimentally or using computer simulation (5). Transition time between states could be evaluated by counting the elapsed number of clock cycles and dividing by the clock frequency. Transition rates λ_{ij} could also be estimated with the θ_{ij} by solving the simultaneous equations:

$$\frac{\hat{\lambda}_{12}}{\hat{\lambda}_{12} + \hat{\lambda}_{13}} = \theta_{12} \qquad \langle 2 \rangle$$

$$\frac{\hat{\lambda}_{13}}{\hat{\lambda}_{12} + \hat{\lambda}_{13}} = \theta_{13} \qquad \langle 3 \rangle$$

$$\frac{\hat{\lambda}_{21}}{\hat{\lambda}_{21} + \hat{\lambda}_{13}} = \theta_{21} \qquad \langle 4 \rangle$$

$$\frac{\hat{\lambda}_{23}}{\hat{\lambda}_{21} + \hat{\lambda}_{23}} = \theta_{23} \qquad \langle 5 \rangle$$

$$\frac{\hat{\lambda}_{31}}{\hat{\lambda}_{31} + \hat{\lambda}_{32}} = \theta_{31} \qquad \langle 6 \rangle$$

$$\frac{\hat{\lambda}_{32}}{\hat{\lambda}_{31} + \hat{\lambda}_{32}} = \theta_{32} \qquad \langle 7 \rangle$$

Once all transition rates have been determined, a transition rate matrix Q would be formulated:

$$Q = [q_{ij}] = \begin{bmatrix} -(\lambda_{12} + \lambda_{13}) & \lambda_{12} & \lambda_{13} \\ \lambda_{21} & -(\lambda_{21} + \lambda_{23}) & \lambda_{23} \\ \lambda_{31} & \lambda_{32} & -(\lambda_{31} + \lambda_{32}) \end{bmatrix} \quad <8>$$

The transition rate matrix Q would then be used to determine the probability $P_{ij}(t)$ of occupying state j at time t given that the process was in state i. This probability is the solution to the following system of differential equations (6):

$$P'_{ij}(t) = \sum_k q_{ik} P_{kj}(t) \quad <9>$$

with initial conditions

$$P_{ij}(0) = \begin{cases} 1 \text{ if } i = j \\ 0 \text{ if } i \neq j \end{cases} \quad <10>$$

The time-varying state probabilities $P_{ij}(t)$ for the Markov model constructed as in figure 3 represent a characterization of the upset susceptibility of the 8080-based microcomputer. Since this system was not designed for upset tolerance, upset detection and recovery states cannot be added to the model for a reliability characterization. However, stochastic modeling could be used to characterize the susceptibility of the digital system to upset.

SUMMARY AND CONCLUSIONS

A laboratory experiment was conducted, using a general-purpose microcomputer, to investigate upset caused by analog electrical transients similar to those that could be induced by lightning. Data were obtained from 120 tests in which 85 upsets and 35 benign errors were detected. Error modes involving a divergence from correct program flow were classed as upset. Benign errors caused no divergence from correct flow between the main program and subroutines but included incorrect values read from or written into memory and repeated or erroneous states within an instruction cycle, and could be a potentially serious anomaly. A statistical analysis was performed in which it was determined that upset and benign error occurrences are not equiprobable for transient signal inputs during execution of the various instruction types, addressing modes, or machine cycles. Additional testing would have to be performed to identify which instruction groups, addressing modes, and machine cycles are most critical to upset vulnerability. This type of analysis could be used as an aid in identifying system weaknesses that could be hardened to upset but may be especially useful during the design phase of system development. A stochastic model, based on upset test data, was defined for the general-purpose microcomputer assuming constant transition rates. Solution of this model would provide time-varying state probabilities that represent an upset susceptibility characterization of the test system. Thus, the application of stochastic modeling for upset susceptibility prediction seems very promising. However, the optimum transition rate distribution must be determined.

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TABLE 1: 8080 INSTRUCTION GROUPS

GROUP	DESCRIPTION
DATA TRANSFER	MOVE DATA BETWEEN REGISTERS OR BETWEEN REGISTERS AND MEMORY
ARITHMETIC	ADD, SUBTRACT, INCREMENT, DECREMENT DATA IN REGISTERS OR MEMORY
LOGICAL	AND, OR, EXCLUSIVE-OR, COMPARE, ROTATE, COMPLEMENT DATA IN REGISTERS OR MEMORY
BRANCH	CONDITIONAL/UNCONDITIONAL JUMP, SUBROUTINE CALL, RETURN
STACK, I/O, AND MACHINE CONTROL	INPUT, OUTPUT, MAINTAINING STACK AND INTERNAL CONTROL FLAGS

TABLE 2: 8080 MACHINE CYCLES

MACHINE CYCLE	DESCRIPTION
INSTRUCTION FETCH	READ INSTRUCTION FROM MEMORY; INCREMENT PROGRAM COUNTER; DECODE INSTRUCTION
MEMORY READ	READ BYTE FROM MEMORY; INCREMENT PROGRAM COUNTER
MEMORY WRITE	WRITE BYTE TO MEMORY
STACK READ	READ BYTE FROM STACK; INCREMENT STACK POINTER
STACK WRITE	WRITE BYTE TO STACK; DECREMENT STACK POINTER
INPUT READ	READ BYTE FROM INPUT PORT
OUTPUT WRITE	WRITE BYTE TO OUTPUT PORT
INTERRUPT ACKNOWLEDGE	READ INSTRUCTION ON DATA BUS; DECODE INSTRUCTION
HALT ACKNOWLEDGE	CPU ENTERS HALT STATE
INTERRUPT ACKNOWLEDGE WHILE HALTED	READ INSTRUCTION ON DATA BUS; DECODE INSTRUCTION

TABLE 3: 8080 ADDRESSING MODES

MODE	DESCRIPTION
DIRECT	BYTES 2 AND 3 OF THE INSTRUCTION CONTAIN THE EXACT ADDRESS OF DATA
REGISTER	THE INSTRUCTION SPECIFIES THE REGISTER OR REGISTER-PAIR CONTAINING DATA
REGISTER INDIRECT	THE INSTRUCTION SPECIFIES THE REGISTER-PAIR CONTAINING ADDRESS OF DATA
IMMEDIATE	THE INSTRUCTION CONTAINS THE DATA ITSELF

TABLE 4: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER INJECTION POINT

INJECTION POINT	NO. OF INJECTIONS	NO. OF UPSETS	NO. OF BENIGN ERRORS
MDI0	30	22	8
MDI1	30	25	5
MDI2	30	21	9
MDI3	30	17	13
	120	85 (71%)	35 (29%)

TABLE 5: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER INSTRUCTION GROUP

INSTRUCTION GROUP	NO. OF UPSETS	NO. OF BENIGN ERRORS
DATA TRANSFER	7	3
ARITHMETIC	3	4
LOGICAL	0	2
BRANCH	52	14
STACK, I/O, AND MACHINE CONTROL	23	12

TABLE 6: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER ADDRESSING MODE

ADDRESSING MODE	NO. OF UPSETS	NO. OF BENIGN ERRORS
DIRECT	1	4
REGISTER	1	2
REGISTER INDIRECT	15	6
IMMEDIATE	47	12
NONE	21	11

TABLE 7: NUMBER OF UPSETS AND BENIGN ERRORS THAT OCCURRED PER MACHINE CYCLE TYPE

TYPE OF MACHINE CYCLE	NO. OF UPSETS	NO. OF BENIGN ERRORS
INSTRUCTION FETCH	27	10
MEMORY READ	36	8
MEMORY WRITE	4	1
STACK READ	2	1
STACK WRITE	5	2
INPUT READ	0	0
OUTPUT WRITE	1	0
INTERRUPT ACKNOWLEDGE	0	0
HALT ACKNOWLEDGE	10	9
INTERRUPT ACKNOWLEDGE WHILE HALTED	0	4

TABLE 8: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER INSTRUCTION GROUP

	C_1 BRANCH	C_2 STRK, I/O, MC	C_3 OTHERS	TOTAL
BENIGN ERRORS	14	12	9	35
UPSET	52	23	10	85
TOTAL	66	35	19	120

$P_{B,U}(C_1)$: PROBABILITY THAT A CATEGORY 1 INSTRUCTION IS BEING EXECUTED WHEN THE UPSET/BENIGN ERROR-CAUSING TRANSIENT SIGNAL IS INPUT

$P_B(C_1) = 0.117$ $P_B(C_2) = 0.100$ $P_B(C_3) = 0.0750$

$P_U(C_1) = 0.433$ $P_U(C_2) = 0.192$ $P_U(C_3) = 0.0833$

$P(B, U/C_1)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT A CATEGORY 1 INSTRUCTION IS BEING EXECUTED DURING TRANSIENT SIGNAL INPUT

$P(B/C_1) = 0.212$ $P(B/C_2) = 0.343$ $P(B/C_3) = 0.474$

$P(U/C_1) = 0.788$ $P(U/C_2) = 0.657$ $P(U/C_3) = 0.526$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 5.51$

(TABLE VALUE: $X^2_{\alpha = 0.10} = 4.61$)

TABLE 9: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER ADDRESSING MODE

	C_1 IMMEDIATE	C_2 NONE	C_3 OTHERS	TOTAL
BENIGN ERRORS	12	11	12	35
UPSET	47	21	17	85
TOTAL	59	32	29	120

$P_{B\ U}(C_i)$: PROBABILITY THAT THE CATEGORY i ADDRESSING MODE IS BEING EXECUTED WHEN THE UPSET/BENIGN ERROR-CAUSING TRANSIENT SIGNAL IS INPUT

$P_B(C_1) = 0.100$ $P_B(C_2) = 0.0917$ $P_B(C_3) = 0.100$

$P_U(C_1) = 0.392$ $P_U(C_2) = 0.175$ $P_U(C_3) = 0.142$

$P(B, U/C_1)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT THE CATEGORY i ADDRESSING MODE IS BEING EXECUTED DURING TRANSIENT SIGNAL INPUT

$P(B/C_1) = 0.203$ $P(B/C_2) = 0.344$ $P(B/C_3) = 0.414$

$P(U/C_1) = 0.797$ $P(U/C_2) = 0.656$ $P(U/C_3) = 0.586$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 4.72$

(TABLE VALUE: $X^2_{\alpha = 0.10} = 4.61$)

TABLE 10: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER MACHINE CYCLE TYPE

	C_1 INST. F	C_2 MEM. R.	C_3 OTHERS	TOTAL
BENIGN ERRORS	10	8	17	35
UPSET	27	36	22	85
TOTAL	37	44	39	120

$P_{B,U}(C_i)$: PROBABILITY THAT THE CATEGORY i MACHINE CYCLE IS BEING EXECUTED WHEN THE UPSET/BENIGN ERROR-CAUSING TRANSIENT SIGNAL IS INPUT

$P_B(C_1) = 0.0833$ $P_B(C_2) = 0.0667$ $P_B(C_3) = 0.142$

$P_U(C_1) = 0.225$ $P_U(C_2) = 0.300$ $P_U(C_3) = 0.183$

$P(B, U/C_1)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT THE CATEGORY i MACHINE CYCLE IS BEING EXECUTED DURING TRANSIENT SIGNAL INPUT

$P(B/C_1) = 0.270$ $P(B/C_2) = 0.182$ $P(B/C_3) = 0.436$

$P(U/C_1) = 0.730$ $P(U/C_2) = 0.818$ $P(U/C_3) = 0.564$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 6.51$

(TABLE VALUE: $X^2_{\alpha = 0.05} = 5.99$)

TABLE 11: STATISTICS FOR UPSET AND BENIGN ERROR OCCURRENCE PER TRANSIENT SIGNAL INPUT POINT

	C_1 MDI0	C_2 MDI1	C_3 MDI2	C_4 MDI3	TOTAL
BENIGN ERRORS	8	5	9	13	35
UPSETS	22	25	21	17	85
TOTAL	30	30	30	30	120

$P_{B,U}(C_i)$: PROBABILITY OF UPSET/BENIGN ERROR OCCURRENCE GIVEN THAT THE INPUT POINT OF TRANSIENT SIGNAL BELONGS TO CATEGORY i

$P_B(C_1) = 0.267$ $P_B(C_2) = 0.167$ $P_B(C_3) = 0.300$ $P(B/C_4) = 0.433$

$P_U(C_1) = 0.733$ $P_U(C_2) = 0.833$ $P_U(C_3) = 0.700$ $P(U/C_4) = 0.567$

CALCULATED CHI-SQUARE STATISTIC: $X^2 = 5.28$

(TABLE VALUE: $X^2_{\alpha=0.10} = 6.25$)

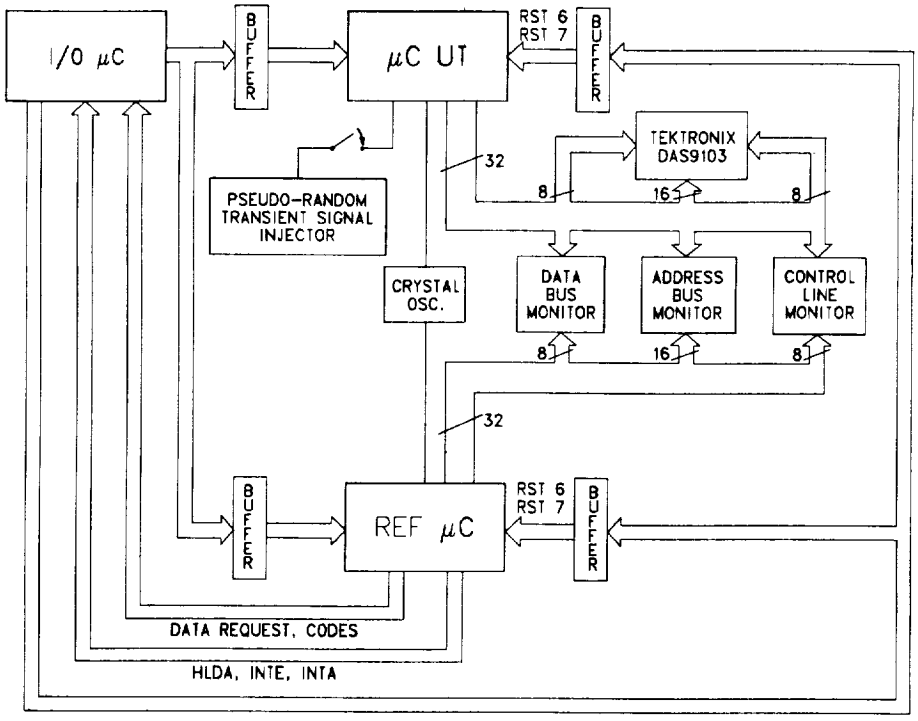


Figure 1. Upset test hardware configuration.

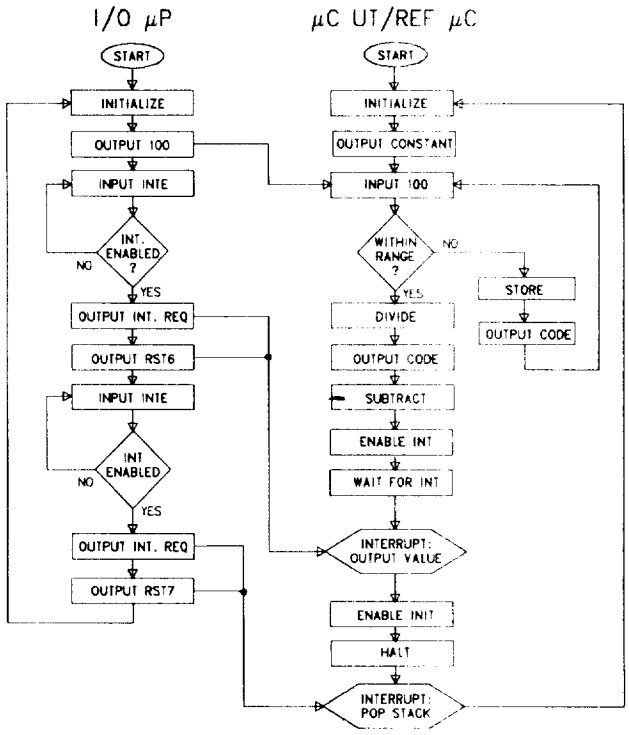
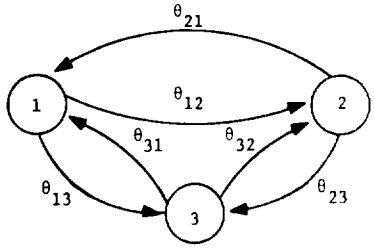


Figure 2. Flow chart of upset test μC programs.



STATE 1: SYSTEM IS FAULTED BY TRANSIENT SIGNALS

STATE 2: UPSET HAS OCCURRED

STATE 3: BENIGN ERRORS HAVE OCCURRED

$\theta_{12} = 0.017$ $\theta_{21} = 0.024$ $\theta_{31} = 0.153$

$\theta_{13} = 0.983$ $\theta_{23} = 0.224$ $\theta_{32} = 0.606$

Figure 3. State model for Intellec 8/Mod 80 system response to analog transient signal.

LIGHTNING RESEARCH--A USER'S LAMENT

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ABSTRACT

As a user of devices and procedures for lightning protection, the author is asking the lightning research community for cookbook recipes to help him solve his problems. He is lamenting that realistic devices are scarce and that his mission does not allow him the time nor the wherewithal to bridge the gap between research and applications. A few case histories are presented.

In return for their help he is offering researchers a key to lightning technology--the use of the Eastern Test Range and its extensive resources as a proving ground for their experiment in the lightning capital of the United States. A current example is given--a joint lightning characterization project to take place there. Typical resources are listed.

INTRODUCTION

The part of this presentation that's reflected in the title highlights the problem we have in the operations arena in adapting findings of lightning research to practical applications. What we need are cookbook recipes.

In the other part of the presentation we offer one key to further discoveries in lightning technology and that is the use of an instrumented proving ground located in the lightning capital of the United States.

THE PROVING GROUND

Invoking author's license I am going to reverse the sequence and tell you about our test facilities first. This way if I succeed in interesting you in using them, you may also decide to get involved in helping out the poor operator with his hardware problems. First of all, as I said a little earlier our proving ground is located in the lightning capital of the United States--well, maybe not the capital but certainly the suburbs. The lightning capital itself is right here in central Florida. Some of the thunderstorms have a tendency to evaporate as they reach the Atlantic Coast but we still get our share of them. The proving ground itself is a combination of two areas: the first one is the Eastern Test Range managed by the US Air Force and extending from Cape Canaveral, about 60 miles east of here, to the Indian Ocean, about 10,000 miles to the southeast. For our purpose here we are talking mainly of Cape Canaveral proper and its restricted airspace allowing 3-dimensional operations with only token coordination with other airspace users. For those of you who are not entirely familiar with our operations all space and missile launches, whether Air Force, NASA, Army, Navy or others, take place from Cape Canaveral with the exception of the Space Shuttle. The Space Shuttle is launched from the other area referred to earlier and that is the NASA Kennedy Space Center on Merritt Island, just west of Cape Canaveral between the Banana and Indian Rivers. Both areas are shown in Fig. 1. It is also intended to have the Shuttle orbiter return to and land at KSC, at least on some of the missions. This has happened once so far, but future landings depend heavily on major improvements in Air Force weather "nowcasting" currently being implemented at a cost of several million dollars jointly funded by NASA and the Air Force.

Even as I write, a lightning characterization project is getting under way there under the direction of the US Air Force Wright Aeronautical Laboratory in cooperation with the Federal Aviation Administration (FAA), the Naval Research Laboratory (NRL), NASA (Kennedy Space Center and Langley Research Center), the French Office National d'Etudes et de Recherches Aérospatiales (ONERA), the Centre d'Etudes Nucleaires de Grenoble (CENG), and other interests. They are bringing with them an instrumented lightning research aircraft and special ground instrumentation. This project is a good example of what we can do for other researchers. The local support is provided jointly by NASA at KSC and by the Air Force at Cape Canaveral and nearby Patrick Air Force Base (PAFB). NASA will be providing a launch site for lightning-triggering rockets supplied by CENG and some data support services. The Air Force will be providing meteorological services which are in the process of being modernized to the extent that next year they will be the most advanced services available anywhere. The Air Force is acquiring a

McIDAS-lineage forecasting system and already has a state-of-the art weather radar, meteorological sounding system, field mill network, lightning location and protection system, and mesoscale network.

The weather radar is a special version of a National Weather Service radar; this version can detect very light precipitation of the order of 0.01 in^3/hr. Next year it will incorporate a volumetric capability for providing displays along any cross section desired. Also next year we will have our own GOES East and West Earth stations instead of depending on a tap. Other Air Force support includes air traffic controllers, precision radar and optical tracking, aircraft vectoring data with respect to thunderstorm cells and other weather features, air and ground voice communication as well as more mundane functions ranging from aircraft fueling and ground support to portapotties for visiting scientists at remote sites. We also provide feeding facilities as well as snake bite and other health care. Last but not least nature unlimited will be unleashing lightning, turbulence, downdrafts, and other violent manifestations but refuses to coordinate them with Cape scheduling so that we'll have to play this part by ear.

So, you ask, how much do you have to pay for this support if you want to conduct lightning research, either natural or triggered, either cloud to ground, or intercloud? Some of it is for free, such as available work space and "routine" meterological services which here go well beyond the usual connotation of "routine." You will also benefit from the multi-million dollar improvements we are making in our "nowcasting" techniques, as mentioned earlier. Some of the support you may need has to be paid for such as site preparation, radar operator time outside of normal shift time, aircraft fuel, and so on. By site preparation, I mean making available access roads, electric power, communications and such at remote sites not now available for your particular requirements. As an example, the on-going lightning characterization project mentioned earlier called for a seashore site where a ground plane could be set up on the beach and a parking site provided nearby for an instrumented research trailer to study electromagnetic propagation over the ocean. No such site existed so that we had to provide stabilizing material for a roadway over the loose sand as well as extension of existing utilities to the selected site. The costs involved are what we call "reimbursable." However, there may be ways of offsetting some of these costs. As mentioned in the opening of this paper and expanded on in the second half of this presentation, we have a lightning protection project for which we need specific application data that we are willing to pay for if not available otherwise; we may be able to enter into agreements with various organizations doing lightning research at the Cape to provide this type of data for a consideration which may be used to subsidize a portion of such research projects. In such cases the resulting net cost to the user of Eastern Test Range facilities is nominal and the benefits are outstanding. And as you can see for yourselves such extensive support facilities are hard to duplicate elsewhere. I can provide additional information on how to apply for the use of our facilities at the end of this presentation.

FROM LIGHTNING RESEARCH TO LIGHTNING PROTECTION

And now for the kind of lightning protection data we need at the Eastern Test Range (ETR) and Kennedy Space Center. We are in need of such data especially at the ETR which is strictly operational and not geared for research, hence my lament and our need for cookbook recipes.

Our main concern is the protection of sensitive electronics and various facilities from the diverse effects of lightning, ranging from direct strikes to electromagnetic pulse (EMP) effects and including surges in power lines and damage to payloads. I'll give some examples of problems we've had and the solutions we've developed for some of them.

Some of the more fundamental problems have already been treated by some of my fellow workers such as Jim Stahmann of the PRC Systems Services Co., at KSC, Martin Uman of the University of Florida, Phil Krider of the University of Arizona and Mike Maier of Lightning Location and Protection, Inc. Some of my friends at the Wright Aeronautical Laboratory, Dick Richmond and Major Pete Rustan in particular, have determined different lightning signatures depending on geographical location and are investigating other possible differences as a function of the generating mechanism. My French colleagues at ONERA, CNEG, and other organizations have pointed out the high-frequency characteristics of lightning signals and the potential of interferometric methods for lightning locations as close to home as Valkaria, Florida, some 30 miles south of Cape Canaveral.

It may even be that the cookbook recipes we are looking for are already in existence but so far they have eluded us. Now I am not talking about "standard" protection such as listed in NFPA 78[1]. Some of it works, and some of it doesn't. What we need are products of the latest findings in lightning characteristics. Particularly lacking is operationally feasible protection against EMP inductive effects.

Some of the things we have done include conventional air terminals and cones of protection, power surge protection, open-phase detectors, transient protection on data lines, grounding of antenna towers with a quarter-wave stub, and so on. A fairly standard procedure is to use a 2/0 instrumentation ground bus. Depending on the location, it may or may not be connected to the power neutral, the power grounding conductor and the building frame. During a cursory survey made a couple of years ago the following and more were found: A current of 0.4 ampere was measured in the ground bus. The shields on communication lines between two sites had been tied back and taped at both ends (probably in a desperate attempt to reduce ground loops). Some grounding cables shown on construction drawings could not be found. A DC return line was jumpered to the AC neutral. Grounding clamps were loose or corroded. Power surge suppressors took three cycles to react.

CONCLUSION

Lightning researchers of the world, have a heart for us practitioners--give us cookbook recipes such as "in case of lightning type X , use device Y to protect component Z ." Tell us about fiber optics for transmitting signals or pneumatic lines for actuating devices neither of which are affected by lightning or its inductive effects. But be specific, give us tried and ready-to-use solutions. We cannot afford to go around testing "off-the-shelf" devices only to find that they don't work. As you well know in the lightning business you usually have only one shot at success--if you mess up, it may well be "curtains" for your project and quite possibly for you too.

REFERENCE

1. "Lightening Protection Code," National Fire Protection Association, vol. 78, 1980.

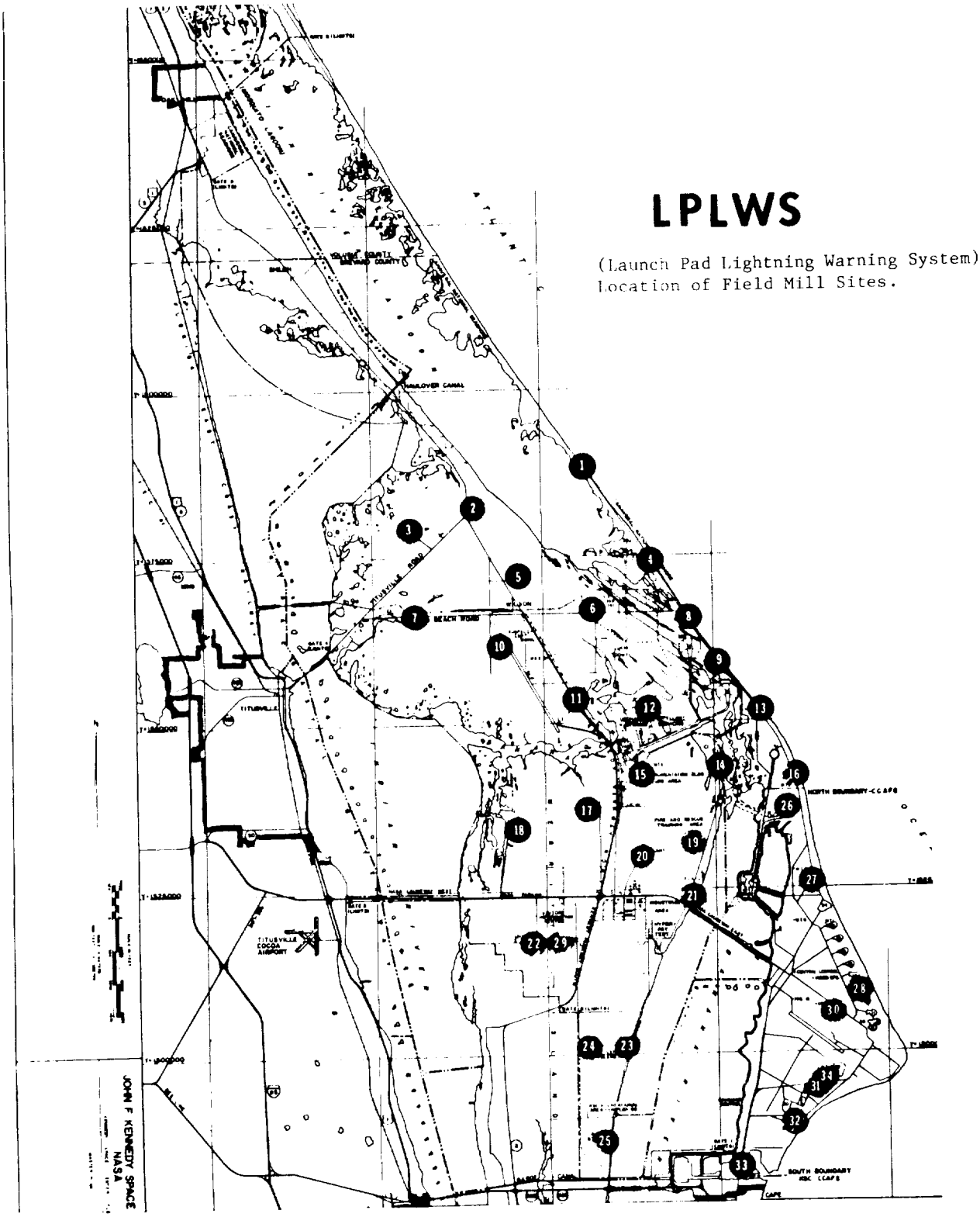

Figure 1. Cape Canaveral Air Force Station and NASA Kennedy Space Center.

AC Power Line Protection For An IEEE 587 Class B Environment

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Abstract

The 587B series of protectors are unique low clamping voltage transient suppressors to protect ac-powered equipment from the 6000V peak open-circuit voltage and 3000A short circuit current as defined in IEEE Standard 587 for Category B transients. The devices, which incorporate multiple-stage solid-state protector components, have been specifically designed to operate under multiple exposures to maximum threat levels in this severe environment. The output voltage peaks are limited to 350V under maximum threat conditions for a 120V ac power line, thus providing adequate protection to vulnerable electronic equipment. The principle of operation and test performance data is discussed.

Introduction

As electronic systems become more sophisticated and make use of the newer higher density integrated circuits, their transient vulnerability increases. Equipment manufacturers are becoming increasingly aware that equipment must be designed to survive in a transient environment. Transient problems should not be left for the user to solve, but unfortunately, this has often been the case. The user is ill equipped for the task because he usually does not know system limitations or have the necessary test equipment to personally evaluate the plethora of protective devices available.

The IEEE 587-1980 Standard is a reasonable worst case definition of the transient environment[1]. By preceding equipment with a suppression network which reduces such transients to a specified maximum level, designers can insure that equipment malfunction or damage will rarely occur.

Topics to be discussed include the IEEE 587 Standard, suppressor design approaches, and test results of a suppressor module designed to protect equipment from the IEEE 587 transient environment.

The Transient Environment As Defined By The IEEE Standard 587

Several years of work by many people on IEEE committees have culminated in the publication of Standard 587-1980 which defines transient conditions occurring in low voltage (less than 600 volts) ac power circuits. It addresses transient voltages which exceed twice the peak operating voltage with durations ranging from a fraction of a microsecond to a millisecond, and originating primarily from system switching and lightning effects. The standard also proposes tests which approximate the real-world transient conditions for the purpose of evaluating the survival capability of equipment connected to power circuits.

Three location categories are defined: "A" and "B" for indoor applications, and "C" for outdoor applications. The location categories are further defined in Figure 1. They take into consideration the increase in source impedance from the outside to locations well within the building. Table 1 summarizes the test waveforms used for categories A and B, which are primarily for indoor residential, commercial and light industry applications. The waveforms are detailed in Figure 2.

Location Categories

A. Outlets and Long Branch Circuits

All outlets at more than 10 m (30 ft) from Category B with wires #14—10

All outlets at more than 20 m (60 ft) from Category C with wires #14—10

B. Major Feeders and Short Branch Circuits

Distribution panel devices

Bus and feeder systems in industrial plants

Heavy appliance outlets with "short" connections to the service entrance

Lightning systems in commercial buildings

C. Outside and Service Entrance

Service drop from pole to building entrance

Run between meter and distribution panel

Overhead line to detached buildings

Underground lines to well pumps

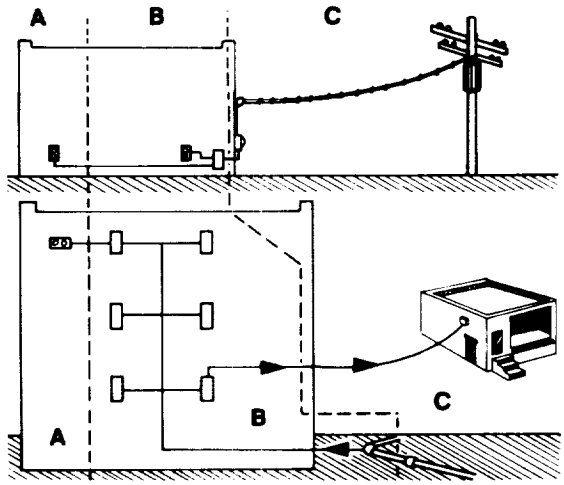

FIGURE 1
IEEE Std. 587-1980, Location Categories

LOCATION CATEGORY	WAVEFORM	OPEN CIRCUIT VOLTAGE	SHORT CIRCUIT CURRENT
A	0.5μs-100kHz Ring (Fig. 2A)	6000V	200A
B	0.5μs-100kHz Ring (Fig. 2A)	6000V	500A
	1.2 x 50μs Impulse (Fig. 2B)	6000V	---
	8 x 20μs Impulse (Fig. 2C)	---	3000A

TABLE 1 — Waveform Characteristics

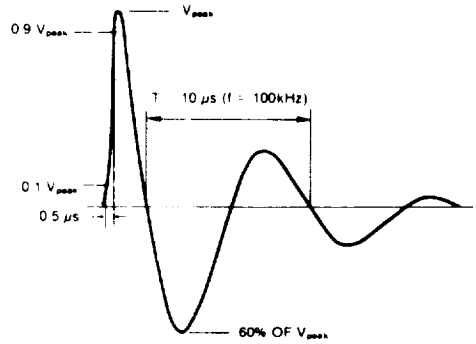

FIGURE 2A
0.5 μs — 100kHz Ring Wave

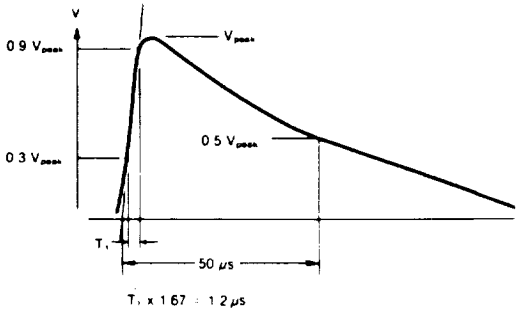

FIGURE 2B

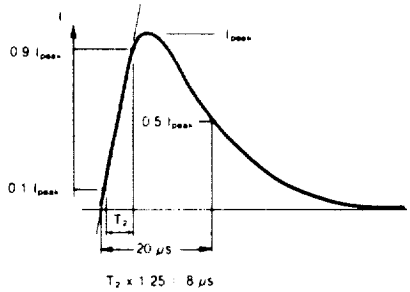

FIGURE 2C

Another area worth summarizing from Standard 587-1980 is the rate of transient voltage occurrence. Transient occurrence varies over wide limits depending upon the power system, its loading and the amount of lightning activity.

Data collected from many sources have led to the plot shown in Figure 3. This prediction shows with certainty only a relative frequency of occurrence, while the absolute number of occurrences can be described only in terms of low, medium, or high exposure. These exposure levels are defined in general terms as follows:

(1) Low Exposure. Systems in geographical areas known for low lightning activity, with little load switching activity.

(2) Medium Exposure. Systems in geographical areas known for high lightning activity or frequent and severe switching transients.

(3) High Exposure. Rare but real systems powered by long overhead lines and subject to reflections at line ends, where the characteristics of the installation produce high sparkover levels of the clearances.

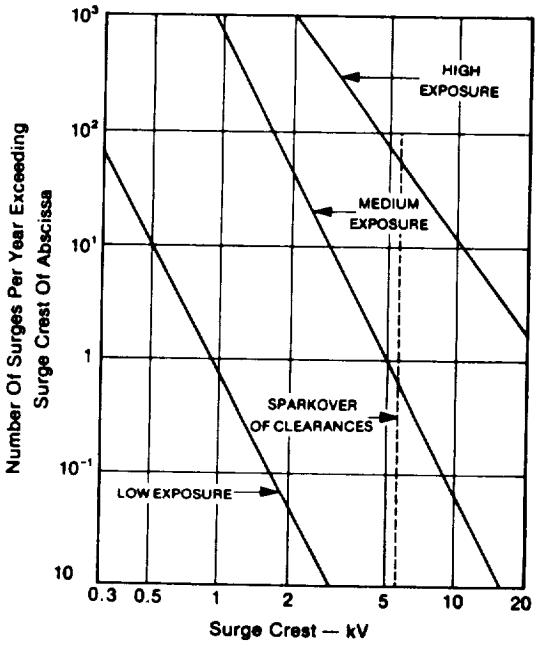

FIGURE 3
Rate Of Surge Occurrences At Unprotected Locations

A suppressor for use in most indoor location categories is adequately designed if it both protects and survives the occurrences shown on the medium exposure line. For example, it should survive a 6kV transient eight times, a 2kV transient 400 times, etc. for a 10-year life expectancy.

It should be emphasized that IEEE 587-1980 is not a test specification. It simply defines the open circuit voltages and short-circuit currents which are most applicable to certain location categories. Transient voltage suppressors tested to the IEEE standard can be easily compared in terms of output voltage under identical input conditions. Besides specifying an output level, it is helpful to have output waveforms available. The fast rising portion of the ring wave (dv/dt = 12kV/μs) is prone to excite self-resonance in L-C networks which may produce spurious output signals.

Other Line Transient Conditions

Fast rising transient wavefronts have also been observed on ac lines caused by switching transients generated close to the point of observation. As the distance between the points of origin and observation increases, line inductance and capacitance causes the wavefront risetime to decrease.

The possibility of a nuclear electromagnetic pulse (NEMP) on the power line should also be considered, particularly if essential military equipment is to be protected. Hard data describing the pulse are scant, but it is believed that, since its point of entry to the power lines is widespread, a fast rising pulse would appear in the power system. The pulse is usually described as having a rise in the kv/ns range and a decay of a few microseconds depending upon the altitude of the burst[2]. The spectrum extends roughly from 10KHz to 100MHz which easily excites the resonant frequencies of a system.

Development Of Suppressor Specifications

Based upon the preceding discussion of the transient environment on ac power lines, an intelligent spec can be composed. A decision must first be made whether the equipment location is best described by category A or B of IEEE 587-1980. Second, the maximum clamping voltage output must be selected. Since 400 volts is a standard voltage rating for economical semiconductors and capacitors, it is desirable to have the output level of the suppressor comfortably below 400 volts. For a Category B location suppressor, Table 2 shows a suitable set of transient specifications.

PROTECTION MODE	MAXIMUM CLAMPING VOLTAGE	OPEN CIRCUIT VOLTAGE	WAVEFORM	SHORT-CIRCUIT CURRENT	WAVEFORM
Differential (Line to Neutral)	350V	6kV	1.2 x 50μs	3000A	8 x 20μs
Common (Neutral to Ground)	500V	6kV	2 x 250ns	200A	2 x 250ns

TABLE 2—Transient Voltage Suppressor Specifications

The NEMP test (2x250ns) is based more on test capabilities rather than on an accurate representation of reality. The intent of the test is to insure that no overshoot occurs at the output, regardless of the rate of rise of the transient waveform.

Design Approaches

A general topology for transient protectors is shown in Figure 4 using the notations of Jacobus[3]. The diverter devices handle high currents but do not offer a precise control of voltage; gas tubes and MOV's are typical diverting elements. The clamp devices have low impedance and therefore offer

better voltage control but have lower current capabilities A TransZorb® Voltage Suppressor diode is a typical clamping device. The series impedances shown semi-isolate the various diverter and clamp stages by causing a voltage drop between them.

To meet the requirements of IEEE 587-1980, Category B, the topology of Figure 4 has proven to be quite cost effective. The series impedances are inductors. Depending upon the intended application, L sections could be added to or removed from the topology of Figure 4.

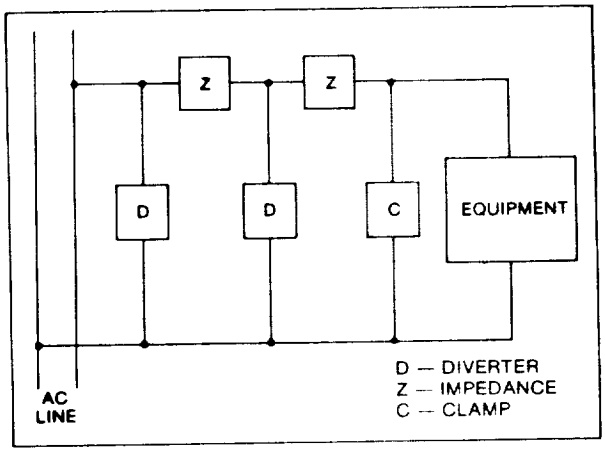

FIGURE 4
General Topology For A Protection Network

Capacitors can be added across the diverting and clamping elements to slow the rate of rise of fast pulses. Properly designed, the network of Figure 4 will provide rather precise voltage limiting, as well as slowing the rate of rise of fast switching transients of NEMP. Methods of sizing the diverter, clamp, and inductive elements are discussed in the Jacobus paper. However, experience has taught that a practical design requires a good deal of attention to component selection and extensive testing.

Specifically, Jacobus suggests using the reactance of the series inductors at 100KHz to calculate network currents and voltages. For the 0.5μs/100KHz ring wave, using 100KHz reactance makes some sense; however, the highest stress is caused by the unidirectional impulse waves which have a much lower frequency content. Furthermore, the clipping action of the diverters creates a somewhat flat-topped wave with a width of about 50μs. In addition, the coils, and shunt capacitors if used for high-frequency filtering, serve to stretch the pulse. Accordingly, a frequency of about 10KHz is more realistic to use for rough calculations; however, testing often indicates that inductors need to be much larger than calculated.

Shunt capacitors across the second diverter and the clamp element perform a valuable service in slowing the fast rise of incoming disturbances. The equivalent circuit of such a filter network is shown in Figure 5. The parasitic stray capacitances of the inductors, C_{S1} and C_{S2}, allow very fast pulse edges to shoot through the filter but they are attenuated by the shunt capacitances and clamped by the element C. A fast responding device, such as a TransZorb

TransZorb® is a registered trademark of General Semiconductor Industries Inc

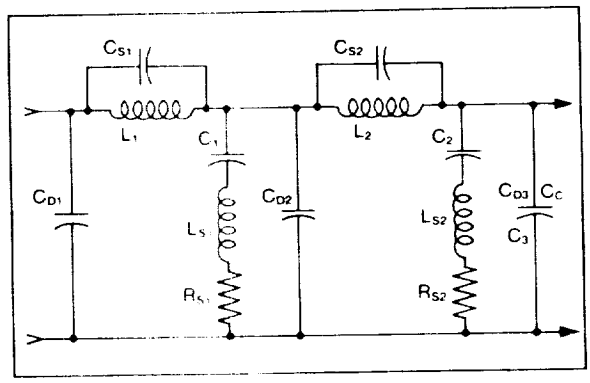

FIGURE 5

Suppressor, is threrefore preferable for element C. The capacitances of the diverter, C_D, and the clamp, C_C, usually provide a lower impedance shunt at very high frequencies than the discrete capacitors C_1 and C_2, which have more pronounced series parasitic inductance.

Note that the LC networks form series resonant circuits. To avoid large circulating current, their resonant frequencies should be well removed from the 100KHz frequency typical of a lightning surge. Empirically, it was determined that having the resonant frequency of L_1 and C_1 considerably above 100KHz and that L_2 and C_2 well below 100KHz provided the cleanest output.

Test Results Of The 587B Series Of Protective Modules

The General Semiconductor Industries' 587B family of ac power line protectors are designed to meet the specification of Table 1. Figure 6 shows the response to the unidirectional wave with open circuit voltage of 6000 volts and short circuit current of 3000 amperes. The top trace shows the voltage across a 12-ohm resistor which represents a 10A equipment load. The lower trace shows the dramatic reduction of the transient peak provided by the protector. Note

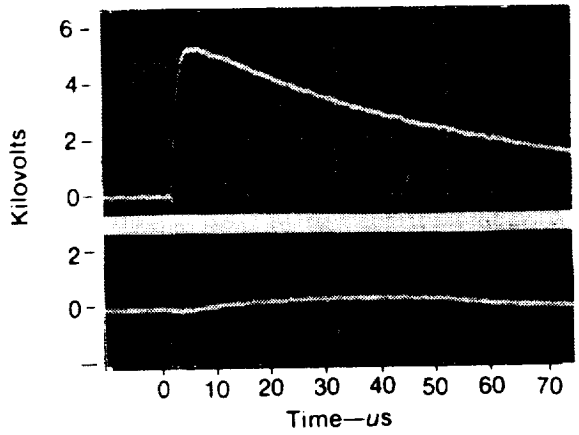

FIGURE 6—Transient Reduction At Equipment Input Provided By Suppressor
Upper Trace: No Protection Lower Trace: Protector Output

the relatively slow rate of rise of the output pulse (25V/μs) and the peak level of 300 volts on the detailed photo of the output shown in Figure 7.

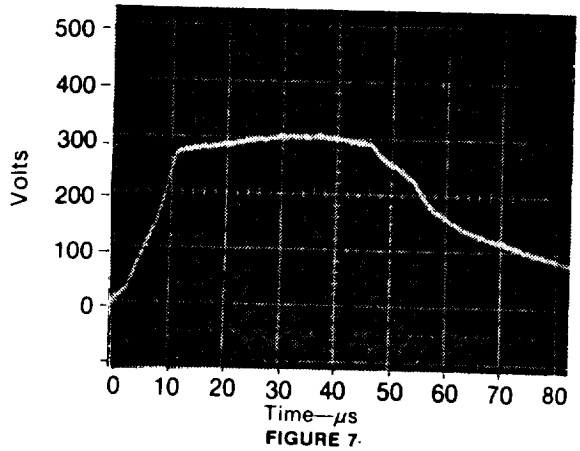

FIGURE 7.
Magnified View Of Protector Output

The output level with a ring wave input is shown in Figure 8. The protector used is rated for 20 amperes ac current; the load simulates a 2-amp resistive load. The output noise is felt to be acceptable for most applications. The noise increases as the load current is reduced below 5A. Should the noise prove objectionable when the ac load is light, a high-frequency load consisting of a 0.5μf capacitor in series with a 62-ohm resistor may be placed across the output.

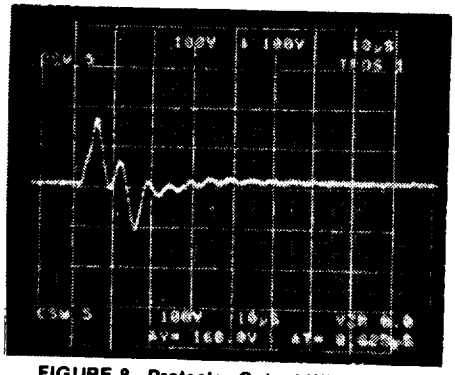

FIGURE 8—Protector Output With Ring Wave Input (6kV, 500A)

Figure 9 shows the output when a simulated NEMP is applied. The extremely fast rise (3kv/ns) generates a small amount of high-frequency noise, which is normally not objectionable.

Applications And Installation

The 587B series of modules can handle the worst expected transients in an indoor environment. The modules are especially valuable when used in data processing and complex communications and instrumentation equipment.

Whenever a high-voltage transient is present on the ac line, a large transient current will flow line to neutral and/or neutral to ground. It is important that the ac input to the module and the ground are distant from other wiring to prevent electromagnetic

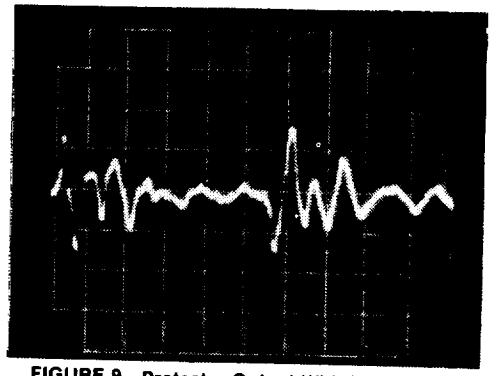

FIGURE 9—Protector Output With EMP Input (6kV, 120A) 20V/Div.; 50us/Div.

coupling. Should the transient current flow out the ground (green) lead, the impedance of the ground circuit causes conductive parts of the equipment cabinet or enclosure to rise—possibly several kilovolts—above the building earth ground. A potentially hazardous situation for personnel and equipment referenced to a different ground connection exists.

To reduce the undesirable potential difference between equipment, a practice called bonding is used. Bonding consists of connecting all conductive items together that are expected to conduct currents to earth. The bonding conductor must be sized properly for the high surge currents expected and must be solidly connected to each piece of equipment using the shortest possible path. All equipment is cross connected together to provide the lowest resistance that is practically achievable. Further information on grounding and bonding—vital to the equipment installer—is given in reference 3 and its references.

Summary

By placing a transient protection module between the ac power line and electronic equipment, failures caused by power line transients can be virtually eliminated, if the module handles the IEEE 587 environment under repeated surges, limits its output voltage to a safe defined maximum, and is installed properly.

Test results of a module fulfilling these requirements have been discribed. Peak output voltage has been shown to be under 350 volts regardless of the input waveform, provided that the stress levels of IEEE 587 are not exceeded. Also, it has been noted that proper grounding and bonding of equipment are essential for the protection of equipment and personnel.

References

(1) "IEEE Guide for Surge Voltages in Low-Voltage AC Power Circuits", IEEE Standard 587-1980, Institute of Electrical and Electronic Engineers, 345 E. 47th St., New York, NY 10017.

(2) L. W. Pinkston, "Electromagnetic Pulse (EMP)", 1984 Interference Technology Engineers' Master, E and B Enterprises, PA, 1984.

(3) N. M. Jacobus, "Designing Power Line Transient Protection Circuits", Proceedings of Powercon 11, Power Concepts, Inc., D-4 pp. 1-11, April 1984.

CORROSION PROPERTIES OF SECOND-GENERATION CONDUCTIVE MATERIALS

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Since the introduction of silver-filled epoxy adhesives and silver-filled nitrocellulose lacquer as RFI control materials in the 60's a number of new materials have been introduced. The resin carriers have been changed in an effort to make the materials more usable or more EPA acceptable and the fillers have been varied in an effort to make the materials less costly.

This work was done to assess the corrosion-related properties of these second-generation materials.

THE CONDUCTIVE ADHESIVES

The adhesives available are either epoxy or silicone with a wide variety of formulations (one and two part, heat activated, flexible, etc.). The fillers are no longer exclusively silver. Copper, nickel and carbon have been added to the list. Table I summarizes the conductive adhesives tested in this study.

These tests were made using the adhesives in typical lap-bond specimens as shown in Figure 1. These were used because both corrosion and adhesive strength data could be obtained on the same specimen. Three sets of five specimens were made up for each adhesive to be evaluated. The substrate material used was bare 2024-T4 Aluminum which had been thoroughly chemically cleaned in a chromic acid-sulfuric acid solution within four hours of the application of the adhesive. Each adhesive was mixed, catalized, thinned and cured according to the manufacturers' instructions.

After curing, the DC resistance was measured across the half-inch overlap using a Keithly 502 meter. The sets were then separated for environmental exposure. One set (5 Specimen) was subjected to 10 days of 5% salt fog according to ASTM B 117[1]; a second set was placed for 10 days in a condensing humidity cabinet at 105°F and the third set was stored under the controlled environmental conditions of 40% RH at 60 $\pm$ 5 °F.

Following these exposures, the DC resistance across the joints was remeasured and all of the specimens were pulled to obtain the lap-bond shear strength of each adhesive.

In addition to using the resistance and lap-bond shear degradation as a measure of the corrosion, the corrosion was evaluated visually at the interface between the adhesive and substrate and inside the opened joint.

CONDUCTIVE ADHESIVE DISCUSSION

The silver-filled epoxy systems in general show increase in resistance value after both salt and high humidity environments. The materials in 1 and 2 (Table I) were the older systems and were used here to act as comparisons for the newer systems. In No. 3 the high resistance and lack of corrosion products are probably a result of the polyamide reaction with the aluminum before curing; even though this change affected DC resistance it did not affect lap-bond shear strength and while the values are higher for the salt spray samples in this set, it was felt to be a characteristic of the set rather than the environment. This is implied by the data spread.

Control data	- high 1480	low 1360
Salt Spray	- high 1490	low 1430
Humidity	- high 1090	low 1040

The edge effect was typical of a silver/aluminum interface; there is a minor attack at this interface just as in samples 1 and 2. The silicone materials (Nos. 5, 6, 7), regardless of filler tend to maintain a uniform resistance. This appears to be a result of the silicone materials not allowing the environment to reach the aluminum. The galvanic corrosion at an interface also appears to be minimum and typical.

Using a copper filler as in sample No. 8 is much like using silver except the corrosion products are blue-green. The nickel-filled materials (Nos. 6, 9, and 10) maintained the

DC resistance quite well and there was little evidence of corrosion in the faying surface; however, at the aluminum interface in all cases there was pitting corrosion. This is probably because the nickel powder is not completely wetted and encapsulated as are the silver particles. Carbon, the one sample tested here, apparently did not contribute to corrosion.

The glass beads in the flexible adhesive (No. 4) apparently kept the overlap joint open so the environment could penetrate the entire half-inch area, as indicated by the dark adhesive through the joint.

The single part, heat-activated epoxy (No. 11) showed the same trend as the chemically cured materials.

CONDUCTIVE COATINGS

A number of conductive coatings were tested in the same environments, i.e., 10 days of 5% salt spray and 10 days of condensing humidity.

These tests were conducted on 6" x 6" acrylic panels which had been sprayed or brushed with two coats of the test material and on 1" x 4" aluminum panels where the coating was either brush or dip applied.

The DC resistance of the acrylic panel(s) was measured before and after exposure to the environments. The data are shown in Table II.

The aluminum, which was 2024-T4 alloy with only chemical cleaning, was used just to evaluate corrosion, since these coatings would not normally be used on aluminum but very often must be in contact with it. Both the salt spray test and the humidity test were used. The pictorial results are shown in figure 2.

The results presented in Table II are not surprising. The original values are reasonably close to manufacturers' advertised values. Humidity does not appreciably affect this value while the salt fog causes some deterioration of the coatings. This deterioration is as much within the resin as within the fillers. The corrosion of the aluminum does show galvanic effects which are accelerated by the nickel fillers but the 2024 alloy by itself is corroded severely in this environment.

CAULKING COMPOUNDS AND GREASES

Caulks and greases shown in figure 2 are: (a) caulks (Nos. 9, 10, 11, and 14) and (b) greases (Nos. 15, 16, and 17). Number 18 is a caulk that acts as a grease.

No resistance values were taken on these except to check the bulk resistance of the "as received" materials. This value is shown with the material description in Table III.

These materials (also) did not protect the 2024 Aluminum sample but on samples 10 and 11 the corrosion product is misleading since the salt could not be removed from the soft material. On sample 14 the corrosion was a green color and a copper color. This is a result of the copper particle which was coated with silver. Another observation not readily observable from these photographs is that the nickel coatings were very prone to pitting. This again is because the nickel does not become completely encapsulated by the resins.

CONCLUSIONS

This has been a very limited study in that 2024 Aluminum has been used as the only substrate material. It is also a very severe test using 10 days of salt fog as the corrosive environment. Both of these were done intentionally. They provide the worst possible conditions and result in the quickest trends.

If a noble material such as silver, nickel or carbon is sandwiched with aluminum an increase in DC resistance will result given time. If this is unsatisfactory electrically it should either not be used or have all corrosive environments excluded. While even under these conditions one would not expect too much mechanical damage, some of the pitting caused by the nickel fillers could cause aluminum rivets to break and the large corrosion product formed in the salt environments can introduce unwanted mechanical stresses.

FUTURE WORK

Using the test arrangement shown in the new APR 1481[2], many of these coatings, used in the more typical environments of electronics, will be evaluated under RF influences. This will help to further characterize the uses in design-related environments.

REFERENCES

1. "Salt Spray (Fog) Testing," ASTM B 117, 1973.
2. "Dissimilar Metals," SAE APR 1481, 1968.

TABLE I
CONDUCTIVE ADHESIVES

#	ADHESIVE DESCRIPTION	RESISTANCE (OHMS) AVE ORIG.	RESISTANCE (OHMS) AVE SALT	RESISTANCE (OHMS) AVE HUMID.	LAB-BOND SHEAR PSI STD.	LAB-BOND SHEAR PSI SALT	LAB-BOND SHEAR PSI HUMID	CORROSION
1	Two-part epoxy--silver filled	0.009	2.55	0.163	865	865	1082	No corrosion of the humidity sample. Slight corrosion of the salt spray. Some edge attack.
2	Two-part epoxy--silver filled	0.014	0.618	0.110	1297	968	1040	No corrosion in the faying surfaces. Some edge attack.
3	Two-part epoxy--polyamide-silver filled	2.056	2.926	2.120	1290	1470	1050	No corrosion in the faying surfaces. Some edge attack.
4	Two-part epoxy--w/ flexibilizer-silver-coated glass beads	0.104	8.94	15.50	598	204	283	Corrosion in faying surface of both environmental samples. Adhesive very dark in salt spray sample.
5	Single-part silicone-silver filled	0.046	0.067	0.064	49	52	48	Corrosion very minimal.
6	Single-part silicone-nickel filled	0.205	0.219	0.200	150	120	130	No corrosion in faying surface. Moderate edge pitting.
7	Single-part silicone-carbon filled	1.05	2.94	1.93	160	82	90	No corrosion attributed to the adhesive.
8	Two-part epoxy--copper filled	0.052	1.52	1.92	1251	1050	1110	Some green in faying surface of salt panel. Same edge attack. No corrosion on the humidity sample. Copper turned dark.
9	Two-part epoxy--nickel filled	0.005	0.86	0.36	Samples came apart during environmental test. Severe pitting at edges.			
10	Single-part heat-cured epoxy--nickel filled	0.012	0.015	0.010	200	160	200	No corrosion. Severe pitting 0.006 deep in the salt test. 0.001 - 0.002 in the humidity test.
11	Single-part heat-cured epoxy--silver filled	0.018	3.6	0.56	1340	920	1032	Quite visable corrosion in the salt spray sample. Little edge attack.

TABLE II

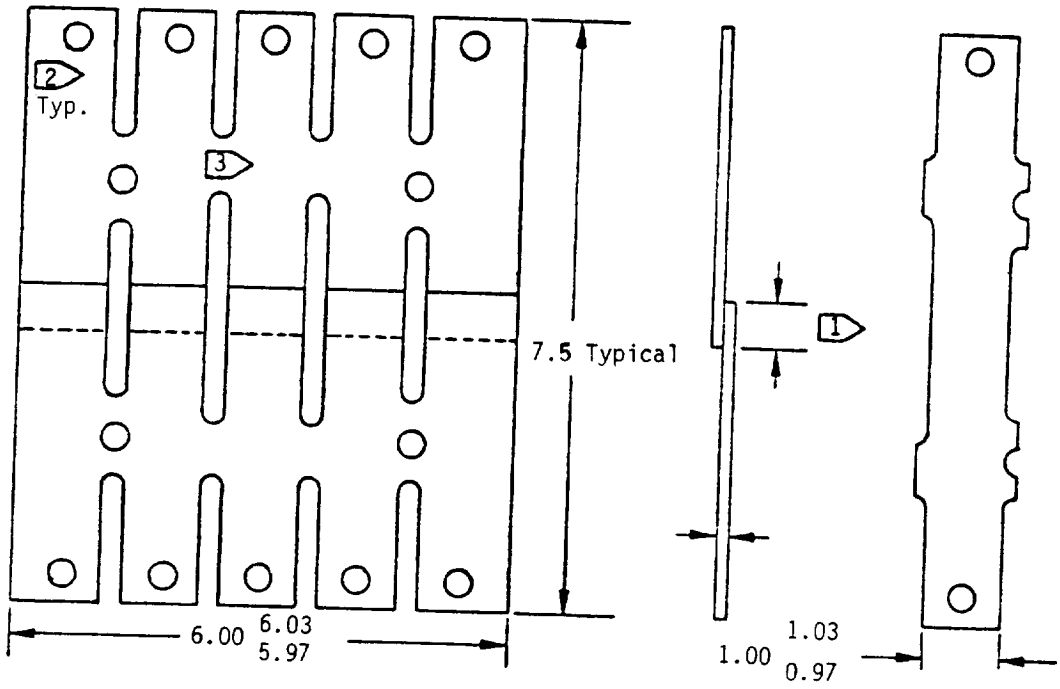
RESISTANCE OF COATINGS

	MATERIAL	RESISTANCE (OHMs/SQ.)		
		ORIGINAL	SALT	HUMIDITY
1	WATER-BASED ACRYLIC - NICKEL FILLED	87.	100 +	84
2	WATER-BASED LATEX - CARBON FILLED	987.	---	100 +
3	SOLVENT-BASED ACRYLIC - SILVER FILLED BLUE	2.71	13.4	4.67
4	POLYURETHANE - SILVER FILLED	.008	.09	.01
5	SOLVENT-BASED ACRYLIC - SILVER FILLED	.098	50.1	1.2
6	ACRYLIC LACQUER-CARBON FILLED	9.8	100 +	9.2
7	HEAT-ACTIVATED ONE-PART EPOXY - SILVER FILLED	0.31	1.7	0.30
8	SOLVENT-BASED ACRYLIC - SILVER FILLED	11.10	100 +	11.5
12	SOLVENT-BASED ACRYLIC- NICKEL FILLED	0.8	2.4	1.2
13	WATER-BASED ACRYLIC EMULSION - NICKEL	0.95	1.9	0.90

TABLE III

CAULKS AND GREASES

NUMBER	MATERIAL DESCRIPTION	BULK RESISTANCE OHM-CM
9	COPPER-FILLED EPOXY - HARDENING	0.092
10	NICKEL-FILLED SILICONE FLEXIBLE	0.14
11	CARBON-FILLED SILICONE FLEXIBLE	79
14	SILVER-COATED COPPER-FILLED SILICONE	.0008
15	SILVER-FILLED GREASE	0.21
16	NICKEL-FILLED GREASE	.0019
17	CARBON-FILLED GREASE	.01
18	CARBON FILLED - GREASE/CAULK	10.1



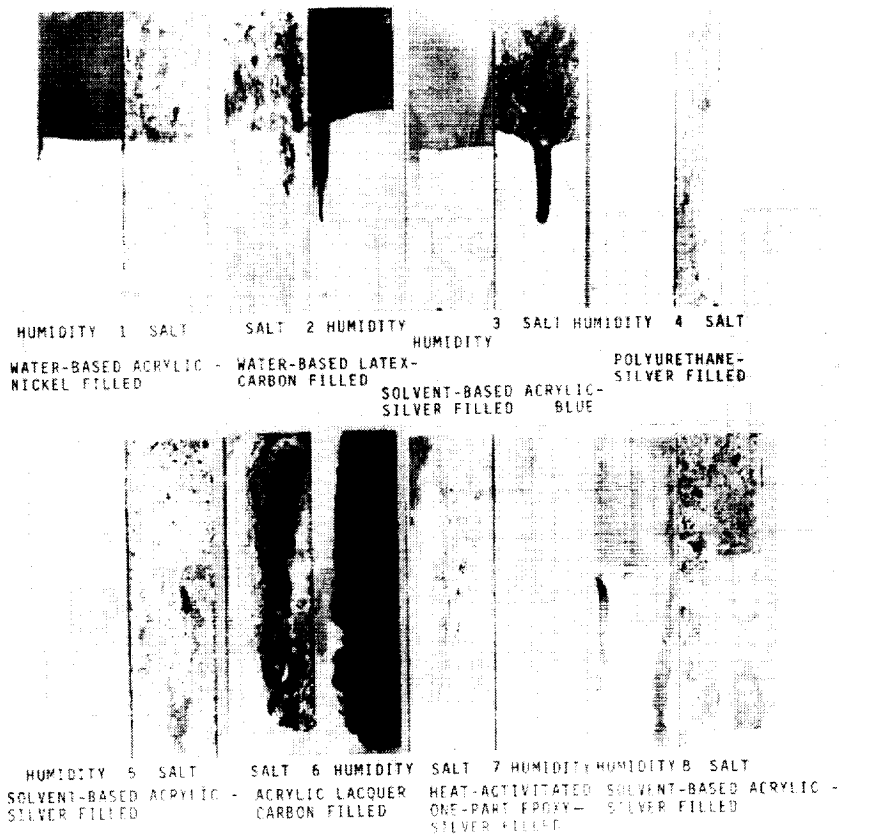
All dimensions in inches.

1 Except as otherwise specified the bond length shall be 0.50 ± 0.030.

2 Test assembly identification. Identify and number each specimen as necessary.

3 It is optional to notch for easy breakaway without sawing.

Figure 1. Standard test assembly and specimen.



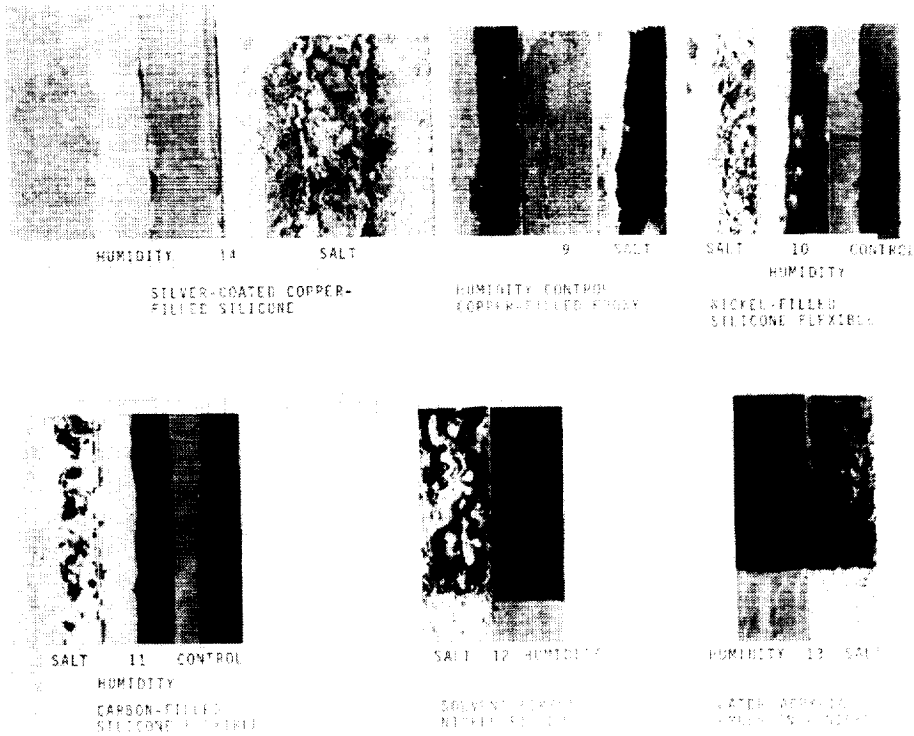


Figure 2. Pictorial test results.

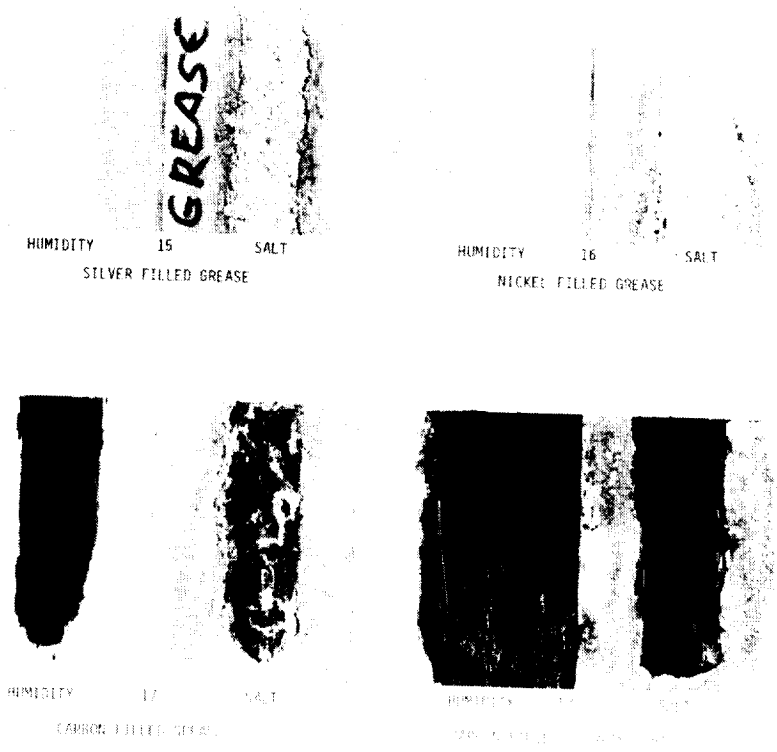


Figure 2. Concluded.

A COMPARISON OF LIGHTNING AND NUCLEAR ELECTROMAGNETIC PULSE RESPONSE OF A HELICOPTER

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ABSTRACT

A numerical modeling technique is utilized to investigate the response of a helicopter to both lightning and NEMP. The analytical approach involves the three-dimensional time domain finite-difference solutions of Maxwell's equations. Both the external currents and charges as well as the internal electromagnetic fields and cable responses are computed. Results of the analysis indicate that, in general, the short circuit current on internal cables is larger for lightning, whereas the open-circuit voltages are slightly higher for NEMP. The lightning response is highly dependent upon the rise time of the injected current as one might expect. The analysis also showed that coupling levels to cables in a helicopter are 20 to 30 dB larger than those observed in fixed-wing aircraft.

INTRODUCTION

One of the technical areas under current debate in the lightning and NEMP community is the relationship of the lightning to NEMP response of an aircraft. Since lightning and NEMP both present a severe electromagnetic hazard to helicopters and other aircraft, it is important to recognize and understand the differences and similarities in response to these two threats. In particular, it is important to recognize that hardening an aircraft to one of these threats does not guarantee that it will be hardened to the other. Currently there is no complete or clear-cut answer to this problem.

The purpose of the analytical study reported in this paper is to make the comparison between the two threats as they affect the same vehicle, utilizing current understanding of the state of the art. The aircraft chosen for analysis is the Sikorsky UH-60A Blackhawk helicopter. This vehicle is a good choice for study because preliminary test data are available that can be utilized to check the analytical results.

DISCUSSION

THE MODELING APPROACH - The method utilized to model the effects of NEMP and direct lightning attachment to the UH-60A helicopter is the three-dimensional time domain solution of Maxwell's equations by finite-difference techniques (1)*. A rectangular coordinate system was chosen with the longitudinal axis of the aircraft oriented in the y direction, the vertical axis in the z direction and the lateral axis in the x direction. The cell size (dx=dy=dz) was chosen to be 0.5 meters and this results in a computational bandwidth of 150 MHz. The overall problem space consisted of 21x49x21 = 21,609 cells. The cell size was selected so that cell boundaries closely approximated the aircraft skin. The aircraft structure is modeled by setting the tangential electric fields on the appropriate cell face to zero for all time steps. The time step utilized was 0.5×10^{-9} seconds, or about half that dictated by the Courant condition for stability.

Fig.1 shows a sketch of the modeled aircraft. The surfaces and lines shown are those representing zero tangential E field. The aircraft cabin consists of a large cavity with apertures at the main cabin windows (A), the windows and composite region forward of the main landing gear (B), and the windows surrounding the cockpit (C). The nose electronics bay (E), and the regions under the cowlings forward and aft of the main rotor pylon (D) were also modeled as apertures open to free space. The computational test point locations are shown in Fig. 2. Cables modeled by the finite-difference thin-wire formalism were included inside the cabin, one horizontal and one vertical as shown. Computations were made of the short circuit current and the open circuit voltage on both of these wires. It is expected that the response of these wires should be somewhat larger than that for the actual wiring because the modeled wires are more exposed than are the actual wires.

THE MODELED ENVIRONMENT - NEMP simulation requires a source outside the problem space. This condition was modeled utilizing Huygens sources (1). The electric field source waveform is the NEMP plane wave double exponential given by

$$E(t) = 5.2 \times 10^{4} \left[\exp\left(-4.0 \times 10^{6} t\right) - \exp\left(-5.0 \times 10^{8} t\right)\right] \quad (1)$$

Responses were computed for both topside and left incidence. Longitudinal and lateral polarization were modeled for topside incidence and longitudinal and vertical polarization were utilized for the left-side incidence case.

Lightning attachment was simulated by injecting a current into the forward tip of the main rotor blade from the left boundary of the problem space. Attachment to the tail rotor was also studied. The exit point was modeled by zeroing the electric fields along a line from the point to the nearest problem space boundary. This corresponds to a perfectly conducting exit channel. Two exit points were chosen for study: the left main landing gear and the aft pointing blade of the tail rotor. Three driving current sources were utilized for the lightning simulation. They are:

1. $\sin^2$ rise to 200 kA in 2 microseconds with exponential decay constant of 50 microseconds
2. $\sin^2$ rise to 72 kA in 300 nanoseconds and constant at 72 kA after 300 nanoseconds
3. $\sin^2$ rise to 7.2 kA in 30 nanoseconds and constant at 7.2 kA after 30 nanoseconds

The lightning current waveforms for 30 and 300 nanosecond rise times reflect a maximum dI/dt of 3.75×10^{11} A/s. This results in a peak current of 7.2 kA for a 30 ns rise time, and 72 kA for a 300 ns rise time. The 200 kA waveform represents the standard MIL-B-5087B waveform (2).

COMPUTED RESPONSES - Five field components were computed for each of the five test points shown and for each of thirteen EMP test environments. In addition, the short circuit current and open circuit voltage on the two thin wires were also computed for each of the 13 modeled threats giving a total of 377 specific time domain plots. Of course, fields at all points in the problem space were available if required.

A summary of some representative response data is given in Table 1. Only the peak values for each response are shown in the table.

*Numbers in parentheses designate References at end of paper.

In the table, E_n is the electric field normal to the nearest surface, H_x is the lateral magnetic field, $I_s(y)$ and $I_s(z)$ are the short circuit currents on the longitudinal and vertical wires respectively, and $V_o(y)$ and $V_o(z)$ are the associated open circuit voltages.

A few sample waveforms are shown in Figs.3 through 10. Note the strong resonance associated with the total length of the vehicle (19 meters) evident in the lateral magnetic field waveform. The thin-wire waveforms also show resonances associated with the length of the wires. A more complete listing of the response data is given in (3).

Magnetic field components parallel to the aircraft skin were computed for several points inside and outside the cabin. The outside values exceed the inside values by a factor of 100 or more indicating a shielding factor in excess of 40 dB. Utilizing peak wire currents on the thin wires and the corresponding peak injection currents, representative current transfer functions for lightning were calculated. The values obtained are 47 dB, 47 dB and 39 dB for 2 microseconds, 300 nanoseconds, and 30 nanoseconds rise times respectively. The approximate transfer functions obtained in this way are seen to be in general accord with the observed shielding effectiveness of the cabin structure.

RESPONSE COMPARISONS - Simulated NEMP measurements were made on a UH-60A Blackhawk at Harry Diamond Laboratories utilizing the biconic dipole radiator (4). A total of 12 bulk current measurements were made yielding currents in the range of 3.8 A to 46 A, when scaled to a 50 kV/m incident field. The mean short circuit currents produced by the computer modeling effort for the same angle of incidence and polarization is 30 A. These two independent results thus compare very favorably.

Lightning tests on the Blackhawk were done by Lightning Transient Research Institute (LTRI) (5). The induced voltage on 26 circuits was measured utilizing a peak test current of 400 A and a rise time of 10 microseconds. The results were scaled to be comparable with the 200-kA 2-microsecond rise lightning excitation utilized in the model. The scaled voltages obtained by LTRI for the forward rotor injection case ranged from 863 Volts to 64.7 kV with the average being 10.5 kV. Of this data set, three of the measured voltages were extremely high, probably because the cables penetrate to the outside of the cabin structure. Removing these three measurements from the data set, the average of the remaining voltages is 5.4 kV, which is in close agreement with the 4.7 kV obtained from the UH-60A numerical model for cables inside the cabin structure.

The analysis of the aircraft's response to the two EMP environments shows that the short circuit current on internal cables is larger for lightning, and the open circuit voltage is larger for NEMP. The lightning response greatly depends upon the rise time of the injected current. Open circuit voltages for a 30 ns rise-time approach that of NEMP (20 kV vs 22 kV), but the lightning-induced short circuit currents are less (54 A vs 72 A) than that caused by NEMP. On the other hand, for a 2-microsecond rise time source, the lightning-induced short circuit current is much larger than that caused by NEMP (441 A vs 72 A) but the lightning-induced voltage is much less (4.9 kV vs 22 kV).

CONCLUSIONS

The responses of a UH-60A helicopter to both lightning and NEMP threats were computed utilizing a finite-difference analytical technique. Results of the analysis were compared with measurements made on the same vehicle. The computed responses and subsequent comparisons give rise to the following conclusions.

1. The UH-60A cabin provides about 40 to 45 dB of shielding to external fields which is considerably lower than for fixed-wing aircraft.
2. The analytical results compare favorably with measurements made for both lightning and NEMP, thus lending credibility to the analytical approach.
3. Short circuit currents on internal cables are larger for lightning than for NEMP.
4. Open circuit voltages on internal cables are slightly higher for NEMP than for lightning.
5. Based on conclusions 3 and 4, the power and energy dissipated in a load resistor at the end of an internal cable will be larger for lightning than for NEMP.

Finally, it should be pointed out that only coupling responses were compared. Assessment of aircraft hardness to the two threats was not investigated. Also, only specific environments were used, and statistics should be included in a more complete investigation. For these reasons, it should be emphasized that the issues regarding the relative importance of NEMP and lightning hazards yet require more study.

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2. "Bonding, Electrical, and Lightning Protection for Aerospace Systems, Military Specification MIL-B-5098B, 31 August 1970.

3. R.A. Perala and C.C. Easterbrook, "Correlation of Lightning and NEMP Response of the UH-60 Blackhawk Helicopter," Report EMA-83-R-19, Electro Magnetic Applications, Inc. (EMA), P.O. Box 26263, Denver, CO 80226, April 1983.

4. R.J. Reyser, "Preliminary EMP Analysis of the UH-60A Blackhawk Helicopter (U)," Harry Diamond Laboratories, January 1983.

5. J.D. Robb and J.D. Herring, "Lightning Tests Sikorsky Blackhawk," L&T Report No. 701, Lightning Transients Research Institute, January 1980.

Table 1 - Summary of peak responses for a representative sample of test points

Test Case	Test Point #1		Test Point #3		Test Point #5		Thin Wires			
	E_n kV/m	H_x a/m	E_n kV/m	H_x a/m	E_n kV/m	H_x a/m	$I_s(y)$ A	$V_o(y)$ kV	$I_s(z)$ A	$V_o(z)$ kV
EMP Top-Side Incidence Longitudinal Polarization	32.6	301	98	226	13.9	35	72	22	47	15
EMP Top-Side Incidence Lateral Polarization	8.6	56	25	17	4.6	12	33	-	20	-
EMP Left-Side Incidence Longitudinal Polarization	29.4	410	88	64	4.3	10	40	-	20	-
EMP Left-Side Incidence Vertical Polarization	25.2	259	28	53	3.1	7	12	-	9	-
Lightning - 2 μs Rise Attach Forward Rotor Exit Left Landing Gear	40×10^3	73×10^3	15×10^3	15×10^3	34	670	441	5	1353	4
Lightning - 300 ns Rise Attach Forward Rotor Exit Left Landing Gear	7.2×10^3	26×10^3	3.2×10^3	5.6×10^3	10	242	162	13	492	12
Lightning - 30 ns Rise Attach Forward Rotor Exit Left Landing Gear	680	4.8×10^3	297	1×10^3	16	85	54	20	109	20
Lightning - 2 μs Rise Attach Forward Rotor Exit Tail Rotor	44×10^3	69×10^3	18×10^3	14×10^3	34	630	196	-	1197	-
Lightning - 300 ns Rise Attach Forward Rotor Exit Tail Rotor	7.2×10^3	25×10^3	3.2×10^3	5.2×10^3	10	231	87	-	450	-
Lightning - 30 ns Rise Attach Forward Rotor Exit Tail Rotor	680	4.8×10^3	322	1×10^3	16	85	54	-	106	-

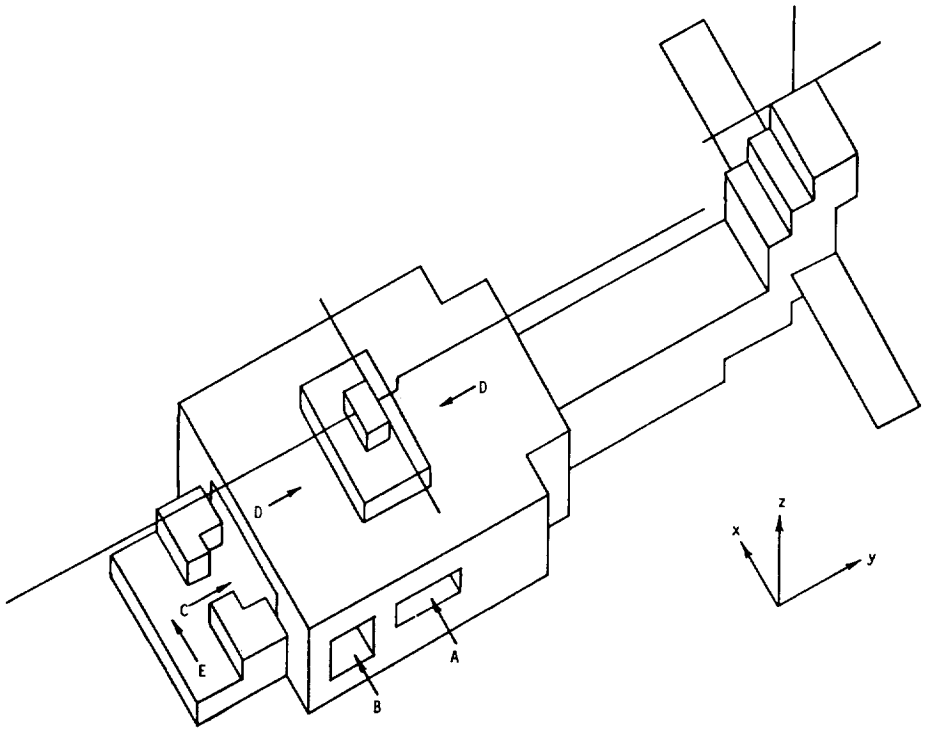

Figure 1. Three-dimensional finite-difference model of UH-60A helicopter.

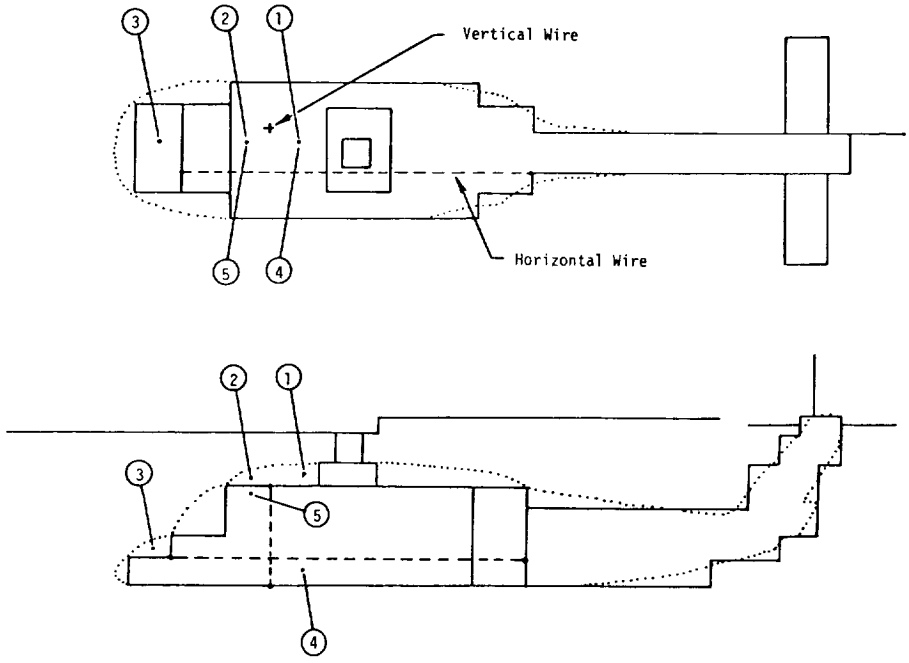

Figure 2. Location of test points and wires.

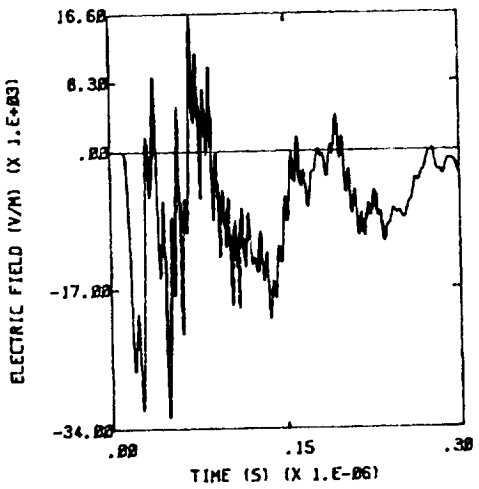

Figure 3. Normal electric field at test point 1, NEMP excitation - vertical incidence, longitudinal polarization.

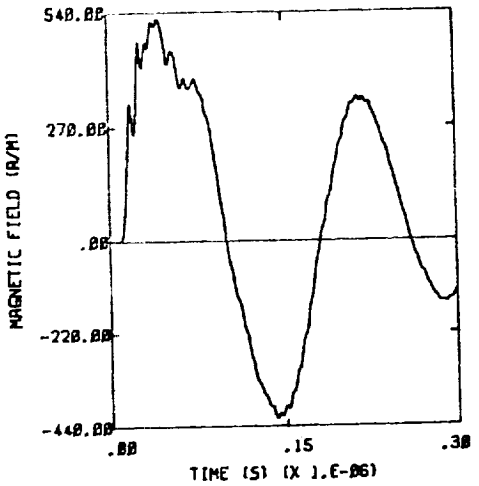

Figure 4. Lateral magnetic field near top of tail boom, NEMP excitation - vertical incidence, longitudinal polarization.

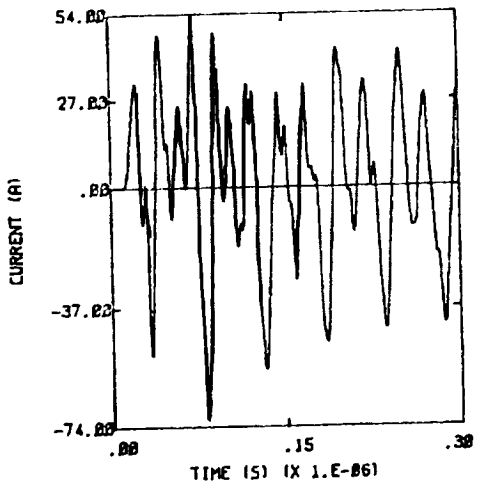

Figure 5. Short circuit current on longitudinal wire, NEMP excitation - vertical incidence, longitudinal polarization.

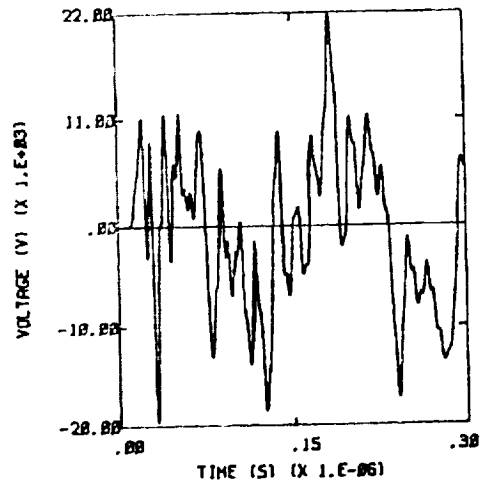

Figure 6. Open circuit voltage on longitudinal wire, NEMP excitation - vertical incidence, longitudinal polarization.

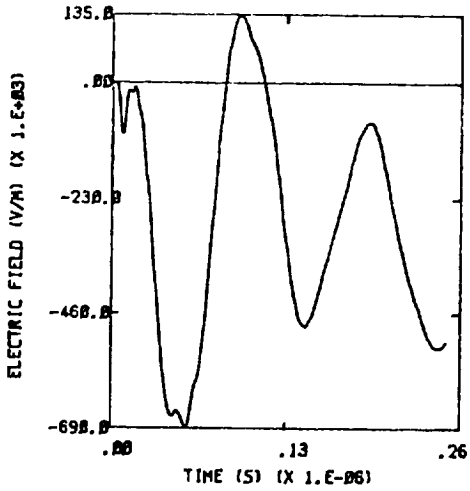

Figure 7. Normal electric field at test point 1, lightning excitation - 30 nanosecond rise time, 7.2 kA peak.

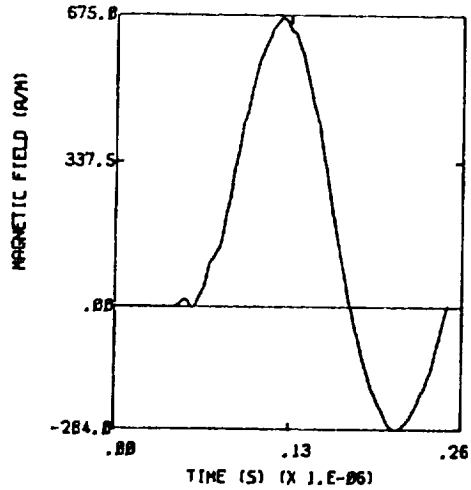

Figure 8. Lateral magnetic field near top of tail boom, lightning excitation - 30 nanosecond rise time, 7.2 kA peak.

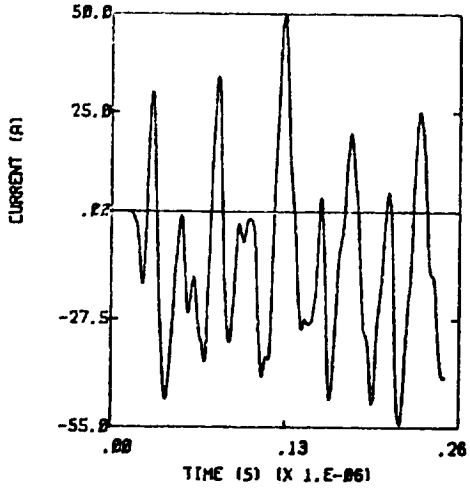

Figure 9. Short circuit current on longitudinal wire, lightning excitation - 30 nanosecond rise time, 7.2 kA peak.

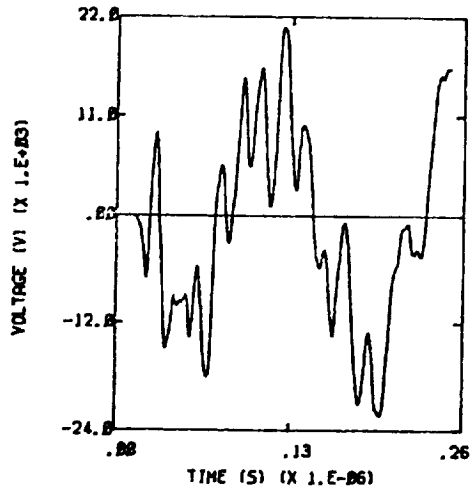

Figure 10. Open circuit voltage on longitudinal wire, lightning excitation - 30 nanosecond rise time, 7.2 kA peak.

A COMPARISON OF LIGHTNING AND NUCLEAR ELECTROMAGNETIC PULSE RESPONSE OF TACTICAL SHELTERS

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ABSTRACT

One of the technical areas under current debate in the lightning and NEMP communities is the relationship between the lightning and NEMP responses of systems. In this paper, we address the internal response (electromagnetic fields and cable responses) of tactical shelters.

Tactical shelters are usually well-shielded systems. Apart from penetrations by signal and power lines, the main leakage paths to the interior are via seams and the environment control unit (ECU) honeycomb filter.

In this paper, we employ the time domain three-dimensional finite-difference technique to determine the external and internal coupling to a shelter excited by NEMP and attached lightning. The responses of interest are the internal electromagnetic fields and the voltage, current, power, and energy coupled to internal cables. Leakage through the seams and ECU filter is accomplished by their transfer impedances which relate internal electric fields to external current densities. Transfer impedances which have been experimentally measured are used in the analysis. The internal numerical results are favorably compared to actual shelter test data under simulated NEMP illumination.

INTRODUCTION

Many DOD C^3 systems are required to be mobile or portable. A typical system consists of a shelter which contains numerous electronic subsystems and some operating personnel. The shelter usually provides an electromagnetic shield for this equipment. The shelter almost always requires penetrations from the outside world via long telephone lines, power lines, antennas, etc. Other electromagnetic penetrations into the shelter occur because of seams in the skin and environmental control unit (ECU) vents.

The objective of the research reported in this paper is to compare the nuclear electromagnetic pulse (NEMP) and lightning response of a shelter. The study is mainly limited to penetrations via seams and ECU vents. The NEMP response is calculated both for field illumination of the shelter and for current induced on the shelter skin by attached long lines.

In this paper we will discuss the basic shielding concepts, give an example comparison between measured and calculated internal responses, and present the lightning/NEMP comparisons. Finally, conclusions are given.

BASIC SHIELDING CONCEPTS

BACKGROUND - The basic element of protection provided by shelters is the shielding provided by the skin. Apart from penetration of this shielding envelope by cables or antennas, energy can penetrate through the shield via diffusion through the skin and by leakage through imperfections in the skin. Therefore, the items of interest to be considered here are:

1. Diffusion through the skin material
2. Penetration through permanent seams
3. Penetration through ECU (environmental control unit) openings
4. Penetration through door seams

DIFFUSION THROUGH THE BASIC SKIN MATERIAL - Diffusion through the skin material can be easily estimated if one knows the external surface current density $J_S(\omega)$ on the shelter skin and the skin transfer impedance $Z_T(\omega)$ according to:

$$E(\omega) = Z_T \; J_S(\omega) \tag{1}$$

and

$$Z_T(\omega) = \frac{\hat{n}}{\sinh jkd} \tag{2}$$

where $\hat{n}$ is the intrinsic wave impedance, k is the propagation constant in the metal skin, d is the skin thickness, and $E(\omega)$ is the internal electric field tangential to the shelter skin. It can be shown (1,2)* that for metal thicknesses commonly used in shelter construction, diffusion is insignificant for EMP. EMP-induced voltages are less than a few millivolts. Diffusion for lightning can be more important, primarily because of the much larger and slower currents which are incident on the shelter exterior. Internal induced voltages on the order of a few volts are possible, depending upon the skin material and thickness.

However, for both EMP and lightning, it can be shown that the largest voltages induced on internal cables occur via the imperfections in the skin, which is the main focus of this paper.

LEAKAGE THROUGH SEAMS - Seams are traditionally the weak spots in any electromagnetically shielded enclosure. The main objective is to provide a low seam impedance Z_S to minimize leakage. In terms of the exterior surface current density J_S (amperes per meter), the voltage V_S induced across the seam is given by

$$V_S(\omega) = \bar{J}_S(\omega) \cdot \bar{Z}_S(\omega) \tag{3}$$

If a wire were routed behind the seam, the voltage V_S would be the maximum voltage that would be induced on it. In addition, there is a seam transfer admittance Y_S which relates the current induced on an internal nearby wire to the external voltage. It has been found for good quality seams that the transfer admittance Y_S is dominated by Z_S in all cases of practical interest and the discussion thereby focuses on Z_S.

Also, V_S depends upon the direction of current flow with respect to the seam. Largest induced voltages occur when J_S is normal to the seam direction. When $\bar{J}_S$ is parallel to the seam direction, the induced voltage is much smaller (3). The discussion therefore centers on the normal orientation indicated in Fig. 1.

For normal current flow, Equation (3) can be written in the time domain as

$$V_S(t) = \left[R_S + L_S \frac{\partial}{\partial t}\right] J_S(t) \tag{4}$$

where R_S and L_S are the transfer resistance and inductance in units of Ohm-m and Henry-m, respectively.

There is a significant amount of seam data in the transfer impedance format (3-6). A few selected examples will be given here to illustrate typical values of seam impedance for various conditions.

An example of the transfer impedance of a bolted seam is given in Fig. 2. It should be noted that this figure also illustrates the effects of exposure to a salt fog environment per MIL-STD-210B Method 509 (7), and a temperature/humidity environment per MIL-STD-202, Method 106B (8). Fig. 3 shows the inpedance of a gasketed seam. A summary of other data on gasketed seams is given in Fig. 4 for different contact surfaces, contact pressures, and for aging effects. The significant feature for this type of data is that seam transfer impedances can be readily made to be less than 10^{-3} Ohm-m.

The magnetic polarizability per unit length m is related to the seam inductance L_S by

$$L_S = \mu_0 m \tag{5}$$

The term m has been measured for several types of bolted and riveted seams under various circumstances (3). A summary of some of the data is shown in

*Numbers in parentheses designate references at end of paper.

Table 1. Of particular interest are the values for aluminum riveted panels (the rivets were on 2" centers). A value of $.63 \times 10^{-6}$ was obtained for 5-cm overlap, 5-cm centers, and an untreated surface.

LEAKAGE THROUGH ECU (ENVIRONMENTAL CONTROL UNIT) OPENINGS - The shelter must have an ECU opening in the shelter skin which must be protected. Two methods are possible: screen or honeycomb filters. Honeycomb is favored over screen although the honeycomb is more expensive. MIL-STD-285 (9) type data comparisons show that honeycomb offers more shielding than does screen from the same air flow aperture (10) for the same shielding effectiveness.

Coupling occurs through air-vent filters by means of the transfer inductance L_s according to:

$$E_t = L_s \frac{\partial J_s}{\partial t} \qquad (6)$$

where E_t is the transmitted electric field. Values of L_s have been measured for several types of filters (4,5,11). Data for a rather good filter are shown in Fig. 5. The inductance for this filter at 10 MHz is about 16 pH.

AN EXAMPLE OF ELECTROMAGNETIC CAPABILITY (EMC) AND ELECTROMAGNETIC PULSE (EMP) SHIELDING OF AN S280 SHELTER (12)

There are no test data available regarding the lightning-induced internal response of shelters. Such data do exist, however, for the NEMP response of several shelters. One example is given here because it compares measured results with numerically predicted results and forms a basis for validating some of the concepts described here.

Harry Diamond Laboratories has developed a prototype single-skin shelter called HATS (Hardened Army Tactical Shelter). EMP and EMC (MIL-STD-285) measurements were done on this shelter (12) and it is informative to compare these results. The pertinent features of the shelter are:

1. Single .03" Al Skin, S280 Size
2. Bolted Seams on 2" Centers
3. 1" Overlap of Seams
4. No Special Surface Treatment of Seams (Ordinary Al)
5. No Special Efforts Were Done to Make This an "RF-Tight" Shelter
6. Manufacturer: Craig
7. Before EMC/EMP Measurements, Shelter Was Subjected to 1981 MILLRACE 9.1 PSI Overpressure Test with Air Conditioning Units Attached
8. MIL-STD-285 Test Done Just Prior to EMP Test
9. EMP Test at HDL's AESOP Threat Level Simulator at More Than Twice Threat
10. Pretest Analytical Predictions Done by EMA Based on Seam Data Previously Discussed
11. ECU Openings Covered by Gasketed Panels

The EMC test was done according to MIL-STD-285. The results are more fully discussed in (12) and are only summarized here. The interesting result from these tests is that the magnetic field shielding at 150 kHz was measured to be as low as 38 dB.

Figs. 6 and 7 show measured typical internal magnetic and electric fields for the NEMP test, which was conducted with the Army's AESOP simulator at more than twice the threat level (123 kV/m vs 50 kV/m). The vertical scales are in volts of sensor output, but the peak values in MKS units are also indicated. It should be pointed out that the late time falloff of the magnetic fields is caused by the probe's low-frequency response limitations. First, the calculated internal responses are somewhat higher than those measured, indicating the 10^{-3} Ω-m is an upper bound for the seam impedances.

Pretest predictions were done (12, 13) of the shelter response for a horizontally polarized plane wave incident at 31° above the horizontal. The modeling approach is described in the next section. The seam impedances which were used in the analysis are 10^{-3} Ω-m, resistive. The incident field is modeled as a fast rising (<10 ns) pulse with a decaying tail whose zero crossover is 900 ns. The responses shown in Figs. 8 and 9 are normalized for a 50 kV/m incident field.

Because the predictions and measurements were done for different angles of incidence and polarization, they cannot be directly compared. However, several important observations and conclusions can be made. Comparisons of predictions and measured data also indicate that the seams are primarily resistive and not inductive. If the seams were inductive, the internal electromagnetic fields would look like the derivative of those given in Figs. 6-9.

The HATS data can be summarized as follows:

1. EMC tests showed 38 dB per MIL-STD-285 at 150 kHz
2. EMP shielding effectiveness for vertically polarized incidence (E_{inc} = 123 kV/m, H_{inc} = 225 A/m):
   a. H Fields (33 Measurements)
      Average: .033 A/m SE = 76 dB
      Max: .16 A/m SE = 63 dB
   b. E Fields (10 Measurements)
      Average: .50 V/m SE = 108 dB
      Max: .80 V/m SE = 104 dB
3. EMP shielding effectiveness for horizontally polarized incidence ($E_{inc} \approx$ 73 kV/m, $H_{inc} \approx$ 190 A/m (estimated)): H-Fields (2 measurements): .01 and .04 A/m, SE = 86 dB and 74 dB
4. Numerical predictions for 50 kV/m incident fields based on 10^{-3} Ohm-m seams gives maximum values for H of .26 A/m and E of 1 V/m, thus indicating that this is a conservative number for actual seams

5. It is observed that the magnetic fields are time integrals of the seam voltages and thus the external surface currents. The inside of the shelter thus acts like an inductor driven by the seam voltage source, with the magnetic field represented by the inductor current.

COMPARISON OF CALCULATED SHELTER NEMP AND LIGHTNING RESPONSE ANALYSIS APPROACH

In this section, the response of a shelter to NEMP and lightning is calculated.

The shelter of interest is indicated in Fig. 10. It is 4.5 ft above the lossy earth and is supported by four metallic supports which are in contact with the soil. The shelter has seams along all edges and all edges of the door. In addition, it is assumed that the shelter is made out of aluminum sheet metal such that there are also vertical seams spaced four feet apart on each vertical surface and horizontal seams spaced four feet apart on each horizontal surface.

There is an ECU vent with honeycomb as indicated. It is assumed to be 18" square.

The shelter is empty except for a horizontal and vertical wire placed as shown in Fig. 10.

Results are calculated for three sources:

1. A standard unclassified (14) 50 kV/m double exponential NEMP plane wave normally incident from above and polarized parallel to the long dimension of the shelter
2. NEMP-induced current from a semiinfinite long line (e.g. power or signal line), injected on the end of the shelter as shown in Fig. 10. The current waveform is shown in Fig. 11 (15)
3. A MIL-B-5087B (16) (200 kA, 2x50 μsec) lightning current waveform attached to a corner of the shelter as shown. The shelter is located above a lossy earth with soil conductivity = 0.01 S/m, and a relative dielectric constant of 10

The analysis approach is the three-dimensional time domain finite-difference technique (17). This approach is a fully three-dimensional solution of Maxwell's equations in a Cartesian coordinate system. The cell size used for all calculations is 1/2 m and the time step is .75 ns. Because the upper frequency limit of the code is determined by requiring that approximately five cells are needed to resolve the wavelength of the highest frequency of interest, the upper frequency limit is approximately 120 MHz.

For external coupling solutions, absorbing boundary conditions are used at the boundaries of the problem space to reduce reflections. For NEMP field illumination, a Huygen's surface is defined around the shelter and some of the soil such that some of this surface includes the shelter and any conductors to ground. The sources for the Huygen's surface include both the incident NEMP plane wave and the ground-reflected field for those sources above the soil-air interface, and the field transmitted in the soil for the sources below this interface. The fields reflected from the soil and transmitted into the soil are determined from the well-known frequency dependent plane wave reflection and transmission coefficients.

The procedure is to first calculate the external current and charge densities on the shelter surface. The external current densities at the seam and ECU locations are then stored in a file and used as source terms to derive the shelter interior.

The boundary conditions on the wall of the shelter interior are the usual ones for the tangential E and normal H fields on a perfect conductor. The interior of the cavity is excited by the tangential E field at the inside surface of a seam or ECU opening. This field is specified by the external surface current density J_s and transfer impedance. The tangential E-field at the inside surface of an ECU opening is given by

$$E_t(t) = L_s \frac{\partial J_s(t)}{\partial t} \qquad (7)$$

and for a resistive seam, by

$$E_t(t) = R_T J_s(t) / \Delta \qquad (8)$$

where L_s is the ECU transfer inductance and R_T is the transfer resistance of the seam, and Δ is the appropriate grid spacing. The seam transfer inductance is neglected because test data show that internal coupling is mainly resistive.

The internal fields are therefore solved by the same 3D finite-difference approach using the expressions in equations (7) and (8) as sources - the response of the internal cables is done by the finite-difference thin-wire approximation (17).

Seam impedances of .001 Ω·m are used in the basic calculations, along with an ECU transfer inductance of 10 pH. Seam transfer impedances are assumed to be resistive because actual shelter test data show this to be the case. Results are also predicted for the door seams degraded by a factor 10 (Z_s = .01 Ω·m). This is to account for the effects of degradation of the door gasketing.

Four responses are calculated for each internal cable: open-circuit voltage, short circuit current, power dissipated on a 10 Ω load, and the total energy dissipated in this load at 1 μsec. A 10 Ω load was chosen because it represents an estimate of the bulk impedance of a semiconductor device.

The electromagnetic fields are observed at six internal locations specified in Fig. 12.

In the interest of brevity, no external coupling results are presented here. A summary of the internal results is given in Table 2. The maximum electric and magnetic fields are the maximum peak values observed at any of the

six observation points. The cable responses are the maximum response for either the vertical or horizontal cable.

The cable responses indicated in Table 2 would be the worst-case response of unshielded conductors and would represent the worst-case hazard to electronics boxes.

It should be pointed out that these results are conservative because:

1. No reliance is made upon cable shielding
2. No reliance is made upon the effect of current sharing on multiple-cable bundles
3. The cables studied are of maximum length

DISCUSSION AND CONCLUSIONS

The results indicate the following:

1. The dominant NEMP shelter response occurs by means of currents induced on the shelter from long cables attached to the shelter, and not from direct field illumination.
2. The attached worst-case lightning induced internal response far exceeds that of the NEMP response. The internal fields and induced cable voltages and currents are larger by more than an order of magnitude. The power and energy induced in a 10 Ω load are about three orders of magnitude larger than those caused by NEMP.
3. Seam impedances can be characterized by seam transfer resistances. The inductance does not appear to play a major role, based on actual measurements and computations.
4. Seam resistances on the order of .001 Ω·m can be used to find the internal response of a shelter.

It should be pointed out that this investigation includes coupling only, and does not constitute an assessment of an actual system to the two hazards. Statistical and operational requirement considerations also need to be included in any complete assessment of a sheltered system. For this reason, it is premature to make any final judgments regarding the relative importance of the lightning and NEMP hazards.

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TABLE 1 - MAGNETIC POLARIZABILITY PER UNIT LENGTH OF VARIOUS SEAMS (3)

	Panel Material	Joint	Problem	Polarizability ($m^3/m \times 10^{-6}$)	
Simulated Surface Contaminants	Galvanized Steel	10-cm overlap 18-cm bolt spacing (3 bolts) 4 m-kg torque	1. None 2. One 7.5-cm wide plastic strip 3. Two 7.5-cm wide plastic strips 4. 0.13-mm plastic spacer in joint	1.3 3.0 4.5 35.0	
	Galvanized steel	5-cm overlap 9-cm bolt spacing (5 bolts) 4-m-kg torque	1. None 2. One 2.5-cm wide plastic strip 3. Two 2.5-cm wide plastic strips 4. Four 2.5-cm wide plastic strips	0.16* 0.43 0.56 0.53	
	Galvanized steel	10-cm overlap 7.5-cm bolt spacing (6 bolts)	1. None 2. Five 2.5-cm wide plastic strips	0.08* 0.26	Note: 2" Center on Rivet
Surface Contamination	Aluminum riveted panels	5-cm overlap 5-cm spacing	1. None 2. Painted surface	0.63 3.1	
	Hot rolled steel	10-cm overlap 7.5-cm bolt spacing (6 bolts) 4 m-kg torque	1. None (galvanized steel) 2. Surface scale 3. Surface scale removed	0.08* 9.9 1.3	
	Cold rolled steel	10-cm overlap 7.5-cm bolt spacing (6 bolts) 4-m-kg torque	1. None (galvanized steel) 2. Rusty joint	0.08* 190	
Panel Distortion	Galvanized steel	5-cm overlap 18-cm bolt spacing (3 bolts) 4-m-kg torque	1. None 2. Warped panels	4.0 4.1	
	Galzanized steel	10-cm overlap 7.5-cm bolt spacing (6 bolts) 4 m-kg torque	1. None 2. Warped panels 3. Bent up edges	0.08* 0.01* 0.29	
Joint Hardware	Hot rolled steel	10-cm overlap 7.5-cm bolt spacing (6 bolts) 4 m-kg torque	1. None (flat washers) 2. Lock washers	2.2 2.5	
	Galvanized steel	10-cm overlap 9-cm bolt spacing (5 bolts) 4 m-kg torque	1. None 2. Rubber washers under bolts and nuts	0.16* 0.21	
	Galvanized steel	10-cm overlap 7.5-cm bolt spacing (6 bolts) 4 m-kg torque	1. None 2. 3-mm rope caulking in joint	0.16* 0.26	

*This Measurement is Near the Measurement Threshold

TABLE 2 - SUMMARY OF INTERNAL SHELTER RESPONSES

Numbers not in parentheses indicate results with all shelter seam impedances = 0.001 Ω·m. Results in parentheses are for the same case except that door seam impedances = 0.01 Ω·m.

	NEMP Field Illumination	NEMP Current Injected From Long Lines	Attached Lightning
E_{max} (V/m)	1.2 (1.7)	1.8 (3.4)	33 (62)
H_{max} (A/m)	.042 (.062)	3.0 (3.4)	37 (77)
V_{oc} (V)	1.2 (1.7)	1.4 (4.1)	22 (57)
I_{sc} (A)	.068 (.087)	.40 (1.1)	9.3 (24)
$P_{10\Omega}$ (mW)	22 (37)	104 (2054)	1.5×10^5 (2×10^6)
$E_{10\Omega}$ (nJ)	14 (19)	181 (3604)	9.7×10^4 (1.3×10^6)

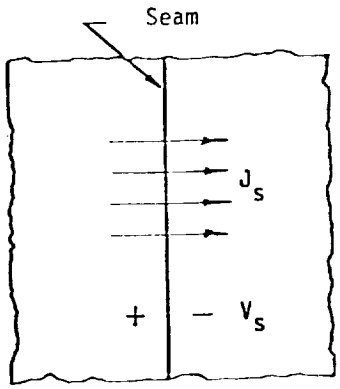

Fig. 1 - Surface current density flowing across a seam.

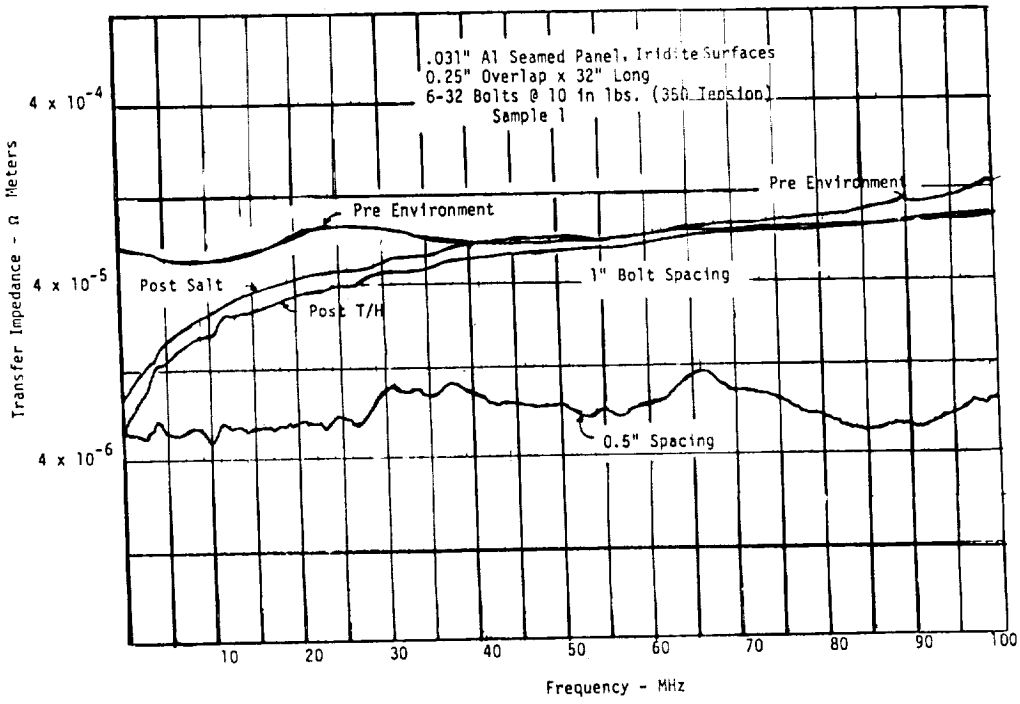

Fig. 2 - Seam impedance for typical bolted seams, showing environment effects (5) T/H - temperature/humidity test.

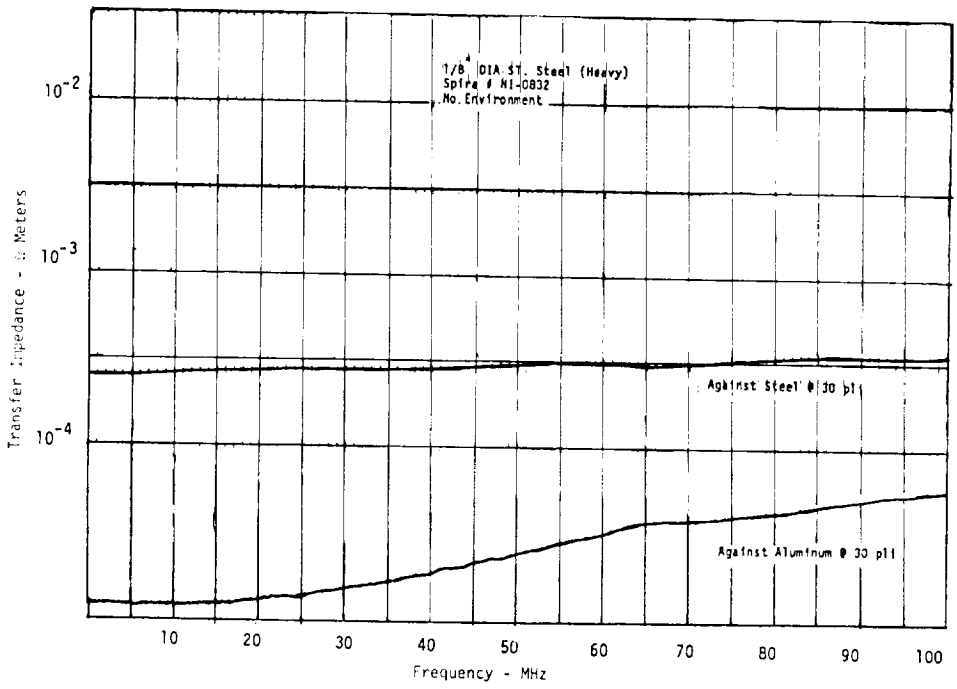

Fig. 3 - Seam impedance for a Spira gasketed seam (5), pli = pounds per linear inch .

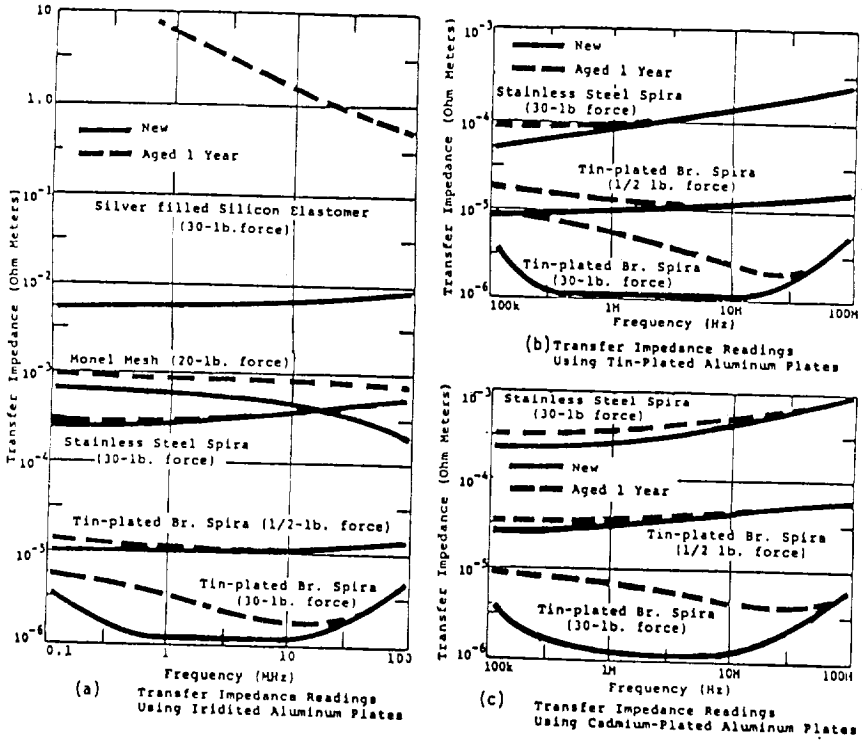

Fig. 4 - Transfer impedance of selected gasketed seams (10).

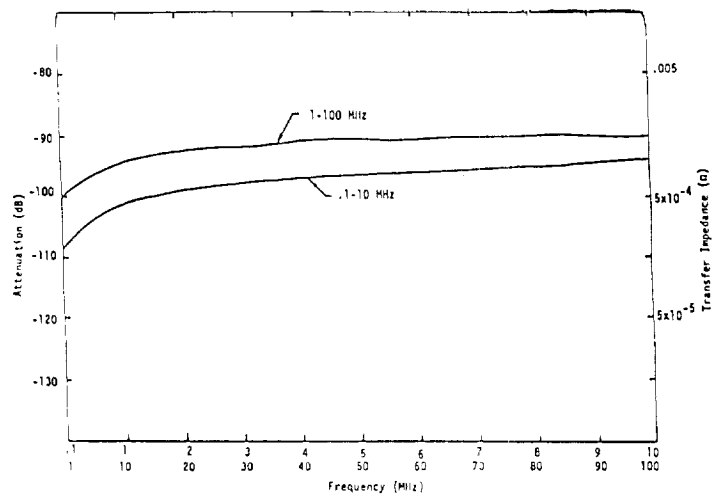

Fig. 5 - The (experimental) values of attenuation and surface transfer impedance Z_{meas} for metallic honeycomb (1/8" x 1/2" steel, 10" x 10" frame, Tecknit #64-90055; steel shield plate) (5, 11).

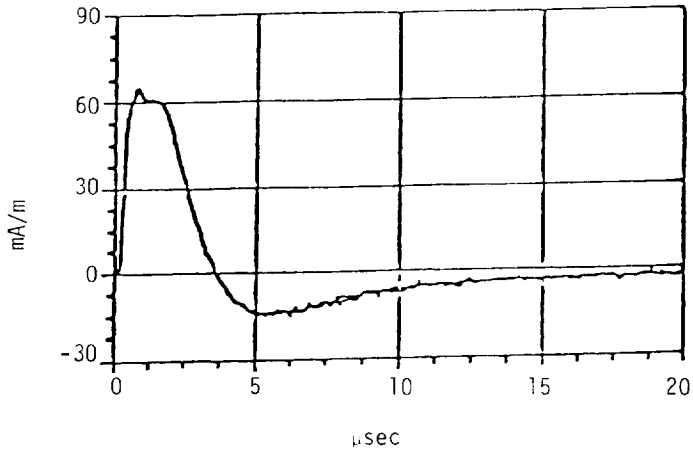

Fig. 6 - Measured internal magnetic field for vertically polarized illumination (E_{inc} = 123 kV/m).

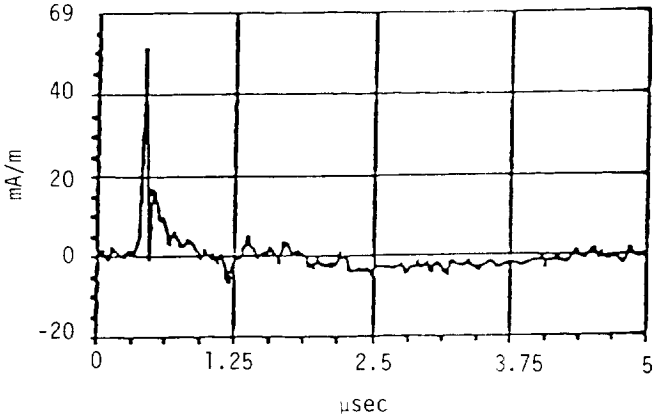

Fig. 7 - Measured electric field for vertically polarized illumination (E_{inc} = 123 kV/m).

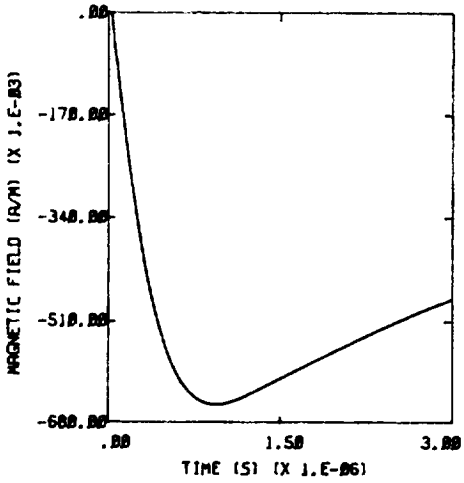

Fig. 8 - Calculated value of H_x, horizontal E-field polarization, angle of incidence 31°, incident field 1 kV/m, maximum peak internal field, shelter 4' above ground, resistive seams 12 each, crossover of incident field is 900 ns.

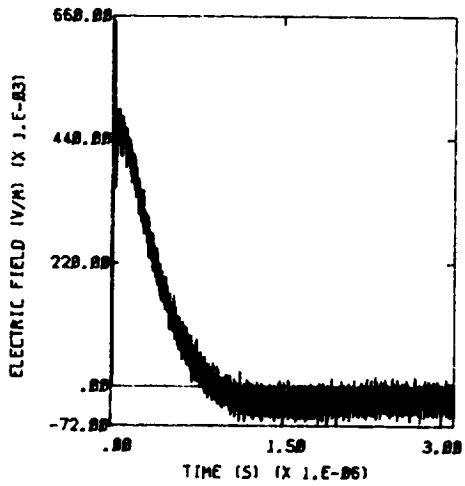

Fig. 9 - Calculated value of E_y.

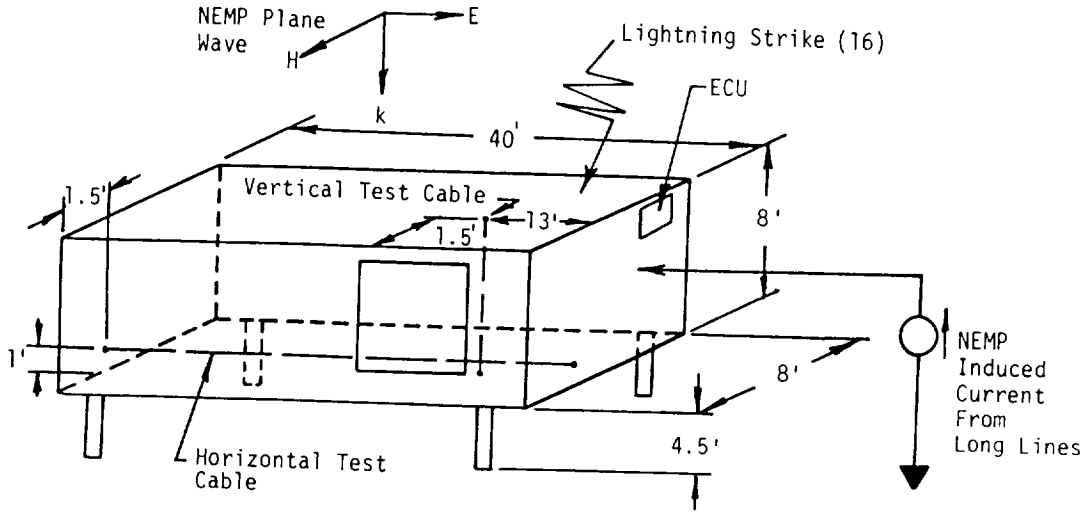

Fig. 10 - Pictorial representation of finite difference model of shelter.

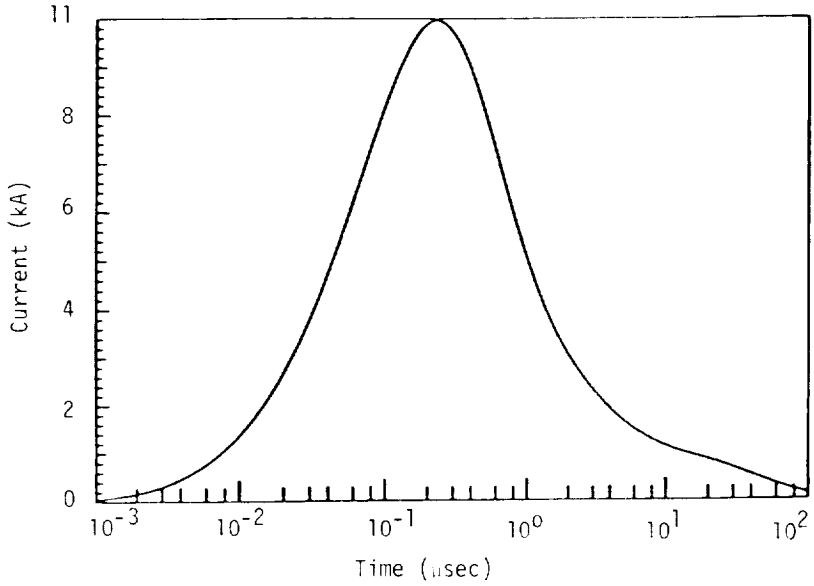

Fig. 11 - NEMP-induced short circuit current injected on a shelter from a semi-infinitely long overland line 10 m above a perfectly conducting ground plane (17).

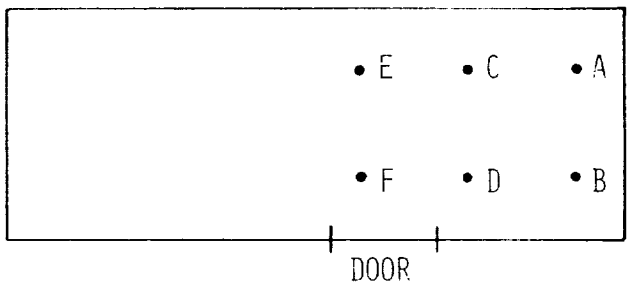

Fig. 12 - Internal measurement points for electromagnetic fields, all points are midway between ceiling and floor.

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16. Abstract

The supplement to the proceedings of the 1984 International Aerospace and Ground Conference on Lightning and Static Electricity held on June 26-28, 1984, in Orlando, Florida, is published herein. This supplement contains papers that were presented at the conference but were unavailable for printing at the time of publication of the proceedings. Major topics discussed in this supplement are indirect effects of lightning on systems, ground systems protection, materials, and lightning versus nuclear electromagnetic pulses.

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