HIGH-EFFICIENCY MODULE DESIGN

SPIRE CORP.

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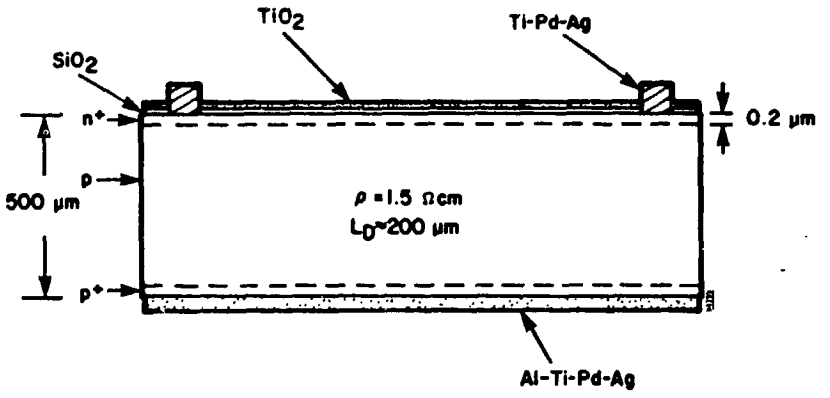
Principal Results

- FABRICATED MODULE WITH HIGH SUB-BANDGAP REFLECTIVITY AND EFFICIENCY OF 13.7%.
- FABRICATED LARGE-AREA CELLS WITH EFFICIENCY OVER 18%.

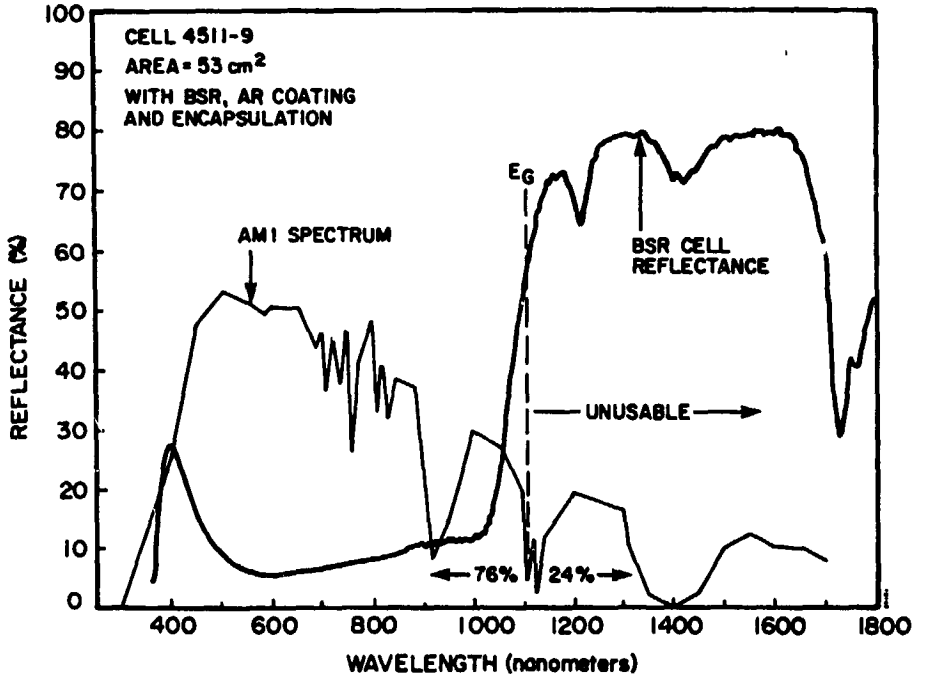
Objectives

- FABRICATION OF MODULES WITH EMPHASIS ON REDUCED OPERATING TEMPERATURE.
- FABRICATION OF HIGHLY EFFICIENT MODULES.
- EVALUATION OF POSSIBLE TRADE-OFF BETWEEN HIGH EFFICIENCY AND LOW NOCT.

Cell Design



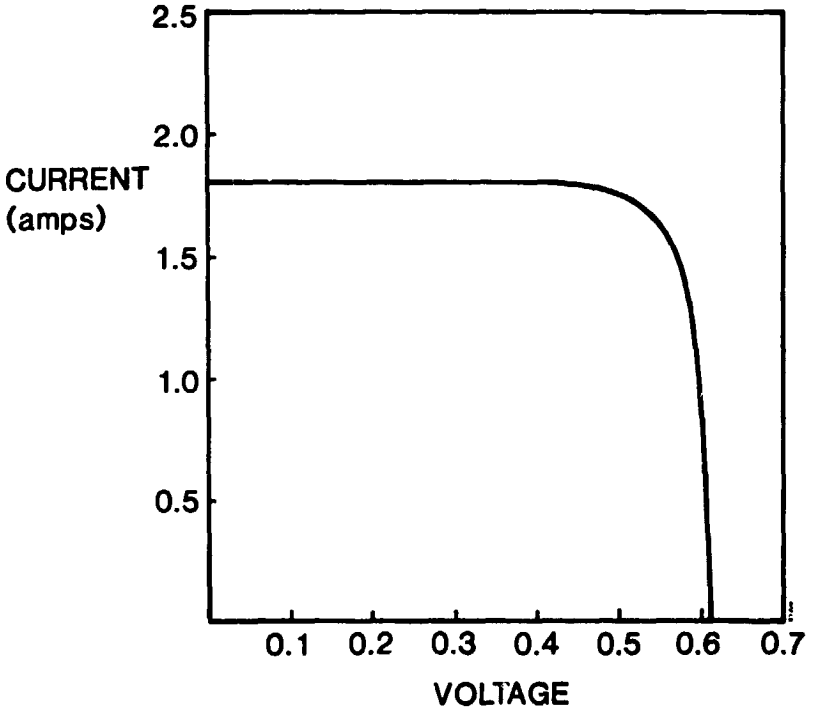
- Al USED FOR BSR
- SiO_2 USED TO PASSIVATE SURFACE
- p^+ SIMPLE OHMIC CONTACT (NOT BSF)
- NO EDGE PASSIVATION USED



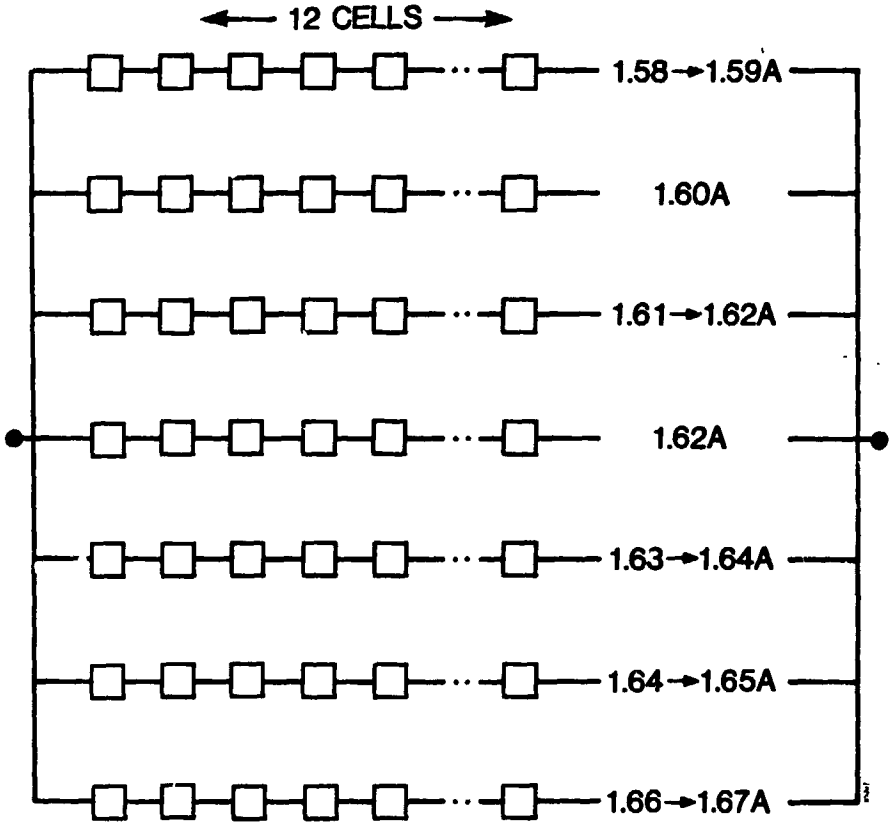
Assembly Performance

(AM1.5, 100 mW/cm^2, T= 25°C)
Tested by JPL

Eff = 17.1%
V_{oc} = 611 mV
J_{sc} = 34 mA/cm^2
FF = 82.5%
AREA = 53.04 cm^2



Module Circuit and Mismatch Loss



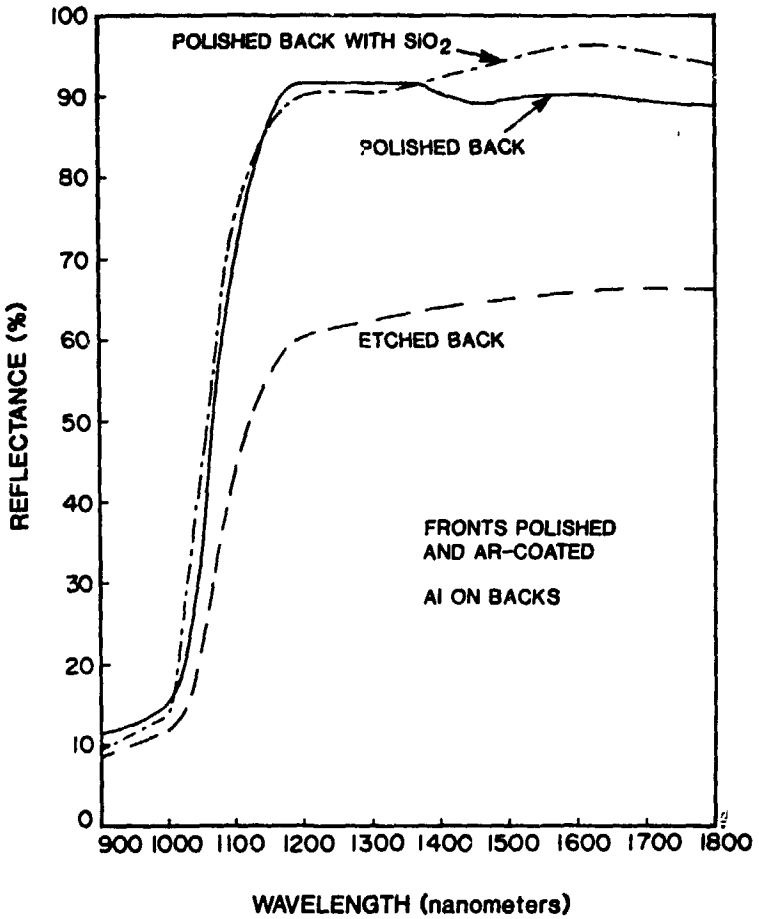
I_{mp} OF EACH CELL WITHIN 1% OF THE STRING AVERAGE.

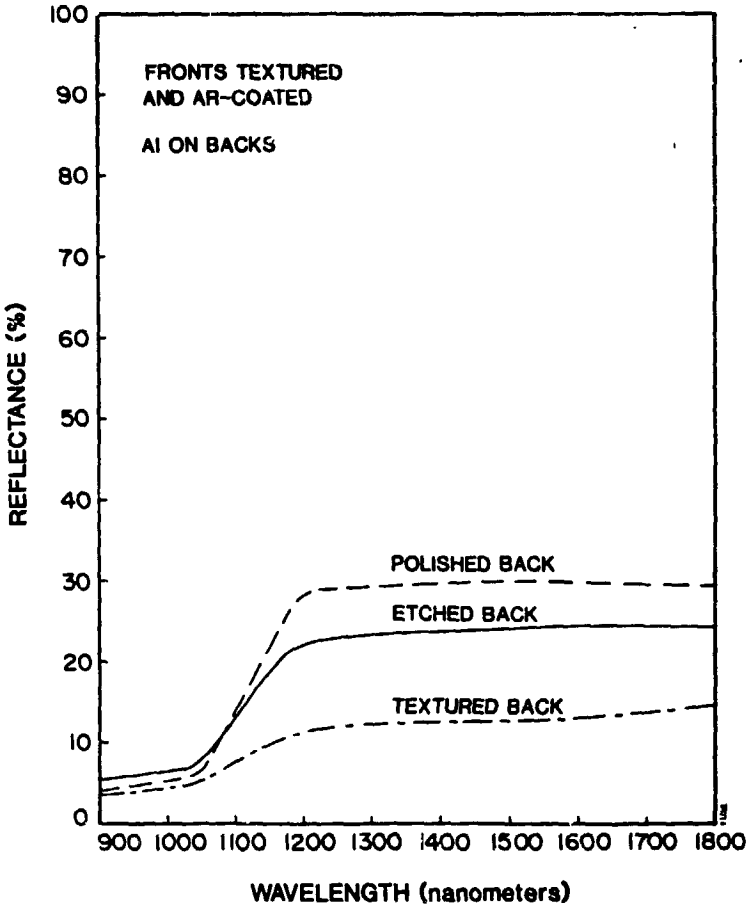
ALL STRINGS HAVE ΣV_{mp} of 6.053± .001 mV.

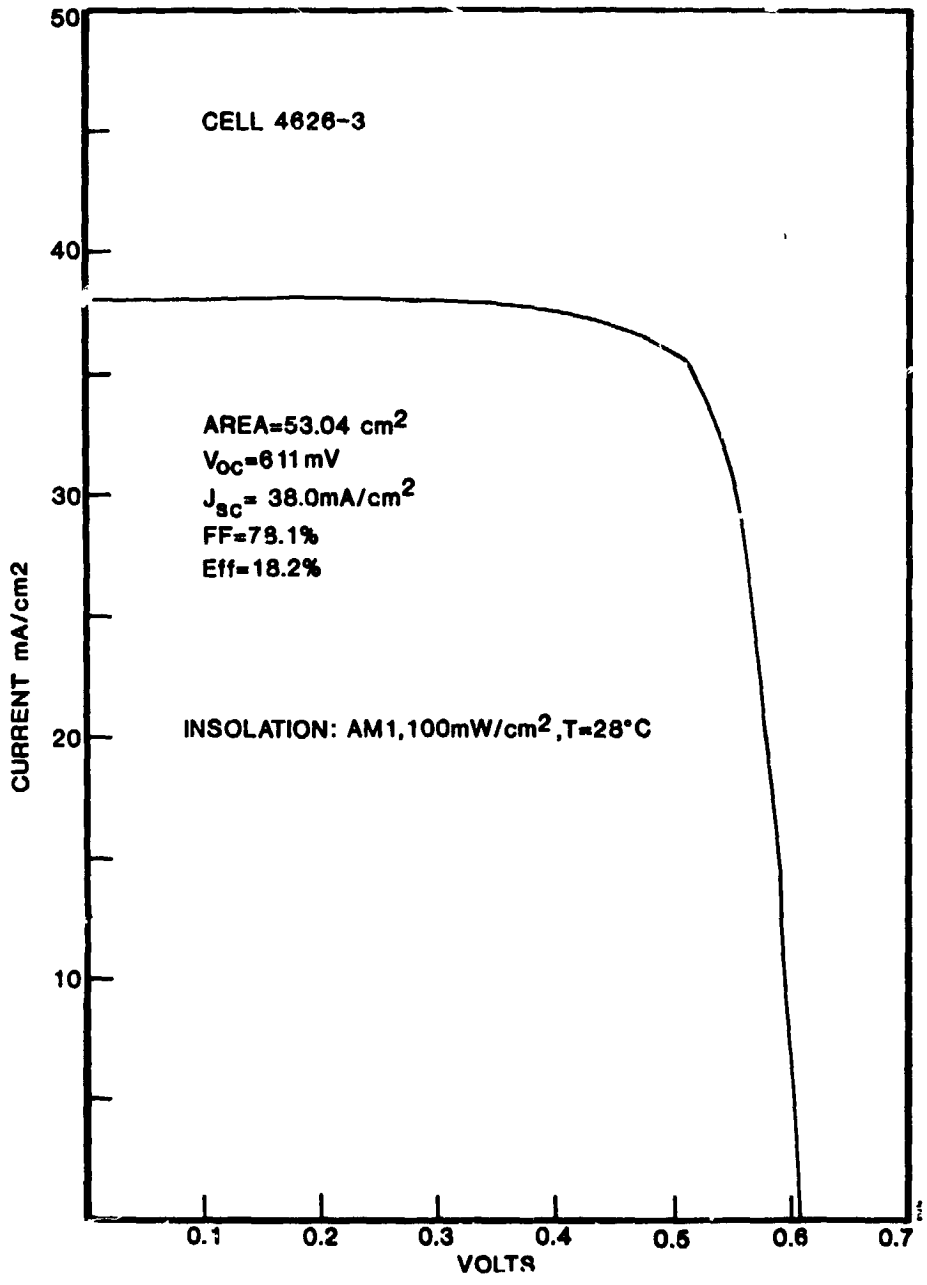
AVE. Eff = 15.4%

Options in Cell Design

- POLISHED VERSUS TEXTURE
  - –POLISHED YIELDS BEST SUB-BANDGAP REFLECTION
  - –TEXTURE YIELDS LOWER OVERALL REFLECTION
- LOW RESISTIVITY SILICON (<0.3ohm)
  - –HIGHER V_{oc} POSSIBLE
  - –REQUIRES PRECISE DOPING
- REDUCE THICKNESS, ADD BACK PASSIVATION
  - –YIELDS PROBLEMS?
  - –REQUIRES PRECISE DOPING
  - –OFFERS HIGHER EFFICIENCY


POLISHED BACK WITH SiO_2
POLISHED BACK
ETCHED BACK
FRONTS POLISHED
AND AR-COATED
Al ON BACKS
REFLECTANCE (%)
100
90
80
70
60
50
40
30
20
10
0
900 1000 1100 1200 1300 1400 1500 1600 1700 1800
WAVELENGTH (nanometers)


FRONTS TEXTURED
AND AR-COATED
Al ON BACKS
POLISHED BACK
ETCHED BACK
TEXTURED BACK
REFLECTANCE (%)
100
90
80
70
60
50
40
30
20
10
0
900 1000 1100 1200 1300 1400 1500 1600 1700 1800
WAVELENGTH (nanometers)


CELL 4626-3
AREA=53.04 cm2
Voc=611 mV
Jsc= 38.0mA/cm2
FF=79.1%
Eff=18.2%
INSOLATION: AM1,100mW/cm2,T=28°C
CURRENT mA/cm2
50
40
30
20
10
0.1
0.2
0.3
0.4
0.5
0.6
0.7
VOLTS

Furnace-Annealed Texture-Etched Large-Area Cells

V_{oc} (V)	Isc (A)	J_{sc} mA/cm^2	FF (%)	Eff (%)
0.610	2.001	37.7	77.5	17.8
0.611	2.018	38.0	78.1	18.2
0.606	1.986	37.4	77.5	17.6
0.602	1.933	36.5	78.1	17.1
0.610	2.016	38.0	78.4	18.2
0.604	1.965	37.1	77.7	17.4
0.610	2.011	37.9	77.7	18.0
0.609	2.028	38.2	77.5	18.1
0.609	2.014	38.0	76.5	17.7
0.609	2.013	38.0	77.9	18.0
0.611	2.026	38.2	77.8	18.2
0.606	1.964	37.0	77.8	17.5
0.608	1.985	37.4	76.9	17.5
0.607	2.018	38.0	76.2	17.6
0.611	2.033	38.3	77.4	18.1
0.607	1.980	37.3	77.4	17.5
0.609	2.022	38.1	77.5	18.0
0.609	2.011	37.9	78.3	18.1
0.610	2.029	38.2	77.0	18.0
0.607	1.984	37.4	77.5	17.6
0.601	1.930	36.4	76.6	16.7
0.603	1.959	36.9	76.2	17.0
0.608	1.997	37.6	77.4	17.7
0.003	0.031	0.6	0.6	0.4

NOTES: AREA=53cm^2. T=28 C. INSOLATION WAS SIMULATED AM1, 100mW/cm^2.

Projections for Module Made of Texture-Etched Cells

	POLISHED CELLS (ACTUAL)	TEXTURED CELLS (PROJECTED)
AVERAGE CELL EFFICIENCY	15.4%	17.7%
PACKING FACTOR (90%)	13.9%	15.9%
INTERCONNECT LOSSES (1.4%)	13.7%	15.7%

Conclusions

- BSR CELLS OFFER HIGH REFLECTION OF SUB-BANDGAP PHOTONS.
- ENCAPSULATED CELL EFFICIENCY OF 17.1% HAS BEEN ACHIEVED, WITH A 53cm^2 CELL (MEASURED AT JPL).
- MODULE EFFICIENCY OF 13.7% HAS BEEN ACHIEVED, NOCT IS 45°C (MEASURED AT JPL).
- TEXTURED CELL EFFICIENCY OF 18.2% HAS BEEN ACHIEVED WITH A 53cm^2 CELL.
- MODULE EFFICIENCY GREATER THAN 15% IS REALISTIC IN THE VERY NEAR FUTURE.