8.2.1 A VARIABLE-FREQUENCY LOCAL OSCILLATOR FOR THE FREQUENCY-HOPPING TECHNIQUE

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The frequency-hopping technique described elsewhere (STITT and BOWHILL, this volume) requires the use of a local oscillator whose output frequency may be rapidly and accurately changed by a fixed frequency increment. Such a device, capable of producing 16 different frequencies separated by 50 kHz over the range 35.02-35.77 MHz, has been build for the Urbana MST radar facility. The following paragraphs describe the design and construction of this device, which is illustrated by the block diagram of Figure 1.

A 5.00 MHz crystal oscillator provides a reference source for the synthe sizer. The oscillator output is divided by 100 to provide a precise 50 kHz input to the 16 separate NE564 Phae-Locked-Loops (PLLs). Each PLL, though locked to the same master oscillator, is set to run continually at its own unique frequency. Although the use of a battery of 16 PLLs may seem a bit extravagant, the NE564 chips employed are very inexpensive, and this approach avoids the problems with capture range and settling time that may occur when a single PLL is used to generate multiple frequencies.

A frequency synthesizer consisting of 16 separate oscillators connected to an analog multiplexer was also considered. Unfortunately, this brute force approach is quite expensive, as it requires the use of high quality oscillators. This is due to the sensitivity of the frequency-hopping technique to random variations in the operating frequencies of the oscillators; if these frequencies deviate by more than a few Hertz from their desired values, the frequency-hopping method simply does not work. The use of 16 separate PLLs, each locked to the same reference oscillator, helps to minimize this problem.

Returning to Figure 1, it may be seen that the local oscillator frequency generated at any given time is determined by the 16-to-1-line multiplexes. When the radar is operated in the frequency-hopping mode, this multiplexes is controlled through a parallel port by an Apple II+ microcomputer. A switch allows control of the multiplexer to transferred to a row of rocket switches on the front panel of the device. In this way, the local oscillator frequency may be fixed at a chosen value when the radar is operated in a more conventional mode.

The output frequency range of the synthesizer is beyond the maximum operating frequency of the NE564 PLL. Consequently, it is necessary to mix the PLL outputs with that of a 40.02 MHz oscillator in order to obtain the desired output frequencies. Since it is difficult to mix a squarewave due to the higher order harmonics present, the PLL outputs are filtered with a low-pass elliptic filter to ensure an approximately sinusoidal waveform before being mixed. The mixer output is then bandpass filtered in order to eliminate the undesirable harmonics produced by the mixing operation. Finally, the resulting signal is amplified by a pair of MWA 120 wideband hybrid amplifiers.

The frequency synthesizer illustrated in Figure 1 physically consists of 10 printed circuit boards inserted into a card cage. Eight of these boards, labeled PLL in Figure 1, contains two PLL circuits apiece. These cards are all identical except for the frequencies the individual PLLS are set to run at. One board (labeled FSO) contains the multiplexer and 5.00 MHz reference

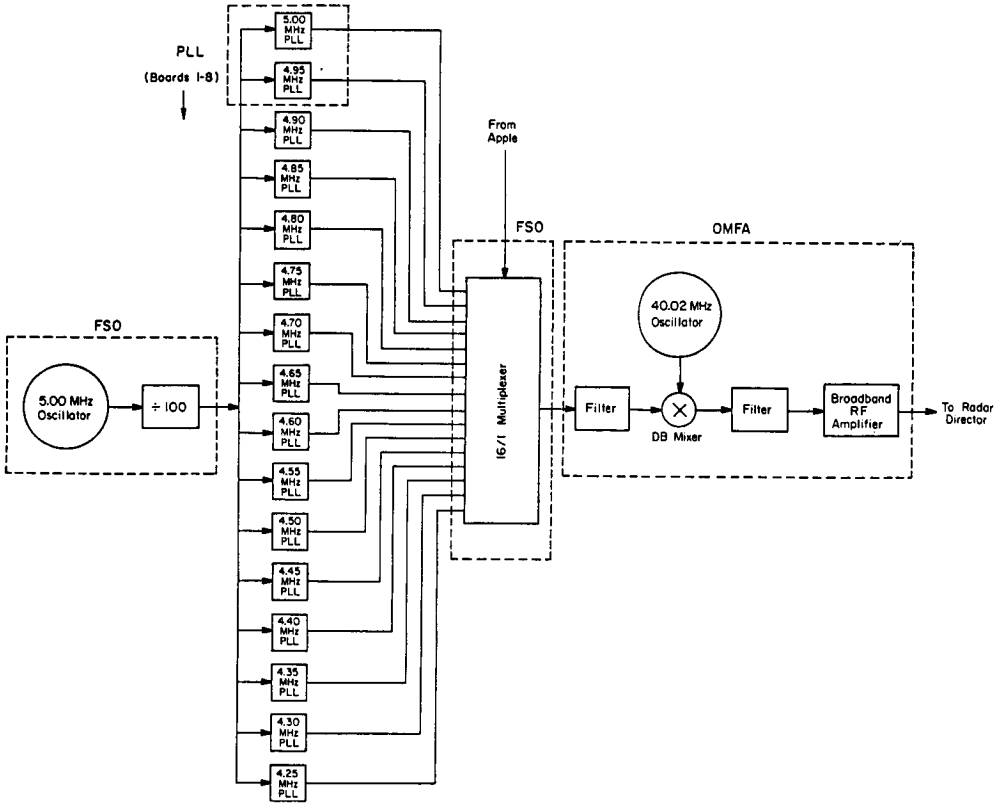

Figure 1. Implementation of the frequency synthesizer.

oscillator. The remaining board (labeled OMFA) contains the 40.02 MHz oscillator, mixer, filters, and amplifiers. The modular construction used for this synthesizer should simplify maintenance, and make it easier to change operating frequencies should that prove desirable in the future.

Figures 2 and 3 show spectrum analyser displays corresponding to the 35.77 MHz output of the frequency generator. Figure 2 indicates that there are no significant frequency components present other than those near the desired frequency. Figure 3, which expands the central peak in Figure 2, reveals that there are undesirable frequency components located $\pm$ 50 kHz and $\pm$ 100 kHz away from the 35.77 MHz component. These undesirable components, whose amplitudes are approximately 23 dB below the central peak, are apparently caused by the phase comparator section of the NE564 chip. If they prove troublesome, it will be necessary to use a different type of PLL.

ACKNOWLEDGEMENT

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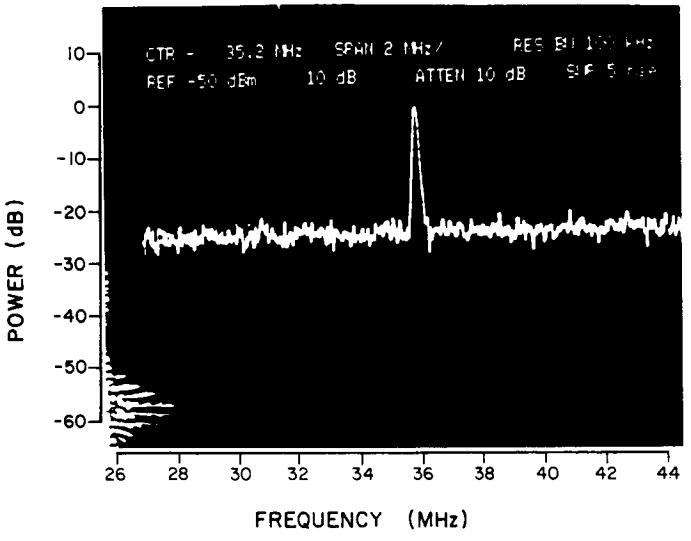

Figure 2. Spectrum analyser display of synthesizer output. Main peak is at 35.77 MHz. Vertical scale is 10 dB/ division, horizontal scale is 2 MHz/division.

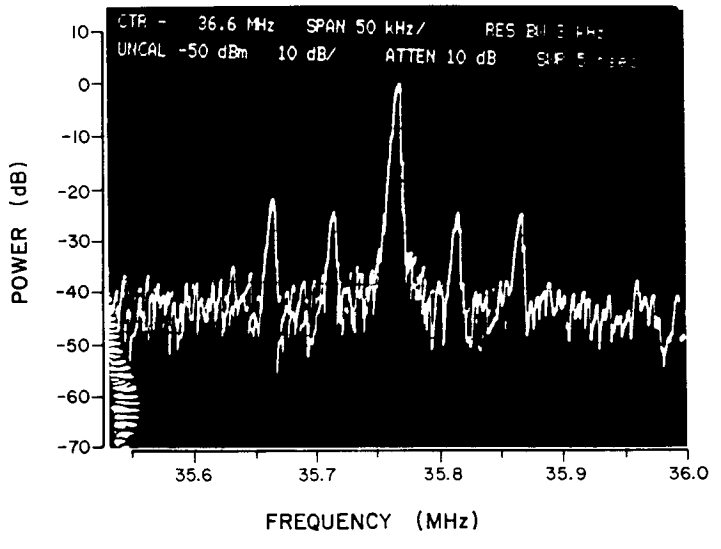

Figure 3. Same as Figure 2, except that the horizontal scale is 50 kHz/division.