RADARSAT HIGH THROUGHPUT SAR PROCESSOR DEVELOPMENT

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I. INTRODUCTION

MacDonald Dettwiler & Associates has been involved with the Canadian Radarsat (RSAT) project for a number of years. This included Phase A definition studies and for the past two years, Phase B ground station design and processor prototyping efforts. This paper describes the current baseline design for the SAR processing facility (SARDPF), its requirements and functional decomposition. This forms the context for then discussing the prototype SAR processor and extensions necessary to meet current ground station processing requirements.

II. GROUND PROCESSING FACILITY

The SARDPF is to be built in two phases. The first phase would have complete functionality but reduced throughout. This phase would be completed in time for the launch of ERS-1 and would be required to process and distribute imagery from an anticipated five minutes of SAR data per day. The second phase would upgrade the facility to accommodate the substantially greater RSAT processing load based on receiving 160 minutes of SAR data per day.

The facility is required to produce a variety of products for ERS-1 and RSAT including:

- raw data CCTS;
- full resolution single look imagery both detected and complex;
- high (25m) and low (50m) resolution multilook imagery in sensor coordinates; and
- high resolution precision (digital terrain model corrected) imagery in various map projections.

Turnaround varies from three hours to two weeks with fast turnaround low resolution imagery being the dominant product. These products are digitally transmitted to the Ice Information Centre for analysis on the MacDonald Dettwiler Ice Data Integration and Analysis System (IDIAS).

SAR data acquisition takes place remotely from the processing facility. Currently two data acquisition facilities (DAF's) are baselined: one at Ottawa (Gatineau) Ontario, and another at Fairbanks, Alaska. Acquired data is relayed to the SARDPF via communication satellite (ANIK).

Figure 1 shows a block diagram of the Ottawa DAF and the SARDPF. RSAT or ERS-1 DATA is received and buffered on HDDT. After the pass, the HDDT is rewound and replayed into the communication link at 1/4 of the real time rate. At the SARDP, the data is received and simultaneously recorded and processed (RSAT only). SAR processor output is buffered onto HDDT for subsequent precision correction and geocoding (MacDonald Dettwiler's Geocoded Image Correction System) and simultaneously fed to a subsampler to form a low resolution product.

Fast turnaround products are delivered to users via a digital transmission network. The remaining products (CCTs/film products) are delivered by post or courier.

III. PROTOTYPE PROCESSOR

The RSAT prototype processor was built using a VAX 750 host and a Motorola TASP 2080 array processor. All processing takes place within the TASP with no intermediate storage to disk. The TASP is a commercially available array processor that has a number of features that make it useful for SAR processing including:

- 40 bit complex word format (16 bits real, 16 bits imaginary, 8 bits common exponent);
- large internal memory (up to 64 M complex words);
- high speed I/O channel (15 Mbs); and
- single instruction multiple data architecture (up to 8 AUs).

The primary objectives of the prototyping effort were:

- to implement a significant subset of range-doppler SAR algorithm sufficient to demonstrate that the TASP was a suitable processing vehicle; and
- to refine timing estimates used in the design and sizing of the SARDPF Radarsat processor.

The range doppler algorithm was chosen because: it can accommodate both L- and C-band processing; it is well understood and successfully implemented (MacDonald Dettwiler SEASAT and GSAR processors). The algorithm was, however, adapted to continuous strip processing from scene processing. As a result several interesting implementation problems had to be addressed including:

- memory limitations and infeasibility of disk storage;
- continuous doppler centroid evaluation;
- potential processing block discontinuities due to centroid updates; and

- continuous processing parameter updates.

Input and output for the prototype was limited to that provided by high-speed 6250 bpi tape drives. Thus the TASP I/O channel was not exercised at rates anticipated in the SARDPR. This lack of testing was considered low risk and not cost effective for the prototyping stage.

Figure 2 shows the algorithm's implementation and partition of activities between host and AP. Multiple 'concurrent' processes on the VAX provide:

- operator command processing;
- CCT input and checking;
- FM rate estimation;
- Doppler centroid estimation;
- control parameter generation;
- host/AP data interchange;
- CCT output; and
- data logging.

Concurrent processes running on the TASP provide:

- input data assembly;
- data processing (both range and azimuth);
- centroid data extraction; and
- output data assembly.

Results to date indicate that image quality goals have been achieved and with optimization of TASP code (both application and executive) throughput goals are achievable.

IV. RADARSAT PROCESSOR

The SARDPF RADARSAT processor must be able to process data at 1/4 real time rates to meet requirements for short turnaround (3 hour) products as well as zero backlog processing (160 minutes received and processed per day).

Figure 3 shows the functional block diagram of such a processor based on multiple TASPs. The input subsystem performs input data unpacking and checking. Range compression is performed by the first bank of processors (AP1 to APN). The processed range lines are broken into M azimuth subswaths

and azimuth processed to imagery by the second bank of M processors. The bus arbitrator allows any processor of the first bank to transfer data to any processor of the second. The output subsystem buffers subswath imagery until blocks of complete range lines are ready for output. It also provides the host with intermediately processed data for doppler centroid evaluation.

V. SUMMARY

MacDonald Dettwiler has successfully undertaken work in the design and construction of a prototype high speed, continuous strip SAR processor of low development risk. The results of this effort are being included in the design of the Canadian ERS-1 and Radarsat SAR processing facility.

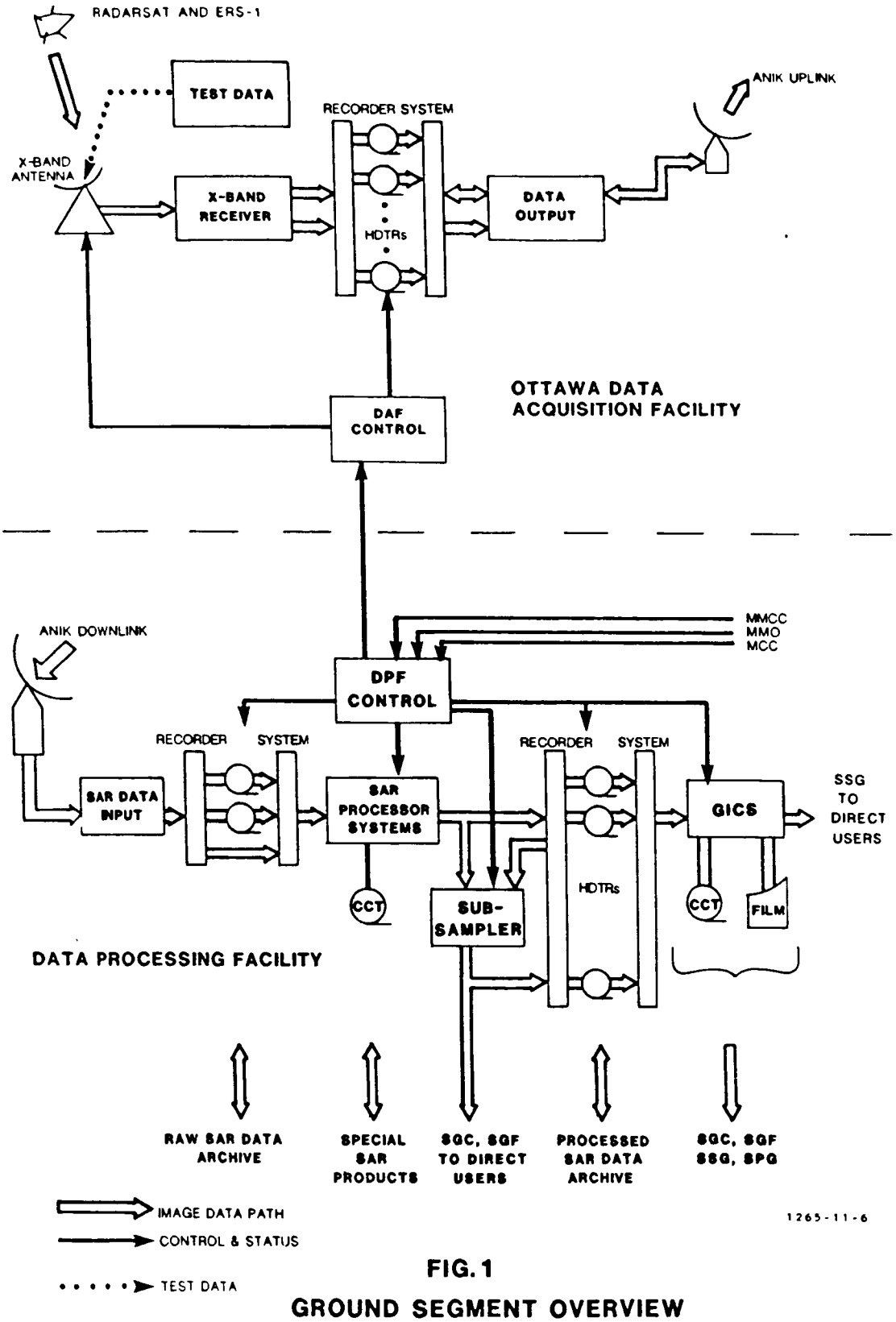

FIG. 1

GROUND SEGMENT OVERVIEW

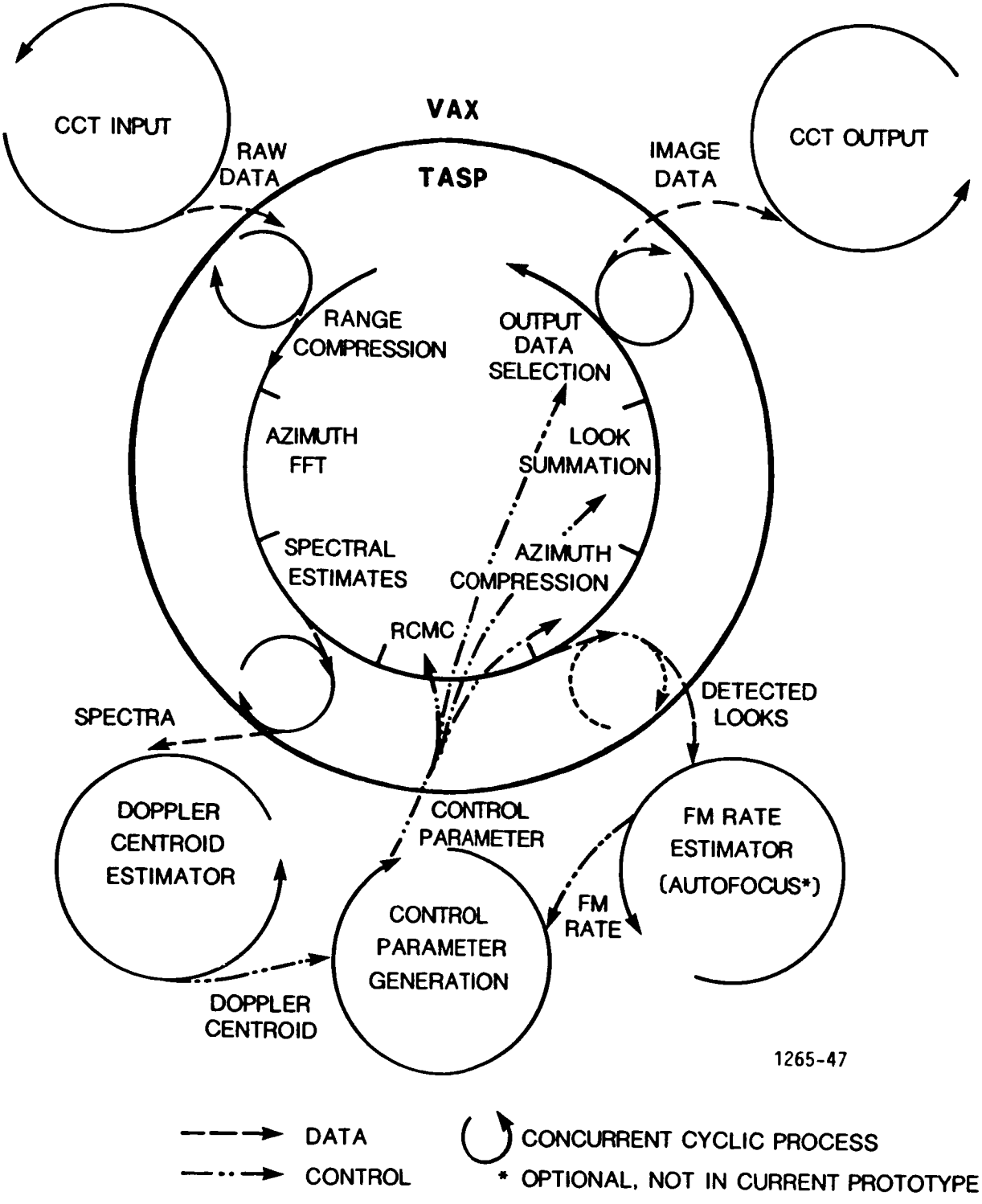

FIG. 2

RADARSAT PROTOTYPE PROCESSOR: ALGORITHM IMPLEMENTATION

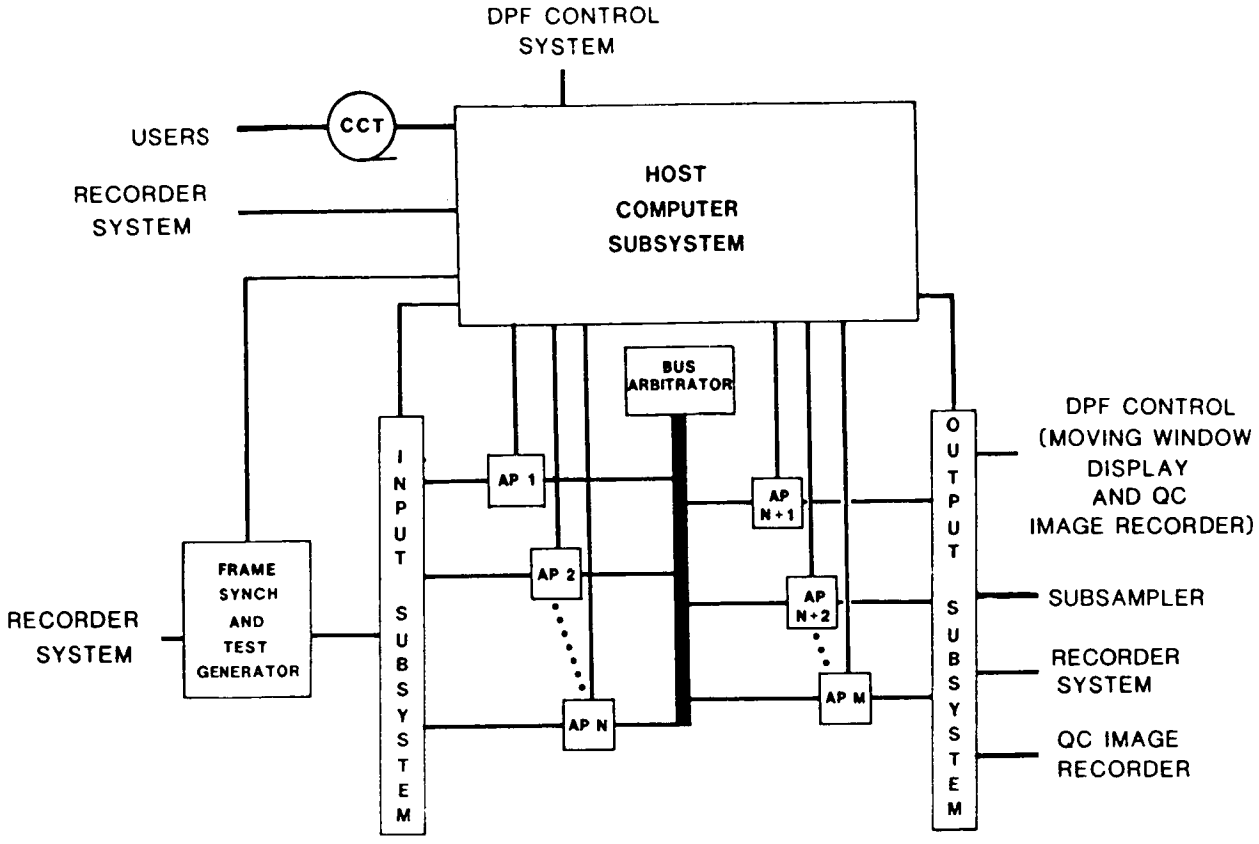

FIG. 3

RADARSAT SAR PROCESSOR

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