Phase-Ambiguity Resolution for QPSK Modulation Systems

Part II: A Method to Resolve the Phase-Ambiguity for Offset QPSK Modulation Systems

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ABSTRACT

Part II of this report presents a new method to resolve the phase-ambiguity for Offset QPSK modulation systems. When an Offset Quaternary Phase-Shift-Keyed (OQPSK) communications link is utilized, the phase ambiguity of the reference carrier must be resolved. At the transmitter, two different unique words are separately modulated onto the quadrature carriers. At the receiver, the recovered carrier may have one of four possible phases, 0°, 90°, 180°, or 270°, referenced to the nominally correct phase. The IF portion of the channel may cause a phase-sense reversal, i.e, a reversal in the direction of phase rotation for a specified bit pattern. Hence, eight possible phase relationships (the so-called eight ambiguous phase conditions) between input and output of the demodulator must be resolved. Using the In-phase (I)/ Quadrature (Q) channel reversal correcting property of an OQPSK Costas loop with integrated symbol synchronization, four ambiguous phase conditions are eliminated. Thus, only four possible ambiguous phase conditions remain. The errors caused by the remaining ambiguous phase conditions can be corrected by monitoring and detecting the polarity of the two unique words. The correction of the unique word polarities results in the complete phase-ambiguity resolution for the OQPSK system.

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I. INTRODUCTION AND BACKGROUND

Part I of this report presented a review of the current phase-ambiguity resolution techniques for the four-phase PSK coherent modulation systems. Part I contained sufficient detail to serve as a background for the study of this part, Part II.

In this part, a technique for resolving the phase-ambiguity of an Offset Quaternary Phase-Shift-Keyed (OQPSK) communication system is investigated in detail. This report is directed toward a method and apparatus for resolving the phase-ambiguity in the OQPSK system.

A well-known problem associated with coherent four-phase PSK communications systems is that of the phase ambiguities at the receiver. The phase-ambiguity in a four-phase PSK system results from the carrier recovery circuits at the receiver locking onto a wrong phase, other than the reference phase of the received carrier. For a four-phase PSK system, there are eight possible ambiguous phase conditions in the recovered carrier that can affect the data in the two parallel channels (so-called quadrature channels) of the PSK demodulator. Here, there are four phase ambiguities associated with the carrier phase without the phase rotation direction ambiguity, and there are four others associated with the carrier phase for the phase rotation direction ambiguity (see Table 1). It should be mentioned here that the phase rotation direction ambiguity phenomenon can occur at the IF portion of the channel if the relationship between the transmit local frequency and receive local frequency is not known. A detailed description of this phenomenon is described in Reference 6. Since the demodulator output of the four-phase PSK system has two channels (the received In-phase (I_R) and the received Quadrature (Q_R) channels), the output data corresponds to the transmitted channels I_T and Q_T. The eight possible ambiguous phase conditions are any combinations of the following three errors:

(a) Type 1 error: I_R = I_T inverted, or I_R = Q_T inverted

(b) Type 2 error: Q_R = Q_T inverted, or Q_R = Q_T inverted

(c) Type 3 error: I_R and Q_R are switched or reversed, e.g.
   I_R = Q_T or I_R = Q_T inverted, and Q_R = I_T or Q_R = I_T inverted.

Only one of the eight combinations is correct, that is, the received channel I_R output containing the true channel I_T data, i.e. I_R = I_T, and the received Q_R channel containing the true channel Q_T data, i.e. Q_R = Q_T.

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There are several techniques presently employed for resolving the phase-ambiguity of four-phase PSK systems (see Ref. 1 for a detailed description of these techniques). The widely used technique is differential encoding/decoding. The major disadvantage of this method is that it results in the double error phenomenon. This phenomenon can cause serious degradation in the detection performance of the transmitted sync markers. Furthermore, the differential coding technique can (1) result in a degradation of bit error rate performance, and (2) make data decoding techniques more complex. One particularly well-known technique for resolving the phase-ambiguity of four-phase PSK systems is described and claimed in U.S. Patent No. 3736507 (Ref. 4). In this technique, there are eight possible combinations of the three possible errors mentioned above; each combination uniquely defines the phase ambiguity. This particular technique utilizes the two unique words that are separately modulated onto the quadrature channels at the transmitter. Thus, each error appearing in the two data channels of the four-phase PSK modulator is uniquely defined by a particular phase error. This technique proposes that the errors associated with eight possible ambiguous phase conditions can be corrected by detecting the true or complement of two unique words that are separately modulated onto the two quadrature channels at the transmitter. Since there are eight possible ambiguous phase conditions, this design requires a rather complicated circuitry for the unique-word detector to resolve the phase-ambiguity. Another technique was described in Reference 5. The technique described in this paper proposed to resolve the eight possible ambiguous phase conditions for OQPSK systems by monitoring and detecting the two unique words using the parallel-to-serial conversion clock. This means that proper timing between the two unique words has to be known precisely for this scheme to work.

It is obvious that in OQPSK modulation systems, the problem of phase-ambiguity can be resolved by the techniques mentioned above. However, when the unique-word detection techniques are used, the demodulator and the unique-word detector in the OQPSK receiver can be redesigned to achieve better performance while minimizing the complexity of the receiver by (1) digital implementation of a Costas loop in the carrier recovery circuitry, (2) removal of the redundant circuits of the previous design, and (3) elimination of the timing dependent on the parallel-to-serial conversion clock.

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II. DESCRIPTION OF THE NEW METHOD FOR
THE PHASE-AMBIGUITY RESOLUTION

This report presents a new design that is related to an OQPSK communication system. The following description is presented to enable any person skilled in the art to make and use this new design. Various modifications to the preferred embodiment will be readily apparent to those skilled in the prior art. This design is intended to be used for any communication systems which utilize OQPSK modulation.

A block diagram of a conventional OQPSK modulator/demodulator is illustrated in Figure 1. The NRZ (Non-Return-to-Zero) data stream D_T entering the modulator is converted by encoding and serial-to-parallel converter 1 into two separate data trains I_T and Q_T. I_T is the in-phase data stream, and the other is quadrature-phase Q_T, with the symbol rate R_S equal to half that of the incoming bit rate R_b. For the OQPSK modulation system discussed here, the Q_T data stream is offset with respect to the I_T data by delaying it by an amount equal to the incoming signal bit duration T_b. Thus, if T_S is the symbol duration, then the delay is $(T_S/2)$.

The relationship between the I_T and Q_T data streams and the input data stream D_T is shown in Figure 2. The timing of the incoming data stream is controlled by the input clock C_T. The timing offset between I_T and Q_T channels is accomplished by the delay line 2. Both I_T and Q_T data streams are separately applied to multipliers 3 and 6, respectively. The second input to the multiplier 3 is the carrier signal $\cos(\omega_c t)$, and the second input to the multiplier 6 is the carrier signal shifted by exactly 90° (i.e. $\sin(\omega_c t)$).

The output of each multiplier is a biphase PSK signal. The output of multiplier 3 has phase 0° or 180° relative to the carrier phase, depending on whether $I_T = 0$ or $I_T = 1$ (also symbolized respectively by $-I_T$ or I_T). The output carrier from multiplier 6 will have the phase of either 90° or 270° relative to the carrier phase, depending on whether $Q_T = 0$ or $Q_T = 1$ (also symbolized respectively by $-Q_T$ or Q_T). The output multipliers are then summed in a linear adding means 7 to give an OQPSK signal. This signal is then transmitted via any suitable transmission medium to a receiver. The noise introduced in the medium is illustrated by a linear adding means 8a. At the receiver, the demodulator performs the inverse operation of the modulator and generates the output data stream $D_R \approx D_T$.

For coherent OQPSK systems, a coherent carrier must be recovered from the received signal, and a coherent clock must be reconstructed from the demodulated data waveform. A conventional OQPSK demodulator is shown in Figure 1, and includes balanced

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demodulators **10** and **13**, carrier recovery circuit **11**, clock recovery circuit **16**, low-pass filters **14** and **15**, detectors **17** and **18** for bit streams recovery, delay line **19**, and decoder and parallel-to-serial convertor **20**.

The received data stream D_R is not always equal to the transmitted data stream D_T because of noise and phase ambiguities in the phase of the recovered carrier. If the carrier recovery circuit can lock on the reference phase of the received carrier, then $I_R \approx I_T$, $Q_R \approx Q_T$, and hence $D_R \approx D_T$. However, for the received data without phase rotation direction ambiguity, the received carrier has four possible phases relative to the reference carrier phase; the receiver can lock on any of the four phases. For received data with phase rotation direction ambiguity, again, there are four additional possible phases relative to the reference carrier, and the receiver can lock on any of the eight phases associated with it. The effect of an incorrect recovered-carrier phase on the demodulated data is shown in Table 1.

TABLE 1. THE RELATIONSHIPS BETWEEN THE TRANSMITTED AND
RECEIVED DATA FOR THE OQPSK SYSTEM DESCRIBED
IN FIGURE 1

CARRIER PHASE ERROR (DEGREE)	RECEIVED DATA WITHOUT PHASE ROTATION DIRECTION AMBIGUITY (NORMAL SENSE)		RECEIVED DATA WITH PHASE ROTATION DIRECTION AMBIGUITY (REVERSE SENSE)	
	I_R	Q_R	I_R	Q_R
0	I_T	Q_T	Q_T	I_T
90	$-Q_T$	I_T	I_T	$-Q_T$
180	$-I_T$	$-Q_T$	$-Q_T$	$-I_T$
270	Q_T	$-I_T$	$-I_T$	Q_T

NOTE: The negative sign indicates the complement of the data.

From this table, it can be seen that for each case (normal or reverse sense) the locked-in phase may be any one of four possible phases. Thus, the resolution of the eight possible relationships between the transmitted and the received phase(s) is a formidable problem in OQPSK systems. Furthermore, this

table reveals that for received data without phase rotation direction ambiguity, a Type 3 error occurs when the carrier phase error is either at 90° or at 270°. For received data with phase rotation direction ambiguity, a Type 3 error occurs when the carrier phase is either at 0° or at 180°.

As described earlier, these eight unique combinations uniquely define the phase ambiguities, which are combinations of the three specific types of errors mentioned above, namely Type 1, Type 2, and Type 3. The classification of the phase ambiguities into three definable errors allows the concepts of (1) integrated carrier loop/symbol synchronizer, and (2) unique-word detection to be applicable to an OQPSK system for resolving the phase ambiguities. Four errors can be corrected by utilizing an integrated carrier loop/symbol synchronizer using a digital Costas loop with matched arm filters. The remaining four errors are corrected by utilizing the unique-word detection technique.

Generalized block diagrams of the OQPSK modulator and demodulator with phase-ambiguity correction in accordance with the teachings of the present technology are shown in Figures 3 and 4, respectively. As illustrated in Figure 3, the block diagram for this modulator is very similar to the conventional OQPSK modulator shown in Figure 1. The only difference is the unique code-word generators **21, 22** for generating and inserting the unique words I_u and Q_u into the quadrature channels **25, 26**. Each of these unique words has length N, and (I_u, Q_u) is periodically clocked by C_T into the data streams I_T and Q_T, respectively. It should be mentioned here that the synchronization markers can be used as the unique code words.

Through recent developments in digital technology, digital implementation of the Costas loop is becoming increasingly more attractive. Advantages of the digital Costas loop include its relative insensitivity to temperature variations and aging, and the programmability of its loop parameters (such as loop gain and loop filter time constants, Ref. 3). Utilizing this technology, an integrated carrier/symbol synchronization system based on a digital decision feedback is proposed for carrier recovery loop. A new block diagram for the OQPSK demodulator is depicted in Figure 4. The new components added in this demodulator are: A/D converters **38, 39**, and the phase-ambiguity resolver **44**. Furthermore, the carrier recovery and clock recovery loops are replaced by integrated carrier loop/symbol synchronizer **40**. In operation, the integrated carrier loop/symbol synchronizer **40** using digital Costas loop with matched arm filters will be responsible for correcting two errors due to Type 3 (for normal sense) and two other errors due to Types 1 and 2 (for reverse sense). The phase-ambiguity resolver **44** will correct the remaining four errors.

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A simple example of the integrated carrier loop/symbol synchronizer loop is illustrated in Figure 5. This figure shows details of the carrier recovery loop structure. It also reveals how the carrier phase and symbol synchronization can be derived jointly. The illustrated carrier recovery loop comprises in-phase accumulate and dump circuits 45a, 45b, quadrature accumulate and dump circuits 47a, 47b, hard limiters 49 and 52, delay lines 51 and 55, symbol synchronizer 50, multipliers 53 and 54, linear adder 56, and loop filter 57.

The sampled baseband signals $I(n)$ and $Q(n)$ (outputs of the in-phase and quadrature A/D converters 38 and 39, respectively) are routed to the in-phase and quadrature accumulators 46 and 48, respectively. It is noted here that the in-phase accumulator 46 consists of the accumulate and dump circuits 45a, 45b, and the quadrature accumulator consists of the accumulate and dump circuits 47a, 47b. The in-phase accumulator 46 is synchronized with the in-phase data stream, and the quadrature accumulator is with the quadrature data stream. The in-phase accumulator 46 produces two signals, $I_i(n)$ and $I_q(n)$, while the quadrature accumulator produces $Q_q(n)$ and $Q_i(n)$.

The estimates of symbol polarity $\hat{d}_1(n)$ and $\hat{d}_2(n)$ for the in-phase and quadrature channels, respectively, are produced by passing $I_i(n)$ and $Q_i(n)$ through the hard limiters 49 and 52, respectively. The in-phase estimate of the symbol polarity is used as the feedback signal to control the timing output of the symbol synchronizer 50. Also, both $\hat{d}_1(n)$ and $\hat{d}_2(n)$ are separately applied to the in-phase and quadrature multipliers 53, 54, respectively.

The second input to the in-phase multiplier 53 is the output of accumulate/dump circuit 45b, and the second input to the quadrature multiplier 54 is the output of accumulate/dump circuit 47a. The output of in-phase multiplier 53 is delayed by the delay line 55. The outputs of the delay line 55 and quadrature multiplier 54 are added by a linear adder 56 to produce tracking error signal $e(n)$. After filtering by the loop filter 57 the error signal is fed back to the local oscillator 33 (Numerical Controlled Oscillator, NCO, see Figure 4), closing the phase-locked loop. A detailed operation of this carrier tracking loop has been described in Reference 2.

It has been shown in Reference 2 that for carrier loop bandwidth (B_L)-to-symbol synchronization loop bandwidth (B_S) ratio much greater than one, i.e., $(B_L/B_S) \gg 1$, this carrier tracking loop can avoid the lock points at 90° and 270°, hence automatic I/Q channel reversal correction. This means that the proposed carrier tracking loop can correct two errors caused by Type 3 for received data without phase rotation, and two additional errors caused by Types 1 and 2 for received data with

phase rotation. A ratio of $B_L/B_S \geq 10$ has proved that the loop can avoid the lock points at 90° and 270° successfully. Since the proposed carrier tracking loop can avoid 90° and 270° lock points, the relationships between the transmitted and received data for the system described in Figures 3 and 4 will be different from that shown in Table 1. For this case, the effect of an incorrect recovered-carrier phase on the demodulated data is shown in Table 2.

TABLE 2. THE RELATIONSHIPS BETWEEN THE TRANSMITTED AND
RECEIVED DATA FOR THE OQPSK SYSTEM WITH PHASE
ROTATION DIRECTION AMBIGUITY

CARRIER PHASE ERROR (DEGREE)	RECEIVED DATA WITHOUT PHASE ROTATION DIRECTION AMBIGUITY (NORMAL SENSE)		RECEIVED DATA WITH PHASE ROTATION DIRECTION AMBIGUITY (REVERSE SENSE)	
	I_R	Q_R	I_R	Q_R
0	I_T	Q_T	Q_T	I_T
180	$-I_T$	$-Q_T$	$-Q_T$	$-I_T$

Translating the above relationships into the effects they create on the demodulated data in the in-phase and quadrature channels, it can be seen that there remain only three errors caused by the phase-ambiguity, and that these three errors are the three unique combinations of the three types of errors mentioned previously. The three definable errors are (1) $I_R = -I_T$, and $Q_R = -Q_T$; or (2) $I_R = Q_T$, and $Q_R = I_T$; or (3) $I_R = -Q_T$, and $Q_R = -I_T$.

The remaining three errors can be corrected by the phase-ambiguity resolver **44**. A complete resolution of the phase-ambiguity is accomplished by correcting these three errors. These errors are corrected by monitoring and detecting the unique words I_u and Q_u in the quadrature channels. If $-I_u$ and $-Q_u$ are detected in the I and Q channels, respectively, this indicates that the data in these channels are inverted. The error can be corrected by inverting the channel outputs prior to serializing the data into D_R. Similarly, if $-Q_u$ and $-I_u$ are detected in the I and Q channels, respectively, the data in both channels should be inverted and reversed. Using this concept, the block diagram of the phase-ambiguity resolver is described in Figure 6b. The illustrated phase-ambiguity resolver comprises invertors **58b**, **59b**, **60b**, gating means **61b**, **62b**, **63b**, parallel-to-serial converter **64b**, flip-flop circuits **65b**, **66b**, **72**, cross-coupling gate **67b**, I_u correlator **69b**, Q_u correlator **70b**, shift register **71b**, and decoding matrix **68b**.

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In normal operation, the I_R and Q_R data streams are fed through gating means **61b** and **62b**, respectively, to combine the data by parallel-to-serial converter **64b**, to produce an output data stream D_R in which an I_R bit precedes the Q_R bit. Each of the gating means **61b** and **62b** is adapted to pass the data directly or after inversion, by invertors **58b** and **59b**, to the parallel-to-serial converter. Control of gating means **61b** and **62b** is accomplished via the outputs of the flip-flop circuits **65b** and **66b**, respectively. The ouput data stream D_R is also applied to the shift register **71b** which has 2N stages (N is the length of the unique code word).

Consider the first two combinations of Table 2 for which $I_R = I_T$, $Q_R = Q_T$, and $I_R = -I_T$, $Q_R = -Q_T$. For these two combinations, the order of the bits in the output data stream D_R is correct, i.e., I_{T0} precedes Q_{T0} by one bit, and so on. The error occurs when both of the data streams are inverted. Let time $t = t_0$ be defined as the time when the shift register **71b** is fully loaded with two unique words I_u and Q_u interlaced, as shown in Figure 6b. Because the stages of correlators **69b** and **70b** are connected to every other stage of shift register **71b**, at time t_0 only the Q_u correlator **70b** is looking at its corresponding unique word. The Q_u correlator will provide either a logic output Q_u on the plus (+) output line or $-Q_u$ on the minus (−) output line. At time $t = t_{-1}$ (one bit earlier), the I_u correlator **69b** will detect the I_u unique word and produce either a logic output I_u on the plus (+) output line or $-I_u$ on the negative (−) output line. If the correlators **69b** and **70b** detect I_u and Q_u respectively, no action is taken. If the $I_R = -I_T$ and $Q_R = -Q_T$, the correlators **69b** and **70b** will detect $-I_u$ and $-Q_u$, respectively, and send the representative logic signals through cross-coupling gate **67b** and toggle flip-flop circuits **65b** and **66b**. The changes in outputs from flip-flop circuits **65b** and **66b** will reverse the state of the gates **61b** and **62b**, and pass the data streams $-I_R$ and $-Q_R$, respectively, to parallel-to-serial converter **64b**.

Consider the third case in Table 2 for which $I_R = QT$, and $Q_R = I_T$. For this combination, the order of the bits in the output data stream D_R is not correct, and so on, Q_{T0} precedes I_{T0} by one bit, etc. In this case, the correlators **69b** and **70b** will detect Q_u followed one bit later by I_u. The decoding matrix will generate a "reverse I_R & Q_R" control signal. Flip-flop **72** will be toggled causing a state reversal of the gate **63b**, and pass the inverted recovered-clock pulses to converter **64b**. This causes a reversal of the data channels at the output of the converter **64b**.

Consider the last case in Table 2 for which $I_R = -QT$, and $Q_R = -I_T$. For this combination, both the data channels are inverted and then reversed. Again the correlators **69b** and **70b** will detect $-Q_u$, followed one bit later by $-I_u$, and send the representative logic signals through cross coupling gate **67b**

while toggling flip-flop circuits **65b** and **66b**. At the same time the decoding matrix will also generate a "reverse I_R & Q_R" control signal. Flip-flop **72** will be toggled, causing a reversal of the data channels at the output of converter **64b**. The in-phase and quadrature data channels must be inverted to be correct, are passing through gates **62b** and **61b**, respectively, rather than gates **61b** and **62b**, respectively, and thus the "invert I_R" control signal must toggle flip-flop **66b** rather than **65b**, and an "invert QR" control signal must toggle flip-flop **65b** rather than **66b**. This is taken care of by the cross-coupling gate **67b**. The switching of flip-flop **72** causes a reversal in the connections between the two input terminals and the two output terminals of the cross-coupling gate **67b**.

The block diagram of the decoding matrix **68b** is shown in Figure 7b. The decoding matrix illustrated in this figure will be responsible for providing (1) a proper clock signal to the data decoder (if the data is encoded) and to the parallel-to-serial converter, and a frame-sync signal for the subsequent data output; and (2) a reverse I & Q control signal. The embodiment comprises one-bit-delay lines **73** and **74**, AND gates **75**, **76**, **77** and **78**, OR gates **79** and **80**. The logic shown in this figure is explained by the truth table shown in Table 3.

TABLE 3. TRUTH TABLES FOR THE LOGIC SHOWN IN FIGURE 7b

I_u	Q_u	O_1
0	0	0
0	1	0
1	0	0
1	1	1

$-I_u$	$-Q_u$	O_2
0	0	0
0	1	0
1	0	0
1	1	1

I_u	Q_{uD}	O_3
0	0	0
0	1	0
1	0	0
1	1	1

$-I_u$	$-Q_{uD}$	O_2
0	0	0
0	1	0
1	0	0
1	1	1

O_3	O_4	REVERSE I_R & Q_R
0	0	0
0	1	1
1	0	1
1	1	1

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TABLE 3. TRUTH TABLES FOR THE LOGIC SHOWN IN FIGURE 7b
(CONTINUED)

O_1	O_2	O_3	O_4	SYNC PULSE
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

In order to ensure a proper lock in the input/output connections of the cross coupling gate 67b (Figure 6b), a short delay line is provided at the inputs to cross-coupling gate 67b.

If the relationship between the transmit local frequency and the receive local frequency is provided, the phase rotation direction ambiguity can be avoided. Table 4 shows the relationships between the transmitted and received data for this case.

TABLE 4. RELATIONSHIPS BETWEEN THE TRANSMITTED AND RECEIVED DATA FOR THE OQPSK SYSTEM WITHOUT PHASE ROTATION DIRECTION AMBIGUITY

CARRIER PHASE ERROR (DEGREE)	RECEIVED DATA WITHOUT PHASE ROTATION DIRECTION AMBIGUITY (NORMAL SENSE)	
	I_R	Q_R
0	I_T	Q_T
180	$-I_T$	$-Q_T$

Based on these relationships, the phase-ambiguity correction system can be redesigned, and the block diagram for this system without phase rotation direction ambiguity is shown in Figure 6a. The illustrated phase-ambiguity correction system comprises invertors **58a**, **59a**, gating means **61a**, **62a**, parallel-to-serial converter **64a**, flip-flop circuits **65a**, **66a**, I_u correlator **69a**, Q_u correlator **70a**, shift register **71a**, and sync generator **68a**. Since there are only two combinations (hence only one error), the operation of this phase-ambiguity resolver is very simple.

In normal operation, the I_R and Q_R data streams are fed through gating means **61a** and **62a**, respectively, to combine the data by parallel-to-serial converter **64a**, to produce an output data stream D_R in which I_R bit precedes the Q_R bit. Each of the gating means **61a** and **62a** is adapted to pass the data directly or after inversion by invertors **58a** and **59a**, to the parallel-to-serial converter. Control of gating means **61a** and **62a** is accomplished via the outputs of the flip-flop circuits **65a** and **66a**, respectively. The output data stream D_R is also applied to the shift register **71a** which has 2N stages (N is the length of the unique codeword).

Consider the (only) error shown in the second combination of Table 4 for which $I_R = -I_T$, and $Q_R = -Q_T$. For this combination, the order of the bits in the output data stream D_R is correct, i.e., I_{T0} precedes Q_{T0} by one bit, and so on. The error occurs when both of the data streams are inverted. Let time $t = t_0$ be defined as the time when the shift register **71a** is fully loaded with two unique words, I_u and Q_u, interlaced as shown in Figure 6a. Because the stages of correlators **69a** and **70a** are connected to every other stage of shift register **71a**, at time t_0 only the Q_u correlator **70a** is looking at its corresponding unique word.

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The Q_u correlator will provide either a logic output Q_u on the plus (+) output line or $-Q_u$ on the minus (-) output line. At time $t = t_{-1}$ (one bit earlier), the I_u correlator **69a** will detect the I_u unique word and produce either a logic output I_u on the plus (+) output line or $-I_u$ on the negative (-) output line. If the correlators **69a** and **70a** detect I_u and Q_u, respectively, no action is taken. If $I_R = -I_T$, and $Q_R = -Q_T$, the correlators **69a** and **70a** will detect $-I_u$ and $-Q_u$, respectively, and send the representative logic signals to toggle flip-flop circuits **65a** and **66a**. The changes in outputs from flip-flop circuits **65a** and **66a** will reverse the state of the gates **61a** and **62a**, and pass the data streams $-I_R$ and $-Q_R$, respectively, to parallel-to-serial converter **64a**.

A simple example of the sync generator **68a** is illustrated in Figure 7a. The embodiment comprises AND gates **75a**, **76a**, and OR gate **79a**. The logic is self-explanatory.

III. SUMMARY

A new technique for resolving the phase-ambiguity in OQPSK communications systems using the digital Costas loop with integrated symbol synchronizer, and the unique-word (or sync-marker) detection method is presented. The purposes of the design presented in this report are (1) to enhance the performance of the carrier recovery subsystem, (2) to minimize the complexity of an OQPSK receiver by removing the redundant circuits from the previous design, and (3) to eliminate the timing dependent on the parallel-to-serial conversion clock.

In accordance with the present technique described in the previous sections, an OQPSK digital Costas loop with integrated symbol synchronization and a unique-word (or sync-marker) detector are provided for digital communications systems that utilize OQPSK modulation.

It has been discovered that there are eight possible combinations of the three possible errors, Type 1, Type 2, and Type 3 error, mentioned above. There are four possible combinations of errors associated with Type 1 and Type 2 error. The remaining four combinations are with the Type 3 error. The technique proposed here will not identify the phase error of the recovered coherent carrier that caused the errors, but correct the errors caused by the phase ambiguities. In the preferred embodiment, the OQPSK receiver is implemented by an integrated carrier loop/symbol synchronizer using a digital Costas loop with matched arm filters, and a unique-word detector. The use of digital Costas loop allows the novel communication techniques to be implemented in the programmable digital processor while the loop gain and loop filter time constants are programmable. The integrated carrier loop/symbol synchronizer is properly designed such that two of the errors caused by Type 3 (I/Q channel reversal due to the phase ambiguities) can be corrected in the carrier tracking loop. For OQPSK systems with phase rotation direction ambiguity, the use of this loop can correct two additional errors caused by Type 1 and 2. Hence, four errors can be corrected by using this carrier tracking loop. The remaining errors are corrected by using the unique-word detector. Since only four possible combinations of errors remain, the unique-word detector can be designed with a very simple circuitry using invertors, AND gates, OR gates, and the like.

## IV. CONCLUSIONS AND RECOMMENDATION

Based on the above description, the following conclusions can be reached:

1. The eight possible ambiguous phase conditions associated with OQPSK systems can be resolved by using (a) the digital Costas loop with integrated symbol synchronization, and (b) the unique-word detection technique.

2. The use of digital Costas loop with integrated symbol synchronization for the carrier tracking loop will resolve four possible ambiguous phase conditions caused by the recovered carrier being at the wrong phase(s).

3. The use of the unique-word detection technique will resolve the remaining four ambiguous phase conditions.

4. The use of the OQPSK digital Costas loop with integrated symbol synchronization for the carrier recovery loop will (a) improve the carrier tracking performance at low signal-to-noise ratio (Ref. 2); (b) make the carrier tracking loop less sensitive to temperature variations and aging; and (c) allow loop parameters (such as loop gain and loop filter time constants) to be programmable (Ref. 3).

5. As compared to the prior claims in Reference 4, the complexity of the phase-ambiguity resolver described here is reduced by half.

6. As compared to the previous design described in Reference 5 the phase-ambiguity resolution technique described here eliminates the timing dependent on the parallel-to-serial conversion clock.

Since the proposed technique has many advantages as compared to the previous techniques, it is recommended that the CCSDS adopt this technique as a standard method for the phase-ambiguity resolution for future OQPSK communications systems.

V. REFERENCES

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FIGURE 1. BLOCK DIAGRAM OF A PRIOR ART OQPSK MODULATOR/DEMODULATOR
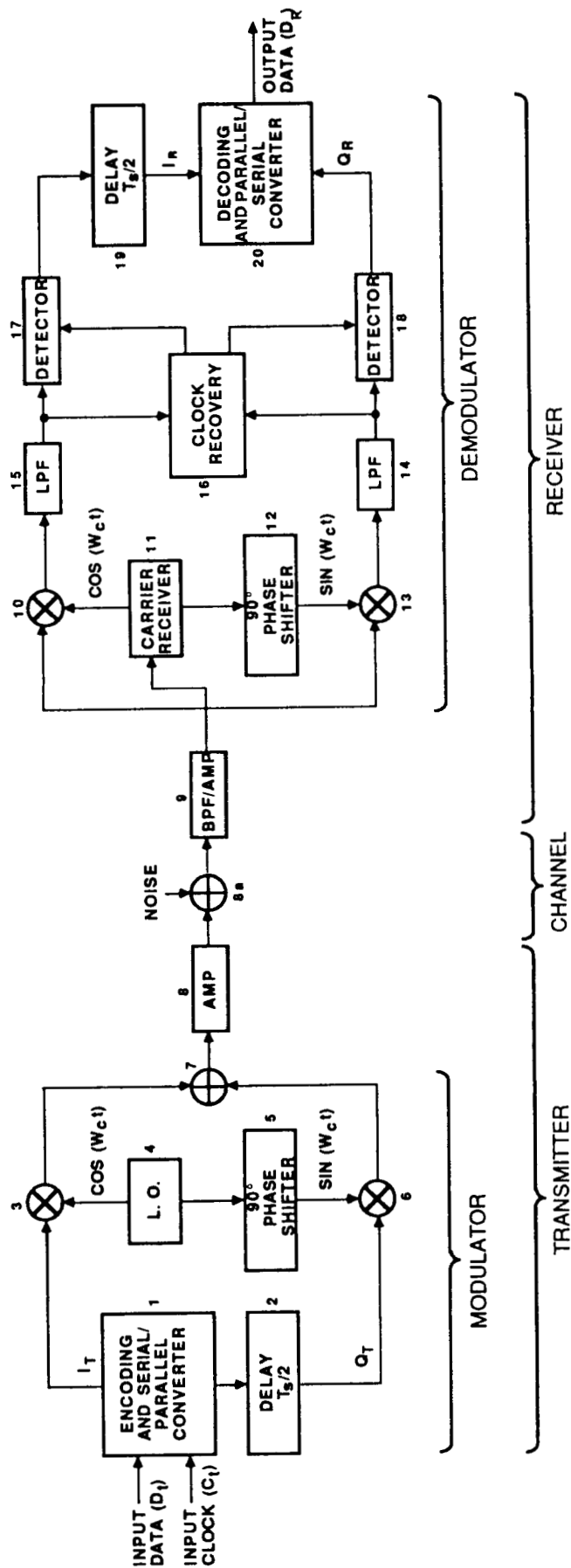
LEGEND:

L. O. = LOCAL OSCILLATOR

W_c = CARRIER FREQUENCY

BPF = BANDPASS FILTER

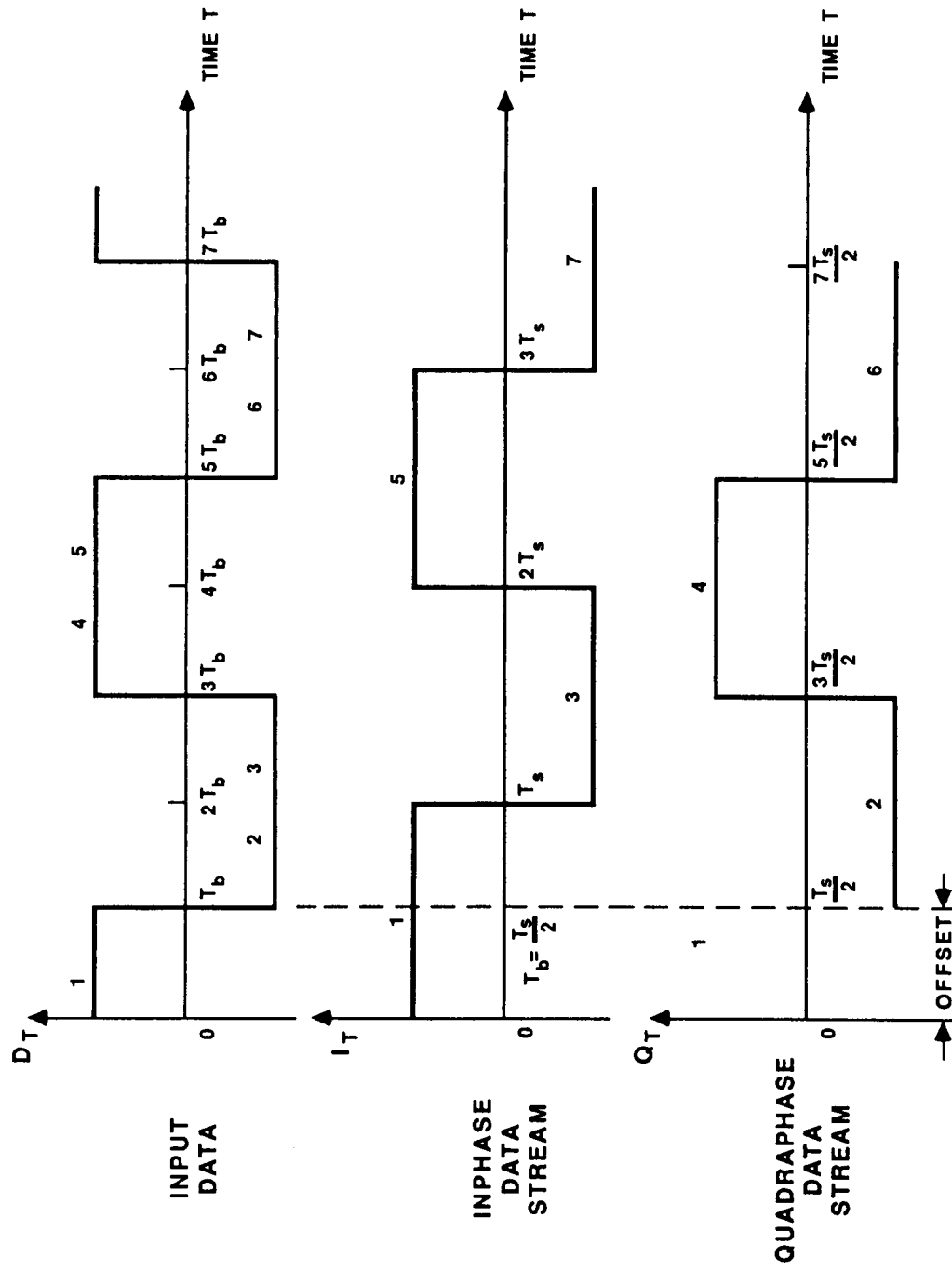AMP = AMPLIFIER

LPF = LOW-PASS FILTER

T_s = SYMBOL PERIOD

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FIGURE 2. THE OQPSK MODULATOR DATA STREAM
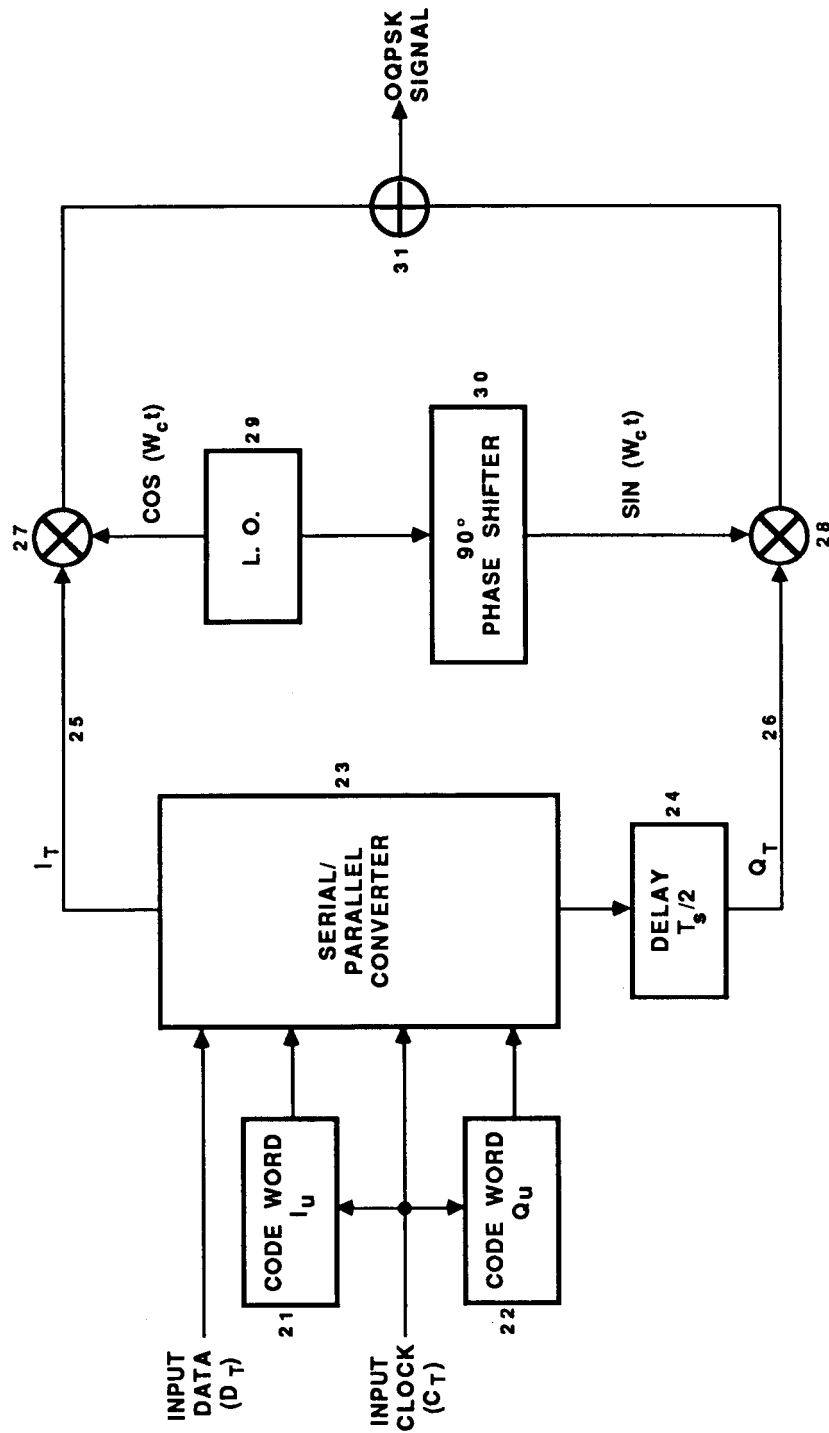
FIGURE 3. BLOCK DIAGRAM FOR OQPSK MODULATOR WITH UNIQUE WORDS MODULATION

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FIGURE 4. BLOCK DIAGRAM OF OQPSK DEMODULATOR WITH PHASE AMBIGUITY CORRECTION SYSTEMS USING DIGITAL OQPSK COSTAS LOOP WITH INTEGRATED SYMBOL SYNCHRONIZER AND UNIQUE-WORD DETECTOR
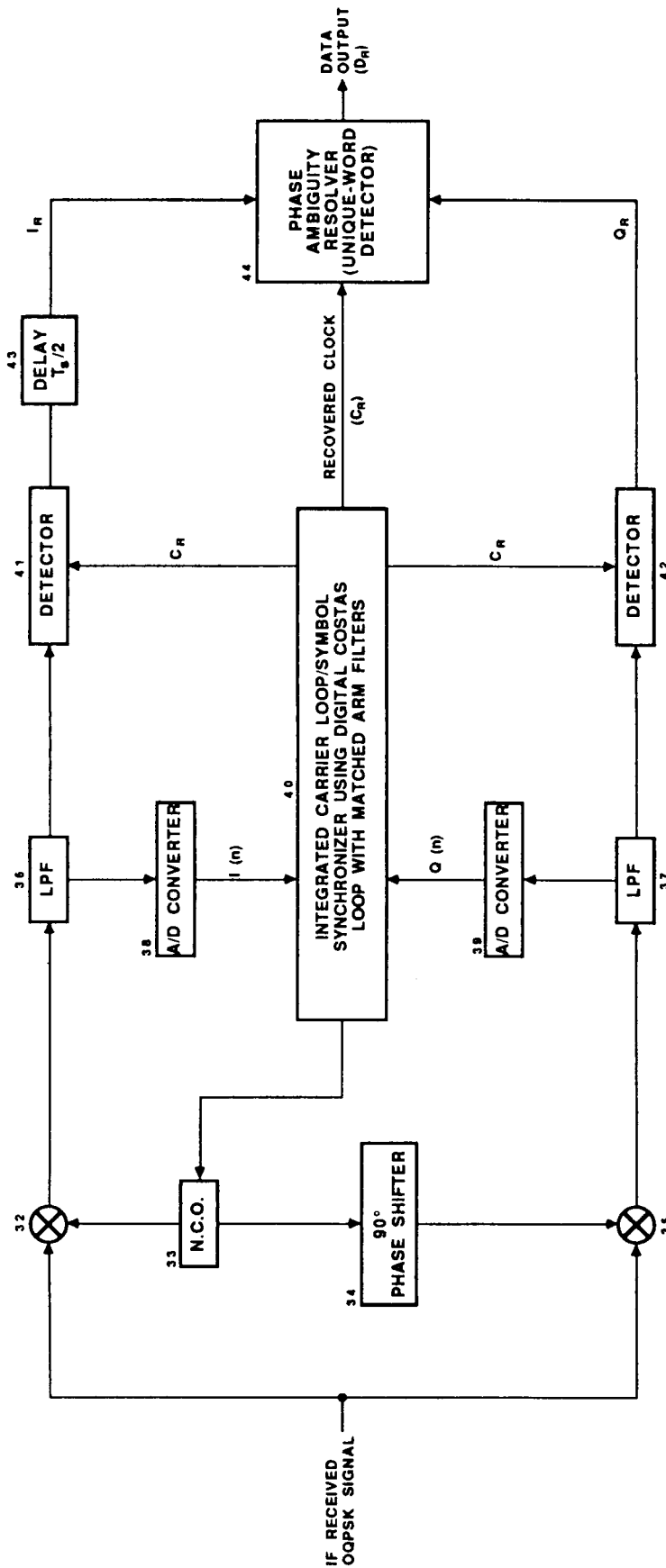
LEGEND:

N.C.O. = NUMERICALLY CONTROLLED OSCILLATOR

A/D = ANALOG TO DIGITAL CONVERTER

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INTEGRATED CARRIER LOOP/SYMBOL SYNCHRONIZER
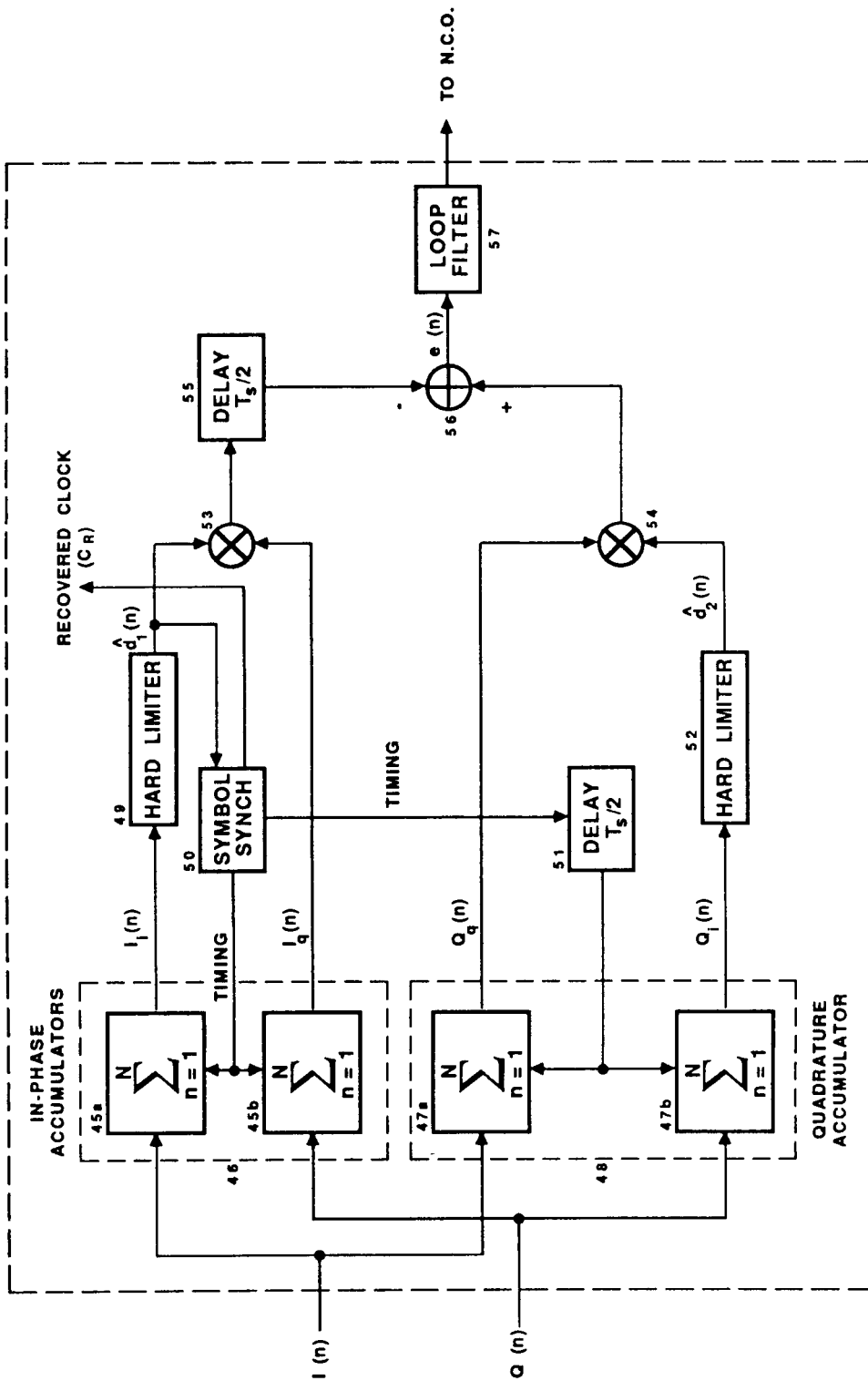
LEGEND:

N = NUMBER OF SAMPLES TAKEN PER SYMBOL PERIOD

e (n) = ERROR SIGNAL

N.C.O. = NUMERICALLY CONTROLLED OSCILLATOR

FIGURE 5. BLOCK DIAGRAM OF AN INTEGRATED CARRIER LOOP/SYMBOL SYNCHRONIZER USING DIGITAL COSTAS LOOP WITH MATCHED ARM FILTERS
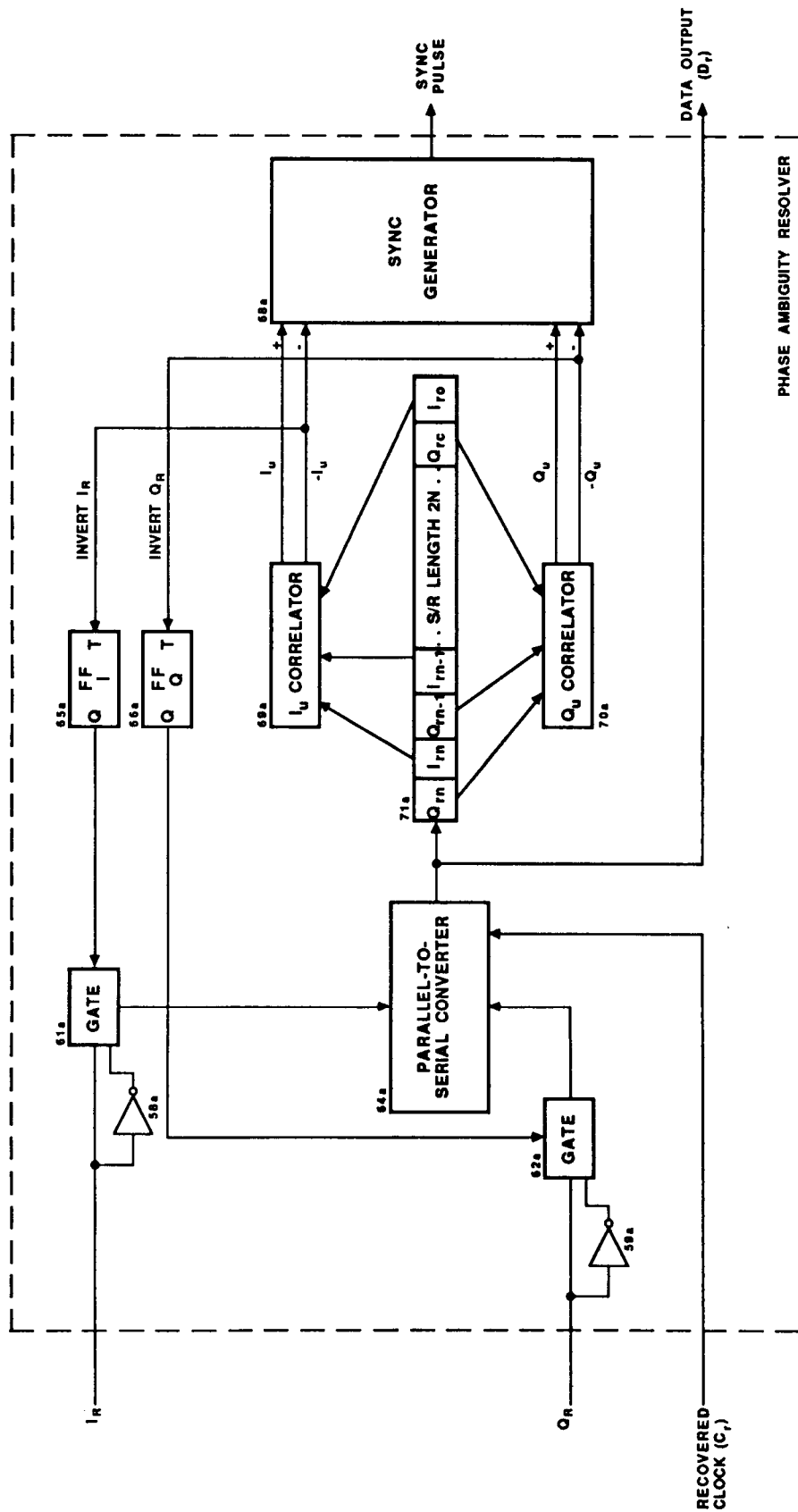
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FIGURE 6a. BLOCK DIAGRAM OF THE PHASE-AMBIGUITY CORRECTION SYSTEM
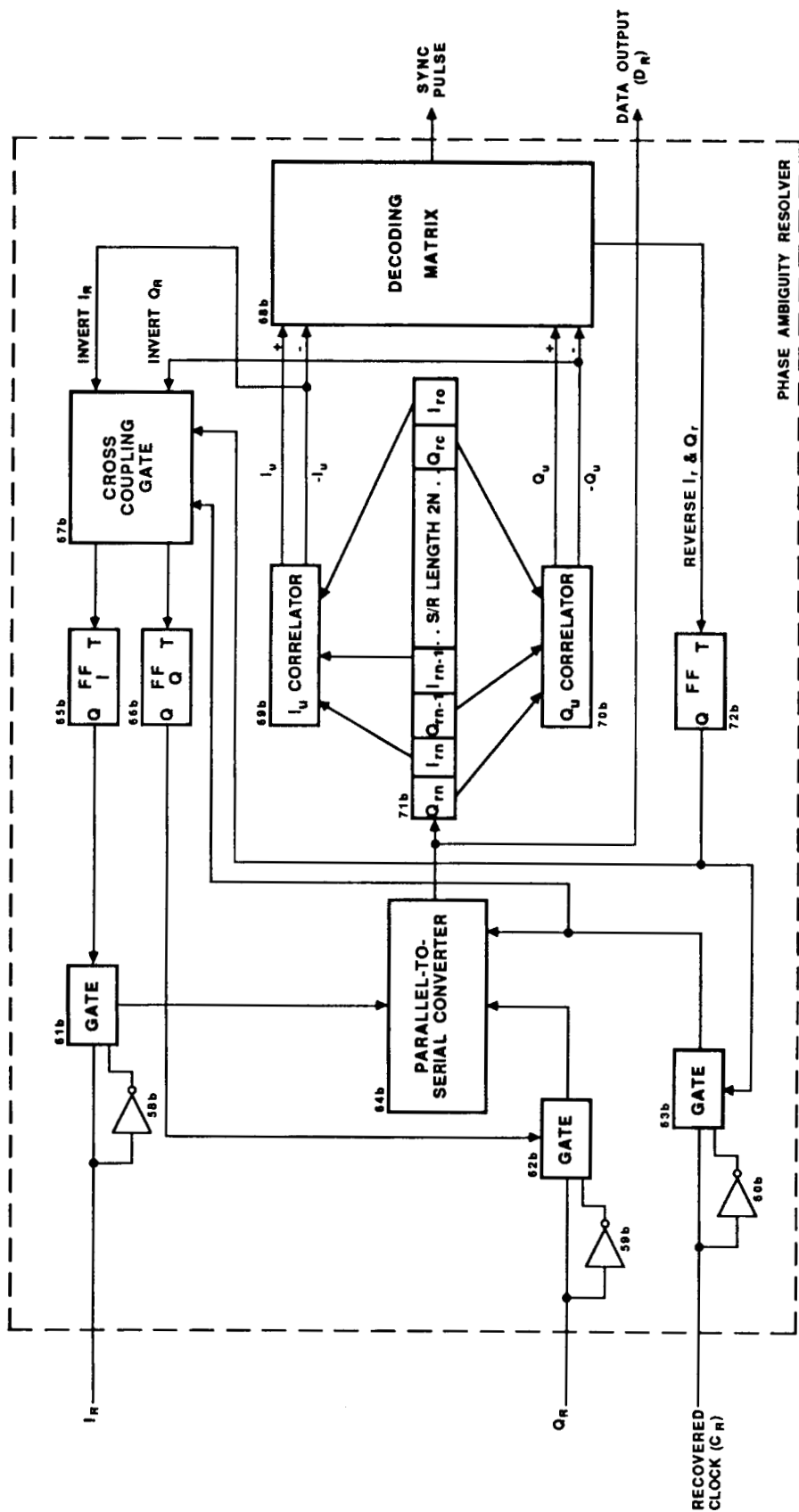FOR OQPSK MODULATION SYSTEM WITHOUT PHASE ROTATION
DIRECTION AMBIGUITY

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FIGURE 6b. BLOCK DIAGRAM OF THE PHASE-AMBIGUITY CORRECTION SYSTEM
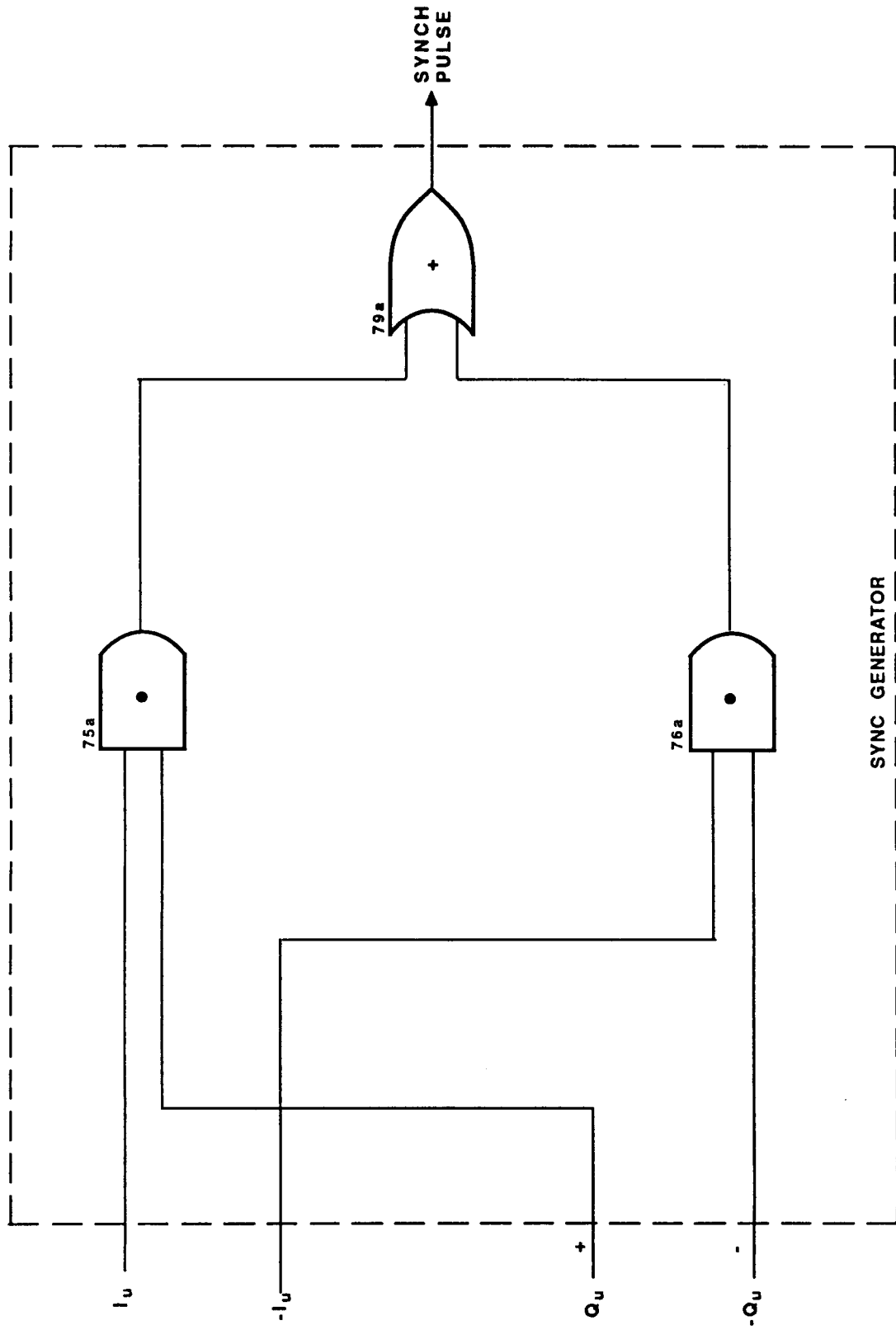FOR OQPSK MODULATION SYSTEM WITH PHASE ROTATION
DIRECTION AMBIGUITY

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FIGURE 7a. BLOCK DIAGRAM OF A SYNC GENERATOR WHICH FORMS A PART OF
THE PHASE-AMBIGUITY RESOLVER FOR OQPSK SYSTEM WITHOUT
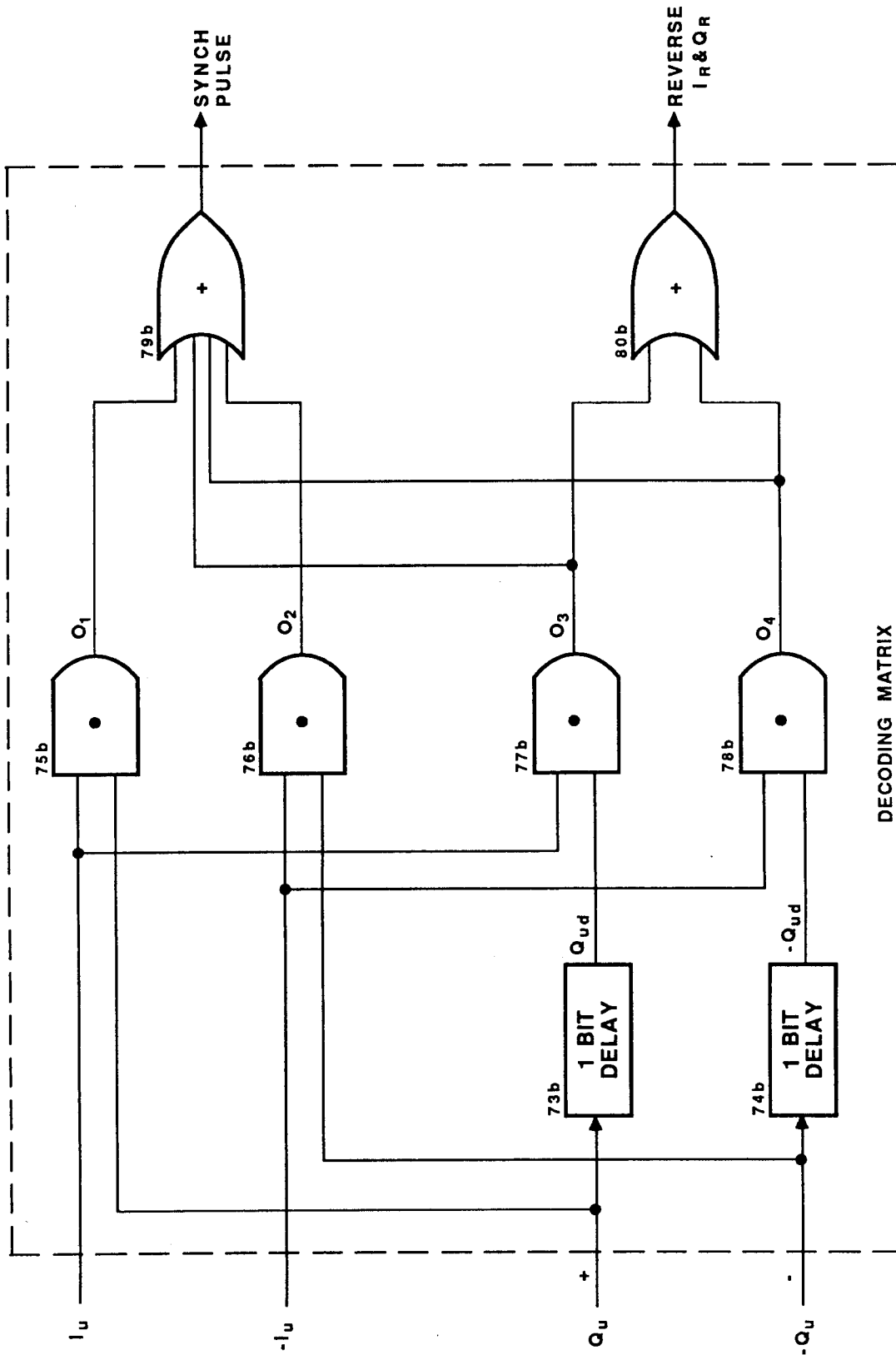PHASE ROTATION DIRECTION AMBIGUITY

FIGURE 7b. BLOCK DIAGRAM OF A DECODING MATRIX WHICH FORMS A PART OF THE PHASE-AMBIGUITY RESOLVER FOR OQPSK SYSTEM WITH PHASE ROTATION DIRECTION AMBIGUITY

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15. Supplementary Notes

16. Abstract

Part II of this report presents a new method to resolve the phase-ambiguity for Offset QPSK modulation systems. When an Offset Quaternary Phase-Shift-Keyed (OQPSK) communications link is utilized, the phase ambiguity of the reference carrier must be resolved. At the transmitter, two different unique words are separately modulated onto the quadrature carriers. At the receiver, the recovered carrier may have one of four possible phases, 0°, 90°, 180°, or 270°, referenced to the nominally correct phase. The IF portion of the channel may cause a phase-sense reversal, i.e., a reversal in the direction of phase rotation for a specified bit pattern. Hence, eight possible phase relationships (the so-called eight ambiguous phase conditions) between input and output of the demodulator must be resolved. Using the In-phase (I)/Quadrature (Q) channel reversal correcting property of an OQPSK Costas loop with integrated symbol synchronization, four ambiguous phase conditions are eliminated. Thus, only four possible ambiguous phase conditions remain. The errors caused by the remaining ambiguous phase conditions can be corrected by monitoring and detecting the polarity of the two unique words. The correction of the unique word polarities results in the complete phase-ambiguity resolution for the OQPSK system.

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