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**PROGRESS ON SINGLE BARRIER VARACTORS FOR  
SUBMILLIMETER WAVE POWER GENERATION**Svein M. Nilsen, Hans Grönqvist, Hans Hjelmgren, Anders Rydberg,  
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160524  
p. 19**ABSTRACT**

Theoretical work on Single Barrier Varactor (SBV) diodes, indicate that the efficiency for a multiplier has a maximum for a considerably smaller capacitance variation than previously thought. The theoretical calculations are performed, both with a simple theoretical model and a complete computer simulation using the method of harmonic balance. Modelling of the SBV is carried out in two steps. First, the semiconductor transport equations are solved simultaneously using a finite difference scheme in one dimension. Secondly, the calculated IV-, and CV characteristics are input to a multiplier simulator which calculates the optimum impedances, and output powers at the frequencies of interest. Multiple barrier varactors can also be modelled in this way. Several examples on how to design the semiconductor layers to obtain certain characteristics are given. The calculated conversion efficiencies of the modelled structures, in a multiplier circuit, are also presented. Computer simulations for a case study of a 750 GHz multiplier show that InAs diodes perform favourably compared to GaAs diodes. InAs and InGaAs SBV diodes have been fabricated and their current vs. voltage characteristics are presented. In the InAs diode, was the large bandgap semiconductor AlSb used as barrier. The InGaAs diode was grown lattice matched to an InP substrate with InAlAs as a barrier material. The current density is greatly reduced for these two material combinations, compared to that of GaAs/AlGaAs SBV diodes. GaAs based diodes can be biased to higher voltages than InAs diodes.

**1. INTRODUCTION**

A SBV device, in its simplest form, consists of a thin layer of a large bandgap material which acts as a barrier, and a thicker layer of a small bandgap material on each side of the barrier. A cross section of a typical SBV diode is shown in Fig. 1. The low bandgap material at both ends of the device is normally highly doped in order to make possible, the formation of low resistance contacts. Provided the layer thicknesses and doping concentrations are symmetrical around the barrier, the current  $I$  vs. voltage  $V$  and the capacitance  $C$  vs. voltage  $V$  will be symmetrical around zero volt. An applied rf-voltage will then generate only odd harmonics. This makes it possible to design higher order multipliers with fewer idler circuits and thus less losses. Also the design procedure and mechanical construction of a higher order multiplier, making use of a SBV device as the non linear element will become much easier compared to that of one using a Schottky diode. It is the purpose of this paper to give an overview of our work on SBV diodes [1][2][15].

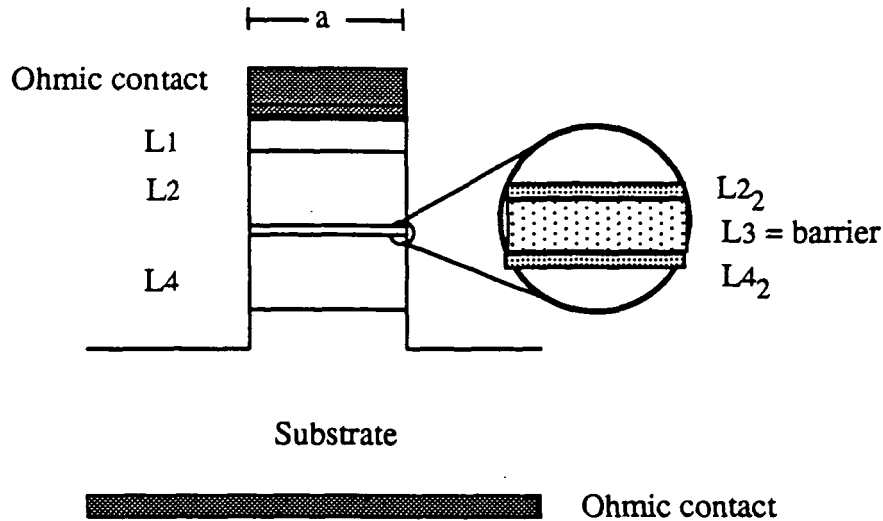


Fig. 1. Schematic cross section of a SBV mesa diode. L1 is the highly doped contact layer, L2<sub>n</sub> and L4<sub>n</sub> are the depletion regions on either side of the barrier, index n denotes sublayers, L3<sub>n</sub> is the barrier and L5 is part of the buffer/substrate layer. In the simulations L1 and L5 are set equal. Mesa diameter = a.

## 2. DIODES

### 2.1 Quality factor of SBV's

The cutoff frequency for a varactor, as defined in Eq. 1, is often used as a quality factor, suggesting that  $C_{\max}$  should be as large as possible for a fixed  $C_{\min}$ .

$$f_c = \frac{1}{2\pi R_{slo}} \left( \frac{1}{C_{\min}} - \frac{1}{C_{\max}} \right) \quad (1)$$

where  $R_{slo}$  is the dc series resistance of the device,  $C_{\max}$  and  $C_{\min}$  are the calculated device capacitances for accumulated and depleted low doped epilayers, L2 and L4 in Fig.1, respectively.

However, a simple analysis show that an optimum  $C_{\max}/C_{\min}$  ratio exist. Choosing a CV characteristic as shown in Fig. 2 and assuming that all harmonics, except the first and third harmonics are shortcircuited over the variable capacitance, only these two frequency components have to be considered. The bias voltage is of course always zero volts. This makes the analysis quite simple. In Fig. 3 we have plotted the efficiency vs.

$C_{\max}/C_{\min}$  for different values of  $R_s$ , assuming  $1/\omega C_{\min} = 180 \Omega$ . The important conclusion from this graph is that there is an optimum value for  $C_{\max}/C_{\min}$ , and that too large  $C_{\max}$  values will deteriorate the multiplier's efficiency. Table 1 shows input and output impedances. Although this model is much simplified the results show that the input is highly reactive with a fairly low resistance while the output seems to be easier to match. This result will be confirmed below in the harmonic balance simulations employing a modified version of the computer program by P.H. Siegel et.al. [8].

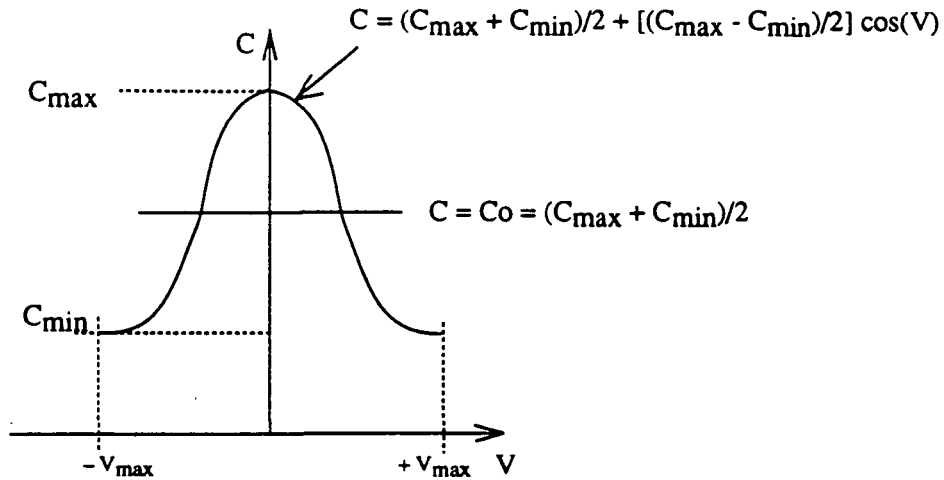


Fig. 2 Approximate CV characteristic of SBV diode used in the simplified analysis.  $V_{max}$  is the maximum voltage across the diode.

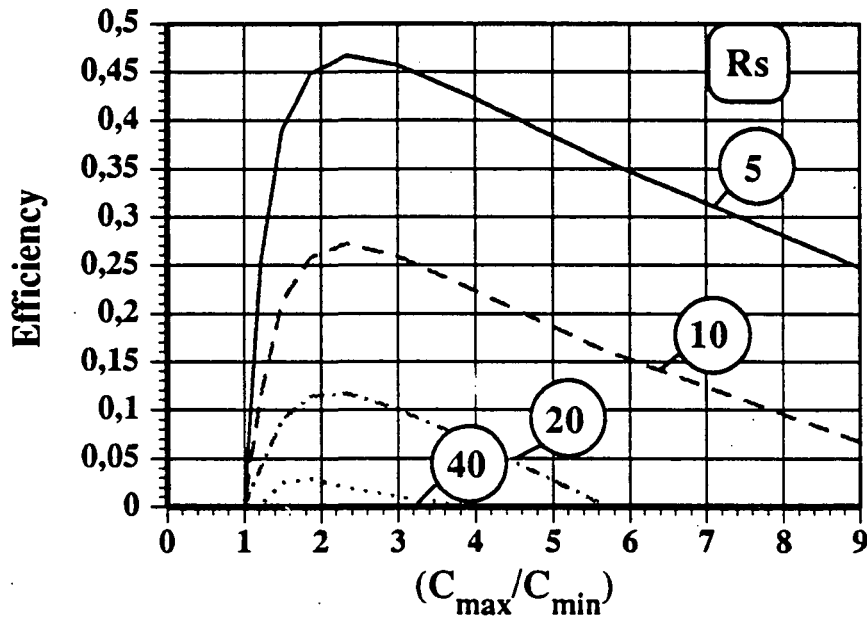


Fig. 3 Efficiency vs. the  $C_{max}/C_{min}$  ratio for different values of  $R_s$ .

Table 1 Calculated efficiencies, optimum input and output impedances for a SBV diode tripler with the approximate cosine shaped CV characteristic for different series resistances.

$R_s \Omega$	$\eta_{max} \%$	SOURCE IMPEDANCE		LOAD IMPEDANCE	
		$R1 \Omega$	$X1 \Omega$	$R3 \Omega$	$X3 \Omega$
2.5	65.5	8.6	91.0	29.5	34.0
5	46.7	10.9	90.0	30.4	33.0
10	27.2	15.7	95.0	30.2	36.0
20	11.8	25.0	90.0	23.0	33.0
40	2.9	44.1	106.0	14.0	38.0

## 2.2 MEASUREMENTS

### 2.2.1 DC measurements

We have fabricated several diodes based on the materials: GaAs, InGaAs and InAs, see Table 2 for details. Our efforts at modelling these devices are however, more recent. For the GaAs based diode we use a barrier of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ , in the InGaAs case we use  $\text{AlInAs}$  as a barrier. The latter diode is grown lattice matched on an InP substrate. For the InAs diodes we use an  $\text{AlSb}$  barrier which gives a very high barrier, 1.3 eV for indirect transitions. It should therefore be very efficient in blocking the current through the varactor. The InAs device is grown on a GaAs substrate with thick GaAs and InAs buffer layers.

Table 2 Material from which diodes of various sizes have been fabricated.

Wafer #ID & Crystal Grower	Material system	Layer thickness (top/down) and doping concentration
#614 IMEC	GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ /GaAs $x = 0.70$ in L3 Buffer: $n^+$ GaAs Substrate: $n^+$ GaAs	L1 = 400 nm, $N_d = 3.4 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$ L2 <sub>1</sub> = 533 nm, $N_d = 1.0 \cdot 10^{17} \text{ [cm}^{-3}\text{]}$ L2 <sub>2</sub> = 5.3 nm, undoped L3 = 21.3 nm, undoped L4 <sub>2</sub> = L2 <sub>2</sub> , L4 <sub>1</sub> = L2 <sub>1</sub> L5 = 1998 nm, $N_d = 3.4 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$
#1566 Chalmers	InAs/ $\text{AlSb}$ /InAs Buffer: $n^+$ InAs, and $n^+$ GaAs Substrate: $n^+$ GaAs Barrier thickness = L3	L1 = 200 nm, $N_d = 5.0 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$ L2 <sub>1</sub> = 400 nm, $N_d = 6.0 \cdot 10^{16} \text{ [cm}^{-3}\text{]}$ L2 <sub>2</sub> = 5 nm, undoped L3 = 20 nm, undoped L4 <sub>2</sub> = L2 <sub>2</sub> , L4 <sub>1</sub> = L2 <sub>1</sub> L5 = 2000 nm, $N_d = 5.0 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$
#1567 Chalmers	InAs/ $\text{AlSb}$ /InAs Buffer: $n^+$ InAs, and $n^+$ GaAs Substrate: $n^+$ GaAs Barrier thickness = L3	L1 = 200 nm, $N_d = 5.0 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$ L2 <sub>1</sub> = 320 nm, $N_d = 1.0 \cdot 10^{17} \text{ [cm}^{-3}\text{]}$ L2 <sub>2</sub> = 5 nm, undoped L3 = 25 nm, undoped L4 <sub>2</sub> = L2 <sub>2</sub> , L4 <sub>1</sub> = L2 <sub>1</sub> L5 = 2000 nm, $N_d = 5.0 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$
#ST1 Tampere	Lattice matched InGaAs/ $\text{AlInAs}$ /InGaAs Buffer: $n^+$ InGaAs Substrate: $n^+$ InP Barrier thickness = L3	L1 = 400 nm, $N_d = 4.0 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$ L2 = 400 nm, $N_d = 6.0 \cdot 10^{16} \text{ [cm}^{-3}\text{]}$ L3 = 25 nm, $N_d = 6.0 \cdot 10^{16} \text{ [cm}^{-3}\text{]}$ L4 = L2 L5 = 1000 nm, $N_d = 4.0 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$
#1047 IMEC	InAs/ $\text{AlSb}$ /InAs Buffer: $n^+$ InAs, and $n^+$ GaAs Substrate: $n^+$ GaAs Barrier thickness = L3	L1 = 200 nm, $N_d = 2.6 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$ L2 = 150 nm, $N_d = 1.0 \cdot 10^{17} \text{ [cm}^{-3}\text{]}$ L3 = 14 nm, undoped L4 = L2 L5 = 3000 nm, $N_d = 2.6 \cdot 10^{18} \text{ [cm}^{-3}\text{]}$

The influence of the epilayer design on the IV-, and CV characteristics has been investigated theoretically in some detail.

The different SBV diodes fabricated by us have been DC characterized with a DC parameter analyzer. Most of the measurements have been done on large area diodes, 100–2500  $\mu\text{m}^2$ . A limited number of measurements have been made on small area, 7  $\mu\text{m}^2$ , diodes of the #614 type.

Diodes characterized are one GaAs varactor with an AlGaAs barrier, one diode grown on InP with InGaAs and InAlAs epilayers lattice matched to the substrate and two InAs diodes with AlSb barriers grown on GaAs substrates. The material from which we have fabricated devices are listed in Table 2. DC characterization of the different SBV diodes show that the current density is decreased as the barrier height is increased as expected, see Fig. 4. The InAs/AlSb material system has a 1.3 eV barrier for indirect transitions and  $\approx 2$  eV for direct. The lowest current density is obtained for InAs/AlSb devices. They also show a large variation in their characteristics, a factor of two or more in current density over a distance of a few millimeters on the wafer. Whether this variation is caused by the epilayers being severely lattice mismatched to the substrate or by some growth parameter, is difficult to say. In comparison, diodes of the lattice matched InGaAs/InAlAs materials grown on InP substrate as well as those of GaAs/AlGaAs show current density variations of only a few percent over the same distance. It can also be noted that the breakdown voltage of the InAs and InGaAs diodes is low, about 2 Volt, in comparison with the GaAs diode. For a varactor to be used in practice the breakdown voltage needs to be higher since the pump voltage otherwise could destroy the diode. One method of increasing the total breakdown voltage is to fabricate several varactor diodes in series. Each of  $n$  identical diodes would then only need to sustain the total pump voltage divided by  $n$ .

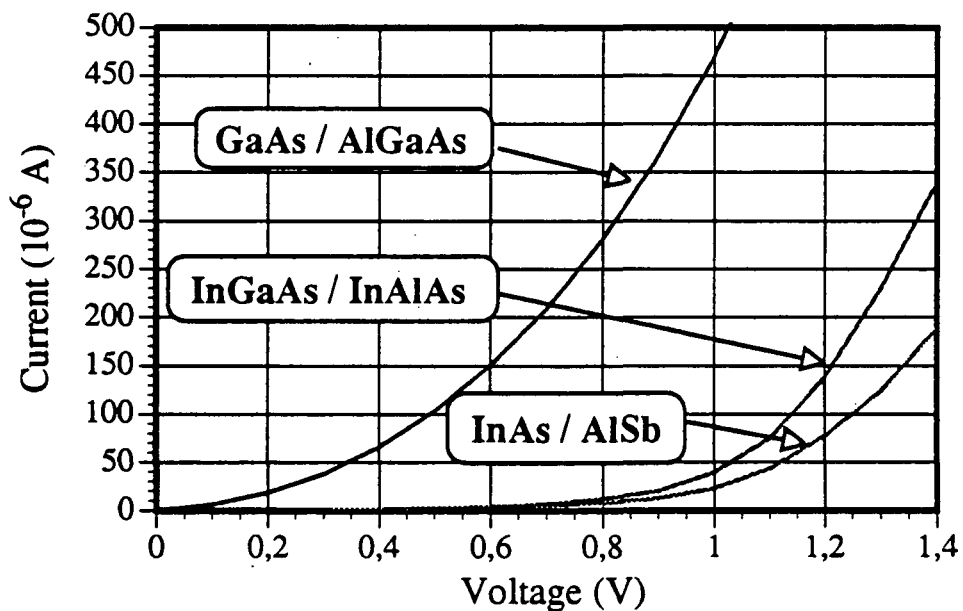


Fig. 4 Measured current vs. voltage for SBV diodes of size  $25 \times 25 \mu\text{m}^2$  in different material systems.

### 2.2.2 RF measurements

Two methods have been developed for measuring the capacitance of these diodes, the results will be published elsewhere [14]. One method is similar to the one by Tolmunen et. al. [15], the other method uses a 60 GHz coplanar probe to contact a mesa diode surrounded by a large ring which is contacted by the two ground contacts of the probe.

## 2.3 MODELLING DEVICES AND MULTIPLIER PERFORMANCE

### 2.3.1 CV and IV modelling

For calculating the CV-, and IV characteristics, the semiconductor transport equations including the energy balance equations for holes and electrons are solved simultaneously using a finite-difference scheme in a detailed one-dimensional energy transport model for GaAs/Al<sub>x</sub>Ga<sub>1-x</sub>As heterojunction structures with 0.0 < x < 1.0. The computer program is a modified version of the program developed by H. Hjelmgren [3][4]. The program can readily be modified further for other heterostructures. A non-uniform grid-mesh is used to obtain the necessary accuracy and acceptable calculation times. Position dependent barrier parameters were implemented following the procedure of M. S. Lundstrom and R.J. Schuelke [5]. The model used is based on the paper by R. Stratton [6]. The five variables are the electric potential, the quasi-Fermi levels for holes and electrons, and hole and electron temperatures. The equation system has a 19 diagonals band-matrix which is solved by LU decomposition. To improve the convergence properties of the program the energy balance equation for holes is not used, hence the hole temperature is set to the lattice temperature for all applied voltages. Hot electrons and lattice heating are not simulated, hence the five equation model is reduced to a three equation (Poisson's and current continuity equations) model. Recombination is modelled with Shockley Read Hall (SRH) recombination. The relaxation time was set to 3.0 ps, the electron life time to 1.0 ns, and the conduction band-offset to 65 % in most simulations for which x < 0.45. The contact resistivity of the two ohmic contacts can be set to a value of choice. They are modelled by modifying the boundary conditions for the potential. The thermoionic emission current, which limits the current through the device, is then calculated from the equation for a reverse biased Schottky diode, using a voltage dependent barrier-height obtained from the shape of the conduction band. Tunneling current is assumed to be sufficiently small and thus neglected altogether. The diode capacitance,  $C = dQ/dV \approx \Delta Q/\Delta V$  is determined numerically from the change  $\Delta Q$  in the stored electric charge in the semiconductor for an incremental change  $\Delta V$  in the applied voltage. The integration of charges is carried out to the middle of the barrier for single barrier devices. To obtain the depletion capacitance one must correct for the influence of the series resistance on the voltage across the depletion layer.

### 2.3.2 CV characteristics and conversion efficiencies of modelled structures.

It is of importance to understand how the CV characteristic can be modified by changes to the design of the epitaxial structure. It is obvious that increasing the width of the barrier will decrease  $C_{max}$ , and that a wider L2 region, see Fig. 1, will allow a larger capacitance swing, i.e. make  $C_{min}$  smaller. Below we will investigate how the doping profile of the diode affects the efficiency of a 3\*60 GHz tripler. The effect of the plasma resonance on the series resistance was not included in the multiplier calculations on structures #100-103B, #112 and #114 at 3\*60 GHz.

The following rules are basic to the understanding of the behaviour of the CV characteristic for different choices of doping concentrations, viz.

- i. Doping the barrier will increase  $C_{\max}$  without influencing the capacitance value at large biases, i.e.  $C_{\min}$  is not much affected. This phenomenon is studied in structures #100-103B. However, too many dopants in the barrier and its blocking capability may be destroyed.
- ii. A similar effect, an increase in  $C_{\max}$ , can be obtained by introducing thin regions with high doping concentration adjacent to the barrier on each side. One such example is #112. This scheme may be less damaging to the barrier's blocking capability, but it may also affect material quality in a negative way or make symmetrical growth more difficult.
- iii. A reduced doping concentration in the L2 layer where the depletion occurs, will cause a more rapid change in the capacitance vs. bias voltage. It will also lead to a larger series resistance. The method cannot therefore be recommended as a stand alone measure.
- iv. To avoid an increase in the series resistance according to iii., a tapered doping concentration in the L2 region will improve the situation. A comparison between #112 and #114 illustrates this phenomenon.

Please note that the choice of doping profile will also influence the series resistance. An advantageous CV characteristic may offer an undesireably large series resistance.

The effect of doping the barrier on the CV characteristic is illustrated in Fig. 5 which show the results for structures #100-103B. The increase in  $C_{\max}$  is as large as 70 % when the doping is increased from  $1 \cdot 10^{15} \text{ cm}^{-3}$  to  $1 \cdot 10^{18} \text{ cm}^{-3}$ . To see any effect at all, the doping in the barrier needs to exceed  $1 \cdot 10^{17} \text{ cm}^{-3}$ . The series resistance remains the same of course, since it is essentially determined by the doping in region L2. In Fig. 6 is shown the conversion efficiency vs. input power (all input power is assumed to be absorbed). It is interesting to note that the efficiency actually decreases as  $C_{\max}$  increases. This is in agreement with the results presented in paragraph 2.1.

The effect of a high doping concentration near the barrier interface is illustrated by the CV characteristic of #112 in Fig. 7. Notice that the CV is almost identical to the one of #103. Since the series resistances are also very similar, the efficiencies vs. pump power are virtually identical as can be seen in Fig. 6 and Fig. 8.

Structure #114 has a linearly graded doping concentration in the L2 and L4 regions, starting with  $1 \cdot 10^{15} \text{ cm}^{-3}$  near the barrier and increasing to  $2 \cdot 10^{17} \text{ cm}^{-3}$  at a distance of 385 nm from the barrier. The ratio  $C_{\max}/C_{\min}$  is increased considerably compared to that of a homogeneously doped L2 region, but the series resistance is larger than for #100-103B. The CV resembles mostly that of #103B. The capacitance swings down faster, but have the same  $C_{\min}$  and a small reduction in efficiency.

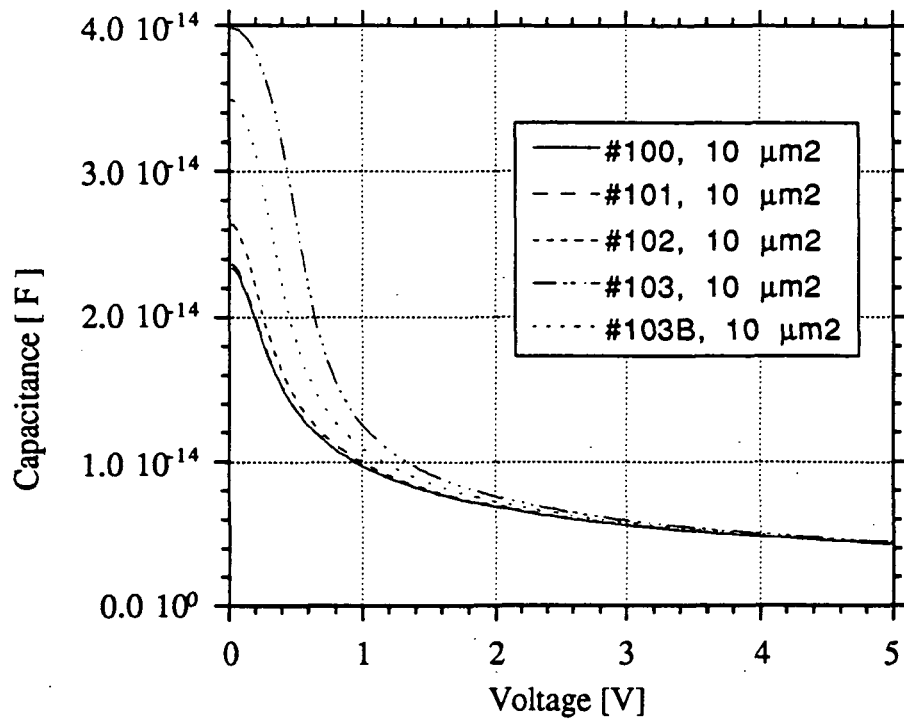


Fig. 5 Calculated CV characteristics for symmetric GaAs/Al<sub>0.44</sub>Ga<sub>0.56</sub>As structures #100-103, #103B with different barrier doping. L<sub>2</sub> = L<sub>4</sub> = 390 nm with 1.0\*10<sup>17</sup> cm<sup>-3</sup>, L<sub>3</sub> = 20 nm, for #100: N<sub>d</sub> = 1.0\*10<sup>15</sup> cm<sup>-3</sup>, for #101: N<sub>d</sub> = 1.0\*10<sup>16</sup> cm<sup>-3</sup>, for #102: N<sub>d</sub> = 1.0\*10<sup>17</sup> cm<sup>-3</sup>, for #103B: N<sub>d</sub> = 5.0\*10<sup>17</sup> cm<sup>-3</sup>, for #103: N<sub>d</sub> = 1.0\*10<sup>18</sup> cm<sup>-3</sup>. For all structures L<sub>1</sub> = L<sub>5</sub> = 100 nm, N<sub>d</sub> = 3.4\*10<sup>18</sup> cm<sup>-3</sup>



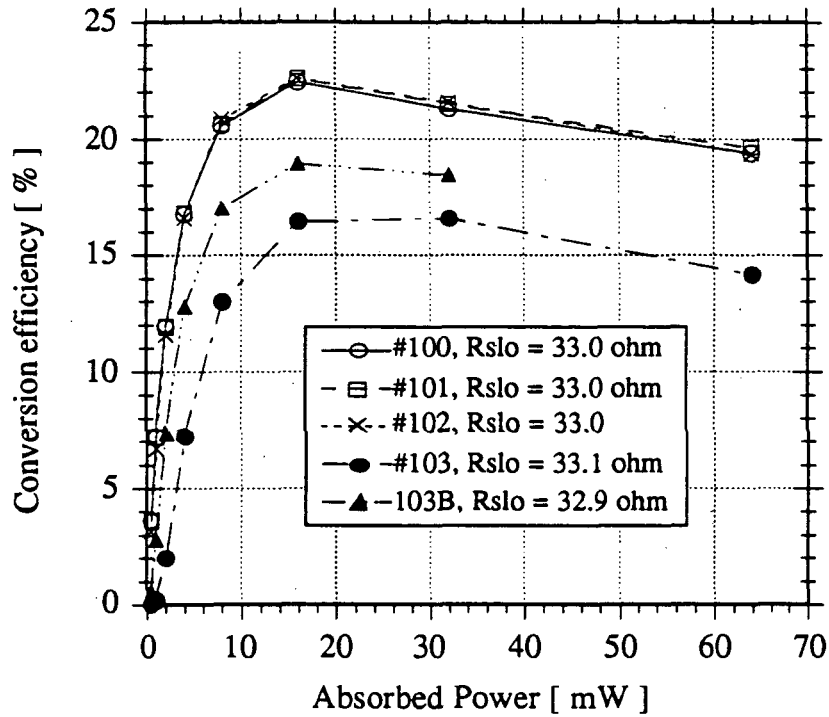


Fig. 6 Calculated conversion efficiency vs. pump power for structures #100-103 and #103B at 3\*60 GHz. It is the devices with undoped or low doped barrier which have the highest conversion efficiency. The series resistance  $R_{slo}$  used was between 32.9 and 33.1 ohm (calculated by the simulation program) for all five structures.

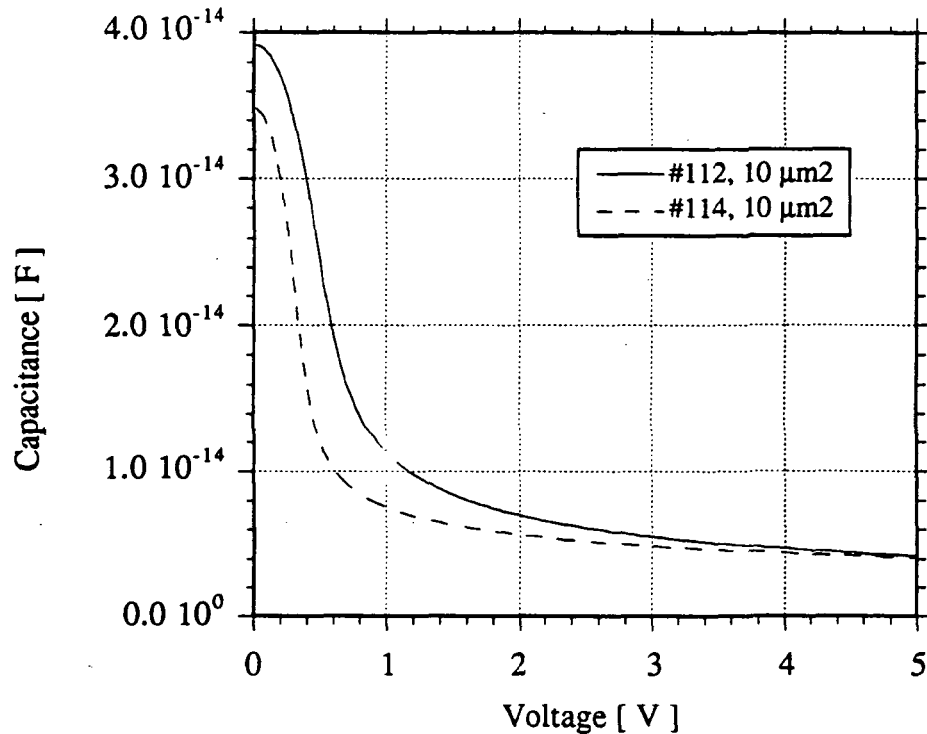


Fig. 7 Calculated CV characteristics for symmetric GaAs/Al<sub>0.44</sub>Ga<sub>0.56</sub>As structures for different doping profiles in the L2 region meant to enhance the  $C_{\max}/C_{\min}$  ratio.

#112 has  $L_{21} = L_{41} = 386$  nm with  $N_d$  going from  $1.0 \cdot 10^{17}$  cm<sup>-3</sup> to  $0.8 \cdot 10^{17}$  cm<sup>-3</sup> at the barrier interface, i.e. a weak gradient,  $L_{22} = L_{42} = 4$  nm with  $N_d = 1.0 \cdot 10^{17}$  cm<sup>-3</sup>, L3 consists of three parts,  $L_{31} = L_{33} = 7$  nm  $N_d = 1.0 \cdot 10^{18}$  cm<sup>-3</sup>,  $L_{32} = 6$  nm  $N_d = 2.0 \cdot 10^{17}$  cm<sup>-3</sup>.

#114 has  $L_{21} = L_{41} = 385$  nm with  $N_d$  going from  $2.0 \cdot 10^{17}$  cm<sup>-3</sup> to  $1.0 \cdot 10^{15}$  cm<sup>-3</sup> at the barrier interface, i.e. a steep gradient,  $L_{22} = L_{42} = 5$  nm with  $N_d = 5.0 \cdot 10^{16}$  cm<sup>-3</sup>, L3 consists of three parts,  $L_{31} = L_{33} = 6$  nm  $N_d = 1.0 \cdot 10^{18}$  cm<sup>-3</sup>,  $L_{32} = 8$  nm  $N_d = 5.0 \cdot 10^{16}$  cm<sup>-3</sup>.

$L_1 = L_5 = 100$  nm with  $N_d = 3.4 \cdot 10^{18}$  cm<sup>-3</sup> for both structures.

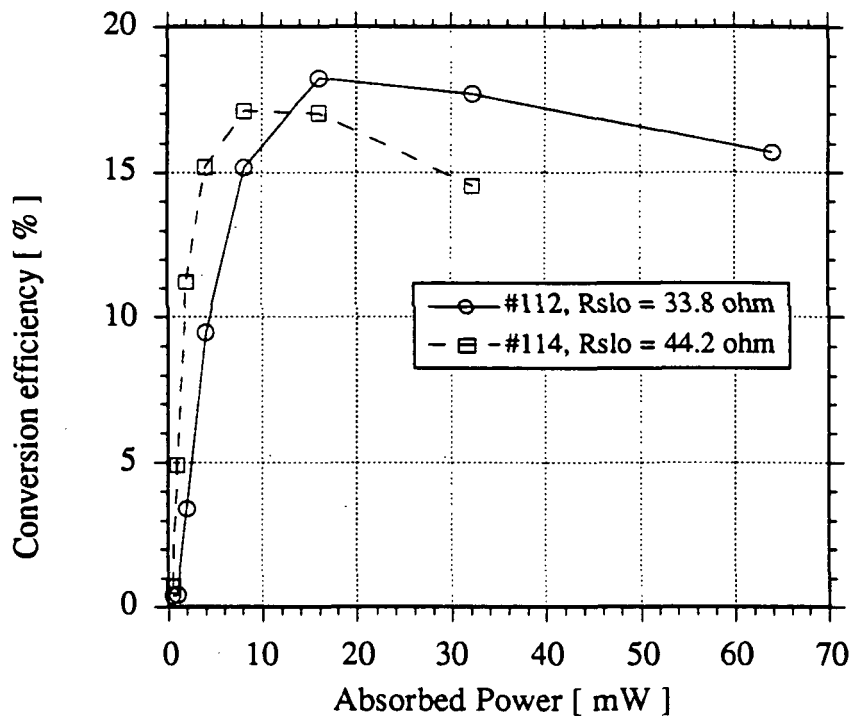


Fig. 8 Calculated conversion efficiency vs. pump power for structures #112 and #114 at  $3 \times 60$  GHz. The value of  $R_{slo}$  was 33.8 ohm for #112 and 44.2 ohm for #114.

### 3. A 750 GHz MULTIPLIER DESIGN STUDY

A study on different 750 GHz multiplier configurations using GaAs and InAs SBV-diodes was performed. The aim of the study was to evaluate theoretically the optimum frequency multiplier configuration for generating  $\geq 50 \mu\text{W}$  of output power at 750 GHz, assumed to be enough for pumping a 750 GHz SIS mixer, using a Single Barrier Varactor (SBV) diode as the nonlinear element.

Different important diode parameters were investigated, such as the cutoff frequency which is a direct function of the doping level  $N_d$  of the low doped epilayers, L2 and L4 in Fig.1, in the device. The cutoff frequency was calculated for GaAs and InAs SBV-diodes of three different sizes, see Fig. 9. In these calculations of  $C_{max}$  and cutoff frequencies, it was assumed that the effective barrier width was three times that of L3 because of the distance necessary for a lineup of the fermi levels at the interface between the low doped layer L2 and the undoped barrier L3. It can be seen that the optimum doping concentration is  $1 \times 10^{17} \text{cm}^{-3}$  and  $2 \times 10^{17} \text{cm}^{-3}$  for GaAs and InAs devices respectively, both having a diameter of  $2 \mu\text{m}$ .

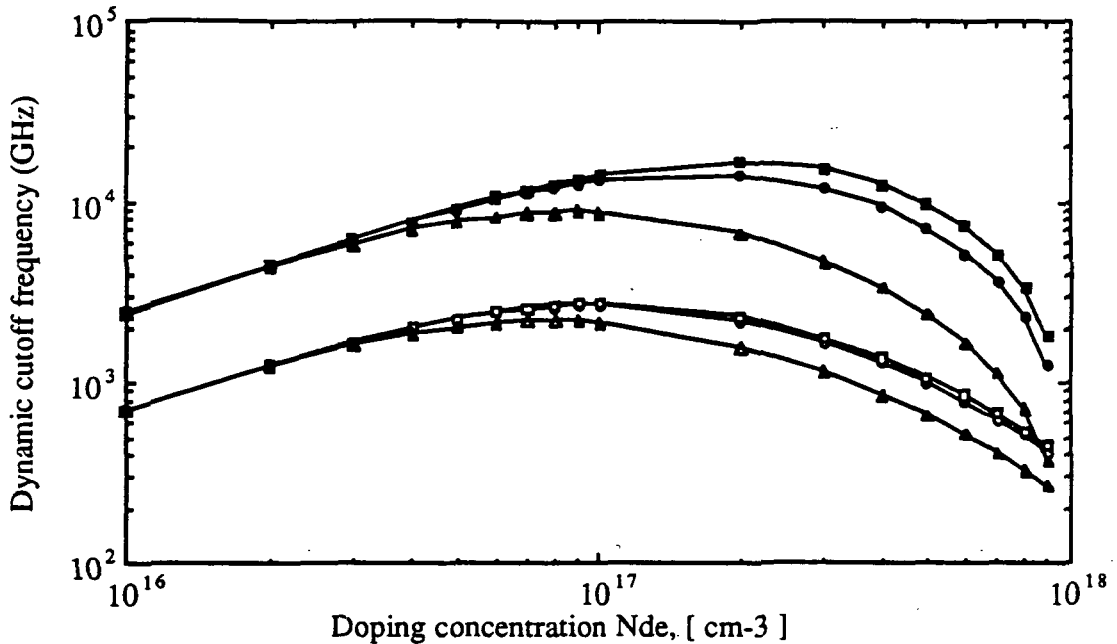


Fig 9 Calculated cutoff frequency vs. doping level  $N_{de}$  for GaAs and InAs SBV-diodes of different diameters a.  $N_{ds} = 3.4 \cdot 10^{18} \text{cm}^{-3}$  in L1 and L5,  $N_{db} = 1 \cdot 10^{17} \text{cm}^{-3}$  in L3, L1 = 100 nm, L5 = 100 nm, L2 varies with  $N_{de}$ , the barrier width L3 is 20 nm.

GaAs: ( $\square$ ): a = 2  $\mu\text{m}$ ., ( $\circ$ ): a = 4  $\mu\text{m}$ ., ( $\Delta$ ): a = 20  $\mu\text{m}$ .

InAs: ( $\blacksquare$ ): a = 2  $\mu\text{m}$ ., ( $\bullet$ ): a = 4  $\mu\text{m}$ ., ( $\blacktriangle$ ): a = 20  $\mu\text{m}$ .

Another important parameter to consider is the effect of the plasma resonance frequency on the series resistance of the diodes [7]. This is of great importance to devices intended for THz frequencies. In Fig.10 is plotted the calculated series resistance for InAs SBV-diodes when the plasma resonance is taken into account. It is found that by using InAs instead of GaAs in the low doped epilayers and in the substrate, the plasma resonance frequencies are shifted to higher frequencies. This is due to the higher electrical conductivity  $\sigma$  of InAs compared to that of GaAs. It can be seen in Fig. 10 that a doping  $N_d$  in L2 and L4 of about  $1 \cdot 10^{17} \text{cm}^{-3}$  gives sufficient clearance up to a frequency of 2 THz

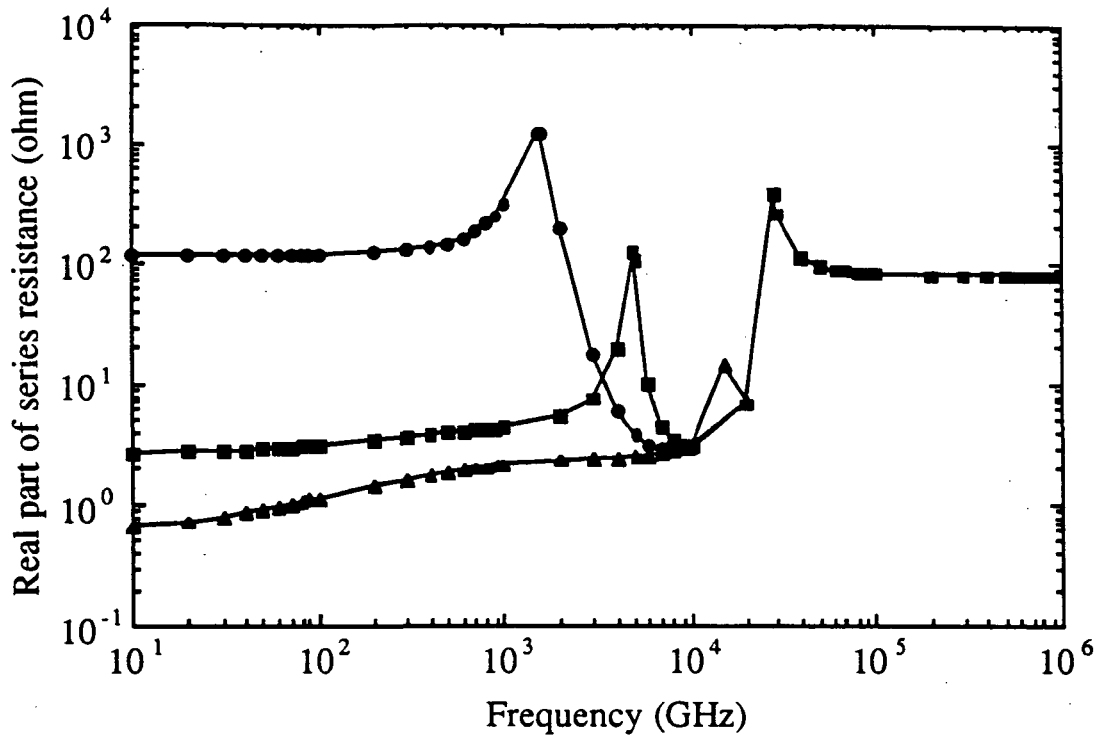


Fig. 10 Calculated series resistance vs. pump frequency for an InAs SBV-diode for different doping levels  $N_{de}$  in the low doped epilayers L2 and L4. Doping concentration  $N_{ds}$  is  $3.4 \cdot 10^{18} \text{ cm}^{-3}$  in L1 and L5,  $N_b$  is  $1 \cdot 10^{17} \text{ cm}^{-3}$  in the barrier L3, L1 = 100 nm, L5 = 100 nm, L2 = L4 = 533 nm, L3 = 20 nm, diameter  $a = 3.57 \text{ } \mu\text{m}$ .  
 (●):  $N_{de}$  is  $1 \cdot 10^{16} \text{ cm}^{-3}$ ., (■):  $N_{de}$  is  $1 \cdot 10^{17} \text{ cm}^{-3}$ .,  
 (▲):  $N_{de}$  is  $1 \cdot 10^{18} \text{ cm}^{-3}$ .

The avalanche breakdown voltage for the low doped epilayers limits the maximum pump power that can be used for the device. Using the optimum doping concentration the breakdown voltage was calculated to be 15.7 V for GaAs and 1.2 V for InAs, and having depletion lengths of 480 nm and 100 nm respectively. Due to the very small breakdown voltage for the low doped InAs epilayers, L2 and L4 in Fig. 1, the doping of the epilayers was reduced slightly to a constant value of  $1 \cdot 10^{17} \text{ cm}^{-3}$  which gives a breakdown voltage of 2 V and a length of 179 nm for the L2 and L4 epilayers.

The structure chosen for further study in the InAs/AlSb/InAs material system was the following: L1 = 100 nm with  $N_d = 3.4 \cdot 10^{18} \text{ cm}^{-3}$ , L2 = 150 nm with  $N_d = 1 \cdot 10^{17} \text{ cm}^{-3}$ , L3 = 14 nm with  $N_d = 5 \cdot 10^{15} \text{ cm}^{-3}$ , L4 = L2, L5 > L1.

Since the barrier length is chosen to be 14 nm thick, the tunneling current may for such a thin barrier not be negligible in reality, especially not at room temperature, why a thicker barrier may be more appropriate. The total current through the SBV-diode consists of (i) the dc-current, mainly thermionic current, and (ii) the displacement current due to the rf-voltage variation over the depletion region. Increasing the dc-current compared to the displacement current makes the tripler work more in a varistor mode with a reduced efficiency, see Fig. 11.

It is assumed in the simulations that the same IV and CV characteristic calculated for a GaAs based SBV-diode can also be used for InAs based diodes, of a similar design. This assumption is due to the fact that the difference in conduction current, see Fig.4, between InAs and GaAs diodes at a fixed bias voltage, has been found to have a negligible influence on the efficiency, see Fig. 11.

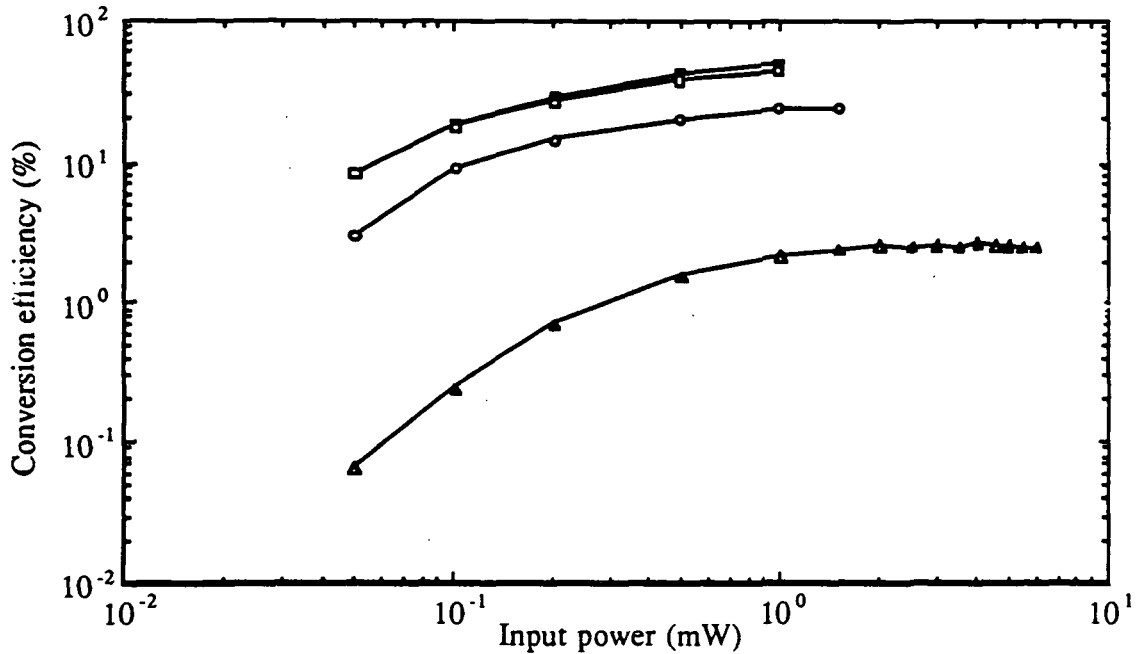


Fig. 11 Calculated conversion efficiency versus input power, when varying the calculated conductance,  $dI/dV$ , for the device in steps of  $(dI/dV) \cdot 10^y$ , where  $y$  is 0, 1, 2 or 3.  $N_{ds} = 3.4 \cdot 10^{18} \text{ cm}^{-3}$ ,  $N_{de} = 1 \cdot 10^{17} \text{ cm}^{-3}$ ,  $N_{db} = 5 \cdot 10^{15} \text{ cm}^{-3}$ ,  $L1 = 100 \text{ nm}$ ,  $L5 = 100 \text{ nm}$ ,  $L2 = L4 = 150 \text{ nm}$ ,  $L3 = 14 \text{ nm}$ , diameter  $a = 2 \text{ } \mu\text{m}$ . (■):  $y=0.0$ , (□):  $y=1.0$ , (○):  $y=2.0$ , (△):  $y=3.0$

Three different multiplier configurations for generating the desired output power of  $\geq 50 \text{ } \mu\text{W}$  at 750 GHz have been investigated, see Fig. 12. In the calculations was the effect on the series resistance from the plasma resonance included.

Due to the different frequencies for pumping the 750 GHz SBV-diode multipliers, see Fig. 12, the expected maximum available input power differs considerably, as shown in the figure. It should be observed that 11 mW of output power from a 250 GHz Schottky-varactor diode tripler, see Fig. 12, is achieved at operating conditions close to the Schottky diode burnout [9]. Thus a more realistic value of a maximum of 6 mW of output power was used for the 250 GHz tripler. In the calculations the maximum allowed input power was set to such a value that the rf-voltage  $V_{rf}$  over the device, minus the rf-voltage over the series resistance, is less than or equal to the breakdown voltage  $V_{br}$  of the low doped epilayer L2.

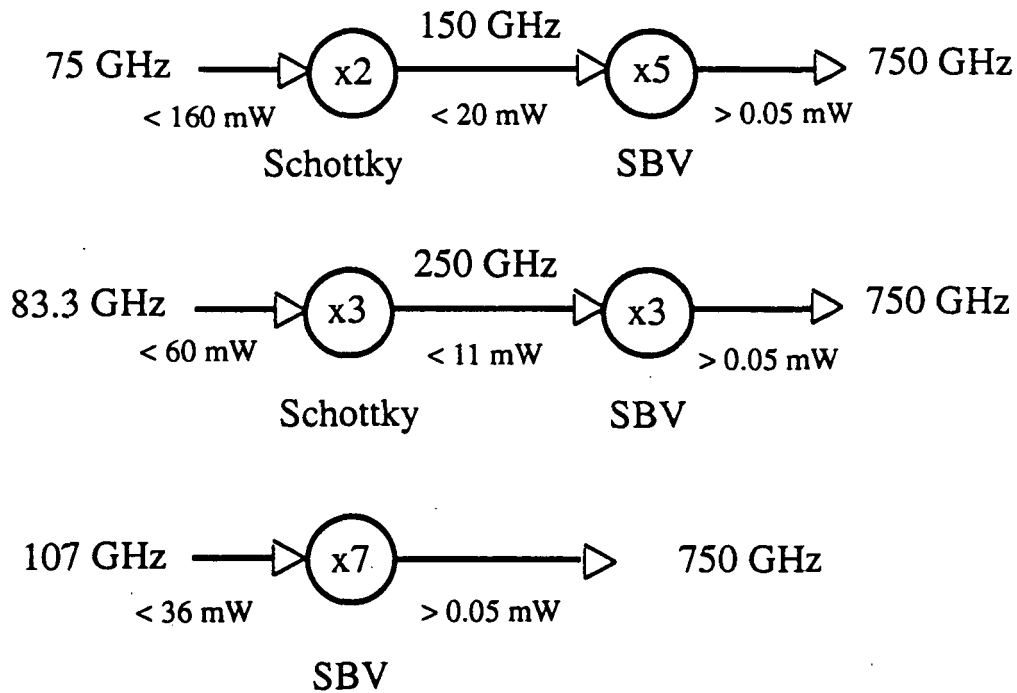


Fig. 12 The different 750 GHz multiplier configurations investigated in this study.

The conversion efficiency for 750 GHz SBV-diode multipliers using SBV-diodes based on InAs and GaAs is shown in Fig. 13. Simulations for two different contact resistances  $R_c = 8 \cdot 10^{-7}$  ohm $\text{cm}^2$  and  $1 \cdot 10^{-8}$  ohm $\text{cm}^2$  were used for the GaAs SBV-diodes, in order to evaluate what implications the choice of material has on the efficiency of the device. The higher electron mobility in InAs reduces the series resistance of the diode, thus giving InAs SBV-diodes an advantage in efficiency for low input powers over GaAs SBV-diodes, having the same ohmic contact resistance. This advantage in efficiency is even larger when a more realistic ohmic contact resistance,  $R_c$ , of  $8 \cdot 10^{-7}$  ohm $\text{cm}^2$  is used for the GaAs SBV-diodes. The efficiency of the multipliers increases with increasing multiplication rate, see Fig. 13, in principle in the same way for the different SBV-diodes. This is due to the fact that at lower frequencies the impedance (resistance  $R_V$  and reactance  $jX_V$ ) of the variable capacitance increases, i.e. becomes larger as compared to  $R_S$ . The efficiency is proportional to  $R_V / (R_V + R_S)$ , see ref.[10]. The cutoff frequency is defined in Eq. 1.

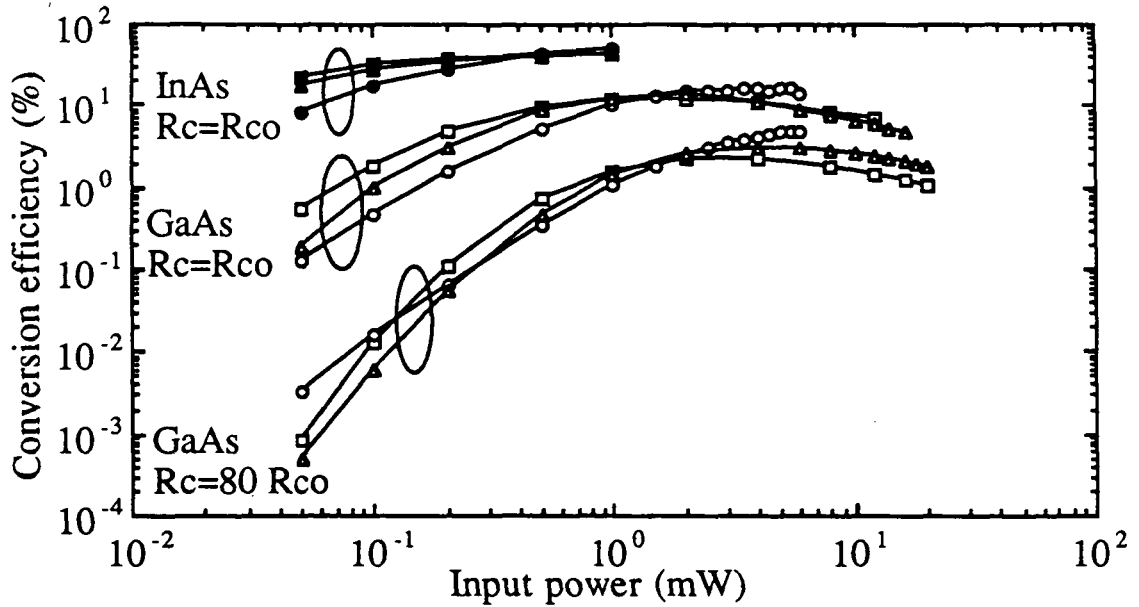


Fig. 13 Calculated conversion efficiency versus input power for various multiplier configurations, see Fig.12, using InAs and GaAs SBV-diodes as the nonlinear element. Two GaAs SBV-diodes having different contact resistances  $R_c$ , ( $=R_{CO}$  in the figure), are shown in the figure where  $R_{CO} = 1 \cdot 10^{-8}$  ohmcm<sup>2</sup>.  $N_{ds} = 3.4 \cdot 10^{18}$  cm<sup>-3</sup>,  $N_{de} = 1 \cdot 10^{17}$  cm<sup>-3</sup>,  $N_b = 5 \cdot 10^{15}$  cm<sup>-3</sup>,  $L_1 = 100$  nm,  $L_5 = 100$  nm,  $L_2 = L_4 = 150$  nm,  $L_3 = 14$  nm, diameter  $a = 2$   $\mu$ m.  
 (○): GaAs SBV-diode tripler, (Δ): GaAs SBV-diode quintupler,  
 (□): GaAs SBV-diode heptupler, (●): InAs SBV-diode tripler,  
 (▲): InAs SBV-diode quintupler and (■): InAs SBV-diode heptupler.

Using a larger diameter SBV-diode means of course a lower impedance, although it can handle a larger input power before  $V_{rf}$  exceeds the breakdown voltage  $V_{br}$ . A larger diameter device will also withstand larger thermal heating, caused by the absorbed pump power, before efficiency degradation occurs due to the reduced mobility of the electrons. The mobility  $\mu$  of the electrons is proportional to the temperature  $T$  of the material, where for GaAs:  $\mu \sim T^{1/2}$  and for InAs:  $\mu \sim T^{3/2}$  [11][12]. Thus InAs is more sensitive to thermal heating. However, since the breakdown voltage for InAs material is small compared to GaAs, the level of the absorbed power is restricted from that point of view. The influence of the thermal characteristics of the SBV-diode on the efficiency is not taken into account in this study.

The calculated output power, using the values for the efficiency shown in Fig. 13, is shown in Fig. 14. The simulated output power for a state of the art 2.8 fF Schottky-varactor diode described in [13], is also shown in Fig. 14 where it can be seen that the maximum output power for the Schottky-varactor diode clearly exceeds the output power for GaAs SBV-diodes having a contact resistance of  $8 \cdot 10^{-7}$  ohmcm<sup>2</sup> ( $80R_{CO}$ ), for the same input power. However, it should be noted that output powers comparable to the Schottky-varactor diode tripler are achieved from the InAs SBV-diode multipliers at much lower input power, even though the Schottky-varactor diode is capable of generating at least twice the output power compared to the InAs SBV-diode before the diode voltage exceeds the breakdown voltage for the device.



It should be noted that the calculations for the Schottky-varactor tripler assume optimum match at all frequencies for the tripler, i.e. including the idler. For the SBV-diode tripler is optimum match only considered for the input and output frequencies. Thus the matching conditions are much easier to obtain for the SBV-diode compared to the Schottky-varactor diode, in reality giving the SBV-diode an advantage in efficiency compared to the Schottky-varactor diode. Also the unavoidable resistive losses at the idler frequency in the Schottky-varactor diode tripler gives the SBV-diode tripler an even greater advantage.

The expected losses in the 750 GHz tripler mount is assumed to be less than 10 dB. However it can be seen from Fig. 14 that the only realistic SBV-diodes capable of generate  $\geq 500 \mu\text{W}$ , necessary for  $\geq 50 \mu\text{W}$  of output power at 750 GHz are InAs based diodes, even though this is achieved close to or at the breakdown voltage  $V_{br}$  limit for the InAs devices. Although the breakdown voltage  $V_{br}$  and thereby also the maximum allowed absorbed input power for the InAs SBV-diodes are much smaller than for the GaAs SBV-diodes, it can be compensated for by connecting several InAs/AlSb junctions in series, creating a multiple barrier InAs SBV-diode.

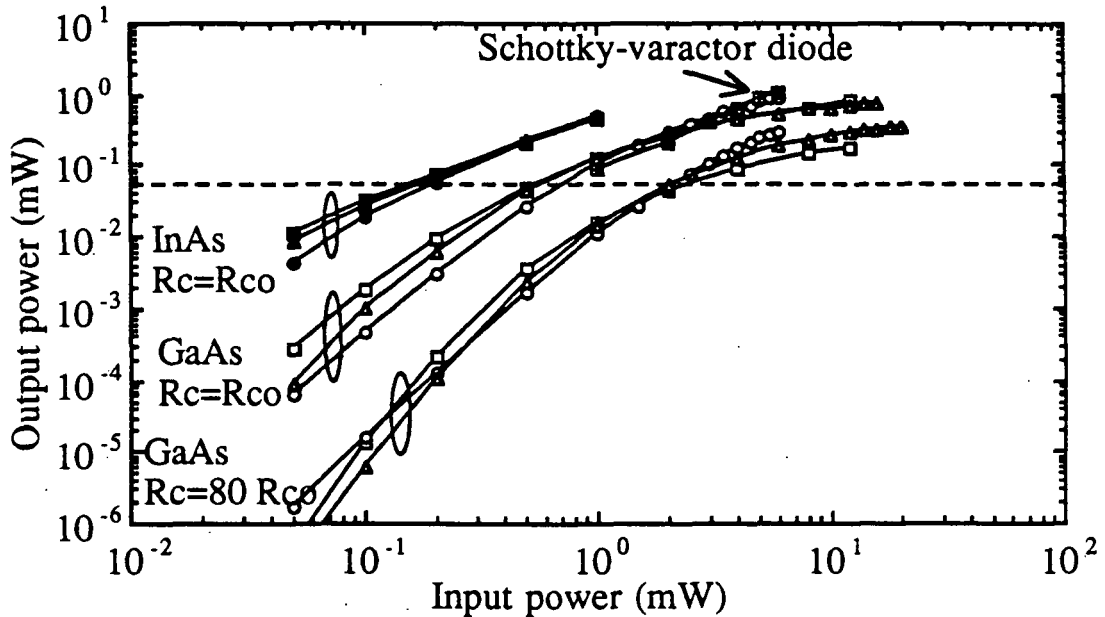


Fig. 14 Calculated output power versus input power for various multiplier configurations, using InAs and GaAs SBV-diodes and a Schottky-varactor diode as the nonlinear element in the multiplier. Two GaAs SBV-diodes having different contact resistances  $R_c$ , ( $=R_{co}$  in the figure), are shown in the figure where  $R_{co} = 1 \cdot 10^{-8} \text{ ohmcm}^2$ ,  $N_{ds} = 3.4 \cdot 10^{18} \text{ cm}^{-3}$ ,  $N_{de} = 1 \cdot 10^{17} \text{ cm}^{-3}$ ,  $N_b = 5 \cdot 10^{15} \text{ cm}^{-3}$ ,  $L_1 = 100 \text{ nm}$ ,  $L_5 = 100 \text{ nm}$ ,  $L_2 = L_4 = 150 \text{ nm}$ ,  $L_3 = 14 \text{ nm}$  and diameter  $a = 2 \mu\text{m}$ .

(O): GaAs SBV-diode tripler, (Δ): GaAs SBV-diode quintupler,  
 (□): GaAs SBV-diode heptupler, (●): InAs SBV-diode tripler,  
 (▲): InAs SBV-diode quintupler, (■): InAs SBV-diode heptupler, and  
 (⊞): Schottky-varactor tripler with  $C_0 = 2.8 \text{ fF}$  and  $R_s = 20 \text{ ohm}$  [13].

It should also be noted that the GaAs SBV-diode,  $R_c = 8 \cdot 10^{-7} \text{ ohmcm}^2$ , could in principle be pumped by a much larger input power than 6 mW, used in Fig. 14, before the diode voltage exceeds the breakdown voltage  $V_{br}$  of the device.

The dotted line in Fig. 14 marks the minimum 50  $\mu\text{W}$  output power limit, which has to be exceeded, assuming no losses in the mount.

As can also be seen in Fig. 14, higher order InAs SBV-diode multipliers can be used for generating the necessary 500  $\mu\text{W}$  of output power. The penalty for using a higher order multiplier is more resistive losses due to a larger number of idler circuits.

#### 4. CONCLUSIONS

Theoretical work on multipliers show a maximum efficiency for a lower  $C_{max}$  to  $C_{min}$  ratio than expected. This has been shown both in simplified calculations as well as in full harmonic balance simulations. These findings have several implications. First, there is no need for a thin barrier. Secondly, a wider barrier reduces the current. This also make simulations easier. The  $C$  vs.  $V$  characteristics have been simulated from epilayer parameters and the impact of different doping structures on both the  $CV$  and the efficiency for the multiplier has been presented. The examples presented can be used as *design rules*. In a case study for a 750GHz multiplier an InAs SBV diode outperforms a Schottky diode.

#### 5. ACKNOWLEDGEMENTS

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