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A FUZZY CONTROL DESIGN CASE: THE FUZZY PLL

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ABSTRACT

The aim of this paper is to present a typical fuzzy control design case. The analyzed controlled systems are the phase-locked loops -- classic systems realized in both analogic and digital technology. The crisp PLL devices are well known.

Introduction

To evidence the requirements of the analyzed case, in this first part of the paper, a review of the PLL systems and their applications is made.

The phase-locked loops (**PLL**) are devices that perform the phase control of an oscillator (see **Figure 1**). As any crisp control can be turned into a fuzzy control, the idea of the fuzzy-controlled PLL (**FPLL**) **[2], [3], [4]** is natural. Of course, one has to analyze if such a control is beneficial or not. This last problem is only partly analyzed here, more details being given in papers **[2], [3], [4],** to which the reader is refereed.

The PPL concept dates to the early days of radio technology.

Phase-Locked Loops (PPLs) devices are systems primarily aimed to generate signals in phase with the input (control) signal phase, while the input signal is (slowly) changing. If the input signal is noisy, the output signal should follow the carrier (basic signal) phase. Thus, the PLL can act as a nonlinear bandpass filter tuned by the incoming signal. In fact, the PLL recreates the original signal rather than to just filter the input signal.

The PLL basically consists in two circuits: a

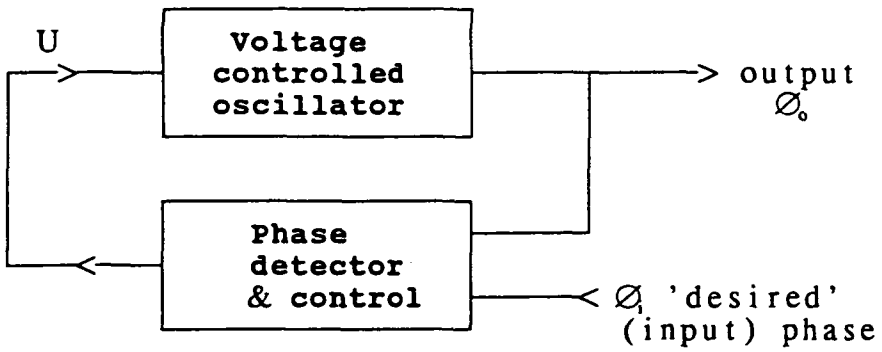

Figure 1: Basic PLL device

controlled signal generator (voltage controlled oscillator - VCO) and a phase detector & control circuit (PD-C). As the control signal is an estimate of the phase (or a function of it), the PLL can be used in demodulation purposes (frequency or phase demodulation). The PLL can also be used in amplitude demodulation, as it generates a constant level output signal, as required by the amplitude demodulators. Moreover, PLLs are used in frequency synthesizers. In this application, a fixed precise generator provides the input signal and the control loop includes a frequency divider to allow for frequency changes. Industrial applications such as motor-speed control were also announced [7]. Other applications include signal synthesis [8].

In many such applications, the dynamical characteristics of the PLL play an important part, mainly the acquisition time and the noise immunity. The time needed to reach the quasi - stationary regime, for a given hop in frequency/phase is most usually determined in terms of equivalent number of periods. This characteristics is important in frequency demodulators and in fast switching frequency synthesizers that must often change the output frequency. (Such devices are used for example in frequency hopping system). Noise output spurious signal suppression power versus noise input power is important in (tele)communications applications such as carrier recovery [9].

In the last two decades PLLs turned from the analog technology to the digital one, due to some important advantages: high frequency range (up to 30 MHz in monolithic integrated circuits), insensitivity to changes in temperature and power-supply voltage, programmable bandwidth and center frequencies.

Moreover, in the digital technology, very high quality factors (i.e. narrow - bandwidth) loops can be achieved, and high order loops are easy to construct by simple cascading operation. Unlike the analog PLLs, where the error signal provided by the phase detector (PD) corrects the (analog) VCO frequency, in usual, digital PLLs the error signal controls the direction of on up - down counter.

Much used are devices from the class of integrated (monolithic) hybrid PLLs. These devices include an analog VCO and low pass filter (LPF), and a digital PD and digital dividers.

Such devices are usually manufactured in CMOS (Complementary-symmetry Metal-Oxide-Semiconductor) or TTL (Transistor-Transistor-Logic) technology and a classical example is the 4046 circuits. (Such devices are often named "digital PLLs" although they are hybrid, while the true digital PLLs are named "all - digital PLLs").

The classic PLL device

In the usual analogic PLLs, the phase control is got by a linear (P) control loop, i.e.

$$U = k*(\varnothing_o - \varnothing_i) \qquad (1)$$

$$\Delta \varnothing_o = \gamma * U \qquad (2)$$

where $\Delta\varnothing_o$ is considered as the phase shift per second. (Indeed, the frequency change is controlled by U, rather then by the phase).

More exactly, in an analogic PLL, the relations are:

$$U = k^* <(\varnothing_o - \varnothing_i)> \qquad (3)$$

$$\Delta \varnothing_o = \gamma * U \qquad (4)$$

where < .. > stands for the mean value, obtained by integration over a fixed time period. Thus, the control is of proportional-integral type (PI).

The difference $\varnothing_o - \varnothing_i$ is performed by the block named 'phase detector'. The integration (average value) in eq. (3) is realized by a block named 'low-pass filter'. The complete block diagram of the basic PLL system is sketched in **Figure 2.**

Turning the crisp control into a fuzzy control

Obviously, such a control as described by eqs. (1) and (2) can be performed in a quasi-linear, or in a nonlinear manner, by using a simple fuzzy control system followed by a defuzzifier block (**Figure 3**).

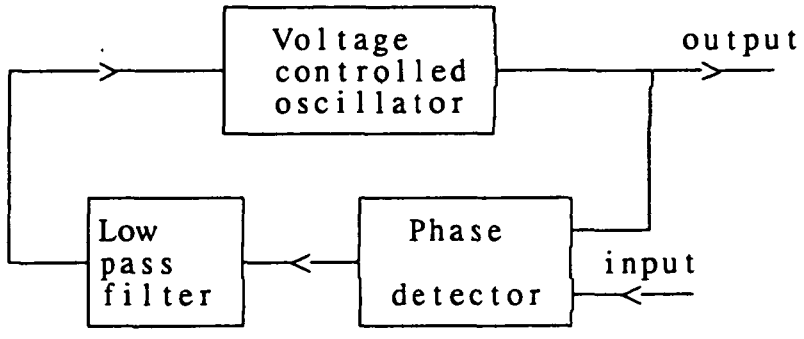

Figure 2: Basic diagram of the classic PLL

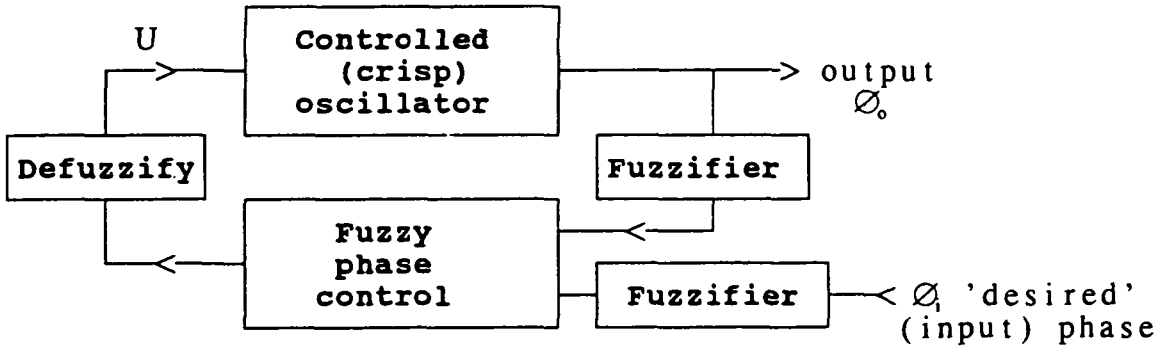

Figure 3: Basic fuzzy PLL device (FPLL)

The linguistic -- and, with appropriate definitions of the membership functions, the fuzzy -- control for a classic, linear PLL system can be described by such simple rules as below:

If $\varnothing_o - \varnothing_i$ is Negative Big THEN U is Positive Big

If $\varnothing_o - \varnothing_i$ is Negative Small THEN U is Positive Small

If $\varnothing_o - \varnothing_i$ is Zero THEN U is Zero

If $\varnothing_o - \varnothing_i$ is Positive Small THEN U is Negative Small

If $\varnothing_o - \varnothing_i$ is Positive Big THEN U is Negative Big

If the membership functions assigned to the above linguistic (input, and respectively output) degrees are equal, isosceles triangles, then the performed control is almost linear. If the triangles have unequal bases, given by a nonlinear law (e.g. **Bi = exp(a*i)**), then the control is nonlinear, approximating the according law. For more details on the characteristic functions of defuzzified fuzzy systems, see **[5]** and the following chapters. Fuzzy control of the PLLs change them into intelligent devices: they behave much similar as if a human operator controls the phase locking process. This has some benefits and some costs. Nonlinear type fuzzy control can be beneficial in PLLs because it can improve the convergence rate of the phase-locking process, and also can improve the noise rejection performance **[2], [3], [4].** On the other hand, using fuzzy control increases the complexity and cost of the systems and can lower the maximum operating frequency of the loop, due to the high amount of computation required by the fuzzy control.

A more complex control, taking into account both the phase and its variation (got by means of the difference between the actual and previous values of the phase) is increasing the loop performance. Such a control is illustrated in Figure 4.

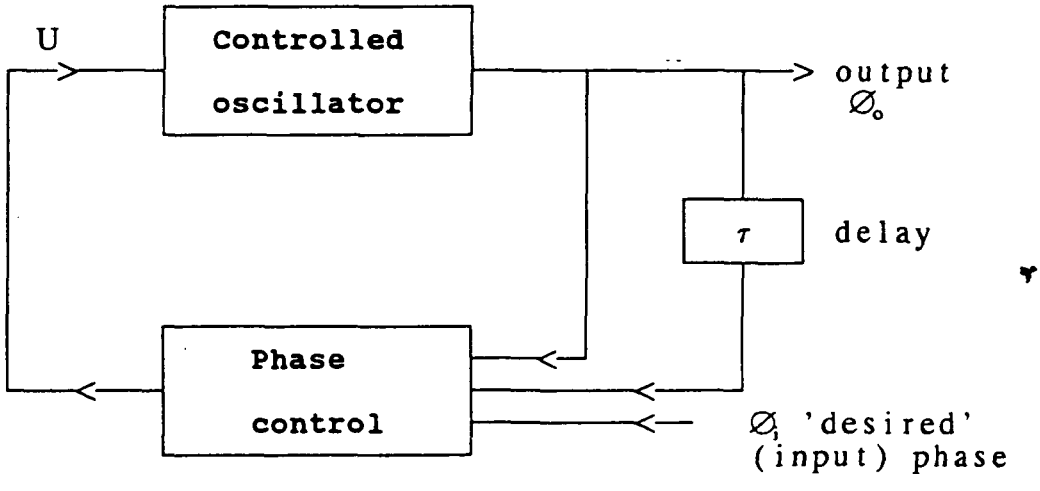

Figure 4: PLL device with double input control

An example of natural control rules for such a control is ($\Delta\varnothing_n$ and $\Delta\varnothing_{n-1}$ mean the differences $\varnothing_o$ - $\varnothing_i$ at the moments t_n and t_{n-1}, respectively):

If $\Delta\varnothing_n$ is Negative Big AND $\Delta\ \varnothing_{n-1}$ is Negative Big
THEN U is Positive Very Big

If $\Delta\varnothing_n$ is Negative Big AND $\Delta\ \varnothing_{n-1}$ is Negative Small
THEN U is Positive Big

If $\Delta\varnothing_n$ is Negative Big AND $\Delta\ \varnothing_{n-1}$ is Zero
THEN U is Positive Low

.....

If $\Delta\ \varnothing_n$ is Positive Low AND $\varnothing_{n-1}$ is Positive Low
THEN U is Negative Very Big

If $\Delta\ \varnothing_n$ is Positive Big AND $\varnothing_{n-1}$ is Positive Big
THEN U is Negative Very Big

If $\Delta\ \varnothing_n$ is Very Big and $\Delta\ \varnothing_{n-1}$ is Very Big
THEN U is Negative Very Very Big

Even at the linguistic description level, the controlled system can behave in an unstable (e.g. oscillating) manner. The global, linguistic stability is very easy to check: the system is stable iff the state transition graph does not include any cyclic sub-graph.

The all digital PLL fuzzy control schematic

Although analogic PLLs are largely used, for demanding applications, they are surpassed by the all-digital PLLs. In what follows, only digital PLL type will be addressed.

An all-digital PLL presented in [1] is claimed to have a good dynamic behavior and a very good rejection of the input phase noise because of the adaptive phase detector it contains. Its transfer characteristic (figure 5) is non-linear so that the phase detector output is zero for phase error absolute values greater than $2\phi_R$. Keeping $\phi_R = \pi/20$ as long as the loop is locked, the PLL completely rejects the input phase noise greater than $\pi/10$, and strongly reduces the one smaller than this value. The phase detector adaptivity consists in changing ϕ_R in accordance with the actual phase error value and maintaining the characteristic top corner abscissa close to it. The characteristic may, also, be translated along the vertical axis in order to cope with the phase detector input signals frequency difference.

The phase noise rejection reported in [1] was confirmed by our computer simulation of the all digital PLL, that yields a curve $Z_{out} = f(Z_{in})$ very closed to that presented in [1]. The same computer simulation shows an about 25 iterations phase locking process for a 3 radian step in the input phase error (figure 6). The transient regime is considered to end when the input

phase error becomes smaller than 0.01 radian (about one tenth from the minimum value of the crisp PLL transfer characteristic turning point abscissa - figure 5).

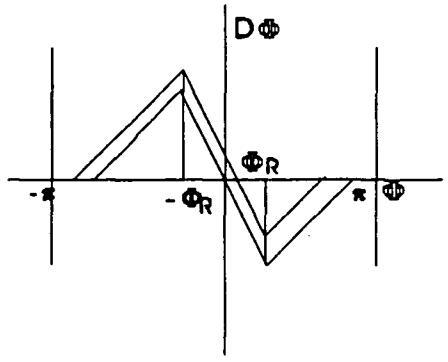

Figure 5: Crisp PD transfer characteristic

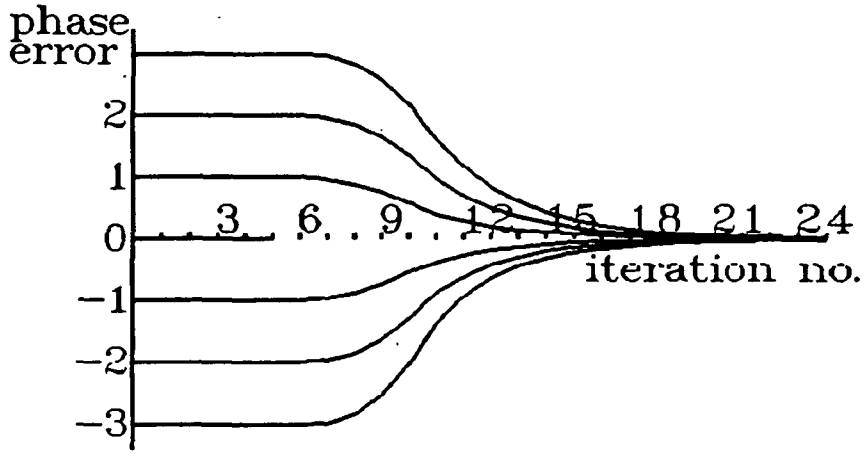

Figure 6: Crisp PLL phase locking transient response

This performant phase detector with non-linear adaptive characteristic is ideally suited to be replaced by a fuzzy control circuit, which is more flexible in design and operation, and may improve the PLL parameters. A possible way to introduce the fuzzy control (figure 7) is suggested in [4]. A fuzzifier circuit yields a 5 degree linguistic variable both for the actual and the previous phase error values. The fuzzy control circuit outputs the truth values for the 11 degrees of an linguistic variable by using inference rules of the above mentioned type:

IF ϕ_{n-1} is NB **AND** ϕ_n is NS **THEN** $D\phi$ is NVB

The phase error is denoted as ϕ, the output correction - as $D\phi$, and the linguistic variable degrees - as NVB (from Negative Very Big), NS (Negative Small) a. s. o. The all 25 rules used by the inference machine and presented in figure 8 are a "fuzzy model" for the phase detector operation in accordance with the authors' "feeling". A defuzzifier circuit produces a crisp correction value by means of the gravity center method.

The transfer characteristic of the phase control circuit from the actual phase error input to the crisp correction output is a rational fraction of 3 degree polynomials [3]. Its expression

[4] (eq. 5 for $\phi_{n-1} = 0$) shows that the fuzzy control circuit has a strongly non-linear characteristic and its shape is easily controlled by means of the inference machine architecture. The actual shape induced by the inference rules from figure 8 is presented in figure 9.

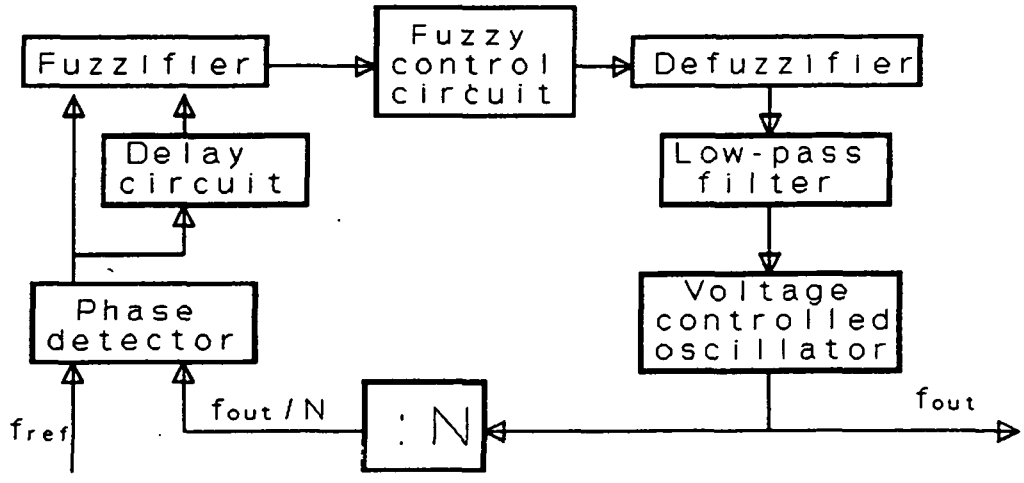

Figure 7: FPLL skeleton diagram

$$\phi_G = D\phi(0, \phi_n) = \begin{cases} \frac{\pi}{5} \frac{14\phi_n^2 + 23\pi\phi_n + 5\pi^2}{4\phi_n^2 + 6\pi\phi_n + \pi^2}, & -\pi \le \phi_n \le -\frac{\pi}{2} \\ \frac{12\pi}{5} \frac{\phi_n^2 + \pi\phi_n}{8\phi_n^2 + 4\pi\phi_n - \pi^2}, & -\frac{\pi}{2} \le \phi_n \le 0 \\ -\frac{12\pi}{5} \frac{\phi_n^2 - \pi\phi_n}{8\phi_n^2 - 4\pi\phi_n - \pi^2}, & 0 \le \phi_n \le \frac{\pi}{2} \\ -\frac{\pi}{5} \frac{14\phi_n^2 - 23\pi\phi_n + 5\pi^2}{4\phi_n^2 - 6\pi\phi_n + \pi^2}, & \frac{\pi}{2} \le \phi_n \le \pi \end{cases} \quad (5)$$

phase error n-1

phase error n	NB	NS	Z	PS	PB
NB	PUB	PUB	PB	PM	PS
NS	PUB	PB	PM	PS	PUS
Z	PS	PUS	Z	NUS	NS
PS	NUS	NS	NM	NB	NUB
PB	NS	NM	NB	NUB	NUB

Figure 8: Inference rule set

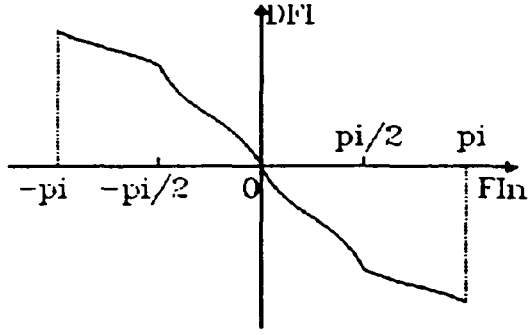

Figure 9: Fuzzy PD transfer characteristic

2. Fuzzy controlled PLL (FPLL) parameters

The FPLL dynamic behavior and noise properties are checked by means of the computer simulation. As figure 10 shows the FPLL needs only 10 iterations to get phase lock for the same step in input phase error, while maintaining the same great input phase noise rejection (figure 11 - Z_{out} and Z_{in} are the input and output phase noise effective values, respectively).

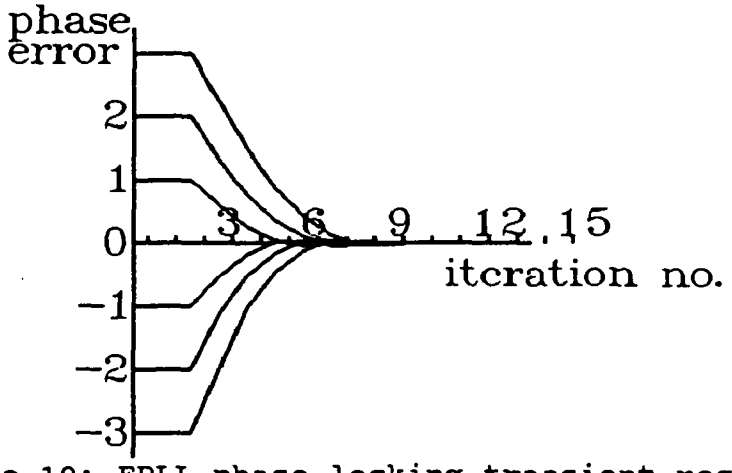

Figure 10: FPLL phase locking transient response

The dynamic behavior is further improved by changing the membership function shape. For a square root function, the number of the iterations till phase locking decreases to about 9. The same is the result of unequal base triangular membership functions.

The FPLL frequency acquisition regime is, also, greatly improved by the fuzzy control [4].

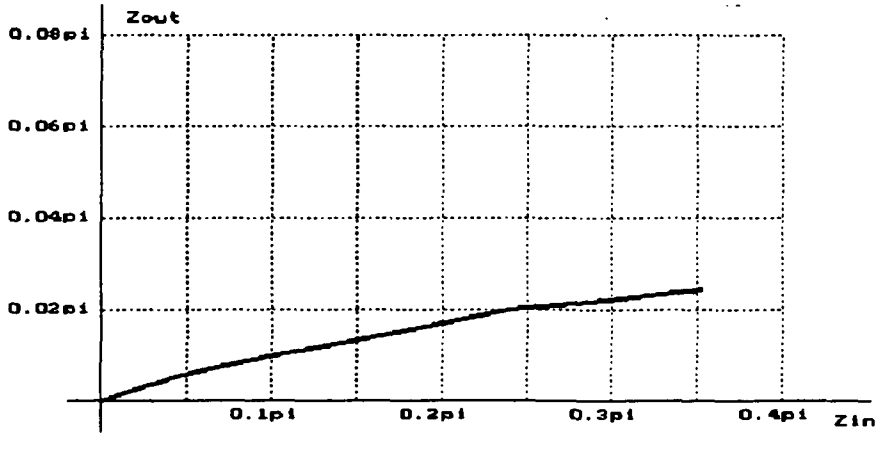

Figure 11: FPLL input phase noise rejection

Some practical design hints: turning a crisp control into a fuzzy control

Fuzzy control of a crisp system asks for a fuzzifier block in front of the fuzzy control block, and of a defuzzifier block at the output. In other words, the overall control is a crisp control, and the fact that the way the control is performed is fuzzy is not seen by the controlled system. Supposing the defuzzification is realized by the center of gravity method, it is easy to determine the crisp input-to-output (characteristic) function of the equivalent crisp control.

Suppose now that the control characteristic function has to pass through a given number of fixed points in the input-to-output (xy) plane. (Only the problem of one-input, one-output control is discussed here, for sake of brevity). Let these points be:

$$\{(x_k, y_k) / k = 1,2,.., n\}.$$

Also suppose that the type of membership functions is fixed, and all the membership functions $x\sim_k$, $y\sim_k$ are unimodal, and they attain the value 1 in just one point:

$$\mu_{x\sim k}(u) = 1 <=> u = x_k; \mu_{y\sim k}(v) = 1 <=> v = y_k.$$

For example, the membership functions can be triangular, sinusoidal, Gaussian a.s.o. Then, the control system is simply designed by using the following rules:

1. choose the membership functions width such as they overlap only two by two;
2. choose the membership functions vertices such as their coordinates are (x_k, y_k);
3. establish the rules describing the system in the form:

If input is $x\sim_k$, Then output is y_k.

Then, the defuzzified output will pass through the given points.

If a two-input system is to be designed being given the points:

$$\{(x_{1k}, x_{2k}; y_k) / k = 1,2,.., n\},$$

the same procedure has to be observed.

Usually, the final step of your design must be the computer simulation, to check for the results.

Conclusions

An analysis example of fuzzy control design problem was presented. The analysis was applied to the concepts of fuzzy controlled PLL.

The fuzzy control of classic analog PLLs is easy to design because the control system has to be a monotonic one. Then, the rules are derived in a very natural manner. The control can be easily changed, either by changing the rules, or the membership functions. The rules can be changed either by introducing new linguistic degrees, or by re-defining the input-to-output mapping of the linguistic degrees. Thus, this design case is most suitable in the classroom.

In the case of adaptive PLLs, the control is more intricate, and an adaptation of the control system configuration, rules and membership functions is needed.

It was shown by computer simulation that the suitably designed fuzzy control greatly improved the dynamic behavior of all digital adaptive PLL, while maintaining the input phase noise suppression properties of the original crisp PLL

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