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AN INTEGRATED EDDY CURRENT DETECTION AND IMAGING SYSTEM ON A SILICON CHIP

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I. INTRODUCTION

Eddy Current probes have been used for many years for numerous sensing applications including crack detection in metals. However, these applications have traditionally used the eddy current effect in the form of a physically wound single or differential probe pairs which of necessity must be made quite large (order of a tenth of an inch) compared to microelectronics dimensions. Also, the traditional wound probe can only take a point reading, although that point might include tens of individual cracks or crack arrays, thus conventional eddy current probes are beset with two major problems: (1) no detailed information can be obtained about the crack or crack array -- simply that local inhomogeneties exist in the region (which just as well could be other surface defects) and (2) for applications such as quality assurance, a vast amount of time must be taken to scan a complete surface, even if robotic applications are used for a physical scan of the surface.

Laboratory efforts have been made to fabricate linear arrays of single turn probes in a thick film format on a ceramic substrate (hybrid technology) as well as in a flexible cable format, however such efforts inherently suffer from relatively large size requirements as well as sensitivity issues.

This paper describes PRELIMINARY efforts to extend eddy current probing from a point or single dimensional level, fully to a two-dimensional micro-eddycurrent format on a silicon chip which might overcome all of the above problems. Moreover, using a serial readout of rows and columns one might be able to achieve eddy current imaging. Thus the scanning (within the area of the chip) would be electronic rather than physical, resulting in an essentially instantaneous scan when compared to the physical scan method. Moreover, although the demonstration vehicle herein described is only a 10 x 10 array on a silicon chip of the order of .25 to .5 inch square, the ultimate chip could consist of an array covering a complete wafer of pizza size (four to eight inches in diameter). Also, in sufficiently thin silicon materials, the surface can conform to non-planar topographies. Also, in sufficiently thin silicon materials, the surface can conform to non-planar topographies.

If successful, the pixel size (based upon integrated eddy current coil size) might range of the order of a thousandth of an inch or smaller, although in our test the coil the spacing is of the order of 5 to 15 thousandths of an inch. This opens up the possibility of a resolution within the typical width of a crack, thus allowing identification of much smaller cracks, early onset of material fatigue from microcracks, classification of cracks and even imaging. Furthermore, with sufficient sensitivity it potentially becomes possible to resolve such things as surface smoothness, grain boundaries and material homogeneity, as fine structure or super fine structure on the signal response. Such a device might also be placed permanently for ongoing health monitoring at critical fatigue points in the vehicle.

There is no other technology but the integrated circuit lithographic technique which allows such miniaturization, resolution and replication uniformity. For example, the masks used for fabricating the geometries were generated by electron beam with a submicron resolution and line uniformity of the order of 0.1 micrometers.

A variety of chip sizes have been made, each consisting of a 10 x 10 array as shown in Fig. 1. Each of the 100 pixels or coil combinations shown in Fig. 2 consists of two flat coils in a "Manhattan" geometry (rectangular) for maximum area utilization, a primary and a secondary. Figure 3 is a scanning electron micrograph of a similar coil, showing a better prespective of the topography. The flat coils are aluminum, separated by insulating silicon dioxide. Figure 4 is an expanded view of the center region of one coil pair.

The aluminum thin film (about a micron thick and typically about 6 to 10 microns wide) lies on two levels, including a return path under the coils, again insulated by a silicon dioxide layer. The silicon substrate simply serves as a convenient substrate into which the initial silicon dioxide layer can be thermally grown using conventional integrated circuit techniques. The other silicon dioxide layers were formed using conventional CVD (chemical vapor deposition) techniques where silane is oxidized at an elevated temperature. The resulting devices (chips) were mounted in a conventional in-line integrated circuit package as shown in Fig. 5. (However it is envisioned that ultimately, vastly larger arrays will be used, requiring special packages.) The chips were encapsulated in a high grade commercially available polymer.

Commercially-available finite-element magnetic field software (MSG-MAGGIE) is being used to model the system and to test improved designs beyond the present demonstration vehicle. Devices have been tested using standard cracks 0.003 inches wide and a few mils deep. These have resulted in a signal above noise of about five percent, using a driving signal at one to ten megahertz.

A rastering circuit was developed for this system, but it was ultimately determined to be more useful to use commercially-available computerized impedance meters (such as those manufactured by Hewlett-Packard and others) which can be programmed to vary such factors as sampling time, settling time, frequency, differential signal between any selected set of coils, etc. However, an interface circuit was built using meter-actuated reed relays and multiplexing, to allow activation and indexing of each coil set (one at a time) in order to avoid inhomogenous mutual impedances and magnetic field couplings over the area of the array. These studies are presently in progress and the results look promising.

Actual imaging has not yet been attempted. Rather we are at this point simply plotting out the serial row-column signals and correlating these with crack sizes and other parameters.

III. BASIS OF THE DESIRED EDDY CURRENT EFFECT

According to Ampere's circuital law,

$$\oint \bar{H} \cdot d\bar{L} = NI$$

where the arbitrary closed line integral of the dot product of the magnetic field H with the vector differential length dL is equal to the ampere turns NI enclosed. Thus in a solonoid, whether of the conventional spreaded-out multi-layer type, or the present single-level coil type, the magnetic field generated in the central core is based upon the current I times the number of linked turns N. Thus for a given configuration, one need only increase the drive current for increased field for a proportional increased sensitivity.

The generated magnetic field from the primary coil is made to penetrate an adjacent electrically conducting material where cracks (or other inhomogeneties) are being examined, such as a space engine material or structural element where imperfections or fatigue cracks are of interest. According to Lenz's law, if the magnetic field is varying in time, eddy currents will be induced in the various possible conducting paths of the subject material in such directions as to generate magnetic fields opposing the change.

These circulating eddy currents will cause a reflected impedance in the secondary coil of the device (wound inside the primary) which will in general consist of an induced or reflected resistance (R), inductive reactance (X_L) and capacitative reactance (X_C) or an overall complex impedence $Z \angle \Theta$ at a polar angle Θ. We are presently attempting to correlate these electrical parameters with fault analysis.

Of course each interwoven coil set (primary/secondary) will have its own resting impedence when contacted to air or other uniform material, therefore the first issue is to record in memory the reference impedance of each coil (with its associated external wiring/circuit impedance) when in contact with the reference or "perfect" material. Then a deviation from this reference should be indicative of the existence of a crack or other material imperfection. With sufficient resolution one should be able to distinguish various types of imperfections -- even to the extent of eddy current imaging.

One of the major problems which we have found is not so much the construction of identical on-chip devices, but rather the differing stray impedances of the individual wiring harness lines to the off-chip signal processing. Of course the ultimate answer lies in doing all preliminary signal processing on-chip, with appropriate buffering to the outside world. This level of integration, however, awaits a planned future level of effort after the present demonstration vehicle is adequately proven. We have every reason to believe, however, that complete on-chip processing of the row/column serial data can be done using bucket brigade or other standard techniques in the same silicon substrate (which at this point merely serves as a rather arbitrary physical substrate).

With elimination of external and wiring harness impedances, one should be able to eliminate the necessity for initial material referencing. It should then be sufficient to program the differential comparison of adjacent reflected impedances in order to sense the existence of local cracks. However for coil spacings of the order of and less than crack sizes, it will probably be necessary to add an integral term to reference the changing background at this level of resolution (unlike present eddy current probes which are much larger than the crack sizes being detected) to exist somewhere between the two coil sets. In this way one might distinguish the "forest from the trees". In fact, with sufficient chip uniformity and on-chip processing, absolute local values should be sufficiently meaningful. Fortunately, with our flexible software-based approach, we can arbitrarily vary the comparison formats among x-y elements in order to arrive at the most meaningful approaches.

Also, the HMTC sensors group has access to several picture and imaging processing experts; the results are not dependent on the originating signals being eddy currents versus conventional optical signals.

IV. DETECTABLE PARAMETERS

At this point integrated coil impedances run in the range of tens of ohms at one to ten megahertz. A crack in the range of a few mils wide will result in a change of impedance of the order of several percent when the sample is set against the packaged sensor array, which we estimate to be separated from the reference metallic (crack-containing) material by approximately 0.020 inch of encapsulating polymer. Since the field drops off at a rate somewhere between the square and cube of the distance, one should be able to increase the sensitivity by one to two orders of magnitude through closer proximity (say 2 or 3 mils). On the other hand, we wish to minimize the placement sensitivity.

Although the beginning reflected impedance of a given coil set ranges in the tens of ohms, we have found that we can obtain meaningful systematic changes in impedance at least out to the third decimal place when bringing an object in from some distance (say a few tenths of an inch away). Thus one can speculate that one might even be able to resolve such material properties as surface smoothness from grinding or processing, as well as more gross defects such as cracks, merely by segmenting gross changes from the fine and superfine structure in the reflected impedances.

As one would suppose, as one brings a metallic object into the proximity of the micro eddycurrent array, the reflected resistance and inductive reactance increase. However if one uses, for example, the human finger, the resistance component increases also (as one would expect, since eddy currents are being induced in the conducting skin), but the increasing reactive component is capacitive, i.e. $\Delta\Theta$ changes size. We interpret this to be due to the basic dielectric nature of the human skin, and the group (along with some physicians and biologists from the University of Cincinnati Medical School Perinatal Research Institute) is contemplating the possible use of this effect for characterizing the very sensitive skin of premature infants for heat and vapor loss characteristics.

Finally, we hope to also ultimately be able to add a third dimension to the crack probing technique by "chirping" the frequency when sampling each coil. The ordinary (inanimate) skin effect, particularly well known to all in the microwave field, would increasingly concentrate the eddy currents toward the surface of materials with increasing frequency. Thus a scan of frequency at each point during column and row rastering, could in principle provide a depth profile of the crack or defect for three-dimensional imaging.

V. POSSIBLE IMPROVEMENTS

Although we are only in the preliminary phases of this work, we can envision several ways to improve the sensitivity up to several orders in magnitude. These includes relatively simple issues such as (1) closer spacing of the coil array to the measurement surface, (2) higher drive current and dense multiple level spiral coils, as well as more involved but "doable" changes such as (3) on-chip processing or even (4) fabrication with high temperature superconductors (which we are contemplating in connection with our High T_C Superconductor Lab). Finally, it should be pointed out that the eddy currents are also induced in the silicon substrate, which merely represent a power loss. The use of deep impurities to increase the resistivity would suppress this loss.

VI. CONCLUSIONS

The present project is yet in its preliminary phases, but real devices have been built and are being evaluated in the form of a demonstration vehicle, particularly for crack detection in metals commonly used for aerospace propulsion systems and structures.

Crack detection results show impedance changes only in the range of a few percent, but improvements are theoretically possible in the range of orders in magnitude through reconfiguration.

It is felt that the potential exists here for three-dimensional imaging, as well as applications to an extended range of possibilities such as surface finishes and perhaps even grain boundaries and other material inhomogeneties.

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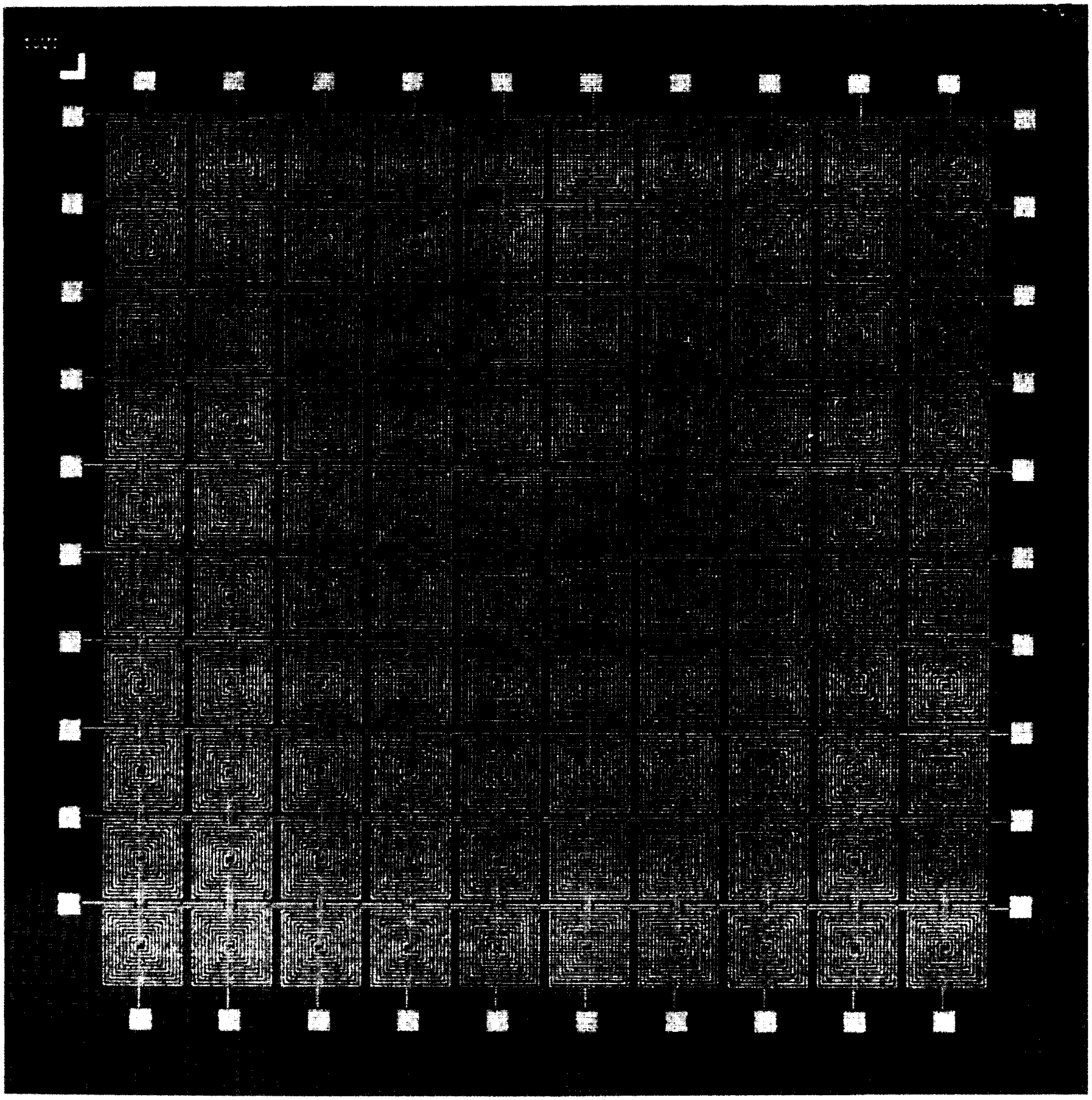

Fig. 1 10 x 10 eddy current coil array on a silicon chip, approximately 1/4 inch square. Each flat coil set consists of a primary for micro eddycurrent generation and a secondary for sensing reflected complex impedance. Each row and column may be externally addressed. Future models will have all signal conditioning on-chip to avoid the necessity for lead compensation.

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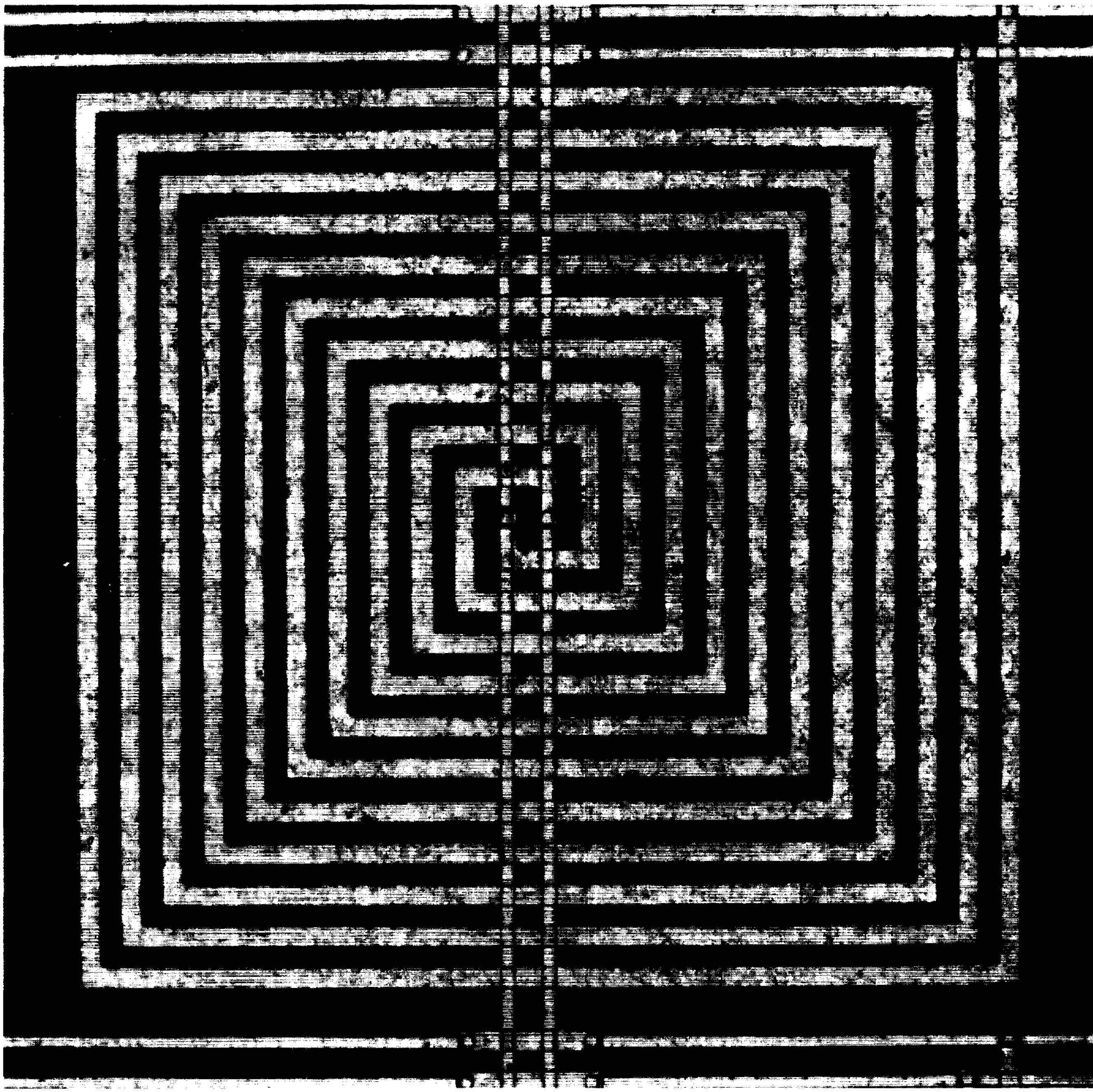

Fig. 2 Expanded view on one of the coil pairs (the two coils have been connected in series in this case for test purposes). The dark lines are aluminum leads, six microns wide in this case, separated by four microns of silicon dioxide.

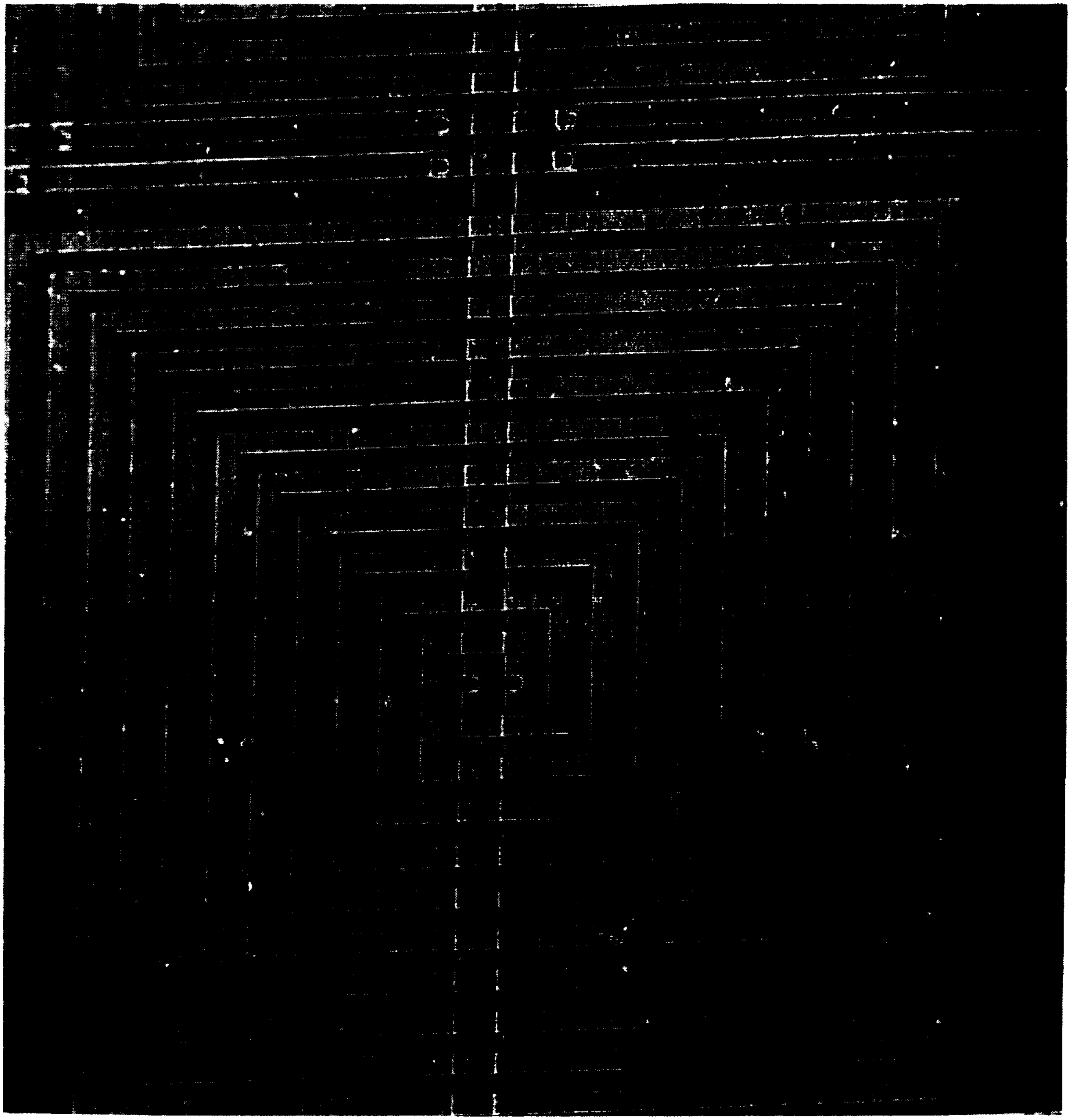

Fig. 3 Scanning electron micrograph of Fig. 2, except in this case the two coils are separated in the form of a primary and a secondary. At the center, each coil connects to a separate aluminum bus (insulated from the top metallization by a silicon device layer) so that all primary and secondary coils can be individually addressed.

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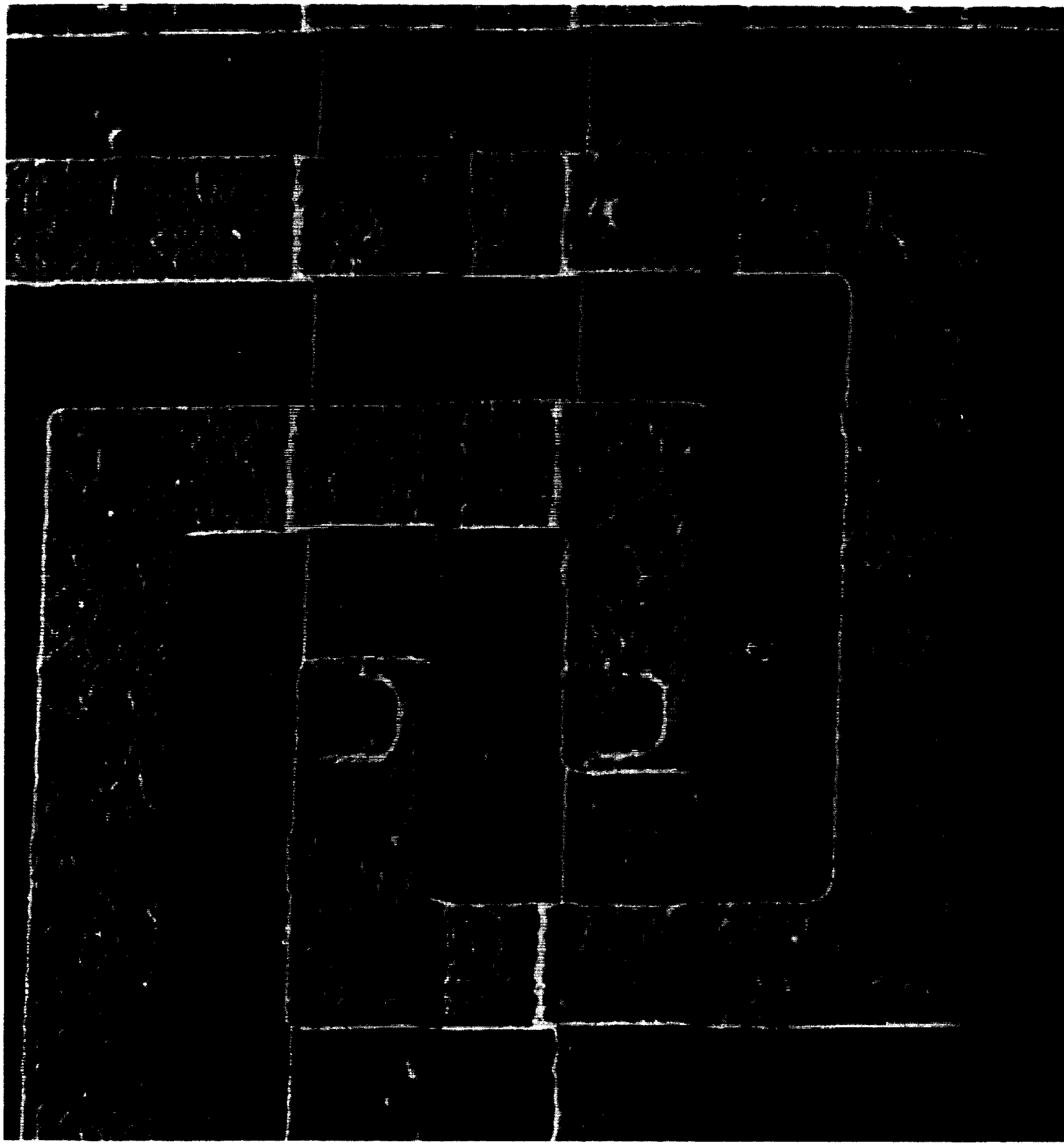

Fig. 4 An expanded view of the center region of Fig. 4, showing the connection of the top side six-micron aluminum leads connected to the lower leads through an intermediate silicon dioxide (about one micron) insulator. Edge definition generally shows a uniformity of two or three tenths of a micron. Note that the last loop can only link about twenty percent of the generating field, but there are five complete loops in the symmetrical primary/secondary coils.

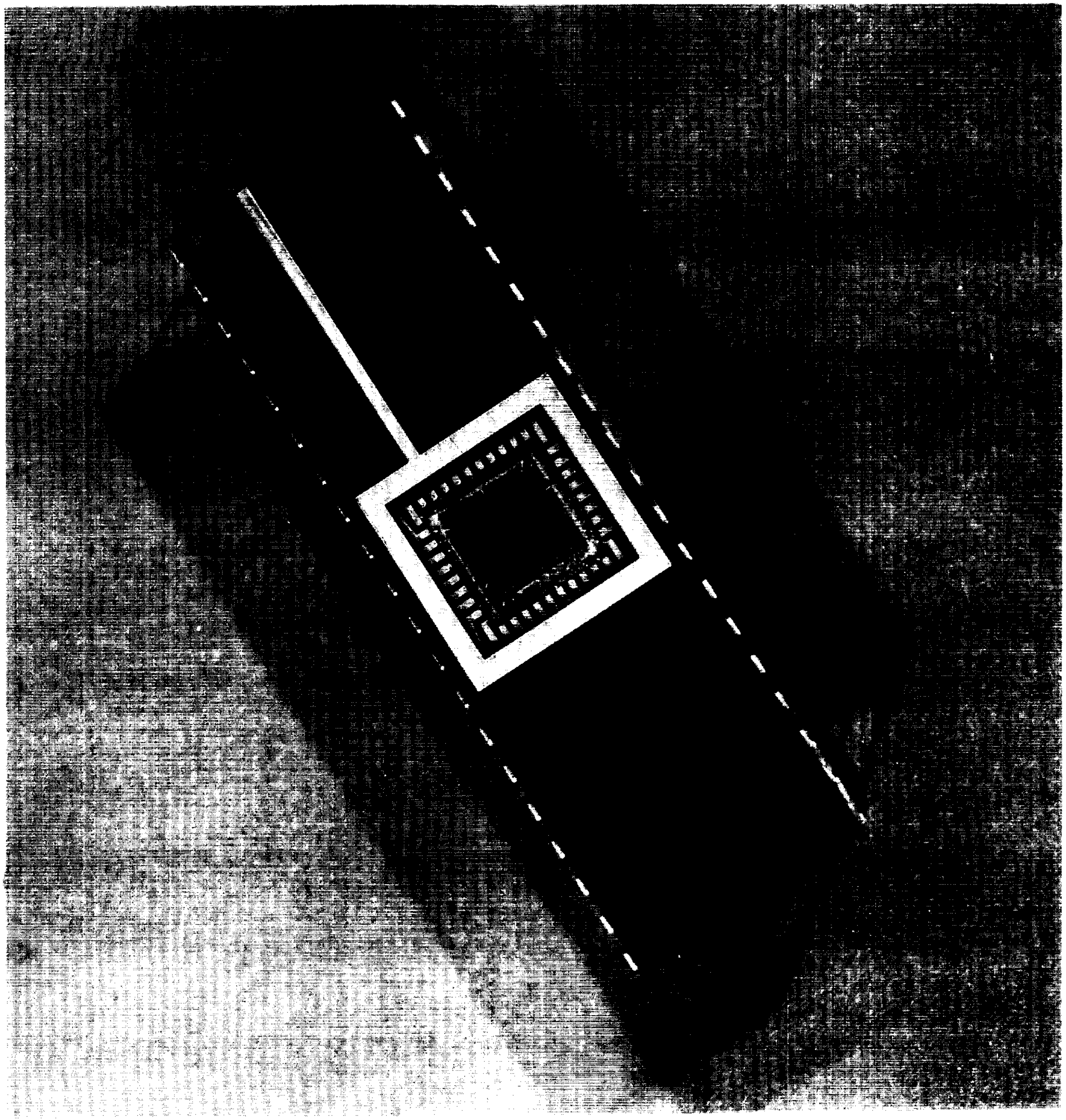

Fig.5 Sensor chip array mounted in a conventional in-line integrated circuit package.