Reliability in CMOS IC Processing

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Abstract - **Critical CMOS IC processing reliability monitors are defined in this paper. These monitors are divided into three categories: process qualifications, ongoing production workcell monitors, and ongoing reliability monitors. The key measures in each of these categories are identified and prioritized based on their importance.**

1 Introduction

IC process reliability starts with a clear description of the entire IC process from IC design through final shipment (Figure 1). In this flow the original development of the IC process, packaging process, test process, and shipping process are shown to the left of the main manufacturing process flow. New processes are expected to meet minimum reliability requirements. These requirements are typically referred to as new process qualification requirements.

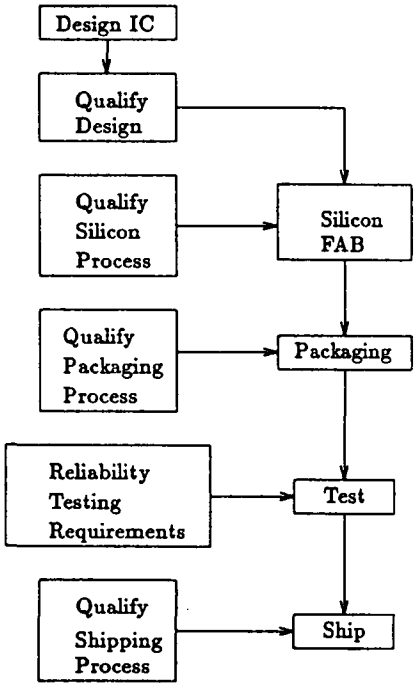

Figure 1: IC process flow

Each of the manufacturing processes like wafer fabrication can be broken down into several smaller processing steps. These steps will be referred to as workcells throughout

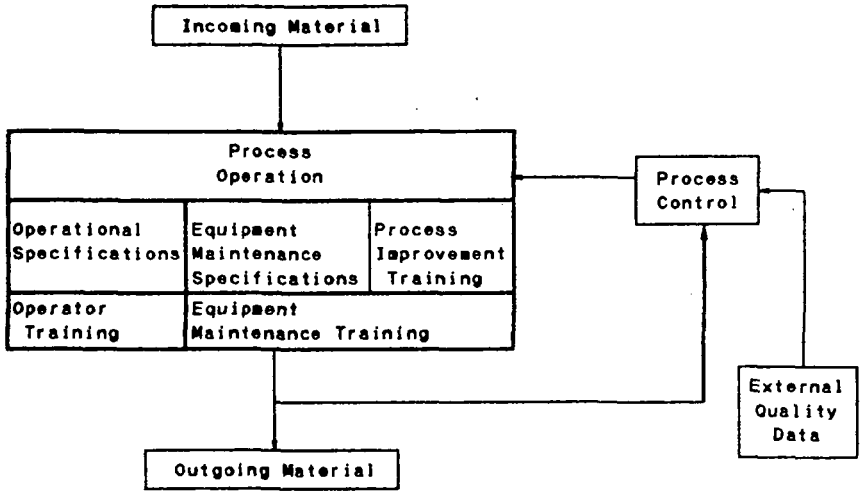

Figure 2: Workcell Description

this paper. Figure 2 shows a general process description of the workcell. The workcell is composed of three major parts: the process operation, internal workcell process control, and external feedback to the workcell. This paper carefully reviews both internal and external process control feedback for key CMOS IC workcells. This feedback is critical to the continuous improvement of the workcell process. These improvements directly affect the material consistency.

Ongoing reliability strife testing plays a key role in continuously improving the reliability of current and future IC processes. Strife testing unlike qualification testing is designed to produce IC failures through excessive environmental stress. Ongoing reliability strife testing is performed at least quarterly on material from released manufacturing processes. This testing has two purposes. First, it is intended to provide feedback so that the overall IC strength can be improved. Second, this testing provides a larger statistical basis for evaluating the consistency of the process (cumulative sample sizes for a single strife test are typically in the thousands).

This paper reviews each of these three areas in much greater detail. A commitment to continuous process improvement is assumed to be a basic operational methodology. IC reliability relies on two key components: material strength, and material consistency. Material strength refers to the ICs capability to resist degradation over time. Typically this degradation results from temperature, humidity, current flow, high voltage gradients, or mechanical stress. Material consistency refers to the ability to make each part exactly the same. IC consistency varies because of normal process variations or unexpected process exceptions (particles typically fall into this category).

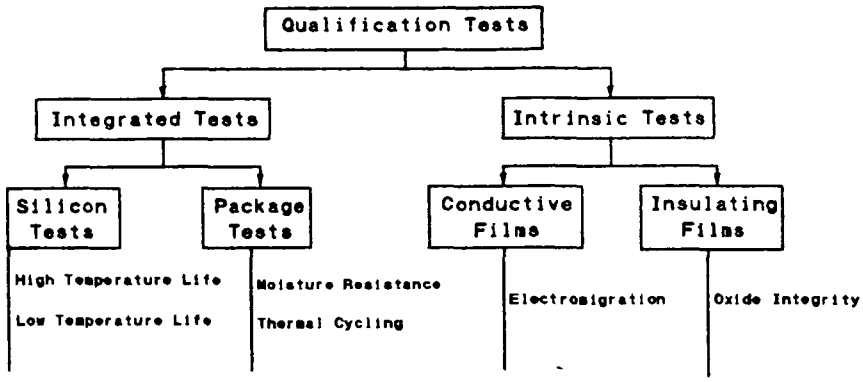

Figure 3: Process Qualification Tests

2 Qualifications

Qualifications are designed to set minimum expectations on the initial IC process. As a result, inherently weak processes are prevented from moving into manufacturing by these qualification standards. Qualification tests can be classified as either intrinsic or integrated. Intrinsic tests directly measure the intrinsic strength of specific films on the silicon die. Integrated tests measure the reliability of the entire packaged IC. Integrated tests typically verify acceptable interactions between different materials. Figure 3 shows the purpose of different qualification tests.

Integrated testing is usually given the greatest importance since it evaluates the reliability of the entire IC rather than one or two elements. However, intrinsic testing is required to supplement integrated testing because of limitations on the stress which can be applied to an integrated system.

High temperature operating life is an example of an integrated qualification test. High temperature operating life testing operates the part at junction temperatures significantly above maximum operating temperatures for extended periods (6 weeks). These higher temperatures will cause defective parts to fail in one tenth to one hundredth the time required under normal operating conditions.

Four key factors define the potential value of integrated qualification tests. These factors are listed in order of importance below:

1. Electrical Testing
2. IC Vehicle
3. Sample Sizes
4. Environmental Conditions

Specifications of qualification tests normally focus on the environmental conditions. However, our experience has shown that this factor is actually less significant that the other three factors. In other words it is typically easy to pass harsh environmental conditions if

the test program is compromised, the IC vehicle incompletely designed, or sample sizes of 10 to 50 parts are used.

2.1 Electrical Testing

Electrical Testing is designed to detect when the part stops functioning. Functional testing has been used for many years to detect these failures. The creation of functional vectors is typically based on a stuck-at-fault model. This model assumes that a failure is characterized by a node stuck at either 0 volts or 5 volts on the IC. In practice this type of failure mechanism is extremely rare. Typical failure mechanisms exhibit leakage current to the supplies or to an adjacent line. In both cases huge leakage currents are required to actually induce a stuck-at-fault failure. Long before the leakage induces a stuck-at-fault failure it will create reliability degradation which is the real failure mechanism in the field. Hence, it is extremely desirable to detect these low level leakages directly on the IC. This is accomplished by implementing a static current test. This test places all nodes on the IC at alternating states (0 volts, 5 volts) and then measures the leakage currents on the supply lines. All nodes on a CMOS IC are connected to either ground or Vdd through a transistor that is turned on. Hence, the leakage current between adjacent nodes can be directly detected at the supply. Useful static current measurements can be made at any level below 10 μA. Typical measurements should be in the 1μA range to produce the appropriate sensitivity to defects. Measurements in the 100nA range are limited not by CMOS process capabilities but rather by electrical test hardware capability. For assessing silicon process reliability this single measurement is far more important than the other qualification criteria discussed.

Packaging process qualifications rely heavily on detecting defects in the silicon to package connection. As a result, I/O leakage current testing is a key measurement for detecting shorts. In addition, I/O conductivity measurements should be made to detect discontinuities at the silicon-package interface.

2.2 IC Vehicle

The IC vehicle is the part on which qualification testing is performed. Usually two different IC vehicles are required to qualify a new process. One vehicle is designed to optimize the sensitivity of the part to silicon degradation. While the other vehicle is designed to optimize the package to silicon thermal mechanical mismatch.

The silicon vehicle is intended to optimize the sensitivity of the IC layout to processing deviations (variations & exceptions). As a result, this device should be as dense as possible using minimal spacings between devices. The vehicle as a whole should dissipate extremely low standby currents so that the maximum defect sensitivity can be achieved. The design of the I/O pads should possess good ESD immunity to prevent unrealistic defects caused by electrical noise in the environmental system. Finally, it is critical that all nodes on the vehicle can be tested, exercised by the environmental test system, and failures can be mapped to the physical site of the defect. At HP we typically use an SRAM part for this

vehicle.

The silicon vehicle is used for high temperature operating life tests and moisture resistance testing. Life testing is designed to accelerate silicon defects. Moisture resistance testing accelerates both silicon and package corrosion. Silicon corrosion is directly related to the layout of the die. Layouts with tight geometries create the most difficult topologies for passivation coverage. Particulate on the die further complicate the difficulty of passivation coverage. Hence, this is the most sensitive vehicle for these two tests.

The package test vehicle is intended to optimize the mechanical stresses induced as the temperature is increased. This is the key vehicle used to qualify new packaging processes. The mechanical stresses result from differences in the coefficient of expansion between packaging and silicon materials. These stresses are optimized by creating large die and placing them in the largest package within a packaging family (i.e. package family= PDIPs, PLCCs). The package test vehicle should also be designed to incorporate direct measurements of the mechanical stress. This increases the sensitivity of the part to failure induced by stress. Corrosion structures should be incorporated to detect failures induced by the combination of moisture and ionic contaminants. Finally, the IC should be designed with a large number of I/O pads. Both the number of bonds on a part and spacing between bonds can be optimized to provide the worst case environment for reliability testing.

The package test vehicle is used for temperature cycling tests and pressure pot testing. Thermal shock, temperature cycling, and solder resistance tests are examples of different temperature cycling tests. The large size of the package test vehicle and the built in mechanical stress monitors optimize the sensitivity of this part to temperature cycling induced failures. The corrosion structures and die size optimize its sensitivity to corrosion during pressure pot testing.

2.3 Sample Sizes

Significant sample sizes are critical to detecting failures during integrated qualification tests. Parts with the same defect can degrade at varying rates. In addition, much of the electrical testing is designed to identify parts that have failed but not all of the parts that have degraded. As a result, in a few cases not all of the defective parts result in failure. This drives the need for significant sample sizes. At the vary least these tests should start with sample sizes of more than a hundred parts for each environmental test.

2.4 Environmental Conditions

Most environmental tests can be classified into one of three categories:

- Life tests
- Moisture tests
- Thermal cycling tests

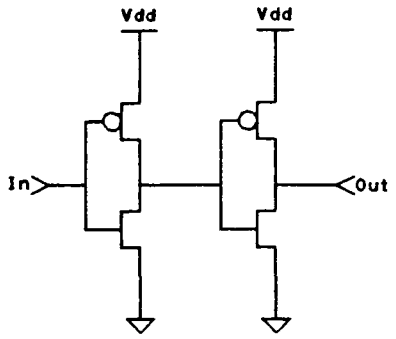

Figure 4: CMOS Inverters

Each of these tests are characterized by the environmental conditions and the operational state of the part. These parameters are consistently less important than the other issues already discussed.

High temperature and low temperature life tests are intended to primarily accelerate silicon defects. The acceleration in high temperature life testing is determined by the junction temperature of the device. Higher temperatures produce higher stresses on the part. Typical CMOS junction temperatures during high temperature life testing are 150C. During life testing the part should be exercised with a set of vectors that simulate normal IC operation. This simulation should satisfy two objectives:

1. Exercise all areas of the IC

2. Exercise the most sensitive portion of the circuit 90% of the time

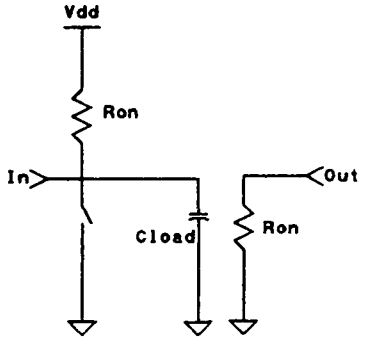

Figure 5: CMOS inverters equivalent circuit

Exercising all areas of the IC optimizes the chances of detecting unexpected problems on the IC. Figure 4 shows a typical CMOS inverter driving another inverter. Figure 5 shows the idealistic equivalent of this circuit. It is obvious from Figure 5 that current flows only when the inverter switches from one state to another. In many cases the cumulative current flow is what causes defects to become failures. The implication for reliability testing is that a circuit must be continuously exercised to identify reliability weaknesses. This is very difficult if the only objective is to exercise the entire IC. As a result, it is necessary

Test Name	Electrical Bias	Pressure (Atm)	Humidity %RH	Temperature (C)	Time (Hours)	Sample Size
65/90	Yes	1	<90%	65	240	105
85/85	Yes	1	85%	85	1000	105
Pressure Pot		2	95%	125	240	50
HAST	Yes	2	95%	125	168	105

Table 1: Summary of Moisture Resistance Tests

to select one small area of the IC that can be continuously exercised a high proportion of the time.

Several different types of moisture resistance tests are summarized in Table 1. Each of these tests use a combination of moisture and temperature to activate reliability failures. 65/90 is the only test designed to cycle the temperature and relative humidity. The purpose of this cycling was to drive moisture into cavity packages. Our experience with this test has demonstrated that it is unlikely to accelerate defects to failure. As a result, HP prefers to use 85/85 testing. Relative humidity is typically used to describe these tests. However, a much better measure is the partial pressure of water. This measure directly describes how much moisture is present in the chamber. Figure 6 shows a graph of partial pressure (for water) at various temperatures when the air is fully saturated (100% RH). Reviewing the 65/90 and 85/85 operational points on this curve illustrate that relative humidity values are quite misleading. The 85/85 test contains twice as much moisture as 65/90 even though the relative humidity is lower.

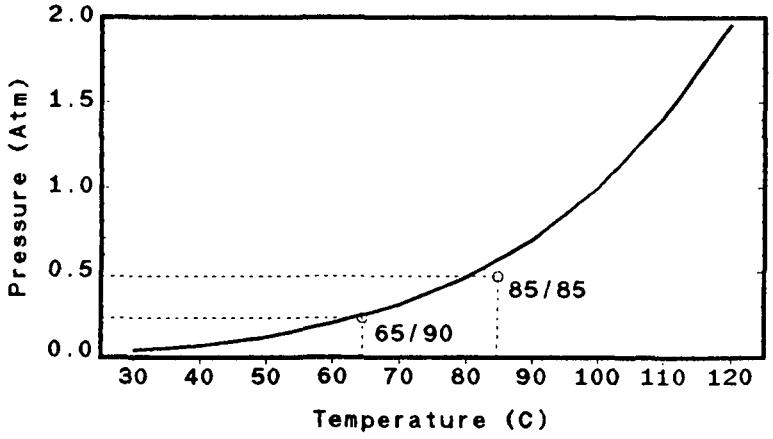

Figure 6:

Thermal cycling tests are designed to detect mechanical stress induced failures. The mechanical stress is a direct result of the differences in the coefficient of expansion for different materials. Figure 7 summarizes several different types of thermal cycling tests. All of these tests should be performed using the largest possible die and package size. Since this produces the worst case internal stress. HP generally considers thermal shock to be the worst case test because the fluorocarbon liquid forces the most rapid tempera-

ture change in the part. The soldering process tests were originally designed to confirm part compatibility with the board assembly processes. However, solderability tests offer a different temperature profile which can result in different failure mechanisms.

Name	Phase of Medium	Low Temperature	High Temperature	Number of Cycles	Dwell Time
Thermal Shock	Liquid	- 55 deg	+ 125 deg	200	5 Min.
Temperature Cycling	Air	- 55 deg	150 deg	500	5 Min.
Wave Solder	Air	25 deg	260 deg	1	10 Min.
Vapor Wave Solder	Air	25 deg	215 deg	4	1 Min.
IR Soldering	Air	25 deg	215 deg	4	1 Min.

Table 2: Summary of Thermal Cycling Test

2.5 Intrinsic

Intrinsic tests are designed to measure the intrinsic film strengths on the silicon die. Two types of films exist on a silicon wafer:

- Conductive
- Insulating

Metal layers are typical conductive films. Gate oxides, intermetal dielectrics, and passivation films are common insulators. Two special intrinsic tests are performed on these films to assure that they will continue to operate throughout the rated lifetime of the product:

- Electromigration
- Oxide Integrity

The verification of these film properties is rarely possible during integrated testing because sufficient stresses can not be applied to the part. In electromigration testing the stress is increased by applying high current densities. Oxide integrity increases the stress on nonconductive films by rapidly ramping the voltage across the film.

Electromigration testing is designed to accelerate metal migration failures. However, it can also be a useful test for accelerating failures from stress migration. In addition, this test can be used to accelerate the failure of intermetal connections (vias) or metal to substrate connections (contacts).

Oxide integrity tests are designed to measure the potential breakdown voltage of oxide films. These breakdown voltages are directly affected by weak film quality or particle contamination of the films. In addition, to normal gate oxide testing the intermetal dielectrics also need to be tested.

3 Workcell Processes

Individual work cells are the building blocks of the production process. Figure 2 shows a general description of a workcell. This section of the paper focuses on the process control monitors for each of the major workcells. This control is necessary to assure consistency from lot to lot. The process operation consists of operational personnel, equipment, inflow, and outflow material. This paper assumes that operational specifications, operator training, equipment maintenance, specifications, equipment maintenance rate tracking, and process change training are parts of the process operation in each workcell.

Figure 1 shows the overall IC process flow. This flow consists of five production processes:

1. Layout
2. Silicon Fabrication
3. IC Packaging
4. Electrical Testing
5. Shipping

This section reviews the major workcells for each of these production processes.

3.1 Layout

The layout of the IC will ultimately determine the reliability of a specific IC design. Three key reliability issues must be considered in the layout:

1. Compliance to process layout rules
2. Electromigration
3. I/O pad protection

Layout rules should be clearly documented. In many cases layout programs and libraries already exist that prevent potential violations of these rules. In addition, a design rule check program is usually run to verify that the physical layout does meet the design rule requirements.

Electromigration is typically handled by providing margin in the initial electromigration rules. Libraries of verified designs provide additional protection from electromigration violations. Some electromigration checkers do currently exist but most are still in the development phase. As a result, it is crucial that the designer identify where potential electromigration violations could exist. This in usually a short list because of the availability of verified libraries and autorouters.

The I/O pads interface to the external world. As a result, they need to protect the IC from transient high voltage or current abuse. This is accomplished by incorporating ESD

protection circuitry and appropriate guardrings for latchup. All pads should be reviewed before the IC artwork is released for mask production. HP also performs ESD and Latchup testing on the first parts fabricated in a new design to verify their protection capabilities. Different ESD test equipment can produce significant differences in the measured ESD protection of an I/O pad. This is especially true with machines that conform to older versions of MIL-STD 883C [1].

3.2 Silicon Fabrication

The following silicon fabrication workcells are reviewed in this section:

- Diffusions
- Gate oxides
- Metalization
- Intermetal dielectrics
- Passivation

Table 3 summarizes the key reliability process monitors for each of these process steps.

Process Step	Process Controls
Diffusions	CD's, dose, temperature, resistivity
Metalization	Thicjness, width, grain structure, sheet resistivity
Gate Oxide	Mobile ion concentration, surface charge density, thickness
Intermetal Dielectric	Leakage currents, thickness, topography, alignment
Passivation	Coverage

Table 3: Silicon process controls for reliability

Island and well diffusion are required to produce the correct dopant concentrations and depth profiles. These issues are typically monitored by measuring the dimensional accuracy of the diffusion openings, monitoring the dose, controlling the drive in temperature, and measuring the final diffusion resistivity.

Metalized films are required to conduct electrical current from one node to another without variations in resistivity over their life. Resistivity variations could result from differences in metal width, thickness, grain structure, or sheet resistivity. As a result, it is desirable to have each of these parameters monitored as part of the metalization workcell.

Gate oxides should block current flow from the gate to the channel without degrading the electrical field. Mobile ion concentration, surface charge density, and thickness need to be monitored to assure consistency from part to part and over the lifetime of the product.

Intermetal dielectrics prevent leakage paths between adjacent metal conductors (both vertical and horizontal). Leakage currents, and thickness are two key monitors of the insulating characteristics of these materials. In addition, the film topography, and alignment to underlying layers must be monitored.

Passivation is usually the final layer deposited onto the silicon wafer. It is designed to protect the metalized layers from chemical corrosion and the transistors from chemical contamination. To provide this protection the passivation must uniformly cover all structures on the IC. Variations in the thickness of the film need to be monitored to assure film reliability.

3.3 IC Packaging

Table 4 summarizes the process steps and process controls for IC packaging. These controls are designed to assure IC packaging consistency.

Process Step	Process Controls
Leadframe	Platting uniformity,frame quality
Die Attach	Backside coverage, excess material
Bonding	Temperature, pressure, tip wear, wire quality
Molding	Temperature, pressure, injection rate
Lead forming	Tool accuracy,tool wear

Table 4: Packaging process controls for reliability

The leadframe is usually considered an incoming material. The leadframe is plated so that a wire can be bonded to the inner lead fingers. This plating must have uniform thickness and consistent purity. The leadframe is stamped or etched to create separate leads. Each of these leads need to be correctly formed and free of contamination.

The die attach step is designed to hold the silicon die to the metal leadframe for the entire life of the product. The attachment method should provide complete attachment across the entire back surface of the die. Any excessive attachment material should be carefully controlled so that it does not come in contact with the top side of the die.

Bonding is designed to make electrical connection between the die and the leadframe. Several different bonding processes exist. The bonding temperature, bonding pressure, bonding tip quality, and wire quality must be carefully controlled to assure consistency. Wire quality is defined by the wire diameter and the wire purity.

Molding is designed to protect the part from chemical and mechanical degradation. To accomplish these objectives the molding material must be uniform and dimensionally accurate. The molding temperature, pressure, and injection rate must be carefully controlled.

The final step in the packaging process is lead forming. In surface mount applications the lead alignment and planarity are critical for creating a good electrical connection to the board. The forming tool determines the results of this operation. The tool needs to meet original specification and stay within specified wear requirements.

3.4 Electrical Testing

Electrical testing is performed at both the raw wafer level and at the final packaged part level. The wafer level testing is usually critical to assuring overall wafer reliability. While package testing is designed to detect packaging induced defects.

Three different types of tests are performed at the wafer level. The first test verifies the appropriate device characteristics by measuring structures like individual transistors, contact strings, or diffusion resistances. These structures are located in the center of the scribe lines on the wafer. A few wafers are tested from each lot. If a wafer does not meet the device specifications then the entire lot is rejected.

The second wafer test is a full functional test. HP typically breaks this test into several parts:

- Open/Short I/O pin testing
- Functional testing
- I/O leakage current testing
- Supply current testing

Functional testing is usually performed at full device operational frequencies with the voltage levels adjusted to compensate for maximum temperature sensitivities. Typical functional vectors sets are expected to meet at least 95% fault coverage. A static current test is one of the supply current tests. This test is a critical element in assuring that the part is free of defects. The Qualification section of this paper explains in detail why this test is critical. One additional screen for wafer testing is called below ship limit wafer scrapping. In cases where the number of good die is less than 25% of the standard wafer yield the entire wafer should be scrapped. This prevents potentially marginal die from being shipped to the field.

The third wafer test is a visual inspection of the wafer. This screen is designed to detect gross visual defects that would affect metal or passivation quality.

Package testing consists of a full functional test of each part. In addition, lead planarity and alignment testing is performed on surface mount devices.

3.5 Shipping

The shipping process packages parts so that they will not be damaged during shipment. Three potential reliability problems must be prevented during this process:

- Electrostatic discharge damage (ESD)
- Pin planarity or alignment damage
- Excessive moisture absorption.

ESD damage can be prevented by using appropriate ESD grounding procedures while packaging and preparing parts for shipment. In addition, the internal protection structures on the part also provide protection. Regular ESD audits on the shipping area assure that the intent of ESD prevention procedures are understood and that the procedures are followed on a regular basis.

Pin planarity or alignment damage can result from poor part handling techniques. This damage can be prevented by correctly selecting shipping containers for the parts, and using appropriate part handling techniques. Workcell process control and therefore consistency are typically supported by both audits of the actual procedures used and sampling audits of the outgoing material.

Parts that absorb excessive moisture before shipment may suffer internal cracking or delaminations (popcorning) during soldering to pc boards. The best way to control this mechanisms is to place parts into inventory in moisture tight packaging. Placing a moisture absorption card in each package is another step that can be taken to guarantee that material soldered onto boards does not popcorn.

4 Ongoing Strife Testing

One purpose of this testing is to identify the weakest element in the IC. Once this element is identified process improvements are developed to further increase the strength of the process. Ideally strife testing should not be a static set of tests but rather a set of tests that continuously evolve to create higher and higher part stresses. Another purpose of this testing is to increase the statistical data available on the process reliability. Running these tests on a regular basis assures that sufficient data is available to make realistic assessments of the actual product reliability. New processes should be tested on a more frequent basis than old processes to develop the statistical data base. At HP we perform strife testing every month for newer processes. After a couple years this testing is reduced to a quarterly basis.

As in qualification testing three major types of integrated tests exist:

- Operating life tests
- Moisture resistance tests
- Temperature cycling tests

To increase the part stress these tests are usually performed sequentially. The stress in operating life tests are increased by using higher supply voltages. Moisture resistance testing is almost always performed using HAST conditions (summarized in Figure 6). Thermal shock is used to induce thermal mechanical stress. These stresses are increased by cycling the parts for at least 1000 cycles.

5 Conclusions

CMOS IC reliability is determined by a combination of material strength and product consistency. Weak materials clearly result in a weak product. Inconsistent product quality will result in inherent product weaknesses that cause field failures. Qualification testing is designed to set minimum intrinsic and integrated material strength standards. Process controls are designed to assure product consistency. Products that do not meet these consistency requirements must be scrapped because they contain defects that will cause early life failures. Finally both material strength and product consistency should improve over the process life. Ongoing strife testing is designed to identify which materials possess the lowest strength and any variations in process consistency. Based on this data appropriate process improvements can be developed and implemented.

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