N94-71101

SEU Hardening of CMOS Memory Circuits

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Abstract - **This paper reports a design technique to harden CMOS memory circuits against Single Event Upset (SEU) in the space environment. A RAM cell and Flip Flop design are presented to demonstrate the method. The Flip Flop was used in the control circuitry for a Reed Solomon encoder designed for the Space Station.**

1 Introduction

In the environment of outer space, electronic circuitry is exposed to a flux of ionized particles. If the energy level of a charged particle is high enough and that particle passes through the diffusion of a susceptible node then the contents of a MOS memory cell can be changed [1]. This is a Single Event Upset (SEU) of the integrated circuit containing the memory cell. The consequences of the SEU depend on the system function of the memory cell. Circuit design techniques which are independent of processing and which are without serious performance degradation have been reported [2]. This paper also reports a circuit design method which is process independent and maintains the performance level. With the techniques presented here, loading on the clock signal is reduced when compared with [2].

2 RAM Design

There are three fundamental concepts that can be used to design SEU immune circuitry. First, information must be stored in two different places. This provides a redundancy and maintains a source of uncorrupted data after an SEU. Second, feedback from the noncorrupted location of stored data must cause the lost data to recover after a particle strike. Finally, current induced by a particle hit flows from the n-type diffusion to the p-type diffusion. If a single type of transistor is used to create a memory cell then p-transistors storing a 1 cannot be upset and n-transistors storing a 0 cannot be upset. These observations lead to the design of the RAM cell as shown in Figure 1.

The RAM cell consists of two storage structures. The top half is constructed from p-channel devices while the bottom half consists solely of n-channel devices. Transistors M2 and M4 are sized to be weak compared to M3 and M5 while M13 and M15 are sized

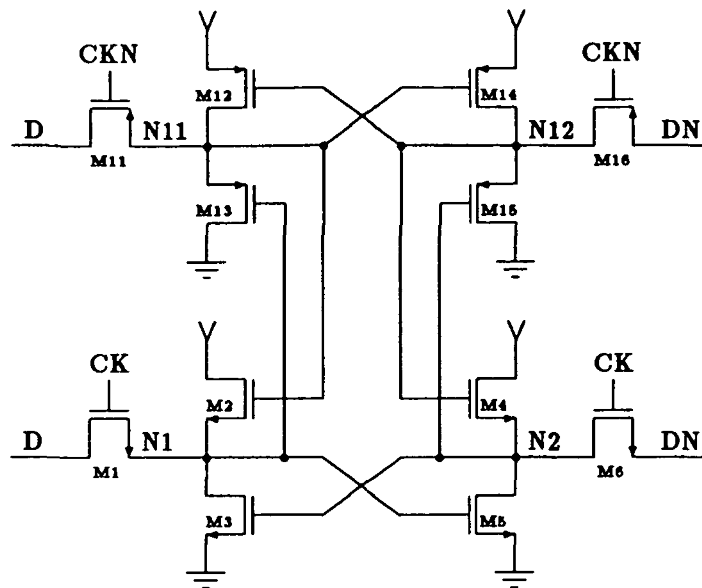

Figure 1: SEU Hardened RAM cell.

to be weak compared to M12 and M14. The other transistors are sized using the normal design considerations for a RAM cell to allow the cell to be written and read to meet the performance required.

Nodes N1 and N2 can store 0's that cannot be upset while N11 and N12 can store 1's that cannot be upset. If N11 is storing a 0 and is hit driving the node to a 1, M14 turns off but node N12 remains at a 1. M2 turns on but is weak and cannot over drive N1 keeping M13 on and restoring N11 to a 0. If N1 is storing a 1 and is hit driving the node to a 0, M5 turns off leaving node N2 at a 0. M13 turns on but is weak and cannot over drive N11 keeping M2 on and restoring N1 to a 1.

The memory cell was then designed for the desired write time and read time resulting in the device sizes shown in Table 1. The layout was drawn and is shown in Figure 2. Parasitics were extracted and SPICE simulations run to verify functionality and performance. SPICE simulations were also performed depositing $5pC$ on N11 and removing $5pC$ from node N1 verifying the cell recovery. Figure 3 shows the response of N11 during the recovery from a particle strike. The simulations were performed under worst case speed conditions ($Vdd = 4.3V$, $T_j = 140C^\circ$ and 3σ parameters). Figure 4 shows the response of N1 during the recovery from an SEU. Both SPICE simulations show a recovery time of only a few *nsec*. The hardness of the cell design is independent of processing and parameters. The logical feedback and ratioing of transistor strengths provides the recovery mechanism. The zero level of N11 is degraded because of the p-MOS device threshold voltage and body effect on the threshold voltage. At N1 the one level is similarly degraded in the n-MOS section. These levels are acceptable and pose no design problems internal to the cell. When reading the RAM cell, the p-MOS section will drive the data line, D, to VDD when a 1 is stored and the n-MOS section will drive DN to VSS providing rail to

Transistor	W_n	L_n	Transistor	W_p	L_p
M1	6.4	1.0	M11	6.4	1.0
M2	2.4	1.0	M12	6.9	1.0
M3	6.9	1.0	M13	2.4	1.0
M4	2.4	1.0	M14	6.9	1.0
M5	6.9	1.0	M15	2.4	1.0
M6	6.4	1.0	M16	6.4	1.0

Table 1: RAM cell device sizes.

rail operation on the cell output.

The circuitry added for SEU immunity doubles the number of transistors required by a RAM cell. The layout requires an increase of about 75% in area over the traditional 6 transistor RAM cell. The method described in [2] also doubled the transistor count, but will result in a more compact layout (only a 40% increase in area). The cell described in this paper does, however, have an advantage in the loading seen by the clock signal and the loading seen by the data drivers during a write cycle is less than that of [2]. This should result in an increase in performance. Cells implemented with these two methods using the same CMOS process need to be analyzed to verify this claim.

3 Flip Flop Design

The memory cells required by the control circuitry of the RS16 encoder [3] are D flip flops. A flip flop contains a master and a slave section. Each flip flop section is basically a RAM cell. Figure 5 shows the schematic for a flip flop section. The RAM cell outputs have been buffered using M8/M18 and M7/M17. The buffers allow Q and QN to have rail to rail operation and isolates the memory portion from potentially high capacitive loads. On the RS16 encoder, the control lines present capacitive loads of about $3pF$ and need to be driven by the output of the flip flop with relatively short delay times when operating at 40MHz. Table 2 lists the required device sizes to meet the internal cell load and speed requirements.

Two of the RAM sections were joined to form the flip flop of Figure 6. The control flip flops were designed to have a single clock and data input. This required inverters CK and DN. The large capacitive load seen by the output required the Q buffer. In many applications, these additional devices would not be necessary. Table 3 lists the device sizes for this additional logic. Figure 7 shows the layout of the D flip flop used on the RS16 encoder.

A shift register consisting of a string of these flip flops was added as a test circuit to the RS16 encoder to allow the SEU immunity of these cells to be easily verified. The input of the 16 bit shift register is driven by an input pad and the output of the shift register drives an output pad.

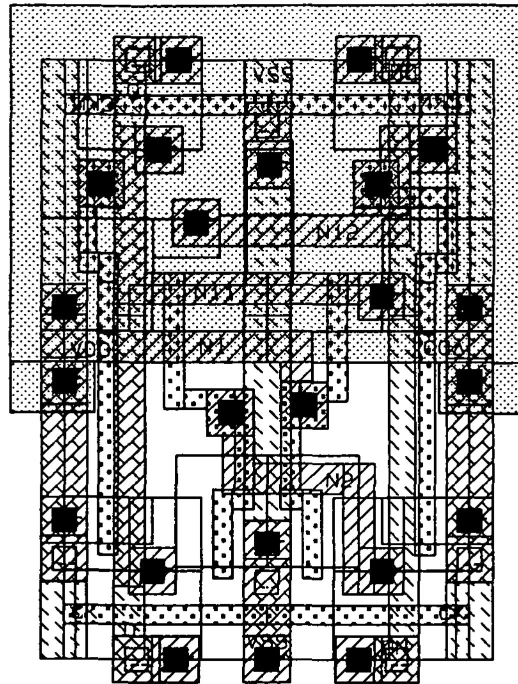

Figure 2: RAM cell layout.

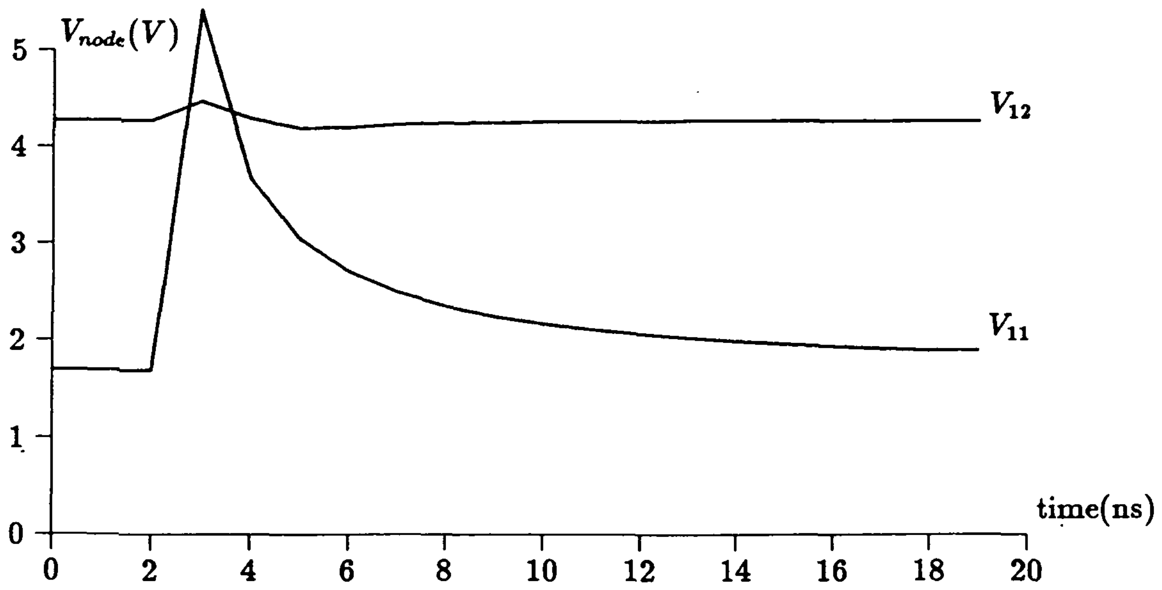

Figure 3: RAM cell N11 recovery from an SEU.

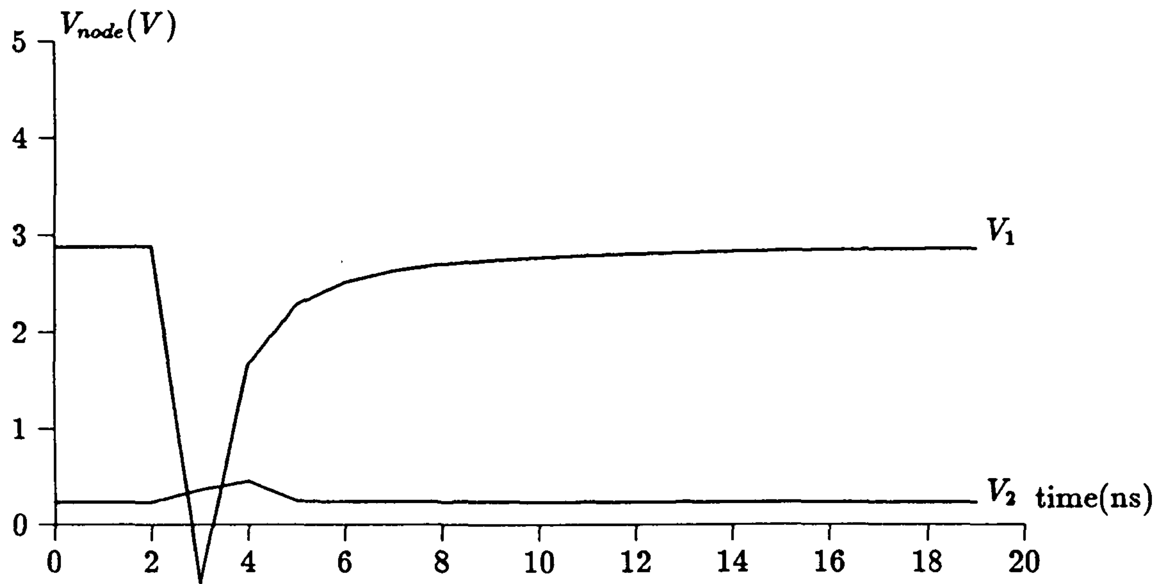

Figure 4: RAM cell N1 recovery from an SEU.

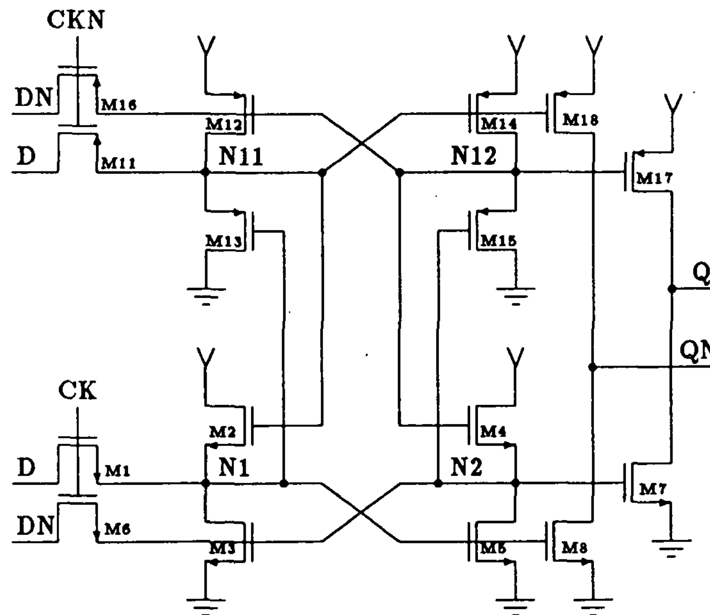

Figure 5: SEU hardened Flip Flop section.

Transistor	W_n	L_n	Transistor	W_p	L_p
M1	7.2	1.0	M11	7.2	1.0
M2	2.4	1.0	M12	7.2	1.0
M3	7.2	1.0	M13	2.4	1.0
M4	2.4	1.0	M14	7.2	1.0
M5	7.2	1.0	M15	2.4	1.0
M6	7.2	1.0	M16	7.2	1.0
M7	12.0	1.0	M17	12.0	1.0
M8	12.0	1.0	M18	12.0	1.0

Table 2: Flip Flop section devices sizes.

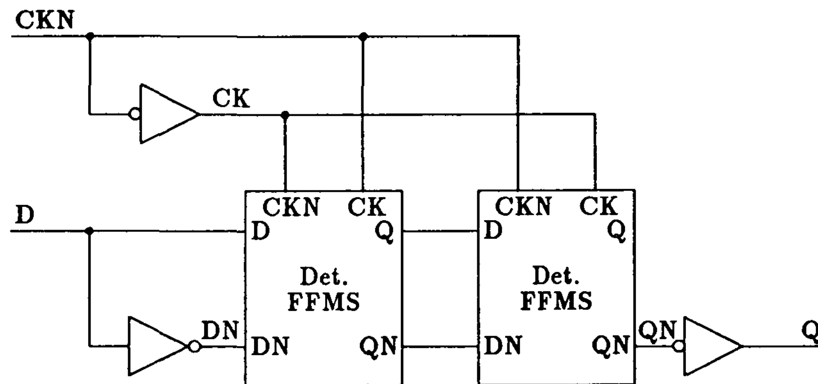

Figure 6: SEU hardened Flip Flop cell.

Node	W_p	W_n
CK	14.4	9.6
DN	12.0	6.0
Q	48.0	24.0

Table 3: Flip Flop cell device sizes.

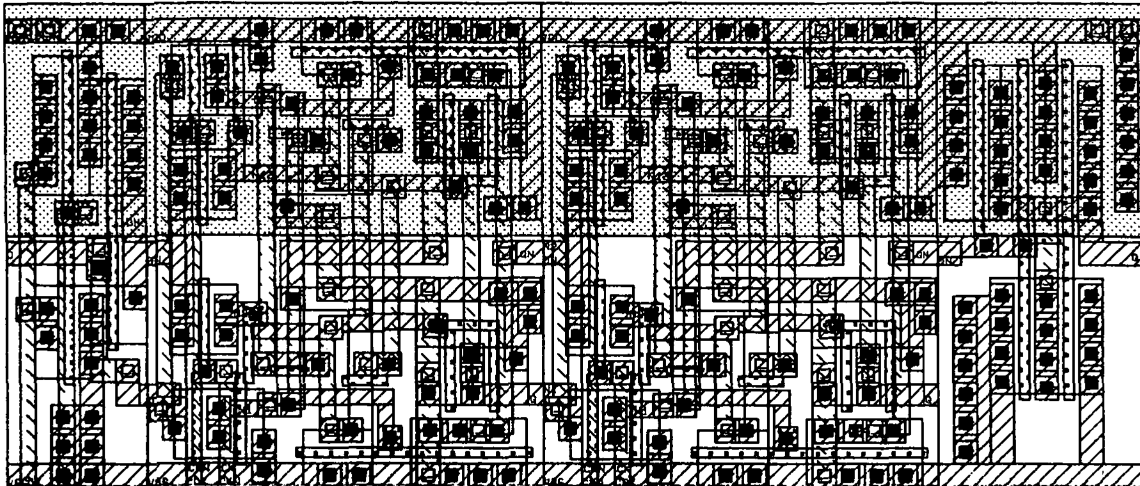

Figure 7: Flip Flop cell layout.

4 Summary

An SEU immune RAM cell has been presented which compares favorably with others in the literature. This RAM cell design was implemented as a D flip flop in the controller for a Reed Solomon encoder to be used in the Space Station. This is a preliminary report. Work needs to be performed to produce a comparison of previously reported SEU immune logic with this cell. Also when the chip fabrication is complete, the shift register will be subjected to cyclotron tests to verify the SEU immunity of this cell and results will be submitted for publication.

References

[1] T. Ma and P. Dressendorfer, *Ionizing Radiation Effects in MOS Devices & Circuits*, New York, NY, John Wiley & Sons, 1089, Chap. 9

[2] L. Rockett, "An SEU Hardened CMOS Data Latch Design", IEEE Transactions on Nuclear Science, Vol. 35, No. 6, pp. 1682-1687, Dec., 1988

[3] S. Whitaker and K. Liu, "A High Speed CCSDS Encoder for Space Applications", 2nd NASA SERC Symposium on VLSI Design, Nov., 1990.