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Assessing the SEU Resistance of CMOS Latches Using Alpha-Particle Sensitive Test Circuits[1]

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1 Introduction

The importance of Cosmic Rays on the performance of integrated circuits (ICs) in a space environment is evident in the upset rate of the Tracking and Data Relay Satellite (TDRS) launched in April 1983. This satellite experiences a single-event-upset per day [1] which must be corrected from the ground. Such experience caused a redesign of the Galileo spacecraft [2] with SEU resistant ICs. The solution to the SEU problem continues to be important as the complexity of spacecraft grows, the feature size of ICs decreases, and as space systems are designed with circuits fabricated at non-radiation hardened foundries.

This paper describes an approach for verifying the susceptibility of CMOS latches to heavy-ion induced state changes. The approach utilizes alpha particles to induce the upsets in test circuits. These test circuits are standard cells that have offset voltages which sensitize the circuits to upsets. These results are then used to calculate the upsetability at operating voltages. In this study results are presented for the alpha particle upset of a six-transistor static random access memory (SRAM) cell. Then a methodology is described for the analysis of a standard-cell inverter latch.

The characterization of the single-event-upset (SEU) resistance of a latch requires four parameters: (a) the sensitive-diode critical upset charge, Q_c, (b) the sensitive-diode area, A, (c) the particle collection depth, D_c, and (d) the particle Linear Energy Transfer, LET. These parameters come from SPICE simulation, device layout, experimental results from particle testing, and atomic physics, respectively. The upset rate for a latch can be calculated from the Petersen Equation [3] which was developed for the 10 percent worst case Cosmic Ray environment at geosynchronous orbit:

$$R\left(\frac{\text{upsets}}{\text{bit}-\text{day}}\right) = 5 \times 10^{-10}\left(\frac{A(\mu m^2)}{[Q_c(pC)/D_c(\mu m)]^2}\right) \quad (1)$$

In the above equation, the most difficult parameter to obtain is the particle collection depth, D_c. In the methodology presented here, the collection depth is determined from heavy ion testing of a specially designed test SRAM [4]. The SRAMs are designed to be sensitive to low LET particles such as alpha particles. This allows the immediate, low cost

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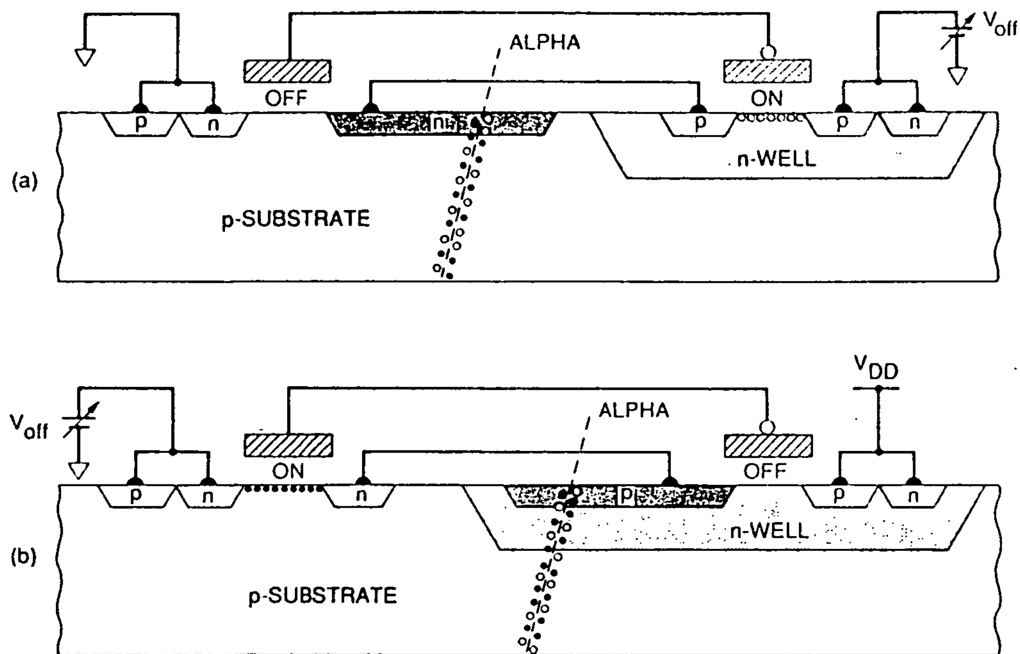

Figure 1: Electron-hole pair tracks from an alpha particle strike through (a) an n+ in p-substrate junction, and through (b) a p+ in n-well junction where truncation of the collected charge occurs

characterization of SEU susceptibility and replaces the time delayed and costly cyclotron testing.

The upset of CMOS circuits depends on the presence of reverse biased junctions. As seen in Figure 1a, n-junctions formed in the p-substrate have a large collection depth. As seen in Figure 1b, the collection depth for p-junctions formed in the n-well is truncated by the well-substrate junction. Such junctions can collect much less charge and are much more difficult to upset. In this study, we will consider the upset of only reverse-biased n-junctions formed in the p-substrate.

2 SRAM Design

For the test SRAM shown in Figure 2, the alpha sensitivity is achieved by imbalancing the cell using an offset voltage, VP2, and by bloating the drain area of the pull-down MOSFET, MN2. The offset voltage, VP2, is placed on the source of the pull-up MOSFET connected to the bloated drain. The SRAM is biased in a sensitive state as seen in Figure 2 where MP2 is ON and MN2 is OFF. As seen in Figure 3, the offset voltage controls the critical charge needed to upset the cell. These curves were obtained from a SPICE analysis of the circuit shown in Figure 2 using a triangle wave with a 200 ps pulse width. This pulse width is typical of an alpha particle strike in silicon and is much less than the response time of the circuit [4].

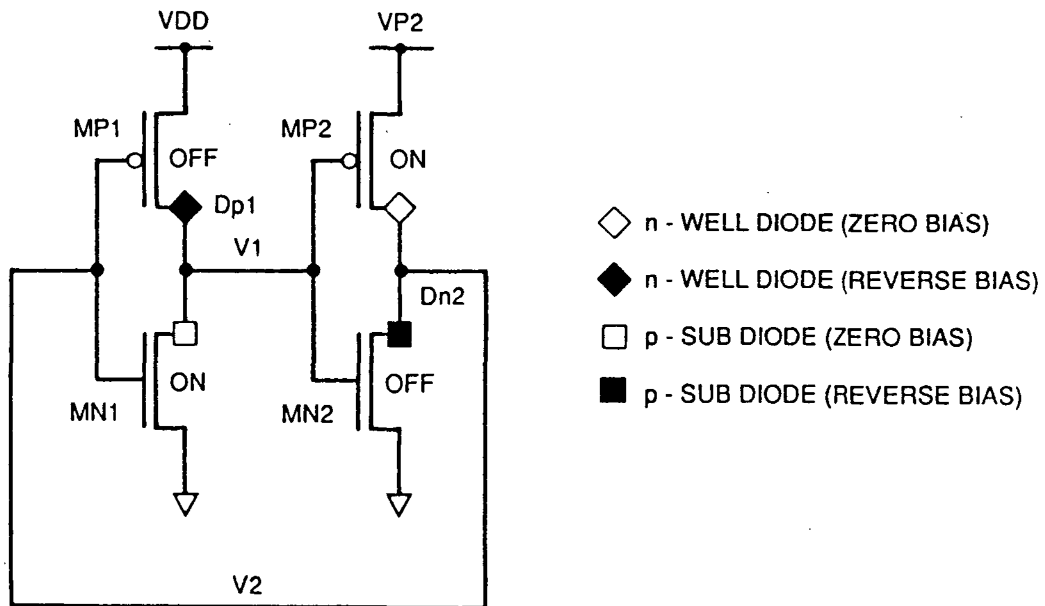

Figure 2: SRAM cell in the zero state with SEU-sensitive drain diodes DP1 and DN2

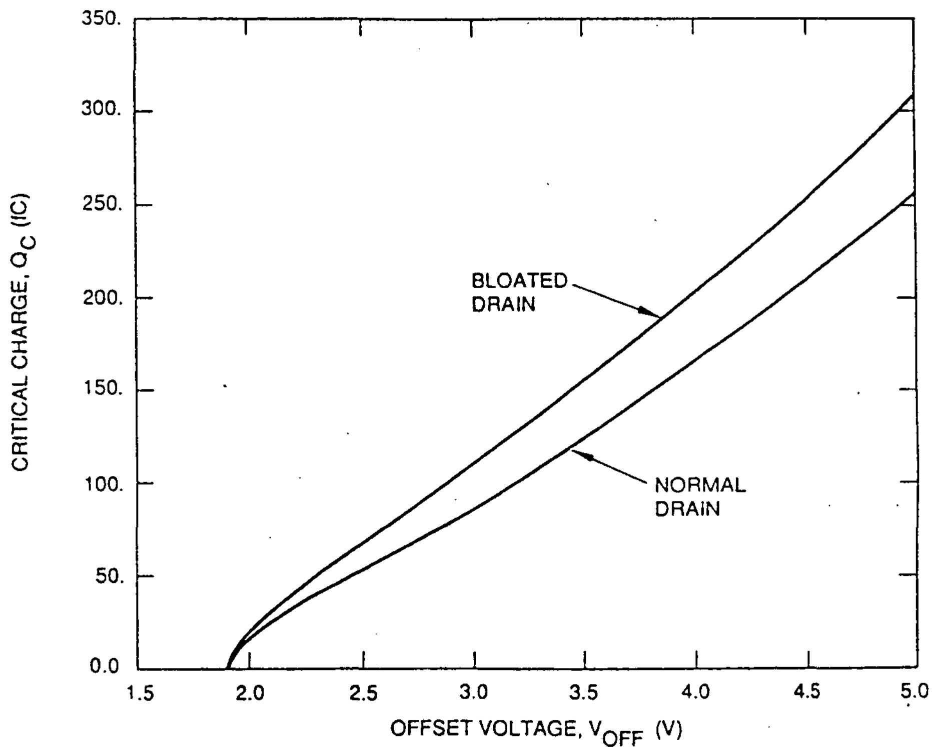

Figure 3: Critical charge characteristics of the SRAM cell using SPICE

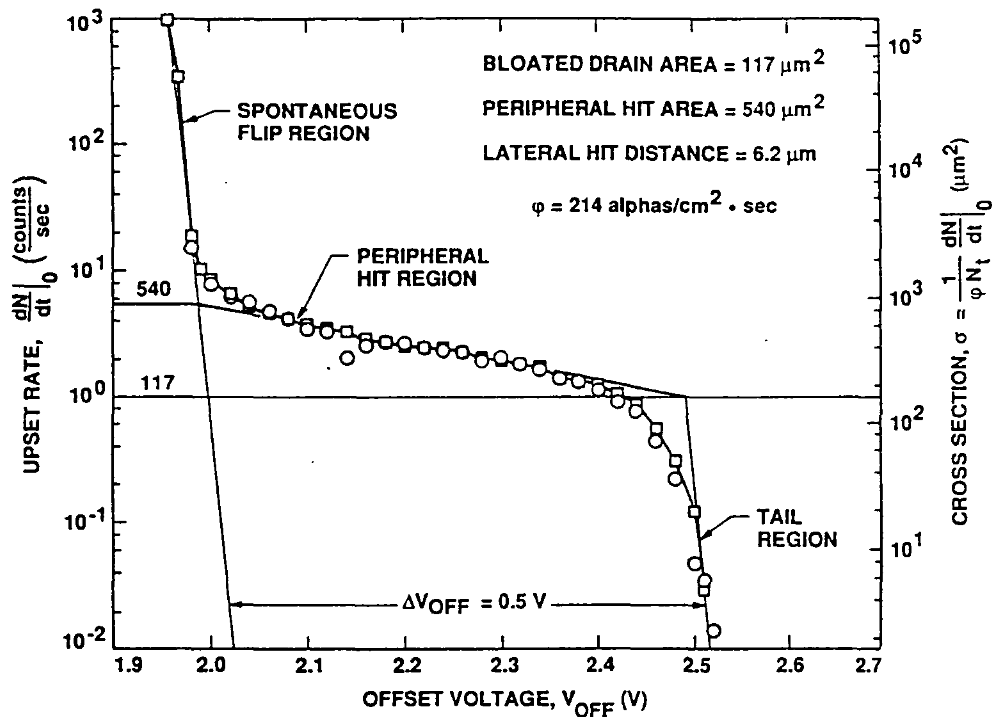

Figure 4: SRAM upset rate characteristics induced by Po-208 alpha particles 32.5 mm above the chip in a vacuum. The cross section observed by extrapolating the peripheral hit and tail regions agrees with the designed cross section of $117\mu m^2$

As seen in Figure 4, the test SRAM offset voltage, VP2, varied from 5.0 V to 1.9 V before the cells spontaneously flipped to the other state. Measurements on 2-μm CMOS n-well 4k SRAMs, indicated that a Po-208 5.1-MeV alpha particle source was able to flip the memory cells for offset voltages between 1.9 and 2.5 V. As seen in Figure 4, the offset voltage shift,ΔV_{OFF} was 0.5 V which corresponds to the critical charge induced by the alpha particle in flipping the cell. For ΔV_{OFF} of 0.5 V, the critical charge was determined from Figure 3 to be 58 fC. Finally the collection depth was determined from the charge deposition profile as shown in Figure 5 to be 8 μm.

For a bloated drain area of ADN2 $= 117\mu m^2$, Qc $=$ 58 fC, and $D_c = 8\mu m$, the calculated upset rate is 1.1×10^{-3} upsets/bit-day and the LET is 0.71 MeV-cm^2/mg. The upset rate can now be calculated for a "normal" cell with a minimum drain area of ADN2 $= 28\ \mu m^2$ and no offset voltage (ie. 5.0 V). Under these conditions the critical charge is 255 fC as seen in Figure 3. Assuming a collection depth of 8 μm as determined above, the calculated upset rate is 1.38×10^{-5} upsets/bit-day and the LET is 3.08 MeV-cm^2/mg.

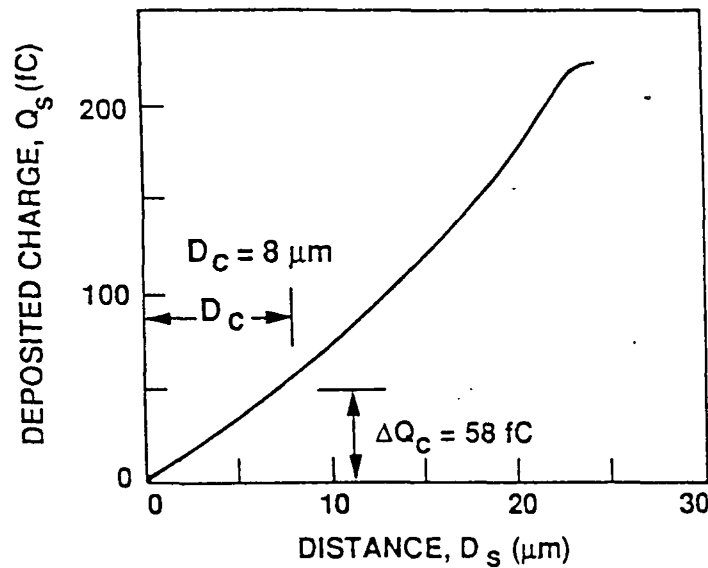

Figure 5: Deposited charge profile of a 5-Me V alpha particle in silicon

3 Standard-Cell Inverter Latch

The above scenario represents the proposed methodology for calculating the SEU resistance of latches used in ASIC designs. This methodology calls for test latches to be designed with selected nodes disconnected from the power lines and connected to offset voltage lines. Currently the latches used in JPL's standard cell library are being designed into a test latch array so their upsetability can be evaluated using alpha particles.

A schematic diagram of a test D-latch obtained from JPL's standard cell library is shown in Figure 6. This latch is shown with the D-input disabled. R is a polysilicon interconnect resistance and is about 200 ohms in the unhardened version of the latch considered here. C1 and C2 are fixed interconnect capacitances. To sensitize the latch to alpha particle induced upsets, a voltage source VP2 is placed on the source of MP2 as shown in Figure 6. The nodes that are most sensitive to upset are nodes 2 and 3 due to their reverse biased p-substrate diodes. The SPICE generated critical charge characteristics of nodes 2 and 3 are shown in Figure 7. The slope of the curves in this figure as well as those of Figure 3 have dimensional units of capacitance. This upset capacitance is a function of the physical capacitance on the node and the "on" MOSFET (restoring path) connected to the node. The upset capacitance increases when the physical capacitance is increased and decreases as the width/length ratio of the restoring MOSFET is increased. Node 3 is the most sensitive node to upset, having the smallest critical charge, primarily because the restoring path is weaker (smaller effective width/length) than that of node 2 due to the series connection of MP2 and MP4.

Using the SRAM result for the collection depth, $D_c = 8$ μm, the minimum LET of a particle that upsets node 2 with no offset voltage (ie. 5.0 V) where $Q_c = 2400$ fC is 29.0 MeV-cm^2/mg. Likewise the minimum LET of a particle that upsets node 3 where

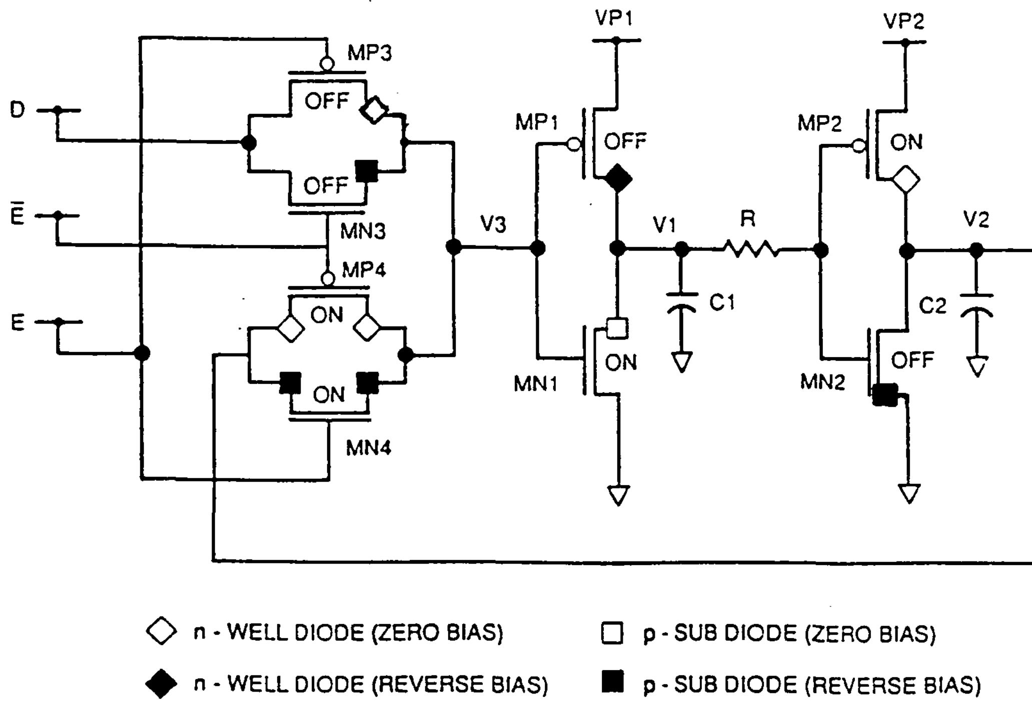

Figure 6: D-latch in the zero state showing reverse biased SEU-sensitive drain diodes

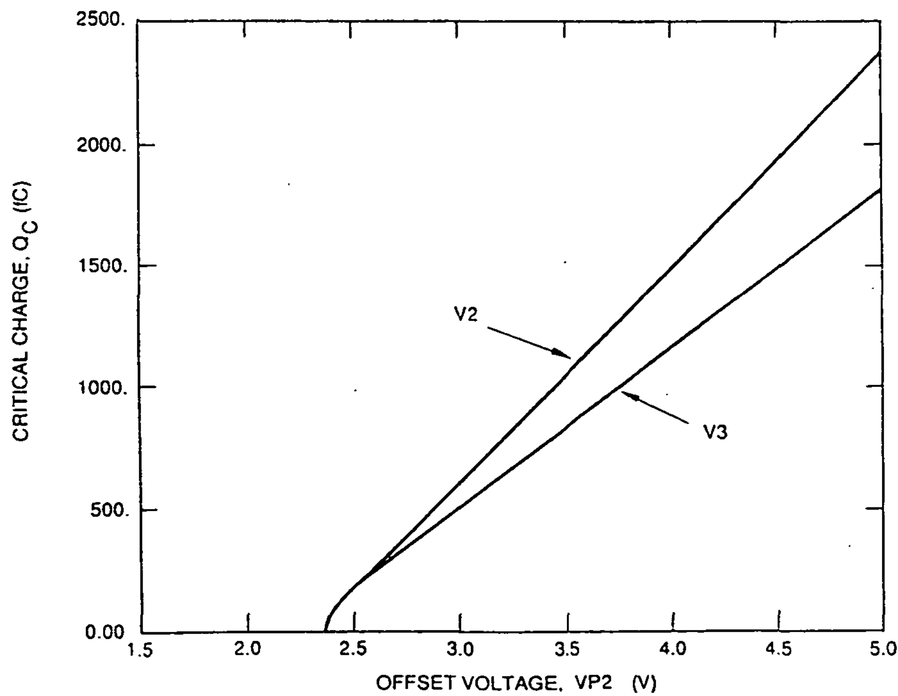

Figure 7: Critical charge characteristics of the D-latch using SPICE

Q_c = 1800 fC is 21.7 MeV-cm^2/mg. Again, assuming a collection depth of 8 μm and using the node 2 sensitive area of 100 μm^2 and the node 3 sensitive area of 64 μm^2, the calculated upset rate using the Petersen Equation is 1.27×10^{-6} upsets/bit-day.

4 Conclusion

An approach has been presented for verifying the susceptibility of CMOS latches to heavy-ion induced state changes that uses alpha particles to induce upsets in test circuits using inexpensive bench-level equipment. In this method, the experimental data is linked to alpha particle interaction physics and to SPICE circuit simulations through the alpha particle collection depth. JPL's standard cell latch array, currently in fabrication, will be used to validate this methodology by comparing the results obtained with alpha particles to that obtained with high LET heavy ions at a cyclotron.

References

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