VLSI Corrector Chip for Space-Borne mm-Wave Radiometer Spectrometers

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Abstract - **JPL has developed a 52-channel 150 MHz bandwidth autocorrelator spectrometer using specially designed ECL gate array correlator chips. This paper describes the characteristics of the ECL chip and the 52-channel autocorrelator. These autocorrelator spectrometers will be used with space-borne mm-wave radiometers for remote sensing of the Earth's atmosphere and astrophysical observations.**

1 Introduction

Radiometer spectrometers using digital correlation techniques are widely used in ground-based radio astronomy observatories. This technique was introduced by S. Weinreb for spectral line radio astronomy in 1961 [1]. Both medium and large scale integrated circuits were used in the earlier digital correlator designs. These correlators required many parts and consumed considerable power. Recent developments in VLSI technology have enabled this important digital processing technique to be implemented as an Application Specific Integrated Circuit (ASIC) and several new digital correlators have been built using ASIC chips. [2] [3] [4]. However, the ASICs made for ground based spectrometer applications were not designed for low DC power consumption.

Stable wideband spectrometers with low DC power consumption are required for space-borne operations. They will be used for remote sensing of the Earth's atmosphere with the Microwave Limb Sounder on the Earth observing system (Eos). There are also requirements for low power spectrometers for future astrophysics space missions such as the Submillimeter Infrared Line Survey (SMILS) and the Large Deployable Reflector (LDR). Correlation spectrometers will also find applications in space-borne thinned antenna arrays and the submillimeter lunar array.

The Jet Propulsion Laboratory is developing digital correlators for space-borne spectrometer applications. This is because of their advantages of high stability, low power, high reliability, small size and low mass. Future developments in both VLSI and material technologies will further reduce the size, DC power requirements and increase the speed for wider signal bandwidths. The digital autocorrelator spectrometer is preferred over other spectrometers, such as the multichannel filterbank and Acousto-Optic Spectrometer (AOS), because of its better stability. Also, the bandwidth and the resolution of an autocorrelator spectrometer can easily be changed by changing the clock frequency and/or by

using additional delay elements. In this paper, the autocorrelator background information will be presented. This is followed by the design of the digital correlator chip and the 52-channel autocorrelator spectrometer.

2 Background

2.1 Autocorrelation Theory

The autocorrelation function of a signal is expressed as follows:

$$R(\tau) = Lim\ 1/T \int_0^T f(t) * f(t+\tau)dt \ \text{ as } T \rightarrow \infty \tag{1}$$

where $f(t)$ is the input signal

τ is the delay time and

T is the integration time.

The incoming signal at microwave frequencies is down converted to baseband frequencies and then divided into two paths. In one path, a delay element with multiple taps at Δt intervals is introduced. The undelayed signal is then multiplied with each output from the tapped delay line and the products are integrated and averaged over the integration time T. The accumulated values represent an estimate of the autocorrelation function of the input signal $f(t)$. A theorem due to Wiener and Khintchine (F. N. H. Robinson, 1974) relates the autocorrelation function, in the time domain, to the power spectrum, in the frequency domain, by the Fourier transform equation:

$$S(f) = \int_0^\infty R(\tau) * cos(2\pi f\tau)dt \tag{2}$$

where $S(f)$ is the power spectrum of the input signal,

$R(\tau)$ is the autocorrelation of the input signal.

The autocorrelation function is even; therefore, only a cosine transform is required.

2.2 Digital Autocorrelator

Figure 1 shows the digital autocorrelator block diagram. In the autocorrelator, the input signal is band limited, sampled at the Nyquist rate and digitized to a few bits. The sampled signal is delayed using shift registers and multiplied with the undelayed sample using simple logic circuits. The multiplied output from each delay stage or channel, is accumulated in a binary ripple counter.

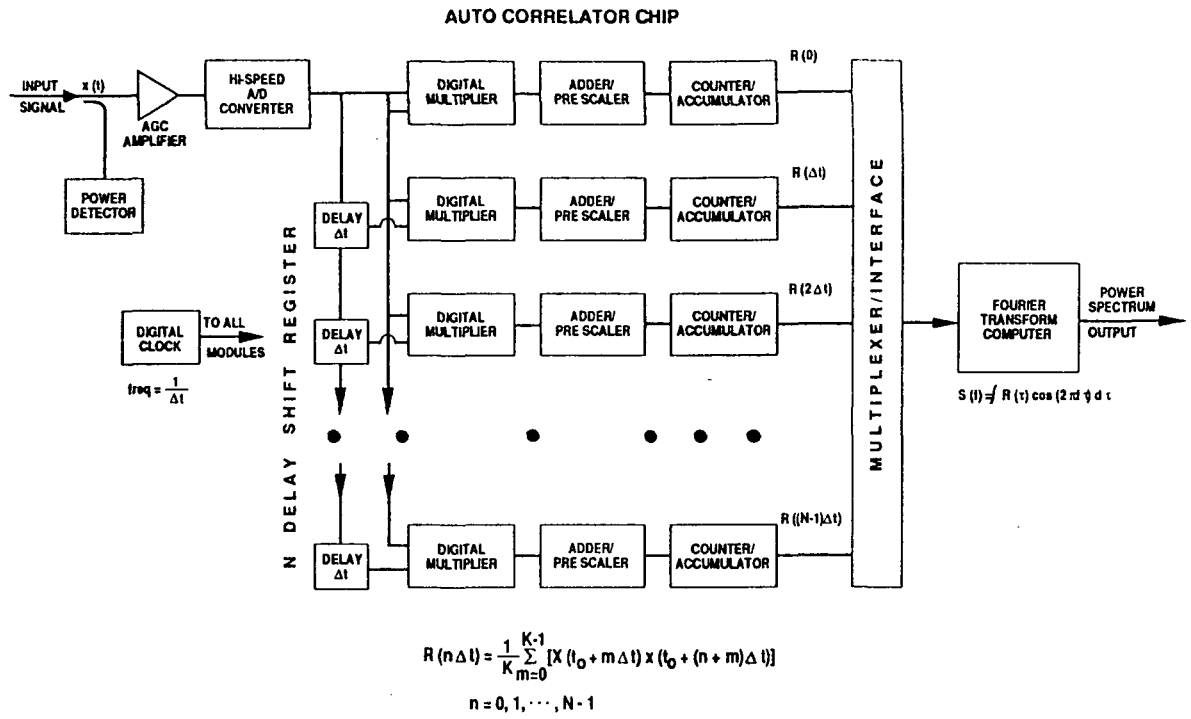

Figure 1: Digital autocorrelator spectrometer

The autocorrelation function for the sampled data can be expressed as:

$$R(n\Delta t) = \frac{1}{K}\sum_{m=0}^{K-1}[X(t_0) * X(t_0 + (n+m)\Delta t)] \tag{3}$$

where $n = 0, 1, \ldots N-1$ represent the delay in one of the signal paths,

K is the number of products in the integration time T,

Δt is the delay, usually made equal to the sampling interval.

The power spectrum is calculated by performing a Fourier transform. The N channels (corresponding to the N delay values) in the autocorrelation function are transformed into N points on the frequency domain by using the discrete Fourier transform (DFT) relationship:

$$P\left[\frac{j}{2n\Delta t}\right] = \frac{1}{N}\left[R(0) + 2\sum_{n=0}^{N-1} R(n\Delta t) * cos(\pi j/N)\right], \tag{4}$$

where $j = 0, 1, \ldots, N-1$,

$P\left[\frac{j}{2n\Delta t}\right]$ represents the power on the jth point on the output spectrum,

$R(0)$ is the correlation coefficient for the zero delay channel (= 1 after normalization) and

$R(n\Delta t)$ is the normalized autocorrelation coefficient for delay $n\Delta t$.

The input signal is digitized to only a few bits to permit a higher sampling rate, and thus increase the signal bandwidth. Limiting the number of bits speeds up the multiplication and addition because fewer digital operations are required. However, the Signal to Noise Ratio (SNR) of the correlator is degraded when only a few bits are used. The loss in SNR is 12% when two bit digitization is used [6]. Quantizing schemes representing the input signal by more than two levels to improve the SNR have also been considered by others [7]. However, the size, complexity and power of the digital circuits grow as the number of bits increases. This is of particular concern for space applications, where low DC power is important. The two bit correlator appears to offer the best trade-off between sensitivity, complexity of the hardware, and minimum power.

2.3 Digitizer

The first element in the digital correlator is the analog to digital converter, called the digitizer. The prototype 52-channel autocorrelator spectrometer uses a 2-bit digitizer. One of the bits represents the sign (zero-crossing detector output), and the second bit represents the magnitude. This magnitude bit is assigned a value "one" if the input voltage is outside the pre-determined limits +Vref. The four states of the 2-bit digitizer and the assigned weighting factors to these states are shown in Table 1.

SIGN	MAGNITUDE	WEIGHT
1	1	-n
1	0	-1
0	0	+1
0	1	+n

Table 1:

Setting the decision level of Vref equal to the RMS voltage of the input signal and $n = 3$, gives an SNR of 88% relative to the continuous correlator [6].

2.4 Correlator Multiplier

The digitized signals, are multiplied after one of the signals is delayed in time using shift registers. Using $n = 3$ for best SNR performance, and normalizing by 3, gives the product table shown in Table 2.

		Undelayed Signal			
	SM	11	10	00	01
Delayed signal	11	+3	1	-1	-1
	10	1	0	0	-1
	00	-1	0	0	1
	01	-3	-1	1	3

Table 2:

The inner products are deleted to simplify the circuit. This only results in 1% loss to the correlator SNR [7]. A bias of +3 is added to the products, so that only positive numbers need to be added to further simplify the adder circuit. Table 3 shows the final multiplication algorithm used in the hardware realization.

		Undelayed Signal			
	SM	11	10	00	01
Delayed signal	11	6	4	2	0
	10	4	3	3	2
	00	2	3	3	4
	01	0	2	4	6

Table 3:

2.5 Accumulators

The binary coded outputs from the multiplier are added, using a four bit adder and the carry output from the adder is accumulated using ripple counters. The length of the binary counters is determined by the rate at which the computer reads the counter values – typically a few times a second. The counter length is determined by the number of product terms that can be accumulated during each integration time.

3 52-channel autocorrelator spectrometer hardware

The prototype 52-channel, digital autocorrelator spectrometer (DACS) uses ECL correlator chips. The chip was designed by JPL, and was made by the Raytheon Corporation using 2 micron ECL gate array technology. This chip has 26 channels, requires 120 milliwatts of DC power per delay channel, and can be clocked up to 300 MHz. The power requirements may be considered as moderate to low compared to the other designs that have been implemented. A block diagram of the prototype autocorrelator spectrometer is shown in Figure 2.

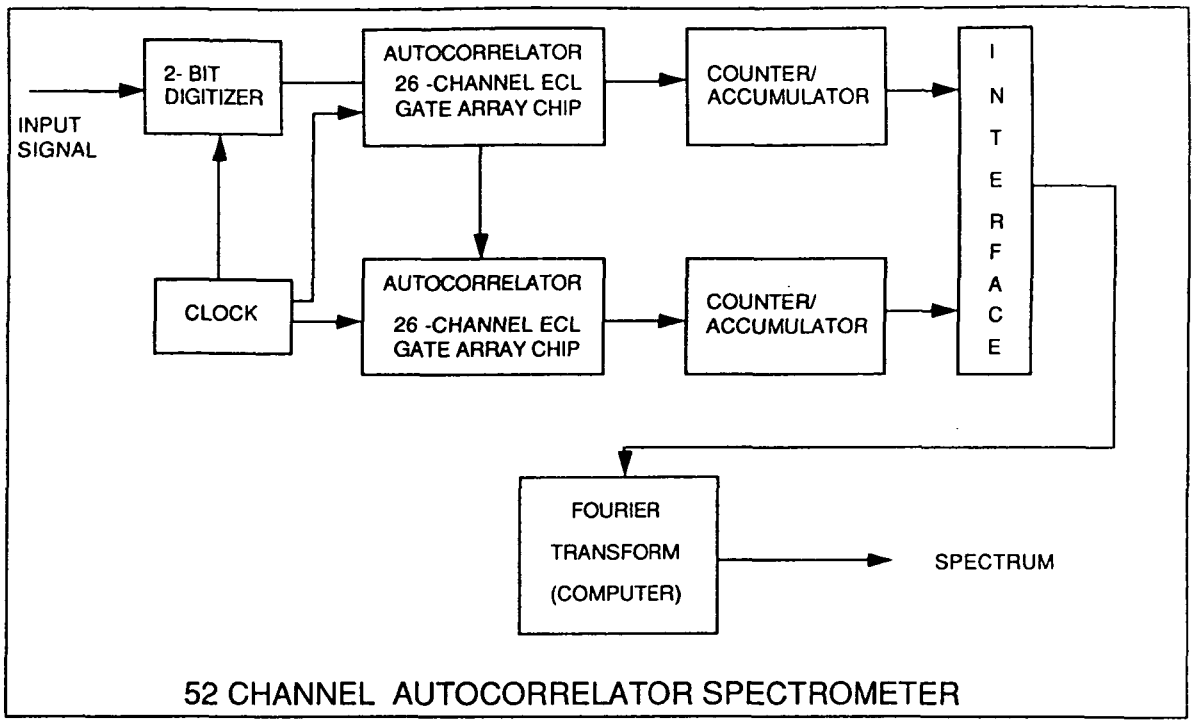

Figure 2: Block Diagram

3.1 2-bit digitizer

The 2-bit digitizer was designed at the California Institute of Technology for mm-wave astronomy (S. Padin and M. Ewing, 1989). The digitizer board uses a Plessey SP 93808 sub-nanosecond octal comparator chip. The digitizer board is made of Duroid-based copper clad material. Microstrip transmission lines are used to provide a 50-ohm characteristic impedance for ECL signals which have edge speeds of 1 nanosecond.

Three comparators are used for digitizing the input analog signal into a 2-bit word. The two comparators which detect the magnitude of the input signal are ORed together. The OR output and the output from a zero-crossing detector provide the simple encoding scheme shown in Table 1 for the two bit output. A stable, low noise, reference voltage generator is used for the comparator decision levels.

3.2 ECL Autocorrelator Integrated Circuit

The digital correlator is an Application Specific Integrated Circuit (ASIC), specially designed for the digital spectrometer development. The chip design was done using the CAD system on a Mentor workstation. The chip was made by Raytheon Corporation using the silicon foundry at Bipolar Integrated Technology Company in Beaverton, Oregon. Their unique wafer fabrication technique reduces transistor and metal capacitances, that reduces the device power, while maintaining ECL speeds.

The autocorrelator design was created using hierarchical design methodology. Pre and post layout simulations were performed on the design to verify the logic function and also to verify the circuit timing for proper operation at clock speeds up to 250 MHz. The design

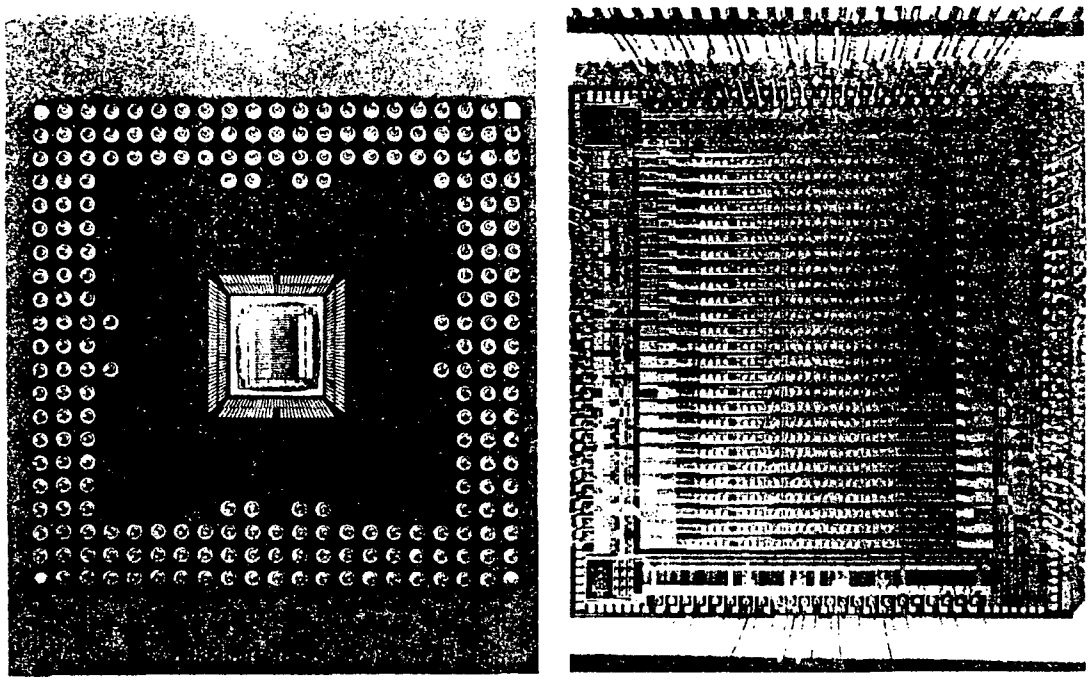

Figure 3:

hierarchy made it easier to run the simulation program on every schematic level and to identify the critical paths. The critical path analysis identified interconnecting lines (nets) in the multiplier/accumulator logic, and also in the pipeline architecture. The propagation delays in these critical paths were reduced by careful layout. A fault grading was done for the design, using the simulation vectors, that revealed a coverage of about 70%. The 30% loss in coverage was because the design utilized macrocell parts from Raytheon's library and some internal nodes in these parts were permanently tied to supply or ground.

The circuit layout was created for Raytheon's CGA 70E18 gate array topology which offers 12,800 gates and 176 input and output connections. The 26 channels of the correlator were laid out in the 26 contiguous rows, as shown in Figure 3. The array utilization for the correlator design is about 61%.

The silicon die, measuring 336 × 364 mils, with the correlator design, was packaged in a custom Pin Grid Array (PGA) package which was developed by Raytheon for its ECL gate array chips. The PGA is a 229-pin square package measuring 2.1 inches on a side. The pinout configuration for the correlator chip was selected so there was minimum skew in the timing of the signals inside the PGA package. It was also developed to make the signal routing easier on the printed circuit board with minimum number of plated through holes in the signal path.

The analog signal which is digitized and sampled is divided into two signals externally

3.2.8

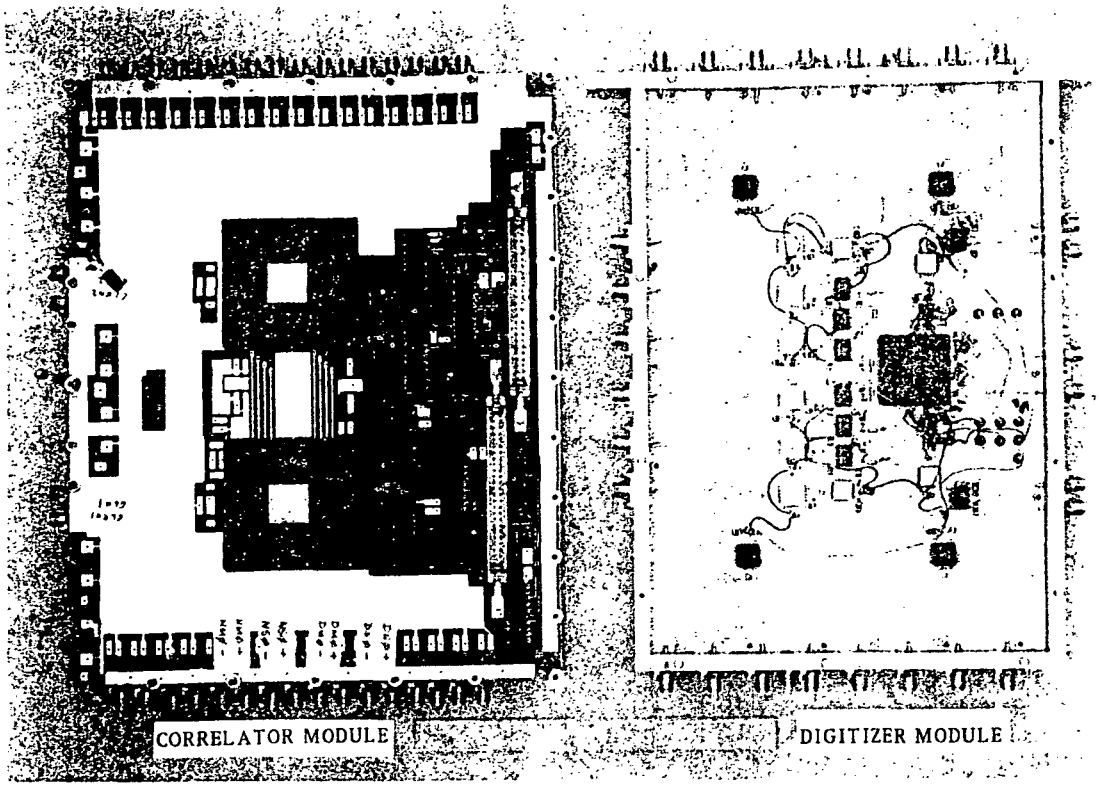

Figure 4:

and then given as inputs to the correlator. There are two signal paths inside the chip. One signal path is the direct or undelayed data, and the second signal path is the delayed data. The data in the second signal path is delayed by a 26 stage shift register inside the chip. The output from each stage of the 26-bit shift register is multiplied with the undelayed sample and the products are accumulated in a binary counter. A pipeline technique is used in the data path to increase the clock speed.

Each channel in the correlator chip has a 4-bit multiplier followed by a 4-bit adder/ accumulator stage. The two bit multiplication algorithm, shown in Table 3, is used. The carry output from the most significant bit (MSB) of the adder is scaled by a 3-bit binary counter. The 3-bit prescaler is used in each channel before the correlator data is output to an I/O pin. The prescaler reduces the output data rate allowing the use of low power CMOS counters for further accumulation outside the chip.

Standard 100K ECL logic is used for the signal inputs and outputs. The high speed signals such as clock, data inputs and outputs use differential drive. The correlated outputs use standard TTL logic.

3.3 52-channel Autocorrelator

The autocorrelator board, shown in Figure 3.3, is a four layer printed circuit board with outside layers used for interconnection and inside layers used as ground and VCC planes. The four layers are arranged in such a way that the outside layer and the layer below have 50 Ohm microstrip transmission lines for the high frequency signals. Two correlator chips are cascaded on the board to provide 52 channels. The TTL outputs from the correlator chips are buffered externally with BiCMOS drivers.

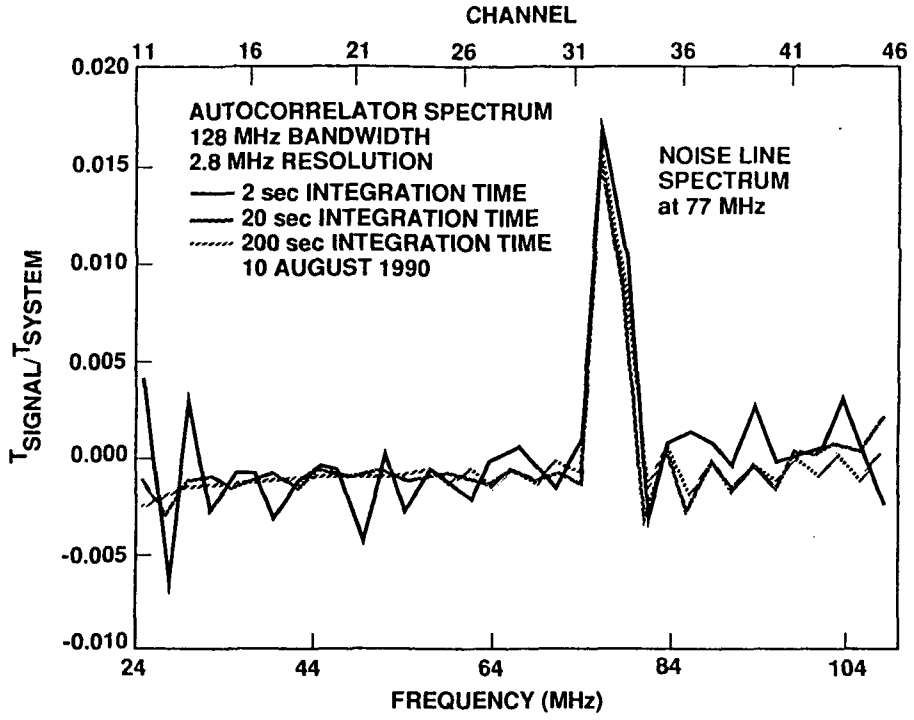

Figure 5: Digital Correlator

The outputs from the 52-channel correlator module are TTL or CMOS compatible. The output from each channel is accumulated using a 24-bit binary counter. Two ASIC CMOS counter chips are used for accumulating the 52-channel outputs. Each counter chip contains 32, 18-bit counters, and accumulate the correlation values for up to a one second integration period.

A PC compatible computer with a digital I/O card are used for the data acquisition and the Fourier transform. A one second pulse interrupts the computer after every integration period. At the interrupt, the computer reads all the 52 counter values in byte mode, and each channel value is arranged as an 18-bit word in memory. The counters are cleared, and the correlation continues for the next integration period.

4 Power spectrum measurement

A wideband noise source, with a simulated spectral line, was used to test the autocorrelator spectrometer. The noise source output is prefiltered with a 100 MHz low pass filter to eliminate aliasing when the digitized signal is sampled at 250 MHz. The simulated line source was generated by passing white noise through a 1 MHz wide bandpass filter centered at 77 MHz and added to the broadband noise. The power spectrum, measured with the simulated line source, for three integration times is shown in Figure 5. These curves show the reduction in spectrum noise as the integration time is increased.

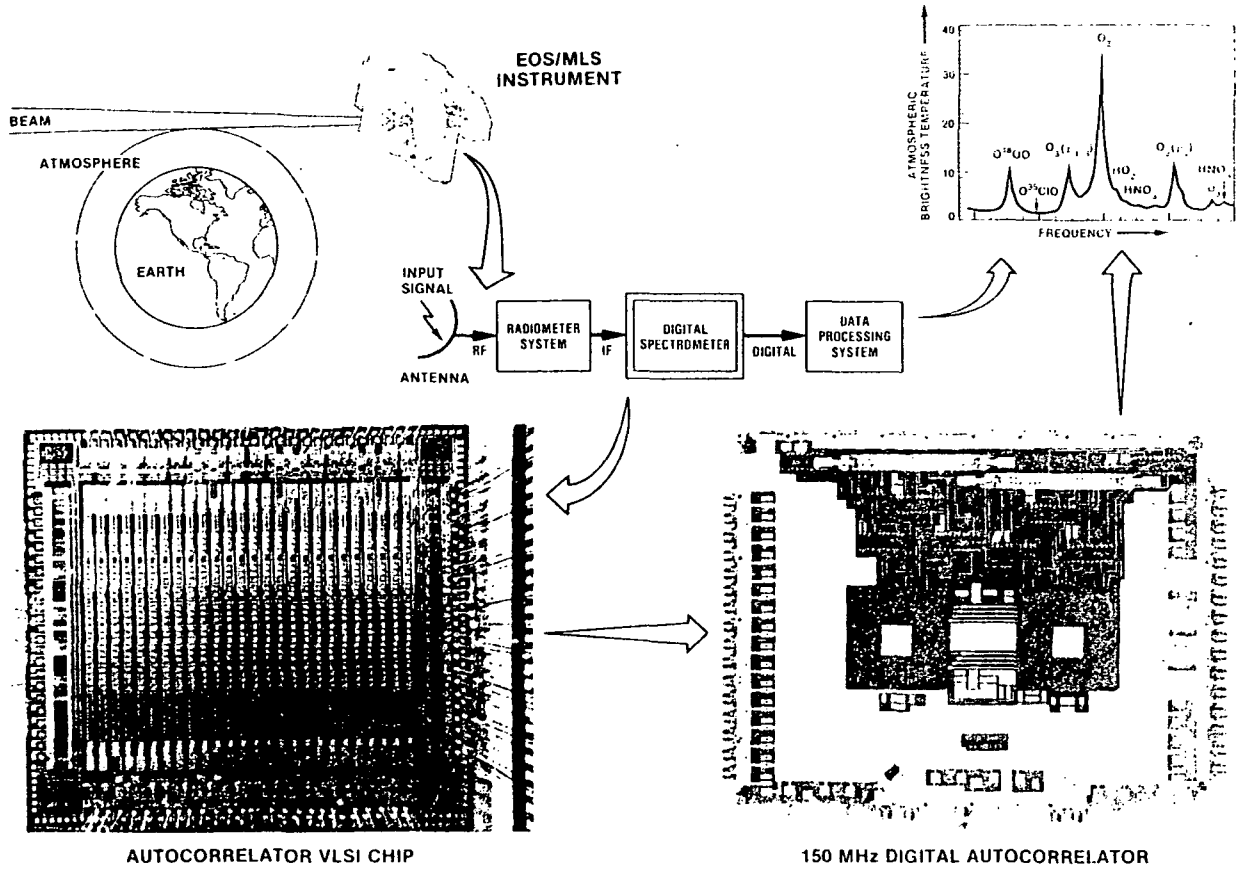

Figure 6:

5 Applications

The digital autocorrelator spectrometer using VLSI chips is an attractive choice for the space-borne applications due to its stability, small size, mass, and low power requirements. Figure 5 shows one of the applications where the digital autocorrelator spectrometer will be used with millimeter-wave radiometers for spectral analysis of molecular emission lines in the Earth's atmosphere. Other space applications, where the digital autocorrelator spectrometers may be used, are shown in Table 4.

6 Conclusion

The digital spectrometer using the autocorrelation technique will replace analog filterbank spectrometers which are large, massive and require a large DC power. The goal of the

Flight Project	Science Objective	Requirement	Launch Date
EOS/Microwave Limb Sounder (EOS/MLS)	Atmospheric Ozone depletion/chemistry	40 Wideband 10 Narrowband low power spectrometers	2000
Submillimeter Moderate Mission (SMMM)	Astrophysics interstellar molecules	5-10 wideband low power spectrometers	2001 cooperative project with France (CNES)
Advanced Microwave Sounding Unit C (AMSU-C)	Earth upper atmosphere temperature sounding	narrowband low power spectrometer	1996
Lunar Submillimeter Interferometer	Astrophysics, high spatial resolution imaging	many wideband low power, cross correlator spectrometers	> 2005
Large Deployable Reflector (LDR)	Astrophysics, interstellar molecules	many wideband low power spectrometers	> 2010

Table 4:

digital correlator development program is to develop spectrometers with bandwidths, to 2 GHz, and low DC power consumption of 5 milliwatts per delay channel. The present ECL correlator chip, operates up to a bandwidth of 150 MHz, and requires about 120 milliwatts of DC power per delay channel. Advances in digital technology and new material processes will increase the bandwidth of the digital technique and reduce the power requirements. These spectrometers will find space applications in remote sensing of the Earth's atmosphere and astrophysical observations.

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