CMOS Output Buffer Wave Shaper

L. Albertson, S. Whitaker and R. Merrell
NASA Space Engineering Research Center
for VLSI System Design
University of Idaho
Moscow, Idaho 83843

Abstract - **As the switching speeds and densities of Digital CMOS integrated circuits continue to increase, output switching noise becomes more of a problem. This paper reports a novel design technique which aids in the reduction of switching noise. The output driver stage is analyzed through the use of an equivalent RLC circuit. The results of the analysis are used in the design of an output driver stage. A test circuit based on these techniques is being submitted to MOSIS for fabrication.**

1 Introduction

There are two main types of output switching noise in CMOS circuits which can cause problems for circuit designers. These types, although closely related, can be defined as ground bounce, which is the variation of the chip ground to the external ground and ringing (undershoot/overshoot) on the output signal lines. Ground bounce, is caused by the rapidly discharging or charging of the output capacitance and is accentuated by simultaneously switching output drivers. Ringing on output signals is caused by the improper damping of the inherent RLC discharge or charging loop. Both of these sources of noise are attributed to having an inherent inductance in the charging or discharging path of the output load capacitance.

There are several reasons why output switching noise should be eliminated or at least reduced below some specified level. Noise caused by ground bounce can cause false switching of internal gates leading to incorrect logic states and reduced reliability of the integrated circuit. Ringing on signal lines is also undesirable in that it can falsely trigger an input resulting in incorrect data to other circuits in the system. Both types of switching noise are also a problem in the area of integrated circuit testing.

Over the past decade or so there has been a significant amount of effort put forth in finding solutions to the problems of output switching noise. Many of these solutions have not been published in the literature due to integrated circuit manufacturers attempting to maintain their competitive edge. However, most of these solutions are based upon three main approaches:

1. providing a slower turn on time of the output transistors,
2. staggering the turn-on times for the different output transistors [1], and
3. a noise sensing feedback approach.

All of these techniques have one main drawback; the output buffer will be inherently slower, thus speed is sacrificed for a decrease in the amount of generated output noise.

This paper concentrates on analysis of the undershoot/overshoot problem and a possible solution for use in high speed CMOS VLSI circuits.

2 Analysis

A typical CMOS output driver circuit is shown in Figure 1. It consists of scaled inverter stages which are generally a factor, f (in the range from 3 to 8) times larger than the previous stage. The problem of scaling to optimize delay and/or area of the driver chain has been examined by several authors [2]-[6]. For the purposes of this work, scaling to optimize delay of the output stage was not addressed, however it can become very important when maximum speeds are required since the ringing noise reduction techniques create an extra time delay.

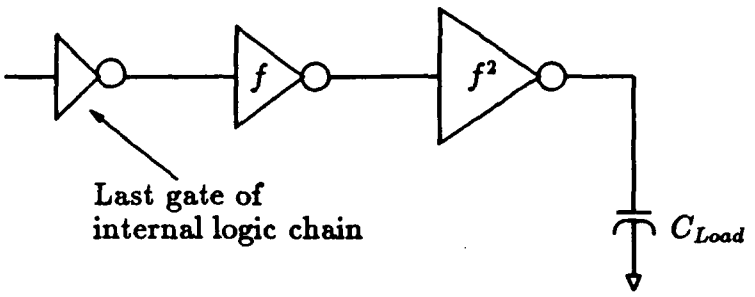

Figure 1: Typical scaled output buffer stage

The output driver structure of a CMOS VLSI circuit can be complicated to analyze, if viewed as a complete circuit. Therefore, it is necessary to break it down into simpler subcircuits which can be easily analyzed. The first part of this analysis will deal with the RLC discharge loop of the load capacitance during a low going transition of the last stage of the output buffer. Secondly, the resistance of the output driver FET will be analyzed and finally a technique for minimizing the problems of ringing will be discussed.

2.1 RLC Discharge Loop

A typical CMOS pull-down circuit of an output buffer stage is shown in Figure 2. It consists of an n-channel transistor with its drain tied to a load capacitance, its source tied through an inductance to ground, and the gate tied to an input voltage source. The pull-up circuit would be very similar, with a p-channel transistor with the source tied through an inductance to Vcc.

Using the simplified equivalent RLC circuit shown in Figure 3, the output switching noise produced by the circuit of Figure 2, can be analyzed.

In the equivalent RLC circuit, the n-channel transistor is replaced by a switch, S and a resistance R. The resistance R represents the ON resistance, R_{on} of the device and the

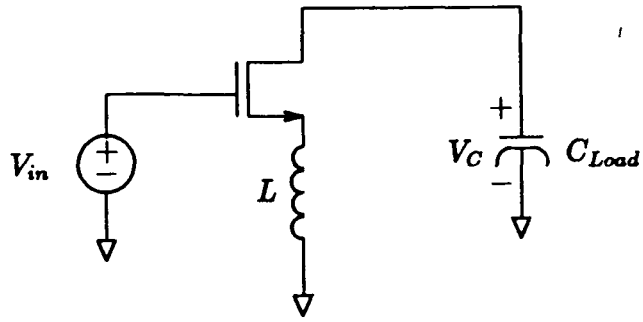

Figure 2: CMOS pull-down circuit of an output inverter stage

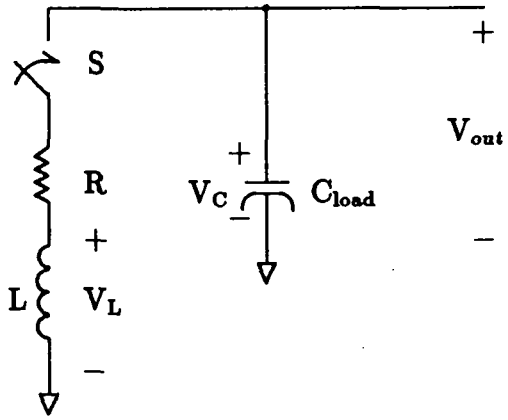

Figure 3: RLC circuit representation of the CMOS pull-down circuit of an output stage

switch S represents the switching point of the device. The value of C_{Load} is the lumped sum of the capacitances associated with the n and p-transistor drain regions, bonding pad, circuit packaging, PWB traces and input capacitances of the receiving devices. The value of L is the sum of the inductances associated with the internal ground ring, the connections between the bonding pads and the IC pins, (packaging parasitics) and the PWB ground trace (plane) and signal trace. The RLC circuit of Figure 3 can be analyzed as follows. Initially the capacitor will be charged to V_c (by the pull-up p-transistor). With the switch open, no current flows in the circuit, thus there is no initial condition for the inductance, L. At time $t = 0$, the switch is closed. The circuit is excited by the initial charge on the capacitance and the total response of the circuit can be determined as follows:

$$\sum V_d = 0 = Ri(t) + L\frac{d_i}{d_t} + \frac{1}{C}\int i(t)dt - V_c(0^-) \tag{1}$$

and

$$V_c(0^-) = Ri(t) + L\frac{d_i}{d_t} + \frac{1}{C}\int i(t)dt \tag{2}$$

Applying the properties of Laplace transforms yields:

$$\frac{V_c(0^-)}{s} = RI(s) + sLI(s) + \frac{1}{sC}I(s) \tag{3}$$

Solving for the network function $\frac{I(s)}{V_c(0^-)}$ yields:

$$\frac{I(s)}{V_c(0^-)} = \frac{1}{L}\left(\frac{1}{s^2 + \frac{R}{L}s + \frac{1}{LC}}\right) \tag{4}$$

The characteristic equation of the network is given by the denominator of the equation given above. Solving the quadratic equation for s yields:

$$s = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{5}$$

Thus the roots of the characteristic equation are:

$$s_1 = -\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{6}$$

$$s_2 = -\frac{R}{2L} - \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{7}$$

Since the quantity under the radical sign can be positive, zero or negative, three distinct solutions exist which will produce an overdamped, critically damped or underdamped response respectively.

Case 1: Roots are real and unequal resulting in an overdamped response

$$\left(\frac{R}{2L}\right)^2 > \frac{1}{LC}$$

Case 2: Roots are equal resulting in a critically damped response

$$\left(\frac{R}{2L}\right)^2 = \frac{1}{LC}$$

Case 3: Roots are complex conjugates resulting in an underdamped response

$$\left(\frac{R}{2L}\right)^2 < \frac{1}{LC}$$

For a typical case of L=20nh and C=5pf, if the MOSFET resistance is less than 127Ω, then the circuit to be underdamped and will ring as shown in Figure 4. If the value of the inductance was even larger and the capacitive load even smaller, then R would be required to be even greater. Thus, in order to properly damp the RLC circuit, it is necessary to analyze the resistance characteristics of the MOSFET so that a good estimation of it's ON resistance can be obtained.

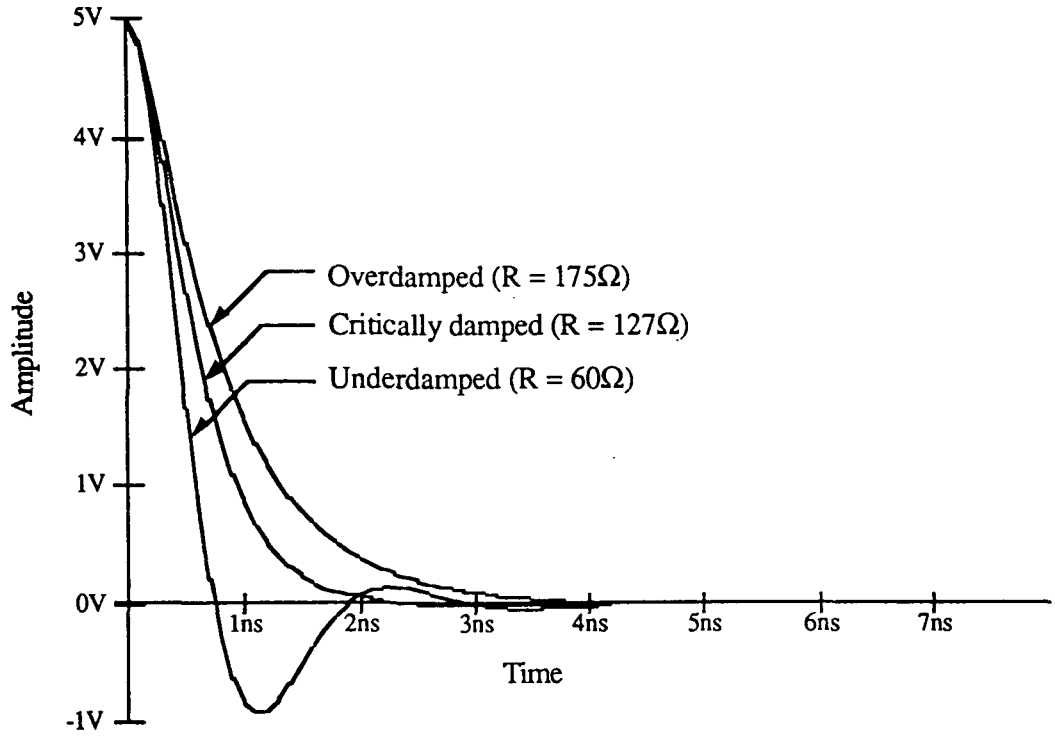

Figure 4: Voltage across the load capacitance for $L = 20nh$ and $C = 5pf$

2.2 MOSFET Resistance Characterization

The ideal (first order) equations describing the behavior of the nMOS transistor in the different regions of operation are given by [7] and shown below.

$$I_{ds} = \begin{cases} 0; & V_{gs} - V_t \leq 0 \quad cut-off \\ \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}}{2}\right]; & 0 < V_{ds} < V_{gs} - V_t \quad linear \\ \frac{\beta}{2}(V_{gs} - V_t)^2; & 0 < V_{gs} - V_t < V_{ds} \quad saturation \end{cases}$$

where I_{ds} is the drain to source current, V_{gs} is the gate to source voltage, V_{ds} is the drain to source voltage, V_t is the transistor voltage threshold voltage, and β is the gain factor of the MOS transistor and is given by:

$$\beta = \frac{\mu_0 \varepsilon_r \varepsilon_0}{t_{ox}} \frac{W}{L} \tag{8}$$

The MOSFET resistance equation for the device in the linear region can be found by taking the partial derivative of I_{ds} with respect to V_{ds}.

$$R = 1/\frac{\partial I_{ds}}{\partial V_{ds}} = \frac{1}{\beta(V_{gs} - V_t - V_{ds})} \tag{9}$$

A simple method of approximating the MOSFET resistance is by using a linear resistor. However, upon a more detailed examination, this does not prove very accurate since the

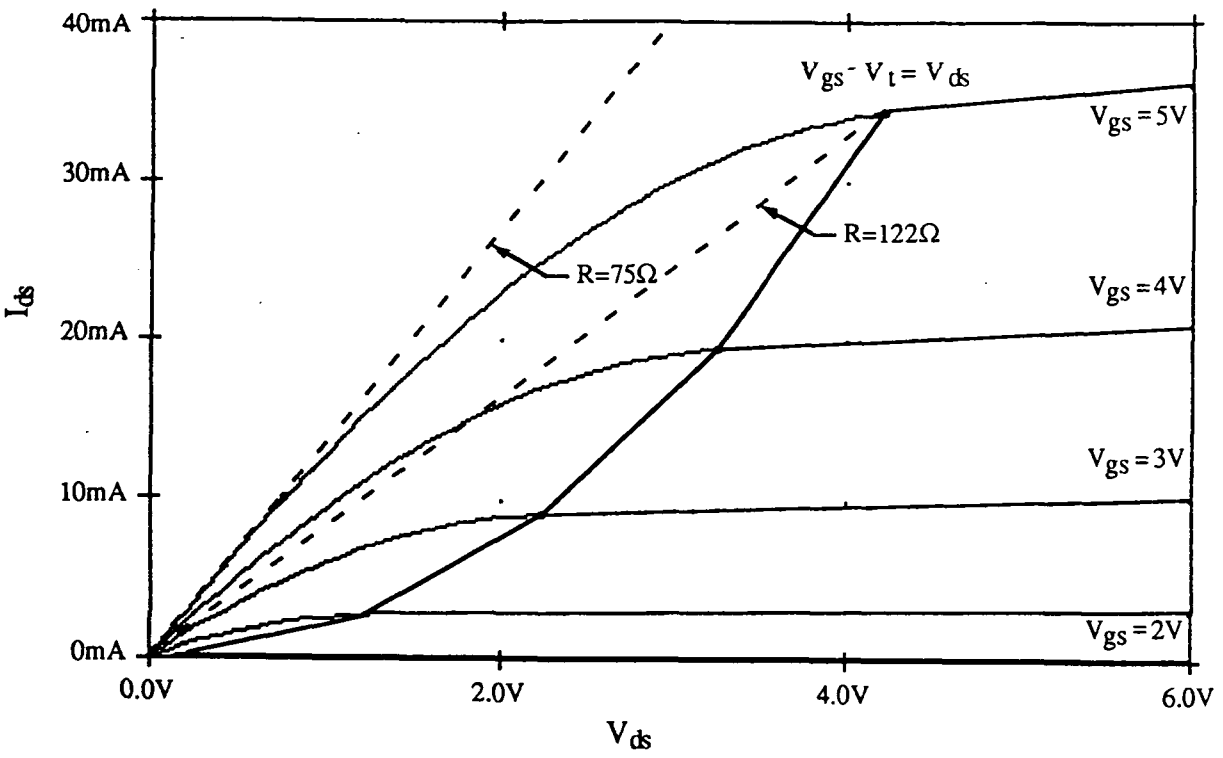

Figure 5: I-V curves and equivalent resistance of a MOSFET

approximation does not account for the nonlinear, time-dependent current-voltage characteristics of a MOSFET. Thus the equivalent resistance is a function of both V_{ds} and V_{gs}, such that $R = \beta f_n(V_{ds}, V_{gs})$. Since the input signal V_{gs}, in a normal system will not have an infinite rise time, this makes the resistance characterization very difficult.

Shoji [8] estimates the equivalent DC resistance in the following manner. Firstly, he assumes that the gate input signal switches instantaneously, thus eliminating V_{gs} from the function yielding:

$$R = \beta V_{gs} f_n(V_{ds}) \tag{10}$$

From Fig. 5, it can be seen that the resistance at the maximum input voltage, $V_{gs} = 5V$ is equal to $\frac{V_{gs}-V_t}{I_{ds}} = R_0 \approx 122\Omega$, the point the transistor moves into the linear region of operation. When the load capacitance has been completely discharged at time $t = \infty$, V_{ds} nears $0V$, and the resistance is equal to $\approx 75\Omega$, the lower bound.

In light of this, and looking back at the previous example where $L = 20nh$ and $C = 5pf$, the circuit would be underdamped when the equivalent resistance was less than 127Ω. This point on the I-V curves is when the capacitor was fully charged to $5V$, thus from that point down to when the capacitor becomes fully discharged, the MOSFET resistance will be less than the required 127Ω for overdamping.

In reality, the transistor operates quite differently on the I-V curves when a finite rise time signal is applied to the gate of the device as shown in Figure 6.

As the gate voltage rises towards $5V$, at $V_{gs} = V_t$ the transistor begins to turn on, and

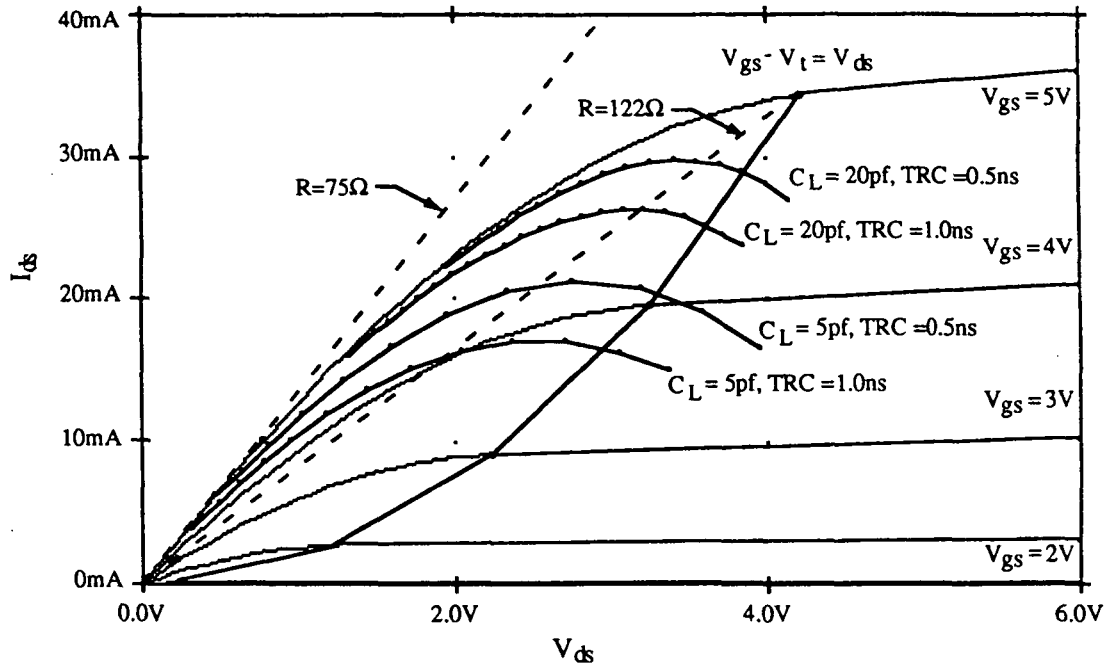

Figure 6: MOSFET I-V curves and equivalent resistance as a function of C_L and input rise time

the capacitive load begins to discharge, thus never reaching the point on the $V_{gs} = 5V$ curve where $V_{gs} - V_t = V_{ds}$. The transistor actually operates for a period of time on the lower V_{gs} curves as a function of the rise time. This is very beneficial to the damping of the RLC circuit since the resistances are higher on these lower curves as V_{gs} is transitioning toward $5V$. Therefore, waveshaping the input voltage such that the transistor operates on the lower V_{gs} curves for a longer period of time is beneficial in damping the RLC discharge loop. The disadvantage to using this technique for properly damping the RLC discharge loop is that an added time delay is introduced.

2.3 Input Signal Waveshaping

There are several techniques which can be used for waveshaping the input signal to the output driver transistor. One possible way would be to size the pre-driver stage such that it can not effectively drive the input capacitance of the output driver transistor, thus slewing the input signal. Another technique [1], uses a nMOS pass-transistor, controlled by a voltage, V_{Bias}, in series with the output driver gate input as shown in Figure 7.

This technique has the advantage that the amount of resistance can be controlled somewhat by varying V_{Bias}. The drawback is that there is not a very large range over which V_{Bias} can be adjusted and still provide enough voltage to the gate of the output driver transistor. The MOSFET resistance also increases dramatically as the input voltage to the pass-transistor is increased.

These problems can be overcome by using a transmission gate in place of the nMOS pass-transistor, as shown in Figure 8.

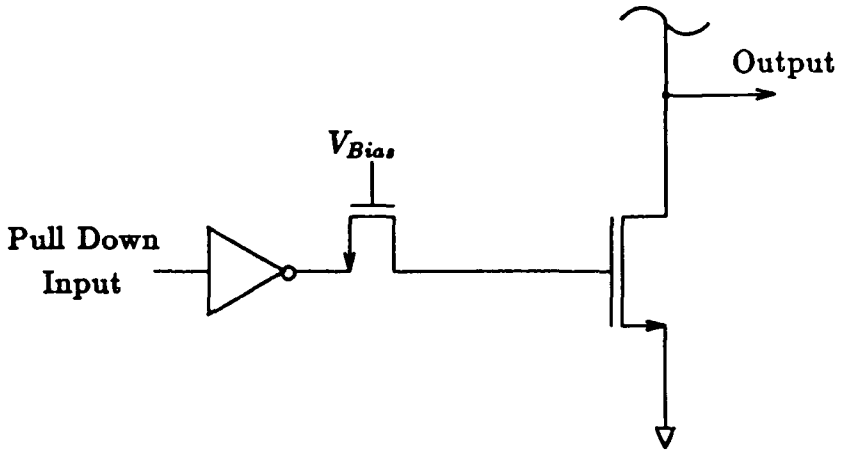

Figure 7: Output Buffer with input rise time control using an n-channel pass transistor

This also has the advantage of being adjusted by bias voltages, and will allow a wider range of adjustment. The resistance is also more constant since it is the parallel combination of the n-transistor and p-transistor resistances.

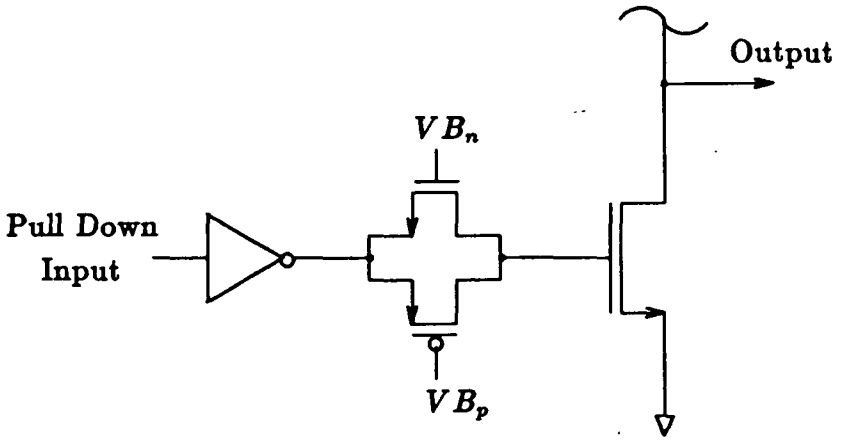

Figure 8: Output buffer with input rise time control using a transmission gate

A bi-directional TTL compatible I/O pad was designed in the MOSIS $2\mu m$ CMOS process using the techniques outlined above and shown in Figure 9.

3 Simulation Results

Shown in Figure 10 is the simulation model which was used to simulate output ringing as well as delay and rise and fall time characteristics of the uncompensated and compensated output buffers. The model includes 30nh of inductance between the buffer and the Vdd and Vss supplies and the 5pf output load capacitance. Simulations were performed using the PSpice level 1 electrical model. A set of typical parameters for the model were derived by averaging extracted parameters from 10 recent runs from a $2\mu m$ CMOS MOSIS foundry.

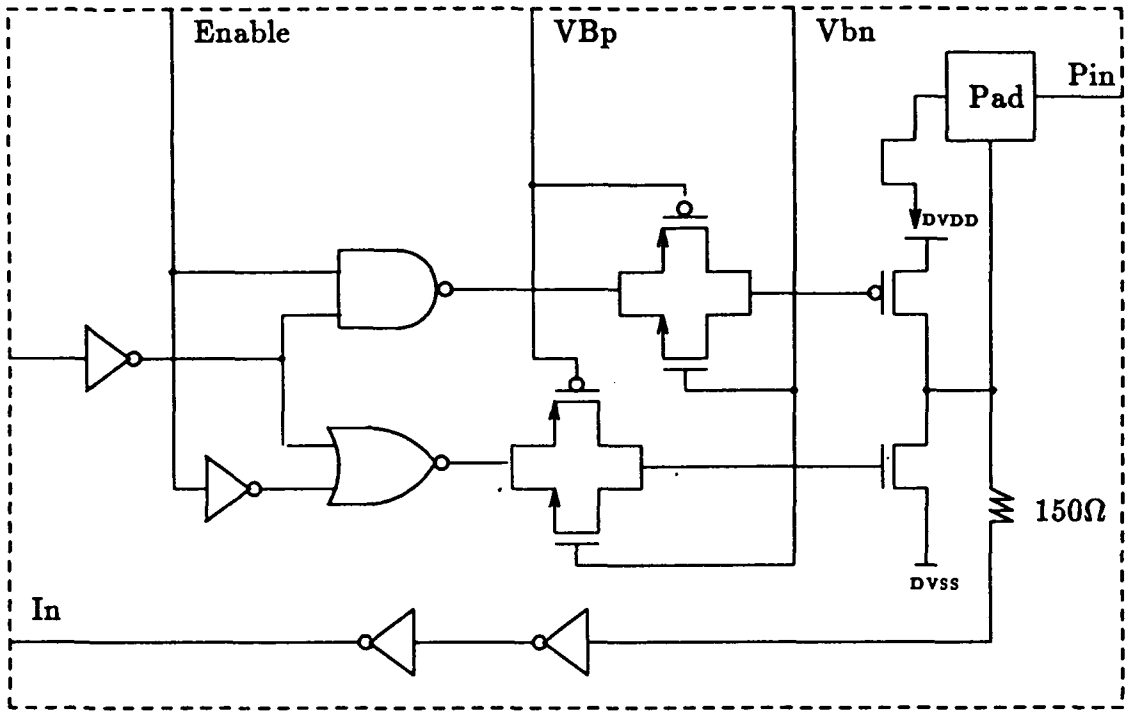

Figure 9: Bi-directional I/O Pad with ringing compensation

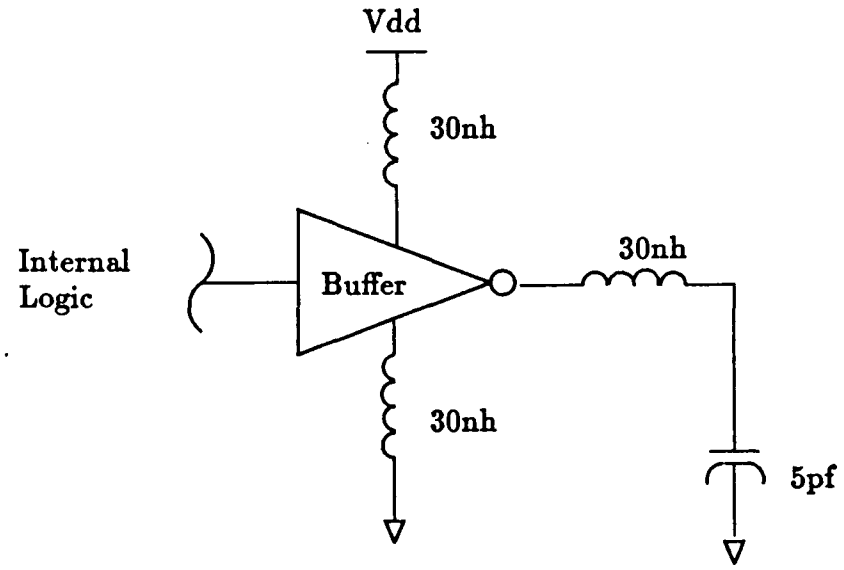

Figure 10: Output buffer simulation model

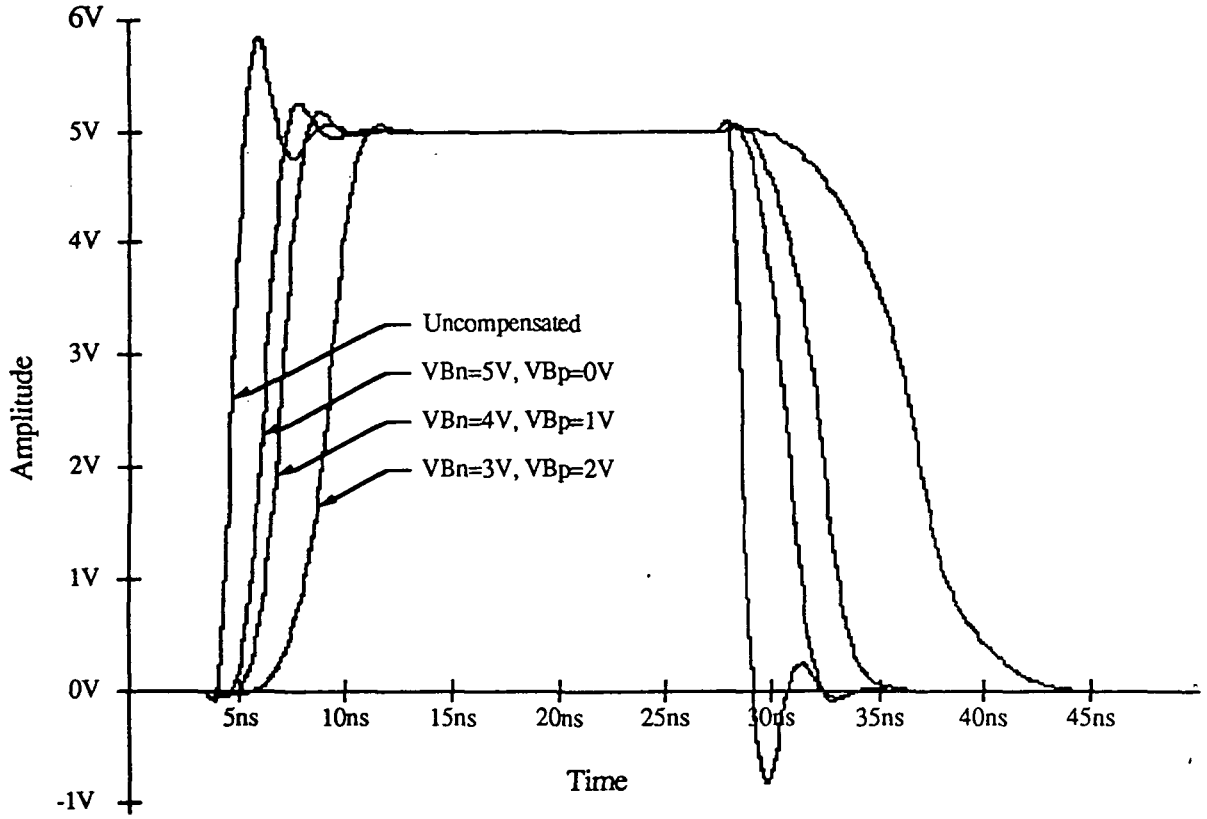

Figure 11: Uncompensated and compensated output buffer waveforms

The results of the simulations of the uncompensated and compensated buffers are summarized in Table 1 and shown in Figure 11. The results for the compensated buffer include three sets of gate voltages for the transmission gates to show the effects they have on the output ringing, delay time and rise and fall time. As can be seen in Figure 11, the cost of reducing the output ringing is sacrificing some speed performance.

Typical Case Parameters, 25 deg $C, Vdd = 5V, C_L = 5pf$				
Simulated Parameter	Standard Buffer	Compensated Buffer @ various gate bias		
		$VB_n = 5V$ $VB_p = 0V$	$VB_n = 4V$ $VB_p = 1V$	$VB_n = 3V$ $VB_p = 2V$
Overshoot (peak)@ $5V$	$0.839V$	$0.168V$	$0.250V$	$0.050V$
Undershoot (peak)@ $0V$	$-0.818V$	$-0.084V$	$-0.002V$	none
Delay Time	$2.34ns$	$4.12ns$	$5.28ns$	$8.53ns$
Rise Time	$0.90ns$	$1.64ns$	$1.96ns$	$2.88ns$
Fall Time	$0.81ns$	$2.38ns$	$3.43ns$	$6.99ns$

Table 1: Comparison of simulation results

4 Evaluation Test Circuit

An evaluation test circuit has been designed in the $2\mu m$ CMOS n-well process, and is being submitted to MOSIS for fabrication. Both an uncompensated and compensated buffer stage were fabricated on the same test chip. Special considerations were given to the layout to help eliminate measurement errors due to the differences in power bus drops, lead inductances, and time delays of input and output paths so that accurate results can be compared. The buffers were designed such that they are identical with the exception of the inclusion of the transmission gates in the compensated version. Their inputs were driven from the same source which was placed an equal distance from each buffer. The pads were placed such that the distance to the Vdd and Vss pads was as nearly identical as possible.

5 Summary

The problems dealing with ringing on the output signals of CMOS VLSI circuits has been discussed, analyzed and a solution proposed. A compensated output buffer was designed, using the techniques discussed, which helps to minimize the ringing effects by changing the resistance of the output driver transistors. This is accomplished by slewing the input signal to their gate using voltage controlled transmission gates. This technique allows for the proper damping of the RLC charging and discharging loops. Simulation results have been presented which substantiate the theoretical analysis. A comparison between the amount of output ringing versus the delay time and rise and fall times of the buffers was presented. A test circuit was designed in the $2\mu m$ CMOS n-well process and has been submitted to MOSIS for fabrication.

Acknowledgements

The authors wish to acknowledge the NASA Space Engineering Research Center program whose support made this investigation possible. Additionally, we would like to thank Barbara Martin for typesetting this document.

References

[1] G. Canepa, et al., "A 90ns 4Mb CMOS EPROM," IEEE Int Solid State Circuits Conf. Dig. Tech. Papers, Feb 1988, pp. 120-121, 323.

[2] H. C. Lin and L. W. Linholm, "An Optimized Output Stage for MOS Integrated Circuits," IEEE J. Solid-State Circuits, vol. SC-10, no. 2, Apr. 1975, pp. 106-109.

[3] R. C. Jaeger, "Comments on 'An Optimized Output Stage for MOS Integrated Circuits'," IEEE J. Solid-State Circuits, vol. SC-10, no. 3, June 1975, pp. 185-186.

[4] A. M. Mohsen and C. A. Mead, "Delay-Time Optimization for Driving and Sensing of Signals on High-Capacitance Paths of VLSI Systems," IEEE J. Solid-State Circuits, vol. SC-14, no. 2, Apr. 1979, pp. 462-470.

[5] M. Nemes, "Driving Large Capacitances in MOS LSI Systems," IEEE J. Solid-State Circuits, vol. SC-19, no. 1, Feb. 1984, pp. 159-161.

[6] N. C. Li, G. L. Haviland and A. A. Tuszynski, "CMOS Tapered Buffer," IEEE J. Solid-State Circuits, vol. SC-25, no. 4, Aug. 1990, pp. 1005-1008.

[7] N. Weste, and K. Eshraghian, "Principles of CMOS VLSI Design, A Systems Perspective," Addison-Wesley, Reading, Massachusettes, 1985.

[8] M. Shoji, "CMOS Digital Circuit Technology," Prentice-Hall Inc., Englewood Cliffs, New Jersey, 1988.