Minimal Test Set for Stuck-at Faults in VLSI

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Abstract – **Minimal test sets have the property that each input vector simultaneously tests several faults in a network. Existing techniques to determine a minimal set of detection tests rely heavily on complicated algebraic techniques. In this paper, two new methods are presented which do not require Boolean algebra or Karnaugh maps. The first is a graphical approach using fault folding graphs. The second is a design by inspection technique. This work follows the unique approach of first finding all the faults that can be detected by a single test. This tremendously reduces the work required to determine a minimal test set. The design by inspection method could be automated for programmatic generation of minimal stuck-at fault tests.**

1   Introduction

System and circuit design, over the years has advanced much and achieved a great deal of sophistication and reliability. Because of increased complexity and the lack of externally available test points, circuits implemented in VLSI are especially difficult to test. Furthermore, the shrinking distance between signal lines due to reduced geometries and complex processes has introduced new types of failures, such as data dependent or neighboring-interaction faults. When devices are tested only functionally their reliability can be relatively low. Specialized fields, viz. Space Engineering and Aero-Engineering often need *zero-defect* systems. To ensure zero-defect conditions all the system components must be tested comprehensively for defects and faults.

The problems of determining whether or not a digital circuit operates correctly and of ensuring its correct operation in spite of failure of certain parts are of both practical concern and theoritical interest. Present day digital systems may be disabled by almost any internal failure. Due to the testing constraints, the emphasis is shifting from efficient designs to testable designs [9]. Considerable work has been done in recent years in the field of Fault diagnosis [6,8,9,10,11]. But there is still a need for simpler, better and more efficient test techniques.

Often the information provided to test engineers concerning a digital circuit consists solely of its logic schematic diagram. Boolean equations, Karnaugh maps and State tables are often not available and are tedious to derive. Since the starting data for generation of the *Fault Diagnostic* tests is often the logic schematic diagram, methods developed to generate fault-tests should take this into account [3].

The main objective of this work is to develop techniques to arrive at a minimal set of test vectors for stuck-at faults. Although this problem has been studied by many researchers, a sufficiently simple solution is not available at present. The *simple* methods usually generate a single stuck-at fault test set which is *nearly minimal* but not *completely minimal*. The methods which do generate minimal stuck-at fault test sets, are quite complicated and can get out of hand for large circuits. This problem first gained the attention of researchers in the Sixties [1] and continued in the Seventies [2,4,5,17], but none of these complex methods became popular. The procedures proposed here are very simple and highly efficient. The only required data is the logic schematic diagram. There is no need to either derive Boolean equations or Fault tables, etc..

Section 2 reviews, the need for testing and various terms and terminologies associated with testing. Section 3 reviews the previous work in connection with minimal fault test vectors. In Section 4, the procedure to arrive at the minimal test set for stuck-at faults is derived and examples are given.

2 Testability in Combinational Logic Circuits

2.1 Testing Approaches

There are two basic approaches to testing digital systems: *Functional* and *Structural*[1]. In functional testing, the aim is to verify that the system under test is fault-free by determining that all its functions (tasks) are being carried out as specified (a counter increments or decrements correctly, Memory locations can be read from or written into, etc.). In structural testing, all the individual hardware constituents of the unit are ensured to be perfect. Thus a structural test assures every AND gate gives an output of 1 iff all its inputs have a logic value of 1: that every flipflop can be properly set, reset or toggled; and so forth.

Functional tests are based on heuristics and are derived manually on the basis of familiarity with the system without regard for fine structural details. It is not unusual for functional tests to be limited in fault detecting capabilities to only half of the possible faults in a digital unit [13]. Structural tests are more amenable to being derived algorithmically and hence the whole process could be automated. Structural testing can be made complete although it might result in excessively long test times for large systems.

2.2 Fault Detection in Combinational Circuits

Faults could be of two types: *temporary* and *permanent*. Temporary faults may occur due to noise and nonideal transient behavior of switching components while the permanent faults may result from component or physical failures. This work deals only with permanent faults. This work is also limited to the fault detection in combinational circuits, that is, feedback loops are not allowed in the circuits being tested.

One way of determining whether a combinational circuit is fault-free is to apply all possible input combinations and verify the veracity of the results by comparing them with the truth table or a faultless version of the same circuit. Any deviation indicates the

presence of a fault. If we know the mapping of all possible faults to the deviations observed, we could diagnose the fault (in the case of 1-1 mapping) or at least classify the faults within a subset of faults whose effects on the circuit outputs are the same (onto-mapping).

Such exhaustive tests are very lengthy and hence impractical. Moreover for most circuits, it is possible to diagnose the faults by a shorter test sequence. Such tests are referred to as either fault detection or fault location tests depending on whether they merely reveal the presence of a fault or in addition locate it and diagnose it. The precise identification of the fault that has occurred is very complicated and often impossible, since two different faults may give rise to identical incorrect responses. Therefore the main effort is directed to devising tests which locate the impaired sub-circuit.

In order to arrive at simple and practical fault detection procedures, it is necessary to make several simplifying assumptions. It is a normal practice in the field of fault diagnosis to assume that only single faults occur. Testing for single faults will simultaneously test certain multiple faults too but not all multiple faults are tested. If a network contains logical redundancy, then not all faults are detectable [5].

2.3 Fault Models

The primitive fault or "stuck-at" fault model is a widely accepted fault model. It supposes that the *failure mechanism* in a gate results in its inputs or outputs being either stuck-at 1 or stuck-at 0. The notation s-a-1(0) and s@1(0) are used interchangeably to represent stuck-at-1(0) faults.

An AND gate with 1 or more inputs or the output s-a-0 supplies a logical signal of 0 to all of the gates to which it is connected. A j-input AND gate with k-inputs s-a-1 becomes a j-k input AND gate, while the output s-a-1 causes the gate to supply a permanent 1 to all its loads. Similar statements can be made about OR gates: one or more inputs s-a-1 cause the OR gate to act as though its output were s-a-1, and OR gate inputs s-a-0 can no longer affect gate operation. An inverter input s-a-0 is equivalent to its output permanently at logical 1 and an inverter output s-a-0 is equivalent to its input permanently at 1.

It is to be noted that under the stuck-at fault model, failures cause fixed signals to appear at leads, ie. signals become *clamped*. Thus tests based on stuck-at fault models deal with *static faults*. Parameters that affect dynamic behavior such as switching speed are verified by other tests.

2.4 Classical and Testability Notions of Redundancy

In switching theory terminology, a circuit is classified as either *Redundant or Irredundant*. The classical definition of redundancy is that a circuit is irredundant if a connection (path) or gate can be cut without altering the output functions. In terms of fault testability, Whitney[2] has classified the circuits as shown below:

1. A path or gate g is *irredundant* if there exists input vectors x_0 and x_1 such that x_0 is a test for g-at-0 and x_1 is a test for g-at-1.
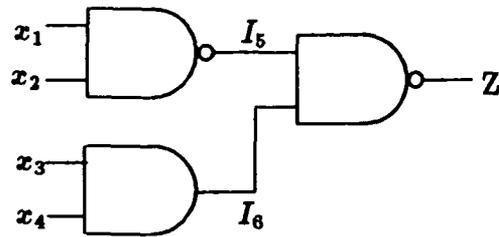
Figure 1: Path I_5 is irredundant
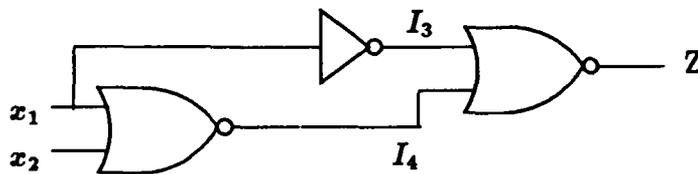
Figure 2: Path I_4 is partially redundant

2. A path or gate is partially redundant iff there exists a test for the fault g-at-0, but there exists no test for the fault g-at-1 , or vice-versa.

3. A path or a gate g is fully redundant iff there exists tests for neither g-at-0 nor g-at-1.

Simple examples for the different classes of the circuits are shown in Figures 1, 2 and 3 respectively. In Figure 1, path I_5 is irredundant, since $< x_1, ..., x_4 >=< 0111 >$ is a test for I_5-at-0 and $< x_1....x_4 >=< 1111 >$ is a test for I_5-at-1. In Figure 2, path I_4 is partially redundant since $< x_1, x_2 >=< 1,1 >$ is a test for I_4-at-1; but there does not exist a test for I_4-at-0. In Figure 3, path x.2 is fully redundant since there does not exist a test for either x.2-at-0 or x.2-at-1. Henceforth x will be called as *fanout origin* and x.1, x.2, x.3 as *fanout branches*.
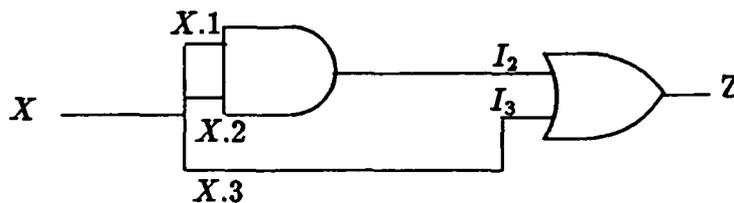
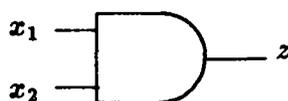Figure 3: Path x.2 is fully redundant

Figure 4: AND Gate

3   Review of Existing Methods

One of the popular methods being used to find a minimal test vector set is the fault table method and the subsequent application of Petrick's method [20]. The fault table could be filled using the path sensitization technique [1] where a given fault is provoked by the test vector and a path is sensitized through the logic to propagate the fault to a primary output. The fault table could also be filled using the Boolean Differences method [12]. This method is an algebraic-type procedure for determining the complete set of tests that detect a given fault. Kohavi [15] developed simple procedure called *a and b tests* but this was restricted to two level AND-OR logic circuits and requires the use of K-maps. Another version of the same technique was given by Bearnson and Caroll [17]. The *enf* method was first demonstrated by Armstrong [1] but this was quite complicated. An improved version of the same was outlined by Fridrich and Davis [5] and S.M.Reddy [4]. However all these methods involve considerable computations and, in addition are time consuming too.

4   Minimal Test set For Irredundant Circuits

In this section, the concept of fault folding is introduced first and then the procedures to derive a set of minimal test vectors is demonstrated. Only irredundant, combinational logic circuits are considered, with the single stuck-at fault assumption.

Fault-Folding is a very powerful technique and was developed by Kilin To [3]. Any two faults x_1-a-α and x_2-a-β where $\alpha, \beta \in \{0,1\}$ are said to be *test equivalent*, (written as x_1-a-$\alpha \leftrightarrow x_2$-a-$\beta$) iff a test for one fault is also a test for the other that is, $t_1(x_1$-a-$\alpha) \in T(x_1$-a-$\alpha)$ implies $t(x_1$-a-$\alpha) \in T(x_2$-a-$\beta)$ and vice-versa, where $\mathrm{T}(x_i$-a-$\gamma)$ is the set of input vectors that can serve as a test for fault x_i-a-γ and $t(x_1$-a-$\alpha)$ is one of the input vectors. Two faults are said to be test implied, (written as x_1-a-$\alpha \rightarrow x_2$-a-β) if the implication is only one way ie. $t(x_1, \alpha) \in T(x_1, \alpha)$ implies $t(x_1, \alpha) \in T(x_2, \beta)$ but there is a $t'(x_2, \beta) \notin T(x_1, \alpha)$.

Consider the AND gate shown in Figure 4. The faults x_1-a-0, x_2-a-0, and z-a-0 are said to be test equivalent where as z-a-0 is test implied by the faults x_1-a-0 and x_2-a-0.

The fault x_1-a-α is said to test cover x_2-a-β (written as x_1-a-$\alpha \leq_t x_2$-a-β) iff x_1-a-α is test equivalent to x_2-a-β(x_1-a-$\beta \leftrightarrow x_2$-a-$\beta$) or x_2-a-β is test implied by x_1-a-α (x_1-a-$\alpha \rightarrow x_2$-a-β). The fault folding operation $<_f$ is defined as

$$F_i <_f F_j = \left\{ \begin{array}{ll} F_i & \text{if } F_i \leq_t F_j \\ \text{undefined} & \text{otherwise} \end{array} \right\}$$

The motivation for folding is that a test for fault F_i also tests the fault F_j; hence it is only necessary to find tests for F_i.

The set of tests T is said to be a complete set of tests iff the presence of all stuck-at faults in the circuit could be detected by exercising the test set T. At this point some of the *classic* Theorems of testability are restated.

Theorem 1 *A set of tests that can detect all single faults at primary inputs of a Non-Reconvergent Fanout (NRFO) combinational circuit is a complete set of detection tests.*

Theorem 2 *A set of tests that can detect all single faults at all primary inputs and fanout branches of a Reconvergent Fanout (RFO) combinational circuit is a complete set of detection tests.*

Lemma 1 *If several faults are equivalent given by $S = \{x_1\text{-}a\text{-}i_1, x_2\text{-}a\text{-}i_2, \ldots, x_n\text{-}a\text{-}i_n\}$ where $i_1, i_2, \ldots, i_n \in \{0,1\}$ then the set of primary input faults F formed by fault folding of an NRFO circuit should contain only one representative(any) from the fault set S.*

Example 1 *For the circuit of Figure 5, find the minimal set of faults by fault-folding.*

First, assume the output f to be s-a-0. A s-a-0 fault on a NAND gate output is test implied by a s-a-1 fault on any of its inputs. Therefore a test for either x_9-a-1 or x_{10}-a-1 is also a test for f-a-0. This is indicated in Figure 6. Using the transitive properties of test cover relations x_9-a-1 is test covered by x_6-a-0 or x_5-a-0. This process is continued till the primary inputs are reached.

The same procedure is also followed for f-a-1 (Figure 7). The graphs formed by the fault-folding are called *fault-folding* graphs. Fault folded classes are formed by tracing different paths of the graphs and applying fault folding. In our example, the fault-folded classes are:

$\{x_5\text{-}a\text{-}0, x_6\text{-}a\text{-}0\} <_t x_9\text{-}a\text{-}1 <_t f\text{-}a\text{-}0 = \{x_5\text{-}a\text{-}0, x_6\text{-}a\text{-}0\}$

$\{x_1\text{-}a\text{-}0, x_2\text{-}a\text{-}0\} <_t x_3\text{-}a\text{-}1 <_t \{x_7\text{-}a\text{-}0, x_8\text{-}a\text{-}0\} <_t x_{10}\text{-}a\text{-}1 <_t f\text{-}a\text{-}0 = \{x_1\text{-}a\text{-}0, x_2\text{-}a\text{-}0\}$

$x_4\text{-}a\text{-}1 <_t \{x_7\text{-}a\text{-}0, x_8\text{-}a\text{-}0\} <_t x_{10}\text{-}a\text{-}1 <_t f\text{-}a\text{-}0 = x_4\text{-}a\text{-}1$

$x_5\text{-}a\text{-}1 <_t \{x_9\text{-}a\text{-}0, x_{10}\text{-}a\text{-}0\} <_t f\text{-}a\text{-}1 = x_5\text{-}a\text{-}1$

$x_6\text{-}a\text{-}1 <_t \{x_9\text{-}a\text{-}0, x_{10}\text{-}a\text{-}0\} <_t f\text{-}a\text{-}1 = x_6\text{-}a\text{-}1$

$x_8\text{-}a\text{-}1 <_t \{x_9\text{-}a\text{-}0, x_{10}\text{-}a\text{-}0\} <_t f\text{-}a\text{-}1 = x_8\text{-}a\text{-}1$

$x_1\text{-}a\text{-}1 <_t \{x_3\text{-}a\text{-}0, x_4\text{-}a\text{-}0\} <_t x_7\text{-}a\text{-}1 <_t \{x_9\text{-}a\text{-}0, x_{10}\text{-}a\text{-}0\} <_t f\text{-}a\text{-}1 = x_1\text{-}a\text{-}1$

$x_2\text{-}a\text{-}1 <_t \{x_3\text{-}a\text{-}0, x_4\text{-}a\text{-}0\} <_t x_7\text{-}a\text{-}1 <_t \{x_9\text{-}a\text{-}0, x_{10}\text{-}a\text{-}0\} <_t f\text{-}a\text{-}1 = x_2\text{-}a\text{-}1$

The minimum set of faults sufficient to derive a set of tests that completely detect all possible faults in the circuits is F=$\{x_5$-a-0, x_1-a-0, x_4-a-1, x_5-a-1, x_6-a-1, x_8-a-1, x_1-a-1, x_2-a-1 $\}$. It is to be noted that only one fault has been chosen from the each of the equivalence classes $\{x_1$-a-0, x_2-a-0$\}$ and $\{x_5$-a-0, x_6-a-0$\}$ as per Lemma 1. The faults x_2-a-0 and x_6-a-0 can also be chosen instead of x_1-a-0 and x_5-a-0 respectively.

It is to be observed that the fault-folding graphs for f-a-0 and f-a-1 are always duals (except for buffers and inverters). In other words, a test implication between two nodes

in one fault folding graph becomes test equivalence in the other and vice-versa. Hence for information representation only one graph is necessary, the other graph can be drawn without any further calculation.

Fault Folding results in a minimal set of faults but it does not yield a minimal test set. In fact To[3] himself states "Note that although the minimal set of faults (F) is sufficient to derive the complete set of detection tests (CSDT's); the number of tests in the CSDT is equal to or smaller than the number of faults in the minimal set F".

4.1   Minimal Test Set for Non-Reconvergent Fanout Circuits

4.1.1   Fault Folding Method

Consider an equivalence class $\{x_1\text{-a-}i_1, x_2\text{-a-}i_2, \ldots, x_n\text{-a-}i_n\}$ where $x_1, x_2, \ldots, x_n$ are the circuit nodes (input or internal) and $\{i_1, i_2, i_3, \ldots, i_n\} \in \{0,1\}$. Then three different cases could exist:-

1. All the nodes $\{x_1, \ldots, x_n\}$ are primary input nodes.

2. Some of the nodes are internal nodes and the rest are primary input nodes.

3. All the nodes $\{x_1, \ldots, x_n\}$ are internal nodes.

Case-1:-
If all the nodes of the Equivalence class $\{x_1, \ldots, x_n\}$ are primary input nodes.
To [3] has proven that it is enough to consider one member from the equivalence class to determine the minimal set of faults and hence the minimal test set.
Case-2:-
Some of the nodes of the equivalence class $\{x_1, x_2, x_3, \ldots, x_n\}$ are primary input nodes.

Theorem 3 *The primary input faults could be neglected (for the purposes of finding minimal test set) in an equivalence class containing primary inputs and internal nodes.*

Proof:-
This theorem follows from the definition of the equivalent fault class. By definition, it is enough to test one member of the equivalent fault class to test the whole fault class. By the Theorem's initial assumption, there exists at least one non-primary node in the equivalence class. Since all non-primary nodes of the equivalent fault class are being tested, it follows that the entire fault class is tested. Hence it is enough to consider only the internal nodes of the equivalence class.
Case-3:-*All the nodes of the equivalent fault class $\{x_1\text{-a-}i_1, x_2\text{-a-}i_2, \ldots, x_n\text{-a-}i_n\}$ are internal nodes.*

Theorem 4 *If m_1 primary input node faults test cover an internal node fault $x_1\text{-a-}i_1$,*
m_2 primary input node faults test cover an internal node fault $x_2\text{-a-}i_2$,
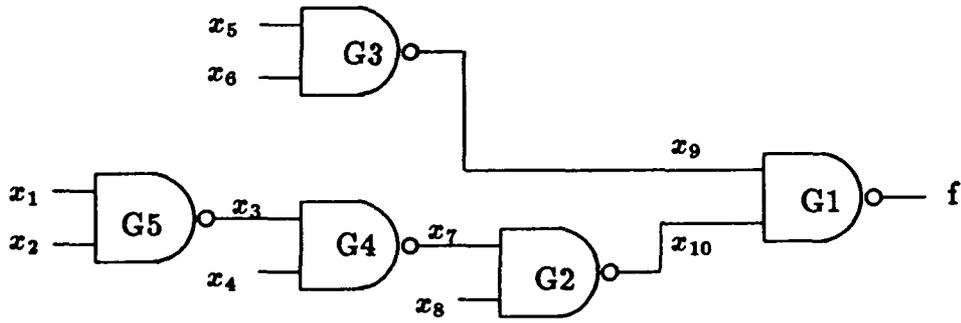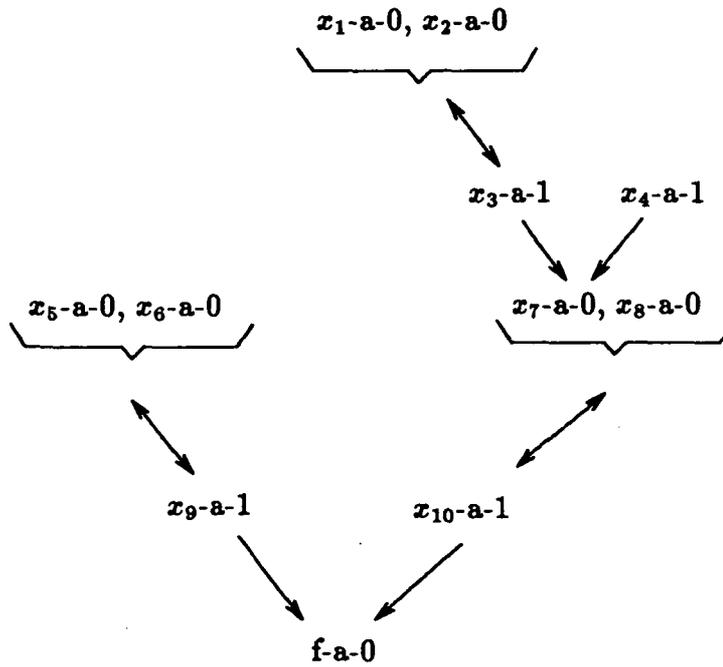
$\vdots$

Figure 5: A fanout free circuit

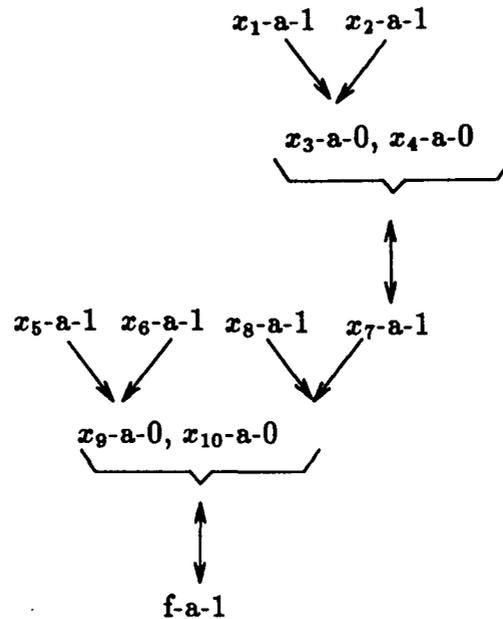Figure 6: Fault folding graph for f-a-0

Figure 7: Fault folding graph for f-a-1

and m_n primary input node faults test cover an internal node fault x_n-a-i_n, and if $\{x_1$-a-i_1, x_2-a-$i_2, \ldots, x_n$-a-$i_n\}$ form an equivalent fault class, then a test vector can be found which would test, any one of the m_1, any one of the $m_2, \ldots$, any one of the m_n faults, simultaneously.

Proof:-
Consider the equivalence fault class $\{x_1$-a-i_1, x_2-a-$i_2, \ldots, x_n$-a-$i_n\}$. Let x_1-a-i_1 be test covered by the primary input faults $\{y_{11}$-a-p_{11}, y_{12}-a-$p_{12}, \ldots, y_{1m}$-a-$p_{1m}\}$ and x_2-a-i_2 be test covered by the primary input faults $\{y_{21}$-a-p_{21}, y_{22}-a-$p_{22}, \ldots, y_{2m}$-a-$p_{2m}\}$.
Let T_1 be the set of test vectors which tests the fault set $\{y_{11}$-a-p_{11}, y_{12}-a-$p_{12}, \ldots, y_{1m}$-a-$p_{1m}\}$ and let T_2 test the fault set $\{y_{21}$-a-p_{21}, y_{22}-a-$p_{22}, \ldots, y_{2m}$-a-$p_{2m}\}$. By the definition of test cover, T_1 and T_2 also test the faults x_1-a-i_1 and x_2-a-i_2. Since x_1-a-i_1 and x_2-a-i_2 are in the same equivalent fault class, $T_1 = T_2$. This means that any test vector $t_1 \in T_1$ will test one member of the fault class $F_1 = \{y_{11}$-a-p_{11}, y_{12}-a-$p_{12}, \ldots, y_{1m}$-a-$p_{1m},\}$, and one member of $F_2 = \{y_{21}$-a-p_{21}, y_{22}-a-$p_{22}, \ldots, y_{2m}$-a-$p_{2m}\}$ simultaneously.

For NRFO circuits, it so happens that a member of the fault class F_1 could be tested with any one member of F_2 simultaneously.

Corollary 1 *For the case described in Theorem 4, only m_p faults need to be tested where $m_p \in \{m_1, m_2, \ldots, m_n\}$ such that $m_p > m_j|_{j \neq p}$ and $m_j \in \{m_1, m_2, \ldots, m_n\}$*

Example 2 *Find the minimal Test set for the circuit shown in Figure 5.*

The fault folding graphs of the Figures 6, 7 are first constructed.
By To's method[3] the minimal fault set is found to be,

$$\left\{ \begin{pmatrix} x_5\text{-a-0} \\ x_6\text{-a-0} \end{pmatrix}, \begin{pmatrix} x_1\text{-a-0} \\ x_2\text{-a-0} \end{pmatrix}, x_4\text{-a-1}, x_8\text{-a-0}, x_5\text{-a-1}, x_6\text{-a-1}, x_8\text{-a-1}, x_1\text{-a-1}, x_2\text{-a-1}, x_4\text{-a-0} \right\}$$

By Theorem 3, the faults x_4-a-0 and x_8-a-0 can be neglected, since these faults will be tested by any test for the faults x_3-a-0 and x_7-a-0 respectively. Applying Theorem 4, one finds that the fault x_5-a-1 can be *conjoined* with either x_8-a-1 or x_1-a-1 or x_2-a-1; and x_6-a-1 can be *conjoined* with x_8-a-1 or x_1-a-1 or x_2-a-1. If x_5-a-1 and x_8-a-1 are conjoined as are x_6-a-1 and x_1-a-1, the following multiple fault set is obtained;

$$F_{m1} = \left\{ \begin{pmatrix} x_5\text{-a-0} \\ x_6\text{-a-0} \end{pmatrix} \begin{pmatrix} x_1\text{-a-0} \\ x_2\text{-a-0} \\ x_8\text{-a-0} \end{pmatrix} \begin{pmatrix} x_4\text{-a-1} \\ x_8\text{-a-0} \end{pmatrix} \begin{pmatrix} x_5\text{-a-1} \\ x_8\text{-a-1} \end{pmatrix} \begin{pmatrix} x_6\text{-a-1} \\ x_1\text{-a-1} \\ x_4\text{-a-0} \end{pmatrix} \right.$$

$$\left. \begin{pmatrix} x_2\text{-a-1} & x_2\text{-a-1} \\ x_4\text{-a-0} & or & x_4\text{-a-0} \\ x_5\text{-a-1} & x_6\text{-a-1} \end{pmatrix} \right\}.$$

Definition 1 *Multiple fault set is a set whose members include multiple faults.*

As an example, the fault set F_{m1} obtained in Example 2 is a multiple fault set whose members are all multiple faults.

Since there are three choices each for conjoining or overlapping the faults x_5-a-1 and x_6-a-1 with other faults, we could obtain different multiple fault sets of the same length which test cover all the single faults. The fault set enclosed by the parenthesis {....} represents the multiple fault set, whose members are multiple faults. Each multiple fault is enclosed by the parenthesis (....). The next step is to find the tests for each of the multiple faults. Each multiple fault might have more than one test vector. In such cases, all the possible test vectors testing a single multiple fault are enclosed within the parenthesis (...) with the agreement that only one test vector is to be chosen among them. The minimal test set for F_{m1} is given by:-
$T_{m1} = < x_1 x_2 x_4 x_5 x_6 x_8 > =$

$$\left\{ \begin{pmatrix} ---110 \\ -01111 \\ 0-1111 \end{pmatrix} \begin{pmatrix} 1110-1 \\ 111-01 \end{pmatrix} \begin{pmatrix} 0-00-1 \\ -00-01 \end{pmatrix} \begin{pmatrix} --0010 \\ 111010 \end{pmatrix} \begin{pmatrix} 011101 \end{pmatrix} \begin{pmatrix} 101011 \\ 101101 \end{pmatrix} \right\}$$

It is again reiterated that only one test from each of the test vector sets enclosed within the parenthesis (...) is to be chosen to form a minimal test set. In the above example, the length of the minimal test set is found to be six.

4.1.2   Method by Inspection

It is *ultimately* desirable that the minimal length multiple fault set covering all single faults be found, by direct inspection of the network, without even drawing the fault folding

graphs. From our observations, by working out a plethora of examples certain conjectures are made (to follow) which eases one's task.

Consider a NRFO circuit with m different paths. This implies that there are m primary gates. A primary gate is a gate whose inputs are all primary inputs. Each gate is assigned a level (in an obvious manner) starting with with level 2 at the output and working backwards. Then,

Theorem 5 *It is only necessary to find s-a-1(0) tests on all primary inputs of the non-primary gates and both s-a-0 and s-a-1 tests on all the input leads of the primary gates in an NRFO NAND-NAND(NOR-NOR) circuit.*

Proof:-
The primary gates may be at odd or even levels. It has been proven [12] for a NAND-NAND circuit that a s-a-0 on an input of an odd(even) primary gate will also be a s-a-0 test for the leads of all the odd(even) gates in that path to the output. Also, a s-a-1 test on an input of an odd(even) primary gate will also be a s-a-0 test for the leads of all the even(odd) gates in that path to the output. Hence if the primary gates(odd or even) are tested for both s-a-0 and s-a-1 faults, all the gates in the path from that primary gate to the output will be tested for s-a-0 faults.

So if all the primary gates are tested for both s-a-0 and s-a-1 faults, all possible s-a-0 faults in the circuit will be checked. It is only needed to test the s-a-1 faults on the remaining primary inputs to ensure that all the primary inputs are checked for both s-a-0 and s-a-1 faults. To[3] has stated that only the primary inputs in an NRFO circuit has to be tested for s-a-0 and s-a-1 faults to completely test the circuit. Since this objective has been accomplished, the entire circuit will have been tested completely. Hence the theorem is verified.

At this point, a conjecture is made to help find directly the multiple fault set which yields the minimal test vectors.
Conjecture 1 *In an NRFO NAND-NAND circuit, the s-a-1(0) fault on a primary input of an even(odd) level gate in a path P_i could be conjoined with one of the following faults in each path $P_j|_{j \neq i}$.*

1. *s-a-1 fault on a primary input of an even level gate.*

2. *s-a-0 fault on a primary input of an odd level gate.*

Example 3 .

Consider the circuit in Figure 5. According to Theorem 5, one needs to consider only the primary gate faults $\{x_1$-a-0, x_1-a-1, x_2-a-1, x_5-a-0, x_6-a-1, x_5-a-1$\}$ and the primary input faults $\{ x_4$-a-1, x_8-a-1$\}$. Gates G_3, G_2, G_5 are even level gates where as G_4 and G_1 are odd level gates. So by Conjecture 1, each member of the fault set $\{x_5$-a-1, x_6-a-1$\}$ (even level gate) can be conjoined with either one of the following faults:-

1. x_1-a-1 or x_2-a-1 (even gate)

2. x_4-a-0 (odd gate)

3. x_8-a-1 (even gate)

The test for x_4-a-0 is not needed as per Theorem 5. If we conjoin x_5-a-1 with x_1-a-1 and x_6-a-1 with x_8-a-1, the following reduced fault set is obtained

$$F = \left\{ x_1\text{-a-0}, x_2\text{-a-1}, x_4\text{-a-1}, x_5\text{-a-0}, \begin{bmatrix} x_1\text{-a-1} \\ x_5\text{-a-1} \end{bmatrix} \begin{bmatrix} x_6\text{-a-1} \\ x_8\text{-a-1} \end{bmatrix} \right\}$$

where $\{x_1$-a-1, x_5-a-1$\}$ and $\{x_6$-a-1, x_8-a-1$\}$ are multiple faults. This fault set could have been obtained by a different choice of conjoining test vectors in Example 2. Obtaining test vectors for this fault set yields a minimal length test vector set. Similar Theorems and Conjectures can be derived for NOR-NOR circuits.

4.2   Minimal Test Set for Internal Reconvergent Fanout Circuits

4.2.1   Fault Folding Method

To[3] has stated and proven the following theorem.

Theorem 6 *Any set of tests which checks all the faults at the primary inputs and fanout branches of a RFO irredundant circuit is sufficient to check the entire circuit.*

To [3] implies that one has to test all the fanout branches in addition to primary inputs. But the faults in the fanout branches can always be folded back to faults on the primary inputs. So for the purpose of finding a minimal set of test vectors,the primary input fault and the fault on the fanout branch which it test covers, are conjoined to form a multiple fault, so that a single test will test both these essential faults. The primary input fault, covering the fault on the fanout branch, is found using the fault folding graphs.

Consider the circuit shown in Figure 8. There are two fanout branches: $I_{5.1}$ and $I_{5.2}$. According to the Theorem 6, the s-a-0 and s-a-1 faults on $I_{5.1}$ and $I_{5.2}$ are essential faults. The tests for s-a-1 faults on x_2 and x_3 propagated through the lines $I_{5.1}$ and $I_{5.2}$ respectively will test cover the s-a-0 faults on the lines $I_{5.1}$ and $I_{5.2}$.

Theorems 3, 4, 5 developed for NRFO circuits can also be used here. But one has to be more careful when dealing with reconvergent fanout circuits. There are three *golden* rules which if followed, might make one's task less arduous.

Rule-1:-*Be sure that the multiple fault set obtained using Theorems 3 and 4 contain the s-a-0 and s-a-1 faults on all the fanout branches.*

Illustration:- Consider the fault folding graphs in the Figures 9 and 10 for the circuit in the Figure 8. If the faults on the fanout branches are not treated as essential faults, then using Theorems 3 and 4 one might get a multiple fault set

$$F_m = \left\{ \begin{bmatrix} x_2\text{-a-1} \\ x_4\text{-a-1} \end{bmatrix}, \begin{bmatrix} x_3\text{-a-1} \\ x_4\text{-a-1} \end{bmatrix}, \begin{bmatrix} x_2\text{-a-1} \\ x_1\text{-a-0} \end{bmatrix}, \begin{bmatrix} x_3\text{-a-1} \\ x_1\text{-a-0} \end{bmatrix}, \begin{bmatrix} x_1\text{-a-1} \\ x_4\text{-a-0} \end{bmatrix}, \begin{bmatrix} x_2\text{-a-0} \\ x_3\text{-a-0} \end{bmatrix} . \right\}$$

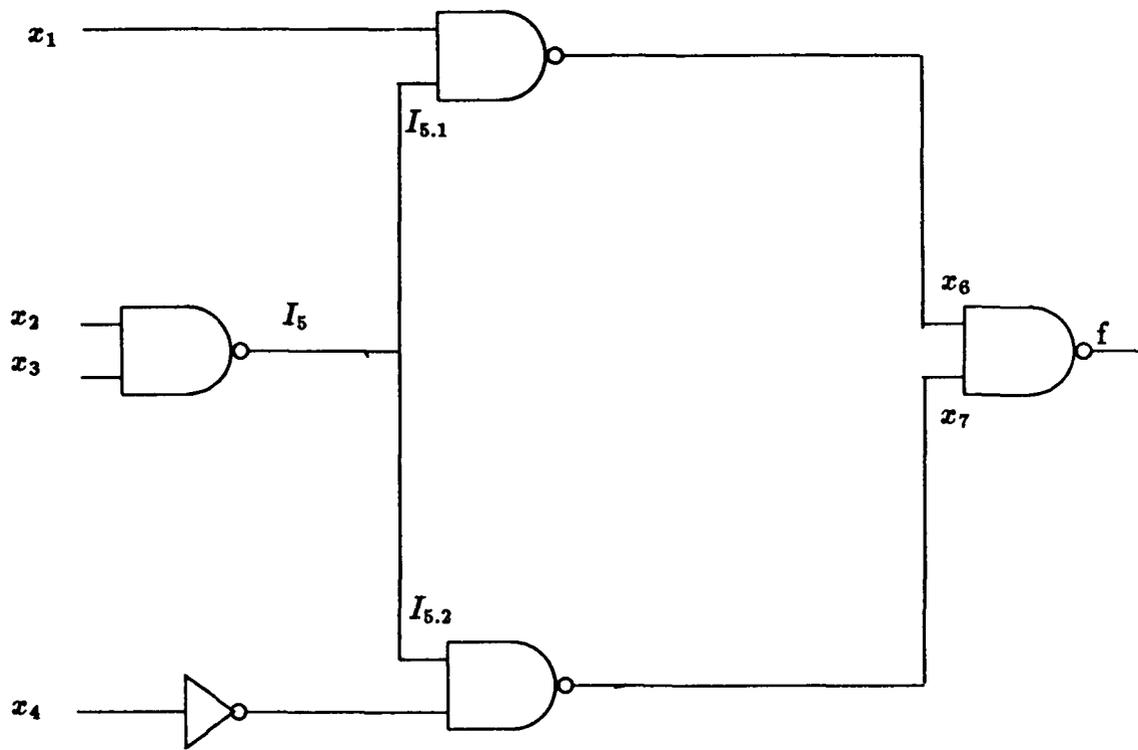From Figure 9, it is found that the equivalence fault class $\{x_2$-a-0, x_3-a-0 $\}$ test covers
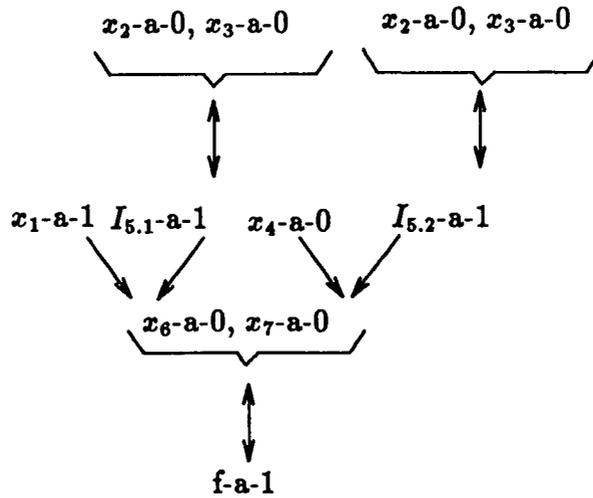
Figure 8: An Internal Reconvergent fanout circuit .

Figure 9: Fault folding graph for f-a-1

x_2-a-1 x_3-a-1 x_2-a-1 x_3-a-1

x_1-a-0, $I_{5.1}$-a-0 x_4-a-1, $I_{5.2}$-a-0
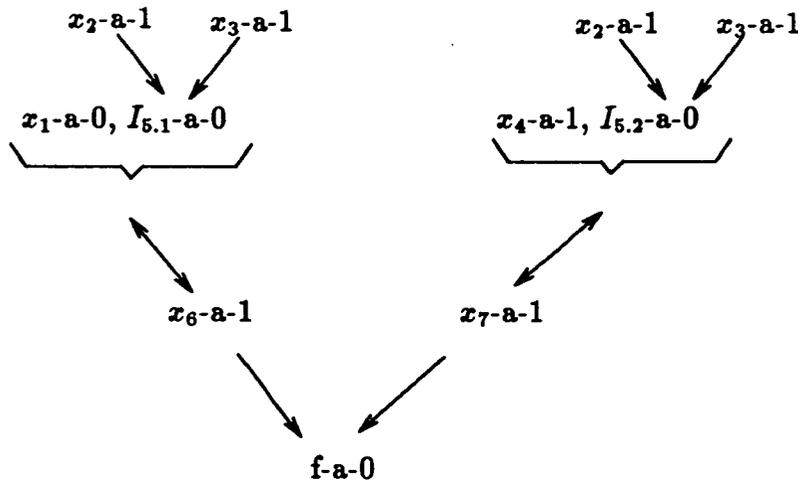
x_6-a-1 x_7-a-1

f-a-0

Figure 10: Fault folding graph for f-a-0

both $I_{5.1}$-a-1 and $I_{5.2}$-a-1. Using Theorems 3 and 4, which say only primary input faults can be conjoined and hence tested, the faults x_1-a-1 and x_4-a-0 have been conjoined as are $\{x_2$-a-0, x_3-a-0$\}$ and $\{x_2$-a-0, x_3-a-0$\}$ to get the multiple faults $\{x_1$-a-1, x_4-a-0$\}$ and $\{x_2$-a-0, x_3-a-0$\}$ respectively.

The first and second, third and fourth multiple faults in set F_m will test cover the faults $I_{5.1}$ and $I_{5.2}$ stuck-at-0 respectively. There are three choices of test vectors to test the last multiple fault in F_m which is $\{x_2$-a-0, x_3-a-0$\}$. The test vectors are $< x_1 x_2 x_3 x_4 > = \{0110,$ 1111, 1110$\}$. The test vector $< x_1 x_2 x_3 x_4 > = 0110$ propagates the multiple fault $\{x_2$-a-0, x_3-a-0$\}$ through the path $I_{5.2}$ and in the process also tests the fault $I_{5.2}$-a-1. Similarly the test vector $< x_1...x_4 > = 1111$ propagates the multiple fault $\{x_2$-a-0, x_3-a-0$\}$ through $I_{5.1}$ and also happens to test $I_{5.1}$-a-1. But the test vector $< x_1 x_2 x_3 x_4 > = 1110$, not only test the multiple fault $\{x_2$-a-0, x_3-a-0$\}$ but also the faults $I_{5.1}$-a-1 and $I_{5.2}$-a-1. According to Theorem 6, the s-a-0 and s-a-1 faults on the fanout branches have to be tested as they are essential faults. So if one chooses $< x_1 x_2 x_3 x_4 > = \{0110$ or 1111$\}$ as the test vector to test the multiple fault $\{x_2$-a-0, x_3-a-0$\}$, the s-a-1 faults on only one of the fanout branches instead of both the fanout branches will be tested. Since all the essential faults according the Theorem 6 are not covered by the test set, this test set is incomplete. Hence the test vector $< x_1 x_2 x_3 x_4 > = 1110$ is to be chosen to test the multiple fault $\{x_2$-a-0, x_3-a-0$\}$ in order to get a valid minimal complete test set.

In order to avoid the problem of a potential incomplete test set, the faults on the fanout branches must be included in addition to the primary input faults which test cover them (faults on fanout branches), while specifying the multiple fault in the minimal multiple fault set.

Therefore in the current example, applying Theorems 3 and 4, the faults on the fanout branches are also specified in the multiple fault. From Figure 9, the multiple fault $\{x_2$-a-0, x_3-a-0, $I_{5.1}$-a-1$\}$ is conjoined with the multiple fault $\{x_2$-a-0, x_3-a-0, $I_{5.2}$-a-1$\}$ to form the

multiple fault $\{x_2\text{-a-}0, x_3\text{-a-}0, I_{5.1}\text{-a-}1, I_{5.2}\text{-a-}1\}$. So the minimal multiple fault set F_m is now modified as

$$F_m = \left\{ \begin{bmatrix} x_2\text{-a-}1 \\ x_4\text{-a-}1 \end{bmatrix}, \begin{bmatrix} x_3\text{-a-}1 \\ x_4\text{-a-}1 \end{bmatrix}, \begin{bmatrix} x_2\text{-a-}1 \\ x_1\text{-a-}0 \end{bmatrix}, \begin{bmatrix} x_3\text{-a-}1 \\ x_1\text{-a-}0 \end{bmatrix}, \begin{bmatrix} x_1\text{-a-}1 \\ x_4\text{-a-}0 \end{bmatrix}, \begin{bmatrix} x_2\text{-a-}0 \\ x_3\text{-a-}0 \\ I_{5.1}\text{-a-}1 \\ I_{5.2}\text{-a-}1 \end{bmatrix} \right\}.$$

The test vector $< x_1 x_2 x_3 x_4 > = 1110$ is the only test for the multiple fault $\{x_2\text{-a-}0, x_3\text{-a-}0, I_{5.1}\text{-a-}1, I_{5.2}\text{-a-}1\}$ which agrees with the earlier finding that only the vector 1110 is to be chosen to form a complete test set.

There is still some redundancy in F_m, that is F_m is still not a truly minimal multiple fault set. The method of removing this redundancy will be explained further on.

Definition 2 *Faults are said to be contradictory if they cannot be tested simultaneously.*

The faults $x_j\text{-a-}i$ and $x_j\text{-a-}\bar{i}$ are complementary faults as they can never be tested simultaneously. Also for any gate (NAND or NOR except XOR) checking one of the inputs for a s-a-0 fault and the other(s) input(s) for s-a-1 fault is impossible. Additionally testing one input for s-a-1(0) fault and the other input(s) of the same gate for s-a-1(0) fault in the case of NAND (NOR) gate is impossible. Hence such faults are said to be contradictory faults.

Rule-2:- *Do not conjoin contradictory faults while using Theorem 4.*

Theorem 4 says that two or more primary input faults can be conjoined if they test cover faults which are in the same equivalence class. This might not always be true in the case of RFO circuits. Hence the theorem is modified as follows:-

Theorem 7 *If m_1 primary input node faults test cover an internal node fault $x_1\text{-}a\text{-}i_1$, m_2 primary input node faults test cover an internal node fault $x_2\text{-}a\text{-}i_2$,*

$\vdots$

and m_n primary input node faults test cover an internal node fault $x_n\text{-}a\text{-}i_n$, and if $\{x_1\text{-}a\text{-}i_1, x_2\text{-}a\text{-}i_2, \ldots, x_n\text{-}a\text{-}i_n\}$ form an equivalent fault class; then a test vector can be found which would test any one of the m_1, any one of the m_2, ..., any one of the m_n faults simultaneously, "provided that these faults are not contradictory".

One comes across such instances of contradictory faults when dealing with RFO circuits, especially where the inversion parity along the reconverging paths is not the same. The inversion parity of a reconverging path is defined to be the number of inversions, modulo 2, along the path between the specified fanout node and the node of reconvergence.

Illustration 2:- Consider the circuit in Figure 8. There is no difference in the Inversion parities along the reconverging paths $I_{5.1}$ and $I_{5.2}$. In the fault folding graph of Figure 9, the multiple fault $\{x_2\text{-a-}0, x_3\text{-a-}0, I_{5.1}\text{-a-}1\}$ and the fault $x_4\text{-a-}0$ cannot be conjoined together though they imply the faults $x_6\text{-a-}0, x_7\text{-a-}0$ which are in the same equivalence class. This is because the provoking conditions for the faults $I_{5.1}\text{-a-}1$ and $I_{5.2}\text{-a-}1$ are the same. It has already been noted before, that for a NAND gate testing both inputs for s-a-1
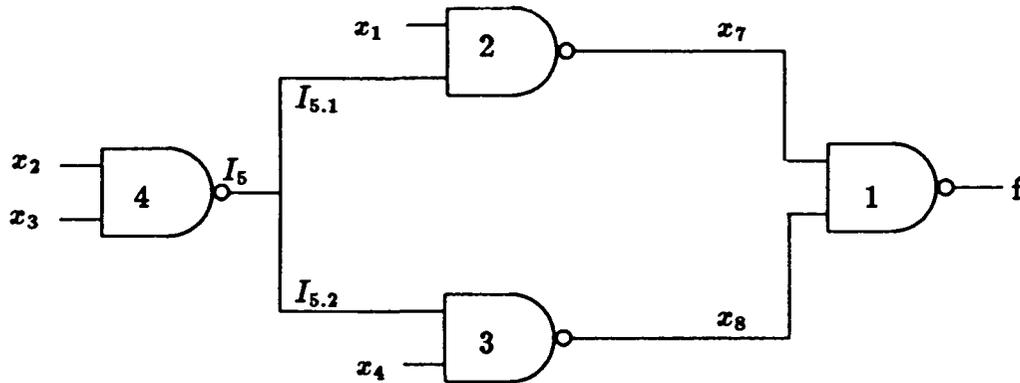
Figure 11: An internal RFO circuit

faults simultaneously is impossible. In the present case, the fault x_4-a-0 if combined with $\{x_2$-a-0, x_3-a-0, $I_{5.1}$-a-1$\}$ will imply that both the faults x_4-a-0 and $I_{5.2}$-a-1 will be tested (provoking conditions of $I_{5.1}, I_{5.2}$ are the same) which is not possible as both $I_{5.2}$ and x_4 are inputs of the same NAND gate and hence are contradictory faults. So the only way to conjoin faults from the fault folding graph for f-a-1 is,

$$\left\{ \begin{bmatrix} x_2\text{-a-0} \\ x_3\text{-a-0} \\ I_{5.1}\text{-a-1} \\ I_{5.2}\text{-a-1} \end{bmatrix} \begin{bmatrix} x_1\text{-a-1} \\ x_4\text{-a-0} \end{bmatrix} \right\}.$$

Rule-3:- *Try not to cover the same fault twice.*

If one is not careful, redundant tests will be incorporated in the minimal test vector set. This usually happens in RFO circuits where the same fault on the primary input might occur more than once in the fault folding graphs.

Conjecture 2 *If two primary input faults x_a-a-i_1 and x_b-a-i_2, implying a fault on the same internal node, appears more than once in the fault folding graphs; then it is enough to consider the fault x_a-a-i_1 in one of the appearances and x_b-a-i_2 in the other appearance.*

Using this conjecture for the circuit in the Figure 8, we find that the implying primary input fault class x_2-a-0 and x_3-a-0 appear twice in the fault folding graph f-a-0. So in the first appearance (implying $I_{5.1}$-a-0) consider x_2-a-0 and neglect x_3-a-0. In the second appearance (implying $I_{5.2}$-a-0) consider x_3-a-0 and neglect x_2-a-0, while forming the multiple fault sets.

The faults x_3-a-0 and x_2-a-0 could also have been chosen (neglecting x_2-a-0 and x_3-a-0) in the first and second appearances of the implying class respectively. This would also have resulted in a different minimal multiple fault set albeit of the same length.

Example 4 *For the circuit in Figure 11, find the minimal test vector set.*

Step 1:- The fault folding graph f-a-0 or f-a-1 is first drawn and then its dual is constructed.

x_2-a-0, x_3-a-0 $\quad$ x_2-a-0, x_3-a-0

I_5-a-1 $\qquad\qquad$ I_5-a-1

x_1-a-1 $\;$ $I_{5.1}$-a-1 $\quad$ x_4-a-1 $\;$ $I_{5.2}$-a-1

x_7-a-0, x_8-a-0

f-a-1
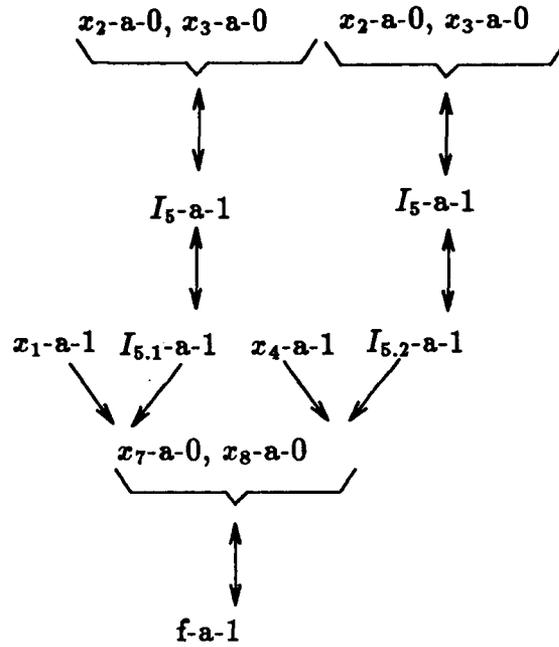
Figure 12: Fault folding graph for f-a-1

x_2-a-1 $\quad$ x_3-a-1 $\qquad\qquad$ x_2-a-1 $\quad$ x_3-a-1

x_1-a-0, $I_{5.1}$-a-0 $\qquad\qquad$ x_4-a-0, $I_{5.2}$-a-0
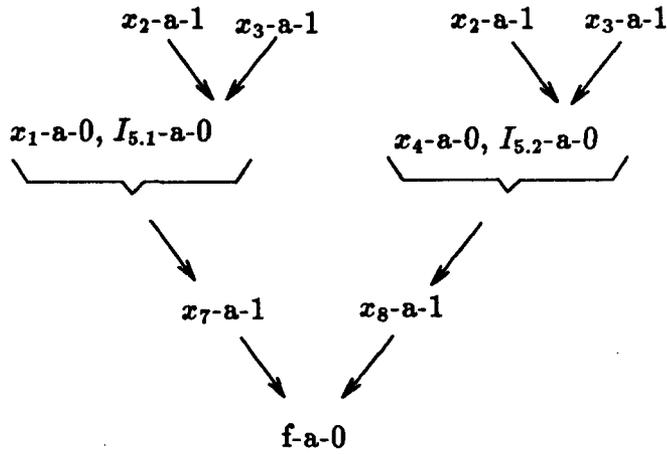
x_7-a-1 $\qquad$ x_8-a-1

f-a-0

Figure 13: Fault folding graph for f-a-0

Step 2:- In the fault folding graph of f-a-1 (Figure 12), the stuck-at fault x_1-a-1 is conjoined with x_4-a-1 using Theorem 7. If x_1-a-1 and $\{x_2$-a-0, x_3-a-0, $I_{5.2}$-a-1$\}$ are conjoined it effectively means that the faults x_1-a-1 and $I_{5.1}$-a-1 are being tested simultaneously because the provoking conditions of the faults $I_{5.1}$-a-1 and $I_{5.2}$-a-1 are the same. Since, both x_1 and $I_{5.1}$ are the inputs of the same NAND gate (gate 2) the faults x_1-a-1 and $\{x_2$-a-0, x_3-a-0, $I_{5.2}$-a-1$\}$ are contradictory faults.

Applying Theorem 7 to the Figure 12, the faults $\{x_2$-a-0, x_3-a-0, $I_{5.1}$-a-1$\}$ and $\{x_2$-a-0, x_3-a-0, $I_{5.2}$-a-1$\}$ are conjoined to form the multiple fault $\{x_2$-a-0, x_3-a-0, $I_{5.1}$-a-1, $I_{5.2}$-a-1 $\}$. Note that though $\{x_2$-a-0, x_3-a-0$\}$ occurs twice, they test cover two different faults namely $I_{5.1}$-a-1 and $I_{5.2}$-a-1. So the test vectors are obviously different. The test vector for the multiple fault $\{x_2$-a-0, x_3-a-0, $I_{5.1}$-a-1$\}$ is given by the $< x_1, x_2, x_3, x_4 > = < 1111 >$, where as the test vector for the multiple fault $\{x_2$-a-0, x_3-a-0, $I_{5.2}$-a-1$\}$ is given by the $< x_1, x_2, x_3, x_4 > = < 0110 >$. The test vector for the multiple faults $\{x_2$-a-0, x_3-a-0, $I_{5.1}$-a-1, $I_{5.2}$-a-1$\}$ is 1110.

From the fault folding graph of f-a-0 (Figure 13), it is observed that two faults x_2-a-1 and x_3-a-1 implying the same fault I_5-a-0 appear twice. Using Conjecture 2, one has the choice of multiple faults as

$$\left\{ \begin{bmatrix} x_2\text{-a-1} \\ x_1\text{-a-0} \\ I_{5.1}\text{-a-0} \end{bmatrix} \begin{bmatrix} x_3\text{-a-1} \\ x_4\text{-a-0} \\ I_{5.2}\text{-a-0} \end{bmatrix} \right\}$$

or

$$\left\{ \begin{bmatrix} x_3\text{-a-1} \\ x_1\text{-a-0} \\ I_{5.1}\text{-a-0} \end{bmatrix} \begin{bmatrix} x_2\text{-a-1} \\ x_4\text{-a-0} \\ I_{5.2}\text{-a-0} \end{bmatrix} \right\}$$

So concatenating the multiple faults from both the fault folding graphs, the minimal length multiple fault set is obtained as

$$F_{m1} = \left\{ \begin{bmatrix} x_4\text{-a-1} \\ x_1\text{-a-1} \end{bmatrix} \begin{bmatrix} x_2\text{-a-0} \\ x_3\text{-a-0} \\ I_{5.1}\text{-a-1} \\ I_{5.2}\text{-a-1} \end{bmatrix} \begin{bmatrix} x_2\text{-a-1} \\ x_1\text{-a-0} \\ I_{5.1}\text{-a-0} \end{bmatrix} \begin{bmatrix} x_4\text{-a-0} \\ x_3\text{-a-1} \\ I_{5.2}\text{-a-0} \end{bmatrix} \right\}$$

The other minimal length multiple fault set is

$$F_{m2} = \left\{ \begin{bmatrix} x_4\text{-a-1} \\ x_1\text{-a-1} \end{bmatrix} \begin{bmatrix} x_2\text{-a-0} \\ x_3\text{-a-0} \\ I_{5.1}\text{-a-1} \\ I_{5.2}\text{-a-1} \end{bmatrix} \begin{bmatrix} x_3\text{-a-1} \\ x_1\text{-a-0} \\ I_{5.1}\text{-a-0} \end{bmatrix} \begin{bmatrix} x_4\text{-a-0} \\ x_2\text{-a-1} \\ I_{5.2}\text{-a-0} \end{bmatrix} \right\}$$

It is to be noted that the fault sets F_{m1} and F_{m2} obey Rule 1, as both s-a-0 and s-a-1 faults on all primary inputs and fanout branches are covered by the multiple faults. Rule 2 is also obeyed by ensuring that contradictory faults are not conjoined together. Rule 3 is also obeyed since we have used Conjecture 2 to form the multiple faults.

Step 3:- The set of test vectors T_{m1} and T_{m2} are found for the multiple fault sets F_{m1} and F_{m2} respectively by path sensitization.

$T_{m1} = \, < x_1, x_2, x_3, x_4 > \, = \{$ [00-0 or 0-00], [1111],[1010],[0101]$\}$
$T_{m2} = \, < x_1, x_2, x_3, x_4 > \, = \{$ [00-0 or 0-00],[1111], [1100],[0011]$\}$
Either of the test vector sets T_{m1} and T_{m2} could be used to test the circuit in a truly minimal fashion. It is to be borne in mind that only one test vector is to be selected from the vectors enclosed by the square parenthesis—[], since they represent the different choices of test vectors for the same multiple fault.

4.2.2   Minimal Test vector set for IRFO circuits by Inspection

The Conjecture 1 developed for NRFO circuits could be used here with a small modification. The earlier conjecture was applicable only for primary inputs. In IRFO circuits, the faults on the fanout branches are also essential faults. So the Conjecture 1 is modified to include both primary inputs and fanout branches in the case of IRFO circuits. In addition, the following conjectures are to be used when dealing with IRFO circuits.

Conjecture 3 *For internal RFO paths in a NAND-NAND circuits with the same parities of inversion,*

1. *The s-a-1(0) faults on the fanout branches must be conjoined together if the gates, to which the fanout branches feed, are even(odd).*

2. *The s-a-i faults on the fanout branches can be conjoined with s-a-$\bar{i}$ faults on the inputs of the gate whose output fans out.*

Conjecture 4 *For internal RFO paths in a NAND-NAND circuits with different parities of inversion,*

1. *The stuck-at faults on the fanout branches must not be conjoined together.*

2. *The s-a-i faults on the fanout branches can be conjoined with s-a-$\bar{i}$ faults on the inputs of the gate whose output fans out.*

Conjecture 5 *The Clause 1 of Conjectures 3 and 4 could also be restated as follows:-*
For NAND-NAND IRFO circuits, the s-a-1(0) faults on the fanout origin is propagated simultaneously through all the fanout paths with even(odd) parities of inversion, if the reconvergent paths have the same parities of inversion.
For NAND-NAND IRFO circuits, the s-a-i (i=1 or 0) faults on the fanout origin should not be propagated simultaneously through the fanout paths which have the different parities of inversion.
Using the above conjectures, the Example 4 will be reworked by inspection.

Example 5 *Find a minimal set of test vectors for the circuit in Figure 11 by Inspection.*

Gates 1 and 4 are odd level gates and gates 2 and 3 are even level gates. It is known that the s-a-0 and s-a-1 faults on all the inputs of the primary gates and s-a-1 faults on the primary inputs of other gates only need to be checked. Since the circuit in question is a RFO circuit, the faults on the fanout branches are also to be checked. From the
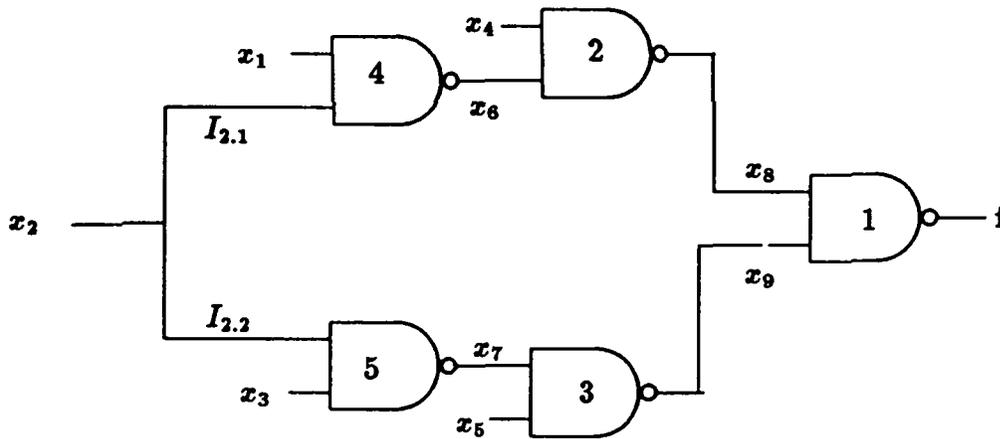
Figure 14: A Primary input fanout Circuit

circuit in the Figure 11, it is observed that the inversion parities along the reconvergent fanout paths are the same. So using Conjecture 3, the s-a-1 fault on line $I_{5.1}$ (Gate 2 is even) is conjoined with s-a-1 fault on line $I_{5.2}$ (Gate 3 is even). By the second clause of Conjecture 3, the s-a-1 faults on $I_{5.1}$ and $I_{5.2}$ are conjoined with s-a-0 faults on x_2 and x_3. It is to be noted that x_2-a-0 and x_3-a-0 are equivalent faults. At this point, the s-a-0 faults on the fanout paths remain to be tested. As the gates 2 and 3 are at even levels, they cannot be conjoined together according to Conjecture 1. Therefore using Clause 2 of the Conjecture 3, the s-a-0 fault on $I_{5.1}$ is conjoined with the s-a-1 fault on either x_2 or x_3. Similarly the s-a-0 fault on $I_{5.2}$ is conjoined with the s-a-1 faults on either x_2 or x_3. For minimality purposes, if $I_{5.1}$-a-0 is conjoined with x_2-a-1, then $I_{5.2}$-a-0 is conjoined with x_3-a-1 or vice-versa. Lastly, the s-a-1 faults on line x_1 is conjoined with s-a-1 fault on line x_4, using Conjecture 1. So the minimal multiple fault set is given by

$$
F_m = \left\{ \begin{bmatrix} x_1\text{-a-1} \\ x_4\text{-a-1} \end{bmatrix} \begin{bmatrix} x_3\text{-a-0} \\ x_2\text{-a-0} \\ I_{5.1}\text{-a-1} \\ I_{5.2}\text{-a-1} \end{bmatrix} \begin{bmatrix} x_2\text{-a-1} \\ I_{5.1}\text{-a-0} \end{bmatrix} \begin{bmatrix} x_3\text{-a-1} \\ I_{5.2}\text{-a-0} \end{bmatrix} \right\}
$$

This multiple fault set F_m is the same as F_{m1} obtained in the Example 4. Using similar arguments it is possible to derive F_{m2}.

4.3 Minimal Test set for Primary Input Fanout Circuits

4.3.1 Fault Folding

The primary input fanout circuits are also treated like the internal RFO circuits. Here the stuck-at faults on the primary input fanout branches in addition to stuck-at faults on the primary inputs are essential faults. The theorems and conjectures developed for RFO
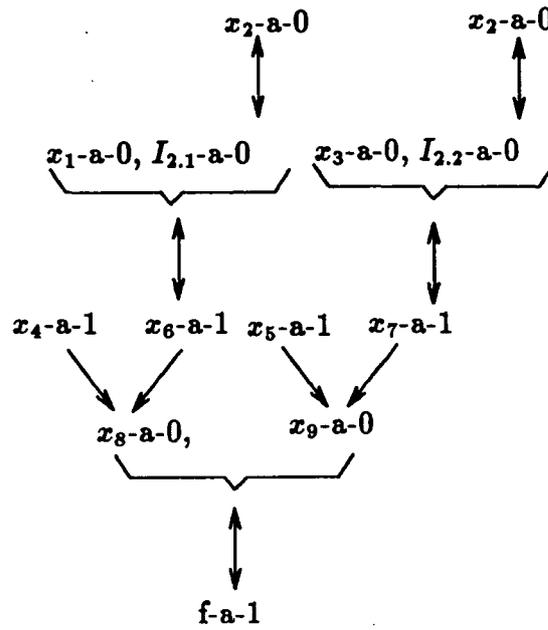
$$x_2\text{-a-}0 \qquad\qquad x_2\text{-a-}0$$

$$x_1\text{-a-}0,\ I_{2.1}\text{-a-}0 \quad x_3\text{-a-}0,\ I_{2.2}\text{-a-}0$$

$$x_4\text{-a-}1 \quad x_6\text{-a-}1 \quad x_5\text{-a-}1 \quad x_7\text{-a-}1$$

$$x_8\text{-a-}0, \qquad x_9\text{-a-}0$$

$$\text{f-a-}1$$

Figure 15: Fault folding graph for f-a-1

$$x_2\text{-a-}1 \qquad\qquad x_2\text{-a-}1$$

$$x_1\text{-a-}1 \quad I_{2.1}\text{-a-}1 \qquad x_3\text{-a-}1 \quad I_{2,2}\text{-a-}1$$

$$x_4\text{-a-}0,\ x_6\text{-a-}0 \qquad x_5\text{-a-}0,\ x_7\text{-a-}0$$

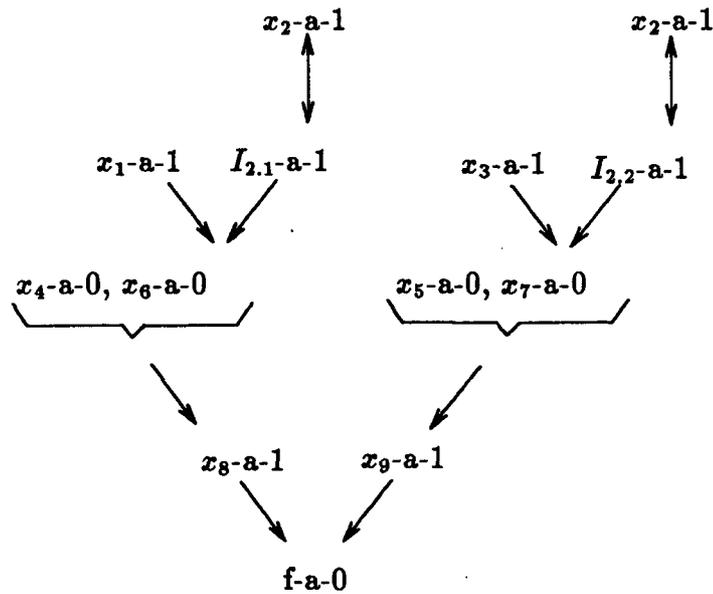$$x_8\text{-a-}1 \quad x_9\text{-a-}1$$

$$\text{f-a-}0$$

Figure 16: Fault folding graph for f-a-0

are also valid here. An example will be considered to describe the process of deriving the minimal test set.

Example 6 *Find the minimal Test set for the circuit shown in Figure 14* .

Step 1:- The fault folding graphs f-a-1 and f-a-0 are drawn (See figures 15 and 16).
Step 2:- From the fault folding graph for f-a-0 (Figure 16) the multiple fault set is formed

$$f_m = \left\{ \begin{bmatrix} x_1\text{-a-1} \\ x_4\text{-a-0} \end{bmatrix} \begin{bmatrix} x_4\text{-a-0} \\ x_2\text{-a-1} \\ I_{2.1}\text{-a-1} \end{bmatrix} \begin{bmatrix} x_2\text{-a-1} \\ I_{2.2}\text{-a-0} \\ x_5\text{-a-0} \end{bmatrix} \begin{bmatrix} x_3\text{-a-1} \\ x_5\text{-a-0} \end{bmatrix} \right\}$$

From the fault folding graph for f-a-1 (Figure 15), the multiple fault set is formed as

$$f_m = \left\{ \begin{bmatrix} x_1\text{-a-0} \\ x_3\text{-a-0} \\ x_2\text{-a-0} \\ I_{2.1}\text{-a-0} \\ I_{2.2}\text{-a-0} \end{bmatrix} \begin{bmatrix} x_4\text{-a-1} \\ x_5\text{-a-1} \end{bmatrix} \right\}$$

One of the minimal multiple fault sets covering all the essential single stuck-at faults is

$$F_{m1} = \left\{ \begin{bmatrix} x_1\text{-a-1} \\ x_4\text{-a-0} \end{bmatrix} \begin{bmatrix} x_4\text{-a-0} \\ x_2\text{-a-1} \\ I_{2.1}\text{-a-1} \end{bmatrix} \begin{bmatrix} x_2\text{-a-1} \\ I_{2.2}\text{-a-1} \\ x_5\text{-a-0} \end{bmatrix} \begin{bmatrix} x_3\text{-a-1} \\ x_5\text{-a-0} \end{bmatrix} \begin{bmatrix} x_1\text{-a-0} \\ x_3\text{-a-0} \\ x_2\text{-a-0} \\ I_{2.1}\text{-a-0} \\ I_{2.2}\text{-a-0} \end{bmatrix} \begin{bmatrix} x_4\text{-a-1} \\ x_5\text{-a-1} \end{bmatrix} \right\}$$

Step 3:- The test vector sets T_{m1} for the fault sets F_{m1} is found:-
$T_{m1} = < x_1 x_2 x_3 x_4 x_5 > =$

$$\left\{ \begin{pmatrix} 01010 \\ 01110 \\ 01111 \end{pmatrix} \begin{pmatrix} 10110 \\ 10010 \end{pmatrix} \begin{pmatrix} 00101 \\ 10101 \end{pmatrix} \begin{pmatrix} 01001 \\ 11001 \\ 11011 \end{pmatrix} \begin{pmatrix} 11111 \end{pmatrix} \begin{pmatrix} 00000 \\ 01000 \\ 10100 \end{pmatrix} \right\}$$

4.3.2   Method by Inspection

The Example 6 will be reworked using method by Inspection. The same rules used for RFO circuits will be followed.

Gates 1, 4 and 5 are odd level gates and gates 2 and 3 are even level gates. Using the Conjectures 1 through 6 the following results have been arrived at:-

1. x_4-a-1(even level gate 2) can be conjoined with x_5-a-1 (even level gate 3).

2. Gates 4 and 5 are to be treated as primary gates since there is no other gate between the primary inputs and inputs of the gates 4 and 5. The parity of inversion through the two primary input fanout branches is the same(odd). Hence, the fault $I_{2.1}$-a-0 (even gate 4) can be conjoined with $I_{2.2}$-a-0 (even gate), using Clause 2 of Conjecture 3.

Note that for a primary gate, it is enough if one of its inputs is tested for stuck-at-0 fault. So when we test multiple fault $\{I_{2.1}$-a-0,$I_{2.2}$-a-0$\}$ we will have tested gates 4 and 5 for stuck-at-0 faults leading to multiple fault set F_m

$$F_m = \left\{ \begin{bmatrix} x_1\text{-a-1} \end{bmatrix} \begin{bmatrix} x_3\text{-a-1} \end{bmatrix} \begin{bmatrix} I_{2.2}\text{-a-1} \end{bmatrix} \begin{bmatrix} I_{2.1}\text{-a-1} \end{bmatrix} \begin{bmatrix} x_4\text{-a-1} \\ x_5\text{-a-1} \end{bmatrix} \begin{bmatrix} I_{2.1}\text{-a-0} \\ I_{2.2}\text{-a-0} \end{bmatrix} \right\}$$

This is the same as F_{m1} obtained previously in Example 6. The test vectors are found as usual either by path sensitization or Boolean differences.

5 Conclusions

Techniques for obtaining a minimal test vector set for stuck-at faults have been developed. Two new procedures have been described, one of which allows the test vector set to be derived by inspection. The other procedure is an algorithmic procedure and uses the fault folding technique. Both techniques are very simple and highly ergonomically efficient as compared to existing methods. Certain well known theorems have been modified to remove their latent redundancies.

The fault folding methods technique is a graphical method utilizing fault folding graphs. This technique has been proven to work for all kinds of irredundant combinational circuits – NRFO, RFO and primary input fanout circuits. This method is simple and straight forward to use when compared with the existing methods.

The second method - Method by Inspection was developed so that the fault folding graphs needed in the first method need not be drawn. All that is needed is the circuit diagram. The conjectures forming this method were developed by translating the graphical language of the fault folding graphs to a layman's language. The only thing one needs to do is to keep track of the gate number. This method, also, works very well with all irredundant combinational circuits.

The whole procedure for stuck-at faults could be automated, such that a computer program could look at a network file and develop a minimal test vector set or minimal fault set. Such software would be of immense help to the industry and test engineering community as a whole.

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