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Invited Paper

Fabricating Binary Optics: An Overview of Binary Optics Process Technology

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ABSTRACT

A review of binary optics processing technology is presented. Pattern replication techniques have been optimized to generate high-quality efficient microoptics in visible and infrared materials. High resolution optical photolithography and precision alignment is used to fabricate maximally efficient fused silica diffractive microlenses at λ =633 nm. The degradation in optical efficiency of four-phase-level fused silica microlenses resulting from an intentional 0.35-µm translational error has been systematically measured as a function of lens speed (F/2 - F/60). Novel processes necessary for high sag refractive IR microoptics arrays, including deep anisotropic Si-etching, planarization of deep topography and multilayer resist techniques, are described. Initial results are presented for monolithic integration of photonic and microoptic systems.

1. INTRODUCTION

Optics systems in the twenty-first century will employ hybrid and integrated diffractive optical elements to effect lightweight, compact designs. This requires the optics industry to adopt a new manufacturing paradigm - i.e., to design the electro-optic system in totality, and to implement the new fabrication techniques necessary to make novel optical components. Binary optics technology adapts the zeitgeist of integrated circuit manufacturing technology, i.e., CADCAM optics tools and design packages coupled with sophisticated and mature VLSI microstructure fabrication techniques, to make both diffractive and refractive microoptics. By sharing a technology base with the microelectronics, photonics, and micromachining communities, manufacturing costs are reduced and integration of these technologies is simplified. From its inception, binary optics technology has been driven by the demand for fast broadband flat optics needed for low cost smart sensors. High functionality binary optical elements streamline the optical train and simplify system assembly.

In the past decade, binary optics technology has evolved through three generations: the first is characterized by slow diffractive macrooptics; the second by fast microlens arrays; and the third by integrated layers of microoptics and photonic devices. First generation binary optics elements have large periods (hundreds of microns); the second and third generations have submicron zone widths. The first generation hybrid diffractive-refractive technology, primarily used to correct aberrations in large-aperture refractive optics, has been adopted by many industrial, government, and defense organizations, as apparent from the papers presented at this conference. The second generation consists of fast microlens arrays comprised of large

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numbers (>10⁵) of identical elements used in such diverse applications as focal plane arrays, laser beam addition, Hartmann sensors, wavefront multiplexers, and beam-steering.¹⁻⁶ The ultimate potential of these microoptics arrays awaits the fruition of third generation binary optics technology - new "amacronic" architectures that integrate multiple planes of optics and electronics.⁷

Two major factors have contributed to the widespread success of binary optics technology: one - the flexibility made possible by the extensive use of preexisting microelectronics fabrication techniques, and two - the inherent reduced processing set, i.e., the binary coding of the fabrication steps which results in 2^M phase levels for M-mask layers.¹ To obtain highquality optics, VLSI-techniques must be customized to meet the specific and distinct concerns of microoptics fabrication. For example, exacting control of etch depth and overlay tolerances are needed to achieve optimal efficiency⁸, while novel "deep-structure" processing techniques are required to fabricate refractive microoptic arrays.⁹

This paper examines the pivotal role of fabrication in translating diverse optical designs into high-quality optics in a variety of materials. In particular, we evaluate how the alignment precision achieved during photolithography impacts the subsequent optical efficiency of diffractive microlenses.^{8, 10} The effect of misalignment on optical efficiency is measured as a function of lens speed (F/2 to F/60) on 200- μ m square fused silica microlenses at 633 nm.¹¹ Next, we describe the multilayer planarization/masking schemes and highly anisotropic Si reactive-ion etching (RIE) processes needed to manufacture high-bandwidth IR binary optics.⁹ Finally, we present a nascent layered system - arrays of CdTe microlenses monolithically integrated with photodetectors on opposite sides of the same substrate.⁵

2. FABRICATION AND OPTICAL EFFICIENCY

Binary optics technology conjoins computer-generated optical phase profiles with VLSI photomask and processing technology to form planar surface relief structures that manipulate optical wavefronts.¹ Conventional binary optics processing, Figure 1, consists of several iterative steps of photolithographic patterning and phase-relief creation. The relief structures can be constructed by a variety of methods, including etching, deposition, and ion- or photon-induced structural changes in the refractive index or the volume. Dry etching techniques, in particular reactive ion etching (RIE), offer the greatest amount of flexibility and are used to manufacture the optics described below. Binary mask coding greatly reduces the number of process iterations required for highly efficient diffractive elements: only M process iterations result in an optic with 2^M phase steps.¹ Each of the M-steps creates a phase step of height d = $\lambda/(2^{M}(n-1))$, where λ is the design wavelength and n is the material index of refraction.

Standard VLSI techniques must be finessed to address the particular requirements of highquality microoptics fabrication. The nested binary optics structures impose three critical restraints on the fabrication process: (1) to register the mask to the substrate pattern with 0% overlay tolerance; (2) to etch vertical sidewall profiles without lateral undercutting or erosion of the mask edge; and (3) to maintain precise control over the phase-step-heights, often to better than 1%, for both shallow ($\approx 10 \text{ nm}$) and deep ($\approx 10 \text{ µm}$) structures. In addition, to achieve high fidelity pattern replication of curvilinear linewidths that can range from 0.5 µm to 50 µm on a single mask level, the bias in the photolithography process must be characterized and accommodated.¹² Failure to obtain positional and dimensional control results in phase-stepwidth errors, which appear as trenches and ridges in the etched structures. Phase-step-width and height errors can significantly reduce the optical efficiency.¹³⁻¹⁵

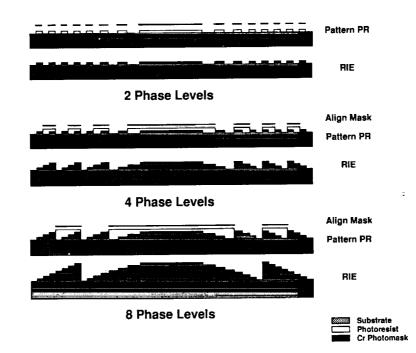


Figure 1: Fabrication steps for an eight-phase-level binary optics microlens. To maximize linewidth control, the mask layer with the smallest features is replicated first. The substrate is coated with photoresist, patterned photolithographically using a contact mask aligner, and then etched in an RIE system. Subsequent mask layers are carefully aligned to the patterned surface. This sequence is iterated until the desired number of phase levels is achieved. The binary coding scheme doubles the number of phase levels after each etch.

Practicality dictates that we establish criteria to determine where the incremental gain in optical performance justifies the required fabrication effort. We have undertaken a substantial effort at MIT Lincoln Laboratory to quantify the efficiency limits of diffractive binary-optic microlenses and to correlate losses in optical efficiency with specific fabrication errors. In particular, we have focused on the interrelation between alignment errors and microlense efficiency. The vehicle for these studies is the "Best Efficiency Array SeT" (BEAST), a fused silica microlens test set comprised of 10 different lenslets having 200 µm x 200 µm square

apertures and focal lengths between 0.17 and 14 mm at $\lambda = 633$ nm.⁸ Test devices contain both isolated single lenslets and 10 x 10 microlens arrays distributed across a 1.2 cm x 1.8 cm area on a background grid of sixteen alignment patterns (Figure 4a). The fine verniers, shown in Figure 2, consist of a two-dimensional grid spanning a \pm 0.5 μ m graduated scale divided into 0.1 μ m increments. The X and Y locations of the centered square can be read to \pm 0.05 μ m precision from these verniers. The vernier grid in Figure 2 indicates essentially "perfect" registration accuracy at this location.

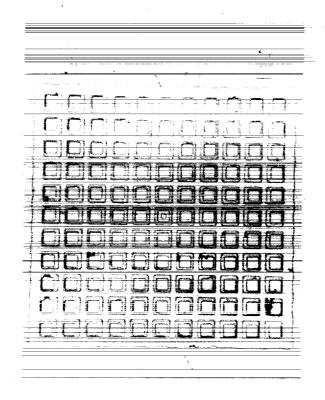


Figure 2: Example of a vernier grid pattern used to determine alignment accuracy. Results are shown for a level $2\rightarrow 3$ alignment.

These verniers are used to determine the alignment accuracy both during the registration process (before photoresist exposure) and after the development of the photoresist pattern. We have achieved overlay registration to better than 0.1 μ m over the two-square-centimeter area of the BEAST pattern by using these alignment marks.⁸ The eight-phase-level F/6 fused silica microlens shown in Figure 3 is representative of the BEAST test set lenslets.

Benchmark optical efficiency measurements have been made on these diffractive quartz microlenses as a function of lens speed and then compared with predictions of direct electromagnetic calculations for 2-, 4- and 8- phase levels.^{8,10} The first order diffraction efficiency is measured at $\lambda = 633$ nm using the "EtaMeter" system.¹⁰ The EtaMeter, which exhibits low-noise and long-term stability, can measure relative efficiency with better than 0.001 precision and, with calibration, absolute efficiency accurate to 0.002.¹⁰ For an eight-phase-level F/4.5 microlens having less than 0.1 µm misalignment error, we have measured an absolute efficiency of 0.85; this is, we believe, the highest efficiency reported to date for such a

fast, binary optics lens in the visible. This result corresponds to 96% of the predicted value for this lens and implies that net fabrication errors contributed only a 4% efficiency loss.

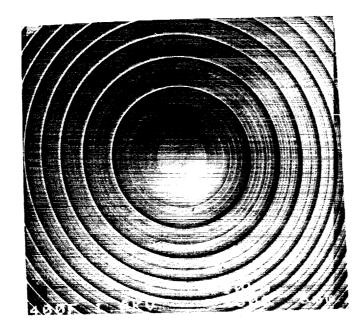
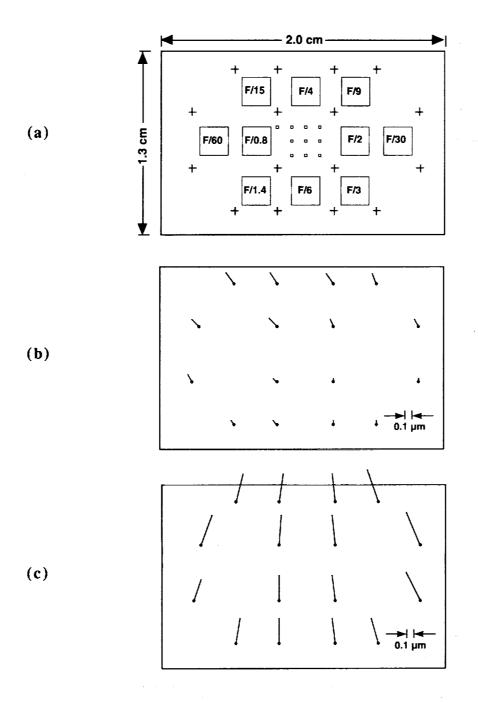


Figure 3: SEM of an eightphase-level 200- μ m square aperture F/6 fused silica microlens. The minimum zone width on level 3 is 0.8 μ m.

To quantify the impact of alignment errors on optical efficiency, we have intentionally introduced a 0.35- μ m translational error between mask layers 1 and 2 in one set of four-phase level lenslets.¹¹ Optical efficiency measured for this "misaligned" set of microlenses are compared with a nominally identical, four-phase level, "well-aligned" set of microlenses. The alignment results are plotted in Figure 4 for both the well-aligned optic, QB2 (Fig. 4b) and the misaligned optic, QB3 (Fig. 4c). The average and standard deviation of the vernier readings at these sixteen sites, weighted equally, are 0.06 ± 0.03 (x), 0.1 ± 0.04 (y) for QB2; and -0.01 ± 0.17 (x), 0.38 ± 0.04 (y) for QB3.

It is apparent from the data plotted in Figure 5 that pattern registration has a significant effect on the absolute optical efficiencies of these two optics, measured as a function of the lens speed. The performance of the misaligned optic falls below the well-aligned optic at F/15; at F/6 the efficiency of the misaligned microlenses is 5% less than the well-aligned lenslets; and at F/2 the misaligned lenslets show a 10% decrease in efficiency below that of the well-aligned microlenses. A strong correlation exists between the sizeable efficiency losses displayed by the fast lenslets and the fraction of the zonewidth intercepted by the intentional misregistration. For example, 0.35 μ m is only 3% of the minimum full zone for the F/60 lenslet, but is 25% of the minimum zonewidth for the F/2 microlens. Even the nominally well-aligned optic exhibits decreased efficiency for the fastest lenslets (F/2). Linewidth errors in the 0.5 μ m outer zones of the fastest lenslets may contribute to the efficiency losses in both sets of microlenses. The etch depth errors recorded for these microlenses - 1-2% of the total phase-step-height - have negligible impact on the efficiency.



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Figure 4: Comparison of mask layer $2\rightarrow 1$ alignment results for a "well-aligned" and a "misaligned" optic at the 16 vernier sites. (a) Schematic of the BEAST mask layout showing the location of the verniers (crosses), 10x10 microlens arrays (large squares), and single lenslets (small squares). Alignment results for (b) BEAST sample QB2 ("well-aligned"); and (c) Beast sample QB3 ("misaligned"). Note the 0.1 μ m scale marker for data plotted in (b) and (c).

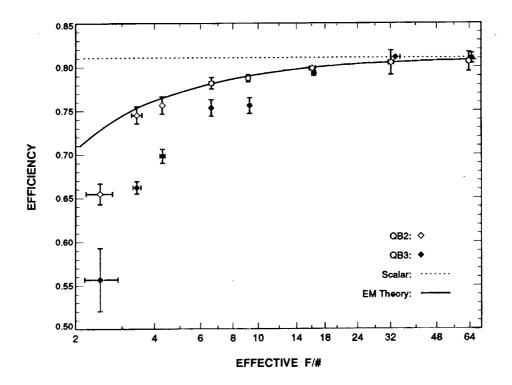
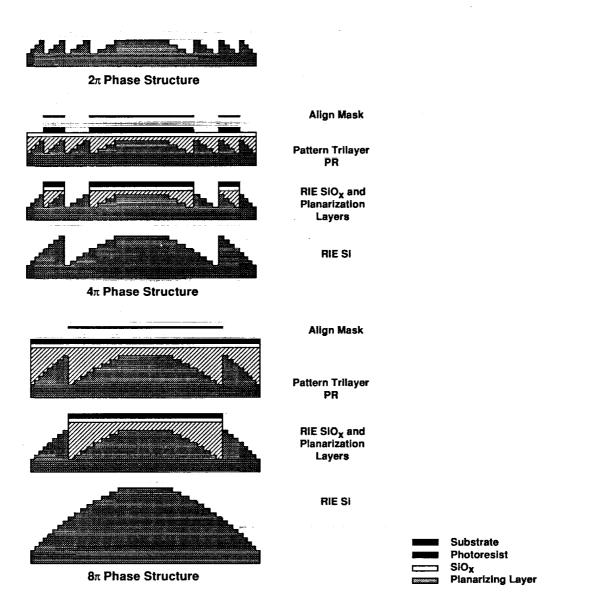


Figure 5: Optical efficiency of four-phase-level microlenses as a function of F/#. The open circles are the data from QB2 the ("well-aligned" sample); the solid circles are the data from QB3 (the intentionally misaligned sample). The dotted line is the scalar theory efficiency for four-phase levels (81%). The solid line is the predicted value from the full electromagnetic calculation.^{12,13}

3. REFRACTIVE MICROOPTICS

3.1 Fabrication of infrared refractive microoptics

The demand for both visible and IR broadband microoptics has driven our development of fabrication capabilities necessary to create deep, high-resolution, three-dimensional structures. In particular, two refractive designs for the 8-12 μ m bandwidth regime - a prototype sensor microlens with 14- μ m sag and a color dispersive microoptic array with 7.5- μ m sag - require deep anisotropic etching with precisely controlled phase-step heights. The desired refractive surface contour of the broadband IR microlens is approximated in a stepwise manner. In effect, we are eliminating the diffractive resets from the traditional binary optics phase-relief structure (i.e., one that has the appropriate phase-quantization for a particular efficiency) by a series of photolithography and deep-etching processes schematically outlined in Figure 6.



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Figure 6: The sequence for fabricating refractive binary optics, consisting of iterated steps of photolithography, multilayer resist processing, and RIE. Assuming an initial stepped structure, multilayer resist techniques are required to complete the fabrication sequence. A thick polymer layer is used to planarize the steep topography. RIE is used to pattern both the intermediate SiO_x transfer layer and the planarization level. This forms the mask for the subsequent RIE of the silicon substrate. Each silicon RIE step doubles the previous etch depth, corresponding to sequential " 2π ", " 4π ", and " 8π " total phase step heights.

To maintain the high fidelity pattern replication necessary for efficient binary optics structures, we must develop techniques to etch deep anisotropic profiles into the silicon substrate. By judicious choice of the plasma chemistry used in the RIE process, we can induce the in situ formation of a sidewall inhibition layer that prevents lateral undercut and enhances vertical profile control.^{16,9} We have achieved vertical sidewalls without mask undercutting and with a 5:1 etch selectivity (ratio of Si:photoresist etching rates) by using an SF₆/O₂ gas mixture in a commercial RIE system (Semigroup TP1000).⁹ Representative results for one-micron lines etched 8 μ m deep in Si are shown in Figure 7. We observe no undercut of the photoresist mask, still present on these high aspect ratio vertical bars.

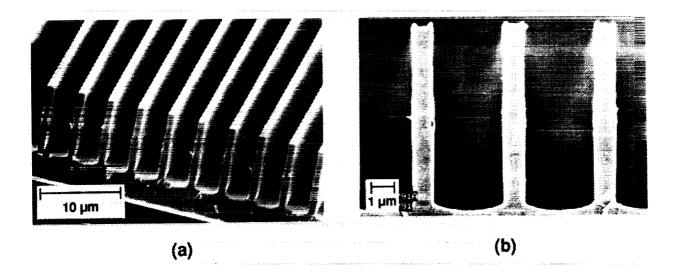


Figure 7: SEM micrographs of anisotropic features etched 8- μ m deep in Si. (a) 3000x, (b) 9000x.

For such deep structures, a single layer of thin photoresist is insufficient to cover the existing substrate topography or to maintain reasonable linewidth acuity. Hence, we must resort to multilayer resist techniques for patterning subsequent levels as shown in Figure 6b and c.⁹ The photoresist stencil in the imaging layer is first etched into the transfer layer, a thin film of SiO_x, in a CHF₃ plasma. This SiO_x mask is duplicated into the thick planarization layer by O_2 RIE, creating the final mask for the silicon substrate etch.

Assuming facile control of these individual processes, we now proceed to combine them to manufacture the desired broadband microoptics. The first example, displayed in Figure 8, is a prototype of a fully refractive Si microlens for an advanced satellite sensor and has a total etched depth of 14 μ m. In an actual device, each of these two-micron steps would themselves be subdivided into quantized phase steps to produce an efficient microlens. In this particular

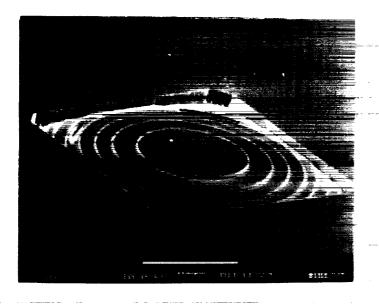


Figure 8: Eight-phase level 200 μ m diameter refractive Si microlens with sag height of 14 μ m.

demonstration, however, our motive is to establish the anisotropic deep etching and planarization capabilities required for broadband Si microoptics.

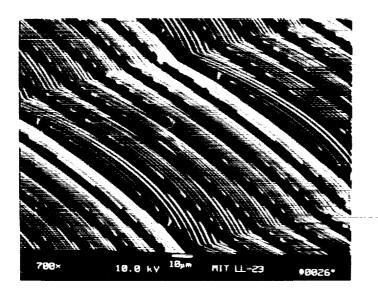


Figure 9: A 16-phase level color dispersing microlens array etched 7.5 μ m deep. Shown is one pixel element from a 64 x 64 array.

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The color dispersive microoptic, pictured in Figure 9, is a combination F/2 refractive microlens for focusing and 17 μ m period diffraction grating for color separation. The total depth of this optic, made with four mask levels, is 7.5 μ m. There are 64x64 identical pixel elements, each 100 μ m x 100 μ m square, in this array. The design and performance of this device are detailed elsewhere.¹⁷

4. LAYERED OPTICS

4.1 Integrated focal plane array optics

What is the future of binary optics technology development? High-quality microoptics will be integrated into layered systems. Such multilayered systems of optics and optics integrated with photonics and microelectronics will form the initial building blocks of amacronic focal plane arrays.⁷ By exploiting the fill factor enhancement made possible by microlens arrays, photodetectors can be made smaller or spaced further apart; the newly available space can be filled with preprocessing circuitry. Monolithic integration of active and passive devices on the same substrate will eliminate difficult and time-consuming alignments between discrete planes of different devices.

Although major research and development efforts are required to realize amacronic focal planes that can combine detection with preprocessing capabilities, we have taken initial steps towards demonstrating dual-sided integration of optics and electronics. In a joint project with LORAL IRIS, we monolithically integrated focal plane arrays of microlenses with epitaxially grown HgCdTe photodetectors on opposite sides of a single CdTe substrate.⁵ The microlens array pattern is registered to the HgCdTe photodetectors on the front side of the substrate to better than 2 μ m, using our Karl Suss infrared backside mask aligner, and then etched into the backside of the substrate. Figure 10 shows the lensed substrate mounted to the carrier chip. Microlenses improved the detector quantum efficiency by a factor of 3.⁵ In addition, by reducing the needed active detection area, the microlenses result in increased gamma radiation hardening.

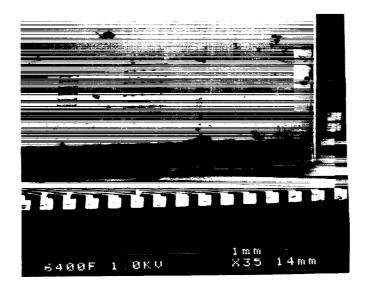


Figure 10: An SEM of monolithically integrated F/4 lenslets and HgCdTe photodetectors focal plane array.

5. CONCLUSION

Fabrication is the cornerstone for the realization of high-quality microoptics. We have highlighted details of the Binary Optics effort at MIT Lincoln Laboratory that lead to significant improvement in optical performance and to new microoptics capabilities. In particular, we have:

- recounted processing techniques used to fabricate benchmark quality, diffractive binary optics microlenses and presented measurements that clearly correlate efficiency loss with registration accuracy.
- described high-resolution Si RIE and multilayer resist processes developed to fabricate deep, three-dimensional, stepped optical structures. Fully refractive IR microoptics for applications in advanced sensors and color dispersive microoptics have been demonstrated.
- demonstrated monolithically integrated focal plane arrays of CdTe microlens and HgCdTe photodetectors the initial step towards smart sensors.

Binary optics technology provides the base for a new class of smart, compact, low-cost sensors. In the future, system designers will integrate optics, electronics and photonics components to exponentially increase sensor processing capability. Implementation of these designs will be limited only by the creativity of microfabricators in inventing new techniques to fabricate them.

6. ACKNOWLEDGEMENTS

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