Heterojunction Bipolar Transistor Technology for Data Acquisition and Communication

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Abstract - **Heterojunction Bipolar Transistor (HBT) technology has emerged as one of the most promising technologies for ultrahigh-speed integrated circuits. HBT circuits for digital and analog applications, data conversion, and power amplification have been realized, with speed performance well above 20 GHz. At Rockwell, a baseline AlGaAs/GaAs HBT technology has been established in a manufacturing facility. This paper describes the HBT technology, transistor characteristics, and HBT circuits for data acquisition and communication.**

1 Introduction

Heterojunction Bipolar Transistor (HBT) technology has shown great capabilities for the realization of high performance analog, digital, and microwave circuits [1-2]. To date, most of the HBT circuits demonstrated are based on AlGaAs/GaAs material system with wide-bandgap AlGaAs emitters and heavily doped GaAs bases. The AlGaAs/GaAs HBT technology offers a number of intrinsic advantages. High f_t and f_{max} (above 55 GHz), as well as high transconductance (above 10000 mS/mm), can be realized. The threshold voltages (Vth) are highly uniform; matching of Vth's of HBTs in differential pairs of about 1 mV has been measured. The intrinsic junctions of HBTs are well shielded from substrate and surface. Trap induced hysteresis effects are absent and $1/f$ noise is low. AlGaAs/GaAs HBTs also offer high breakdown voltages. The HBTs are fabricated on semi-insulating GaAs substrate, which reduces parasitic capacitances of transistors and interconnect lines and allows integration of multifunctional circuits. Rockwell pioneered the research of AlGaAs/GaAs HBT technology and developed a baseline technology with high current gain for analog, digital, and A/D conversion applications. The technology is now established in a manufacturing facility (Rockwell's Microelectronics Technology Center-MTC). High performance HBT circuits can be realized with high yields. As a result, recently Rockwell announced its initial HBT products. This paper presents Rockwell's baseline HBT technology and its applications in data acquisition and communication. Development of HBT-based technologies will also be described.

2 Rockwell's Baseline HBT Technology

The HBT technology features emitter-up/single-heterojunction bipolar transistors, monolithically integrated Schottky diodes, NiCr thin film resistors, MIM capacitors, and up to

three levels of metal interconnect. AlGaAs/GaAs HBTs are fabricated on MBE or MOCVD grown epitaxial wafers. The epitaxial layer structure and a schematic cross section of an integrated HBT and a Schottky diode are shown in Fig. 1. The minimum geometry device used for the circuits has an emitter area of $1.4\mu m \times 3\mu m$, defined by projection optical lithography. The measured Gummel Plot of this device as shown in Fig. 2(a) illustrates current gain of about 100 at $Ic = 1mA$. The measured RF characteristics of the transistor at $Vce = 2\ V$ and $Jc = 8 \times 10^4 A/cm^2$ are shown in Fig. 3(b). F_t and f_{max} above 55 GHz are obtained.

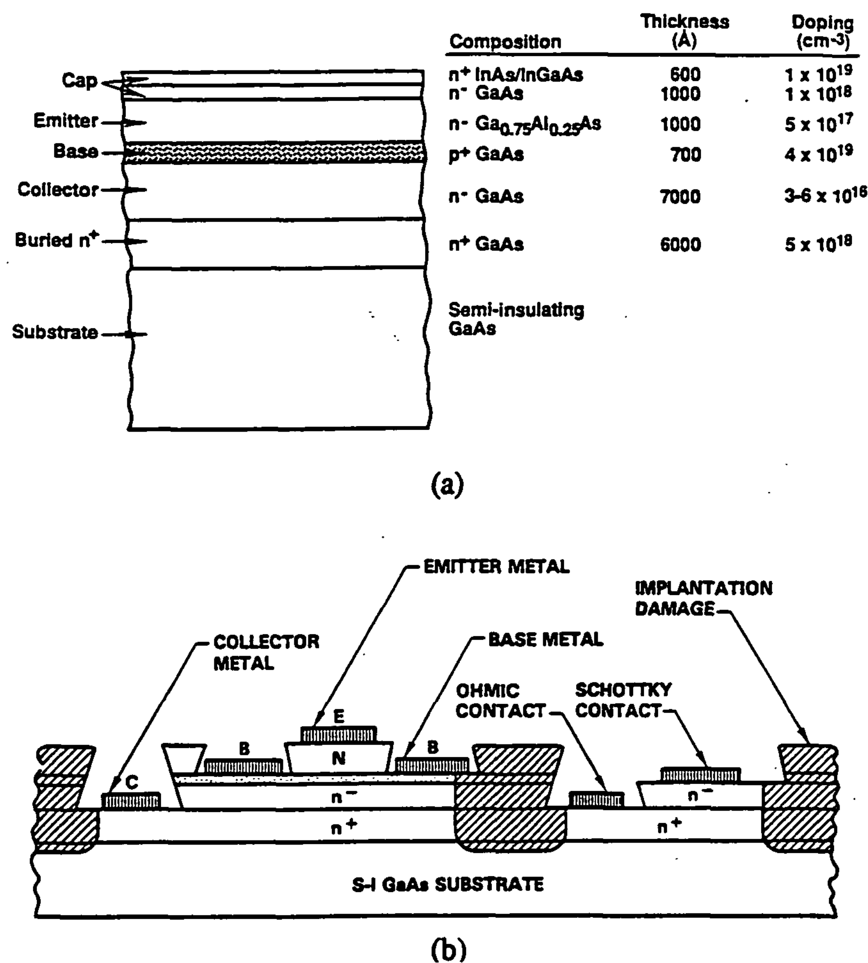


Figure 1: (a) HBT epitaxtal layer structure (b) Simplified cross section of an HBT and a Schottky diode

The diodes are realized using same layer structure and process as the HBTs. Typical series resistance and parasitic capacitance are 40Ω and $12fF$ for a $2\mu m \times 4\mu m$ diode.

Many high-performance digital and analog circuits have been realized with the Rockwell baseline HBT technology. Frequency dividers have been demonstrated to work above 25 GHz [3]. 8-GHz 1000-gate gate arrays and 15-GHz 500-gate gate arrays were also realized

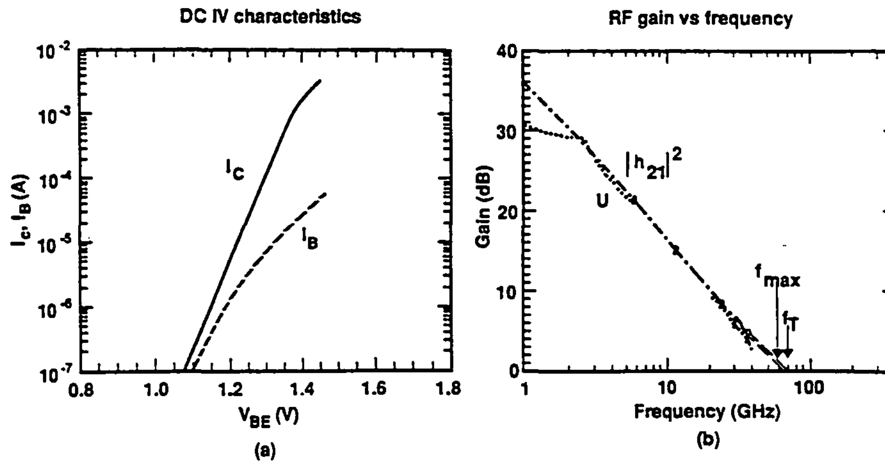


Figure 2: (a) Gummel Plot and (b) RF characteristics of an HBT that has an emitter area of $1.4\mu m \times 3\mu m$

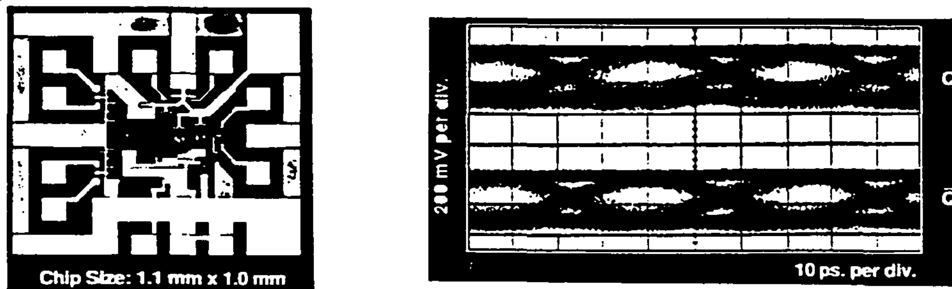


Figure 3: (a) Microphotograph of a fabricated HBT 2:1 mux. (b) Eye pattern of the mux output at 30 Gb/s operation.

(jointly developed with IBM) [4-5]. We have demonstrated a number of ultra-high speed HBT circuits for lightwave communication, jointly with Bellcore. These include a 30 Gb/s 2:1 mux, a 27 Gb/s 1:2 demux, a 27 Gb/s 4-bit mux/demux, and a 7 Gb/s 8-bit mux/demux [6-7]. The microphotograph and operation of the 30 Gb/s 2:1 mux are shown in Fig. 3.

In the A/D conversion area, we have realized HBT voltage comparators that operate up to 20 GSps [8], as shown in Fig. 4. We have demonstrated 2 GSps sample-and-hold (S/H) circuits with less than -40 dB distortion (jointly with HP Labs.), and Multi-GSps 4-bit and 6-bit quantizers [9-10]. We are developing high performance ADCs and DACs with the HBT technology. These include: a 6-GSps 6-bit ADC (also with HP Labs.), a 1.5-GSps 8-bit ADC, a 100-MSps 12-14 bit sigma-delta ADC, and a 1.2-GSps 12-bit DAC.

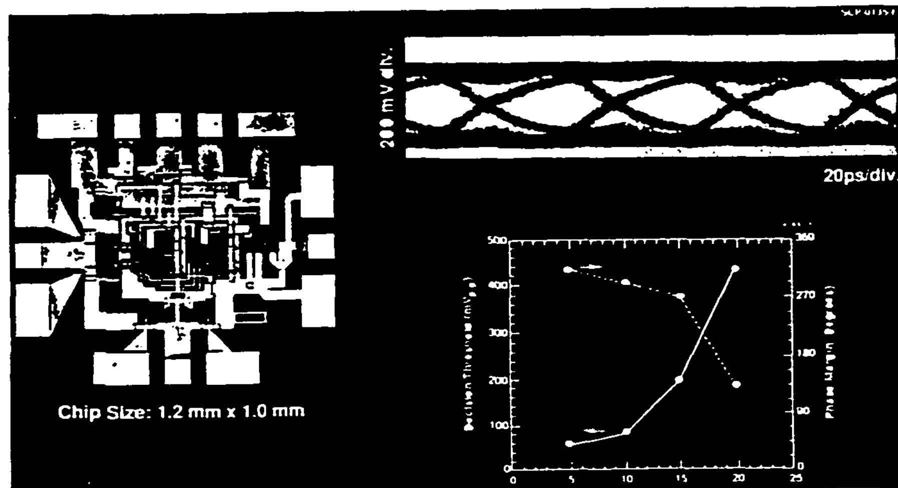
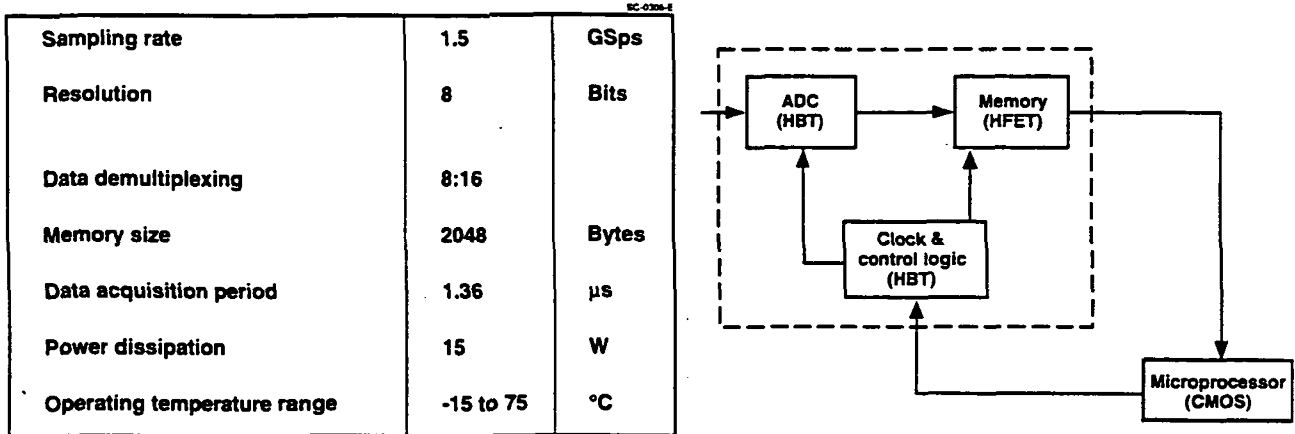


Figure 4: (a) Microphotograph of a fabricated HBT voltage comparator. (b) Output eye pattern of the comparator at 20 GSps operation. (c) Measured sensitivity and phase margin.

3 An HBT Based Data Acquisition System

We are developing a 1.5-GHz 8-bit data acquisition system (DAS), under a NASA/ONR contract. The primary goal is for laser altimeter applications, although the system can be used for general purpose ultra-high speed data acquisition. The system specifications are shown in Fig. 5. The system includes an HBT ADC, an HBT clock driver, 16 HFET (heterojunction FET) 1K memory circuits, and Si CMOS interface circuits. A schematic block diagram is also shown in Fig. 5.

The key component of the system is an HBT 8-bit 1.5-GSps ADC. The ADC employs a folding and interpolating scheme [11] that features flash ADC speed at significant savings in device counts and power. The block diagram of the ADC design is shown in Fig. 6.



Sampling rate	1.5	GSps
Resolution	8	Bits
Data demultiplexing	8:16	
Memory size	2048	Bytes
Data acquisition period	1.36	μs
Power dissipation	15	W
Operating temperature range	-15 to 75	°C

Figure 5: System specifications and Block diagram of an HBT based DAS.

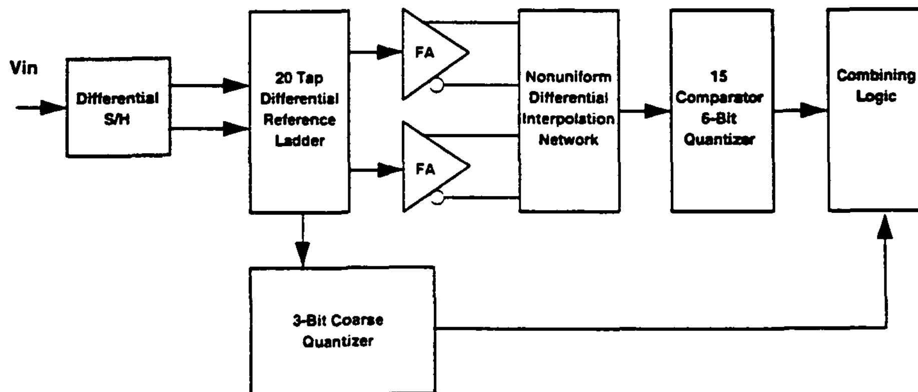


Figure 6: Block diagram of the 8-bit 1.5-GHz ADC design.

It contains an on-chip S/H circuit, a 3-bit coarse quantizer, a 6-bit fine quantizer, and a combining logic. We chose an all-differential architecture to reduce common-mode errors. An on-chip 1:2 demultiplexer for each output bit reduces the output data rate. The circuit contains about 1700 HBTs (950 in the A/D and 750 in the demux). The estimated power consumption is 3 W. Figure 7 shows a fabricated 8-bit 1.5 GSps HBT ADC.

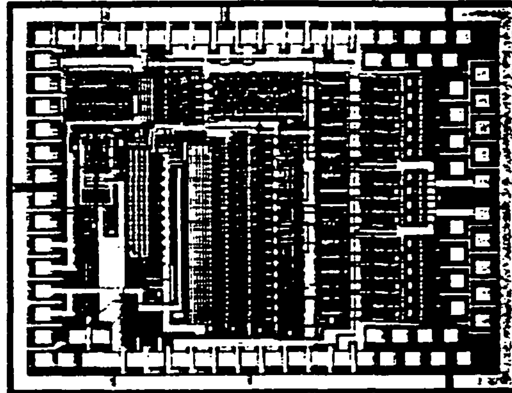


Figure 7: Microphotograph of a fabricated 8-bit 1.5 GSps HBT ADC.

To evaluate the expected dynamic accuracy of the HBT 8-bit ADC design, we have simulated the performance of the whole ADC circuit (except the data demuxing) with HSPICE, and analyzed the results. The digitized input waveform for a 1.6 MHz input at 1.5 GSps operation was reconstructed as shown in Fig. 8. The vertical scale of the signal waveform (shown on the right side of the figure) is in units of LSBs (least-significant bits). The distortions and noises were calculated, with much finer vertical scale (on left side). The calculated signal to noise + distortion ratio (S/N) is about 47 dB, which corresponds to 7.5 effective bits. Operations of the ADC at other sampling rates and input frequencies were similarly simulated and analyzed. Good S/N ratios were obtained. Initial fabricated ADCs are being evaluated.

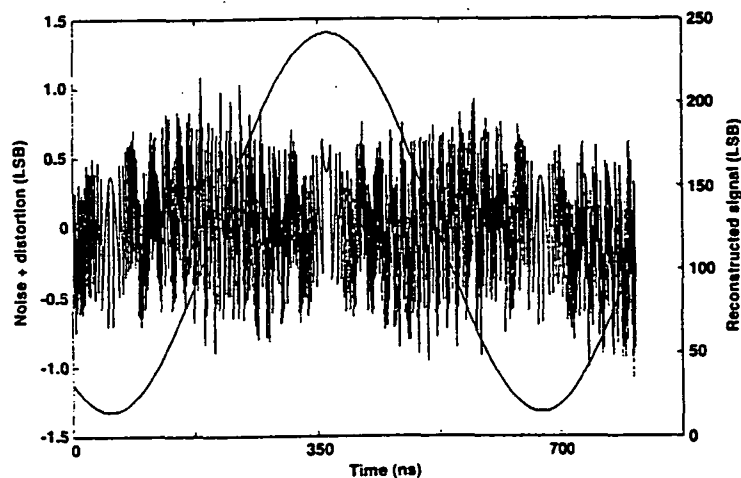


Figure 8: Simulated output waveform and noise + distortion of the 8-bit HBT ADC operation at 1.5 GSps and with a 1.6 MHz input.

The HBT clock driver circuit provides control logic and synchronized complimentary clocks to the 16 memory chips. It also contains a high speed frequency divider as a part of a phase locked loop for a clock generator. Other important components of the DAS are the 16 1K-bit FIFOs (first-in first-out memory). They are implemented with Rockwell's HMESFET which has a large noise margin.

The access time is 1.3 ns, with an estimated power consumption of 0.8 W per chip. Design of the FIFO allows convenient cascading of a series of chips for memory extension. The HBT clock driver and HMESFET circuits are also in fabrication now. We used an off-the-shelf CMOS transceiver chip to interface the GaAs chips with a personal computer.

4 Packaging Considerations

The HBT ADC and clock driver will be packaged with commercially available multi-layer ceramic packages, such as the TriQuint MLC132/64. They can be tested by direct capture of output data using logic analyzers (e.g. HP 16500) up to 1.5 GSps operation (with the help of on-chip demux). The memory chips will be packaged in MSI 3H32CM chip carriers. The data acquisition system will be assembled on a printed-circuit board (PCB). Figure 9 shows the design of the eight-layer PCB. The outer two layers will be implemented with polymide for high performance microstrips. The inner six power and ground layers will be realized with FR4 material for strength and low cost. The layout of one outer layer is shown in Fig. 10(a). The PCB measures $20cm \times 15cm$. The ADC and clock driver will be mounted back-to-back, so that the ADC output and clock signals can be routed to each FIFO identically. The PCB provides a clock synthesizer, a DMA (direct memory access) interface to computer, and SMA connectors for analog and clock inputs.

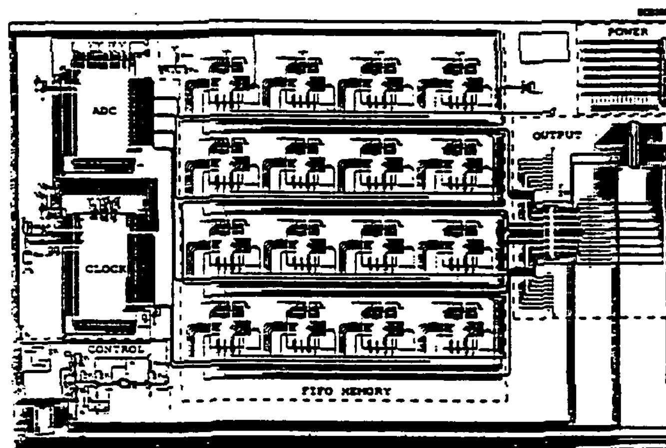


Figure 9: PCB design of the data acquisition system.

At Rockwell Science Center, advanced packaging technologies are being developed. One idea is to use Total Substrate Removal (also known as epitaxial layer lift-off or peeled film process) of the GaAs circuits, and attach them on a substrate of high thermal conductivity (e.g. diamond or AlN) in high density. The thin (about $5\mu m$) circuits and high thermal

conductivity of the substrate allow extra-dense chip packaging. This shortens the metal interconnect, thus increasing the allowed signal rates. A conventional Multi-Chip Module (MCM), using polyimide and Au/Cu wires, can be used for signal interconnect and power supply. The circuits on diamond or AlN substrate will be flip-chip bonded to the MCM. We estimated that $15cm \times 10cm$ of PC board area can be reduced to $2cm \times 1.1cm$ of the new MCM are a, as shown in Fig. 10(b). The packaging concept is illustrated in Fig.11. In addition to the size and speed benefits, the new packaging allows for increased ADC accuracy due to lower temperature variation over the chip, and improved lifetime/reliability due to improved thermal management. Furthermore, the HBT clock driver circuit may not be needed since the clocks to the memory chips may be distributed with a common bus in the new packaging. This will result in about 20% reduction in power consumption.

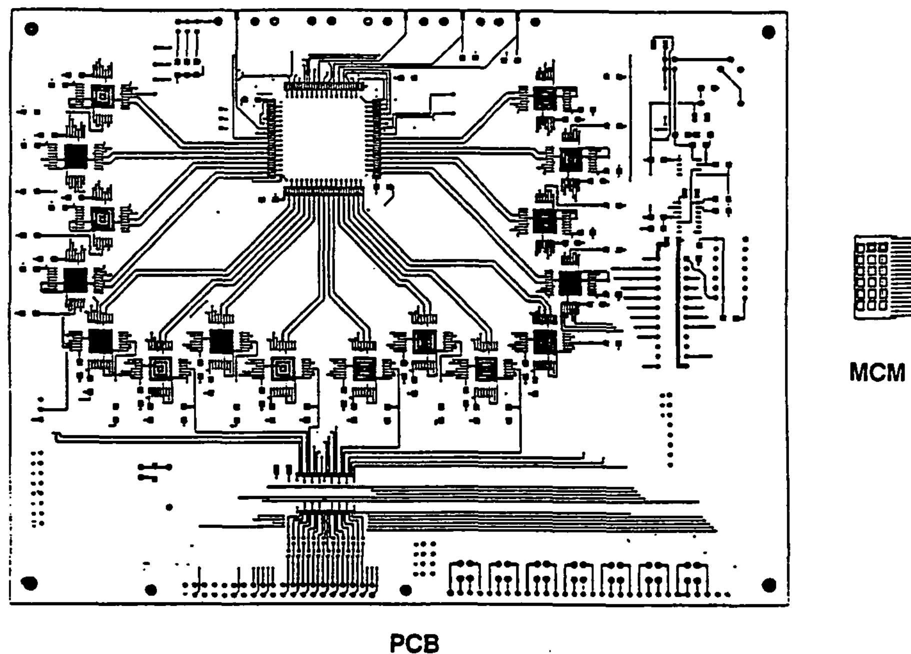


Figure 10: (a) Layout of one outer layer of the PCB. (b) Schematic layout of an advanced MCM, that contains the two HBT circuits and sixteen HFET memory chips.

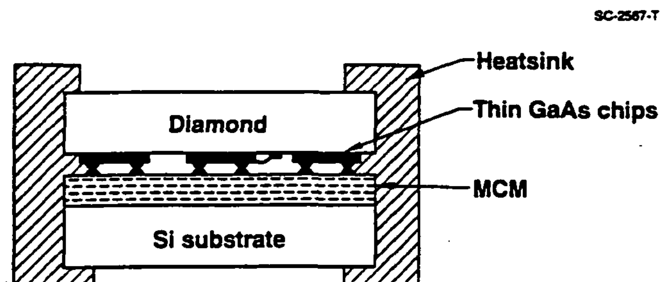


Figure 11: Advanced MCM packaging concept.

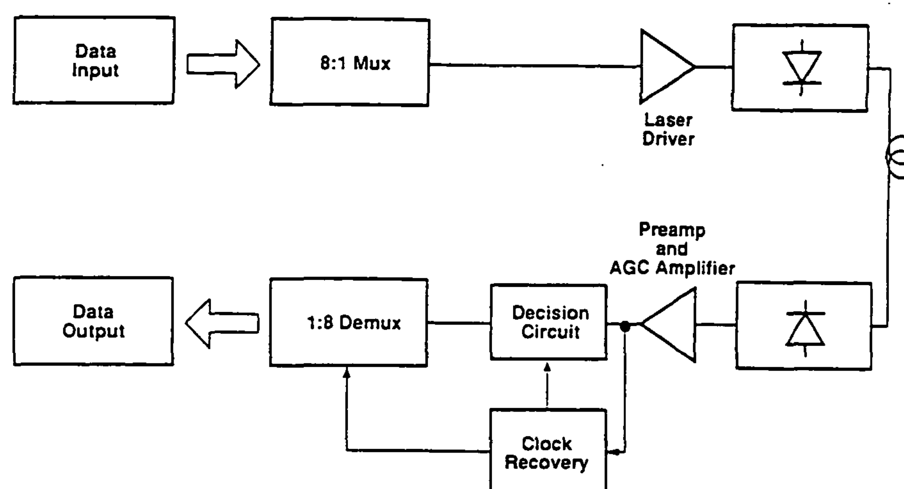


Figure 12: A simplified lightwave communication system.

5 HBT Circuits for Communications

HBT technology offers great capabilities to meet speed, accuracy, and power requirements of many communication systems. High-performance HBT circuits for lightwave and wireless communications have been demonstrated and many more are being developed.

Figure 12 shows a simplified lightwave communication system. Parallel digital data are serialized by a mux into a bit string of high data rate. A laser driver receives the bit string and generates current pulses to modulate a laser diode. The light signal is transmitted to a photo-detector through an optical fiber. The detector converts the light energy back to current pulses that are then translated into voltage pulses by a transimpedance amplifier. The signal is amplified, and a clock recovery circuit is used to regenerate synchronized clocks for the decision circuit and demux. Finally, the demux de-serializes the data into parallel outputs. As mentioned in Section 2, we have demonstrated ultra-high speed mux and demux circuits for this application. The 20 GSps voltage comparator can serve as the decision circuit to distinguish data 1's from 0's. In addition, we have realized an 11 Gb/s HBT laser driver that can modulate more than 50 mA of AC current into a 50 ohm load [6]. For the receiver side, a D C coupled, differential transimpedance amplifier has been demonstrated [12]. We have also realized DC coupled amplifiers of 10-dB gain and 14 GHz bandwidth. An HBT phase detector for clock recovery operated at 5 GHz. We are now developing complete clock recovery circuits for 2.5 and 10 Gb/s operation. These building blocks will be integrated monolithically into transmitter and receiver circuits, and in 4- to 8-channel arrays, for various fiber optic applications.

Pseudo-random bit generators (PRBS) are used for scrambling and descrambling data and for testing communication modules (as part of a bit-error-rate detector). They can also be used in pseudo-random code modulated laser altimeters for NASA [13]. We have realized an HBT PRBS (with a 15-stage shift register) and tested it up to 5.3 GHz, as shown in Fig. 13.

For wireless communication, power HBTs implemented with thebaseline technology have

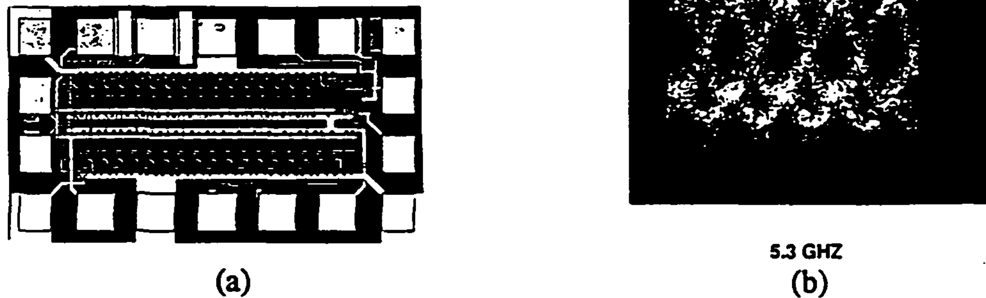


Figure 13: (a) Microphotograph of a fabricated HBT PRBS. (b) Output eye patterns at 1 and 5.3 GHz.

shown > 60% of power added efficiency at 825-850 MHz. High performance HBT mixers were realized. We are developing an HBT based DDS (direct digital synthesizer) for I and Q demodulation. The DDS includes a DAC (digital to analog converter), an accumulator, and a ROM for sine/cosine look-up table. In addition, we are designing high-resolution sigma-delta ADCs with high speed HBT modulators. These ADCs are aimed at 12- to 14-bit 100 MSps for digital radios.

6 Development of Advanced Technologies Involving HBTs

HBT technologies with material systems other than GaAs are being developed at many research laboratories. InP based HBTs and integrated circuits have been demonstrated [14-16]. The technology offers low power, high speed, and OEIC compatibility with 1.3 and 1.55μm lights. It does not have good Schottky diodes, however. The breakdown voltages of simple single-heterojunction transistors with InGaAs collectors are low, compared with those of GaAs HBTs. High-performance Si/Ge HBTs have also been realized, with ft's up to 75 GHz [17]. Si/Ge HBT technology allows use of many established techniques of Si transistor technologies. It suffers, however, because of conductive Si substrate. This leads to finite collector to substrate capacitance and prohibits integration of analog, digital, and microwave circuits. Other III-V HBTs being investigated include GaInP/GaAs HBTs (for wider bandgap and less DX problems than AlGaAs), InAs and GaSb based HBTs (for low power), and GaP/AlGaP HBTs (for high temperature electronics).

Monolithic integration of III-V HBTs with field-effect transistors (FETs) are being pursued. FETs extend the capability of HBTs by providing high input impedance, low noise, active loads, and current sources and sinks. A simple manufacturable process of GaAs HBT and MESFET process has been proposed by a UCSD/Rockwell collaboration team [18]. High performance MESFETs (with 300 mS/mm transconductance, 11.5 GHz f_t, and 16 GHz f_{max}) have been demonstrated on the baseline HBT material. Integration of GaAs HBTs and HEMTs are being developed at Rockwell, supported by Air Force Wright Laboratory. This development involves regrowth of HEMT layers on HBT wafers, followed by

etching away HEMT layers from areas devoted to HBT. SPICE simulations predict that sub-0.5 ns 1K SRAMs and 7-bit 4-GSps sample-and-hold circuits can be implemented with this technology. Monolithic optoelectronic receiver circuits have been fabricated with the baseline HBT technology [19]. The base-collector junction of HBT layers was used for the photodetector. The OEICs have measured bandwidths as high as 13 GHz for optical signals in the $0.8\mu m$ band. This implies suitability for 17 Gb/s digital transmission with a -12 dBm sensitivity for 10^{-9} bit error rate. Furthermore, Rockwell has also demonstrated integration of complementary Pnp and Npn HBTs, under an ARO contract [20]. The Pnp transistors exhibit f_t = 20 GHz and f_{max} = 19 GHz. Gain blocks implemented with the Pnp HBTs showed a gain of 8 dB and a 3 dB bandwidth of 6 GHz.

A Rockwell/Lincoln Laboratory/UCSD collaboration team has proposed integration of resonant tunneling diodes (RTDs) and HBTs [21]. A schematic cross section of the integrated RTD/HBT technology is shown in Fig. 14. RTD layers will be grown on top of HBT layers, and RTDs will be fabricated in series with HBTs. RTD/HBT integration achieves several objectives. When RTDs are integrated on the emitter side of HBTs, circuits with high functional density can be obtained, similar to that of RHETs-resonant tunneling hot electron transistors [22]. Active device counts can be reduced by about a factor of four for same logic functions. RTDs can be integrated on the collector sides of HBTs as loads with differential negative resistance (NDR) to realize circuits of minimum static power consumption. Power reduction of about a factor of three is achievable. The high density and low power features can be combined on the same circuits. We have experimentally verified the operation of a basic RTD/HBT gate with a discrete RTD and a discrete HBT packaged together. Subnanosecond operation of RTD/HBT circuits has been demonstrated with SPICE simulations.

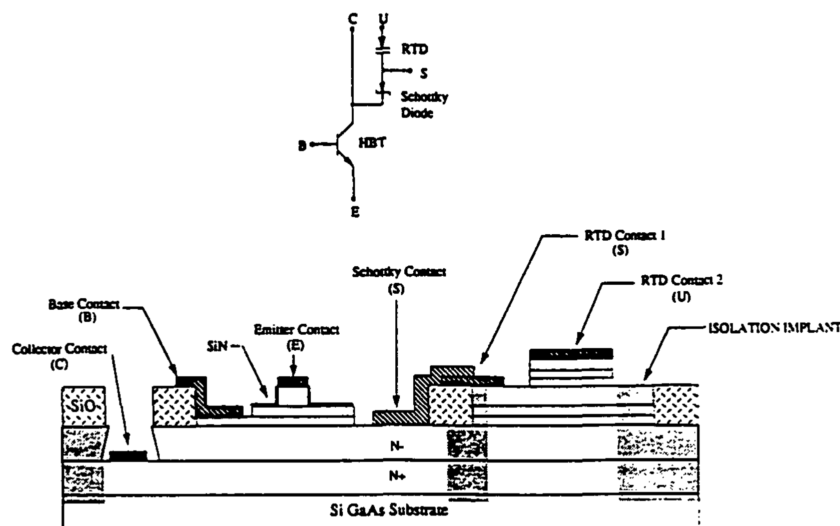


Figure 14: Schematic cross section of integrated RTD/HBT technology

7 Summary

Rockwell has established a manufacturable AlGaAs/GaAs HBT technology in a production facility. The technology features emitter-up single heterojunction Npn transistors with integrated Schottky diodes, NiCr resistors, MIM capacitors, and three levels of metal interconnect. The HBT has a current gain of about 100, and f_t and f_{max} of about 55 GHz. Rockwell has announced initial HBT products based on this technology.

In this paper, we have described a 1.5 GSps 8-bit data acquisition system. The system contains an HBT ADC, an HBT clock driver, 16 HMESFET 1K FIFO memory chips, and Si interface ICs. The GaAs circuits are in fabrication. The system will be assembled on a printed circuit board, with DMA interface to a personal computer. We have presented advanced packaging ideas for reduction in size and power, and for improved performance. Ultra-high performance HBT circuits for lightwave and wireless communications have been demonstrated or are being developed. Integration of these building block circuits into transceiver modules and arrays is being pursued. HBT related technologies being developed at Rockwell and its collaborating institutes include InP based HBTs, GaAs HBT/FET integration, OEICs, and RTD/HBT integration. With successful realization of these technologies, we will be able to support many system innovations and improvements for NASA.

8 Acknowledgments

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