# Analog/Digital pH Meter System I.C.

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*Abstract* - **The project utilizes design automation software tools to design, simulate and fabricate a pH meter I.C. system including a successive approximation type seven-bit analog to digital converter circuits using a $1.25\mu m$ N-Well CMOS MOSIS process. The input voltage ranges from 0.5V to 1.0V derived from a special type pH sensor and the output is a three-digit decimal number display of pH with one decimal point.**

## 1 Introduction

The recent availability of automated integrated circuit design software tools and the dramatic increases in the hardware tool performances make it feasible to design a VLSI circuits and systems on a personal computer. Also the unavailability of a commercial, small, inexpensive digital and single chip-electronic pH measuring system prompted authors to make use of these tools for creating a pencil-size pH measuring system. Since Tanner tools provided only digital cell libraries and no extensive analog cell libraries at present, additional libraries cells were created. Also other integrated circuit design tools were added to complete the system design on a personal computer.

## 2 System Operation and Features

A sensor which outputs a linear voltage proportional to pH value drives an analog input to the device. When a user depresses the "sample" momentary switch (see Figure 3), then the system displays a pH value between 1.1 and 13.8. The device is powered by a 3 volt battery. An internal timing is used to start and stop the system clock to conserve battery life. The device is intended to be used with three seven-segment displays. A seven-bit conversion was chosen, because the number of increments of tenths (131 step3). Since solutions with pHs at the extreme ends of the range are fairly exotic, the range of displays was set at between 1.1 and 13.8. These values are attained by adding a value of 11 to a seven-bit digital representation of the linear input analog voltage.

### 2.1 Successive Approximation

This method was chosen for it's simplicity of implementation (Figure 4). The seven-bit register holds an approximation of the input analog voltage. The approximation takes place in

seven clock cycles, one for each bit.

A seven-bit shift register, one bit for each of the approximation bits, controls the approximation. Approximation takes place one bit at a time, beginning with the most significant bit (msb). All of the control register bits are set to zero, except the bit that is currently being sampled. In effect a "1" is shifted through a field of zeros in the control register. The "1" enables loading of a mux-flipflop for the bit of the approximation register being sampled. The sampled bit of the register is set to a "1", and the output of the register is fed to an analog comparator via a D/A converter. If the approximation value is less than the input value, then that bit of the register is left at a "1." If making the sample bit a "1" causes the approximation to exceed the value of the input voltage, then that bit is set to a "0." Sampling begins at the msb and proceeds "SUCCESSIVELY" to the least significant bit (lsb).

## 2.2 D/A Conversion

A straight voltage divider resistors requires $2^n$ resistors for n-bits. A capacitor-based (charge scaling) approach requires capacitors which increase in area exponentially, both of the above methods were not chosen because of their large chip size [1].

A voltage-scaling R-2-R ladder method (Figure 5) was selected [2] because of it's simplicity and good area utilization. With the R-2-R ladder, 2n resistors are required for an n-bit conversion. The output voltage accuracy depends on the accuracy of the resistances and the ratio of the "2R" resistor values to the "R" resistor values. The ratio can be improved in layout by orientating the "R" and "2R" resistors in the same direction so that processing variations will track between them, and the effects on their resistance ratio can be minimized.

N-Well (R=2, 4KOhm/Square) is used for the resistors. Resistance Values of 30K ohms and 60K ohms are used.

## 2.3 Reference Voltages

The output of the R-2-R ladder is from 0.5 to 1 volt. For this work, the bottom of the ladder must be referenced at 0.5 volts. The input to the ladder must be referenced to 0.5 volts for a logic "0" and 1.0 volts for a logic "1" (Figure 5). Diodes are used here as voltage references with a current limiting MOS transistor controlled by an external voltage for this device. This approach is used, because of the single 3 volt power source and the closeness of the reference to the threshold voltage for this technology.

## 2.4 Analog Comparator

A two-stage comparator (Figure 6) comprising a differential stage and an inverting stage was selected. The poor gain of the differential stage is augmented by the inverting stage and problems controlling the trip point of the "current-sink" inverter stage are reduced by the differential stage [3].

## 2.5 Digital Decoding and Display Logic

As mentioned previously, the decoding was somewhat simplified over a pure 7-bit-binary-to-bcd decoder, by adding a decimal value of 11 to the output of the approximation register, and then converting that binary value to bcd. The bcd conversion method is that of a standard 74HC185 [4]. The BCD-to-7-segment decoder/drivers are derived from equation generated using Altera's Maxplus EPLD synthesis tool driven by a tabular ASCII input. Tabular input implementations of the binary-to-BCD decoding were also made, but proved to be much less area-efficient than the 74HC185 method. Self test is centered around signature generation and the output of a "go-no-go" indication. Self testing is initiated by setting an external test-node signal active. In the self test mode (Figure 7), the analog circuit feedback to the approximation register is tapped out and driven off-chip. A digital comparator is connected in its place, with the difference that the test now becomes greater than or equal to, instead of greater than. An on-chip counter, driven by the clock generator circuit provides exhaustive inputs to the approximation register. The decoded display outputs are compressed into a signature register, and a "go-no-go" indicator is set based on hard-wired comparison to the known good signature.

# 3 Simulation and Design Tools

This design required an IBM PC with at least 4 Mb of RAM. The design files all fit onto a 1.44 Mb floppy diskette. OrCAD was used for schematic entry. An OrCAD library was replaced by that of Tanner Research. This library includes ASCII "macro" files describing ports on the physical cell designs for the MOSIS library parts in order to tie the library into the place-and-route tool. Also it has a collection of macros for the logic simulator, GateSim.

OrCAD's annotation utility is used to flatten the design, annotate the cell references (instance numbers) and generate a flattened OrCAD wirelist. Two passes are made with the annotator. The first pass, with a switch on, causes edits to the schematic files, changing all the "reference" designators. Values for multiple instances of a work sheet are accounted for in the renumbering of references. The second pass, with difference switches on, flatten the design, elaborates references for the multiply instantiated sheets and generates a flattened wirelist. Tanner's netlist tool, NetTran, is run next, again in a two-pass process.

The first pass translates the wirelist to a silos format which includes the entire cell library of MOSIS cell macros. The second pass prunes the unused cell macros form the netlist.

## 3.1 Logic Simulation

Simulation was based on cell/primitive. The top-level of the design contained 407 schematic components (about 1250 two-input gate equivalents). The top-level functional simulation of all 128 input steps ran in 1 minute to 2 minutes on a 486/PC clone with "limitless" memory. The simulation comprised a "test-bench", where the digital portion of the chip was instantiated, which was connected to a counter and a comparator. The digital successive approximation register outputs were run into the digital comparator, whose output was fed back to the digital portion of the chip. Therefore, the test patterns for the chip consisted of a reset pulse for the counter and clear pulse for the chip.

## 3.2 Static Timing Verification

GateSim includes a static timing verification routine where a delay window must be specified for the verifier reports on all paths within the window. No delays above 200 ns were found. Since the target speed is more a function of the very slow R2R ladder, whose response time is in ms, timing in the digital logic did not give a problem.

## 3.3 Analog Simulation

Hand designs were done for the analog circuits and manually entered as netlist for P-SPICE. Based on these approximations, analog cells were laid out. Parametric information from the layout is then extracted using L-Edit. P-SPICE simulations were based on parametric from the actual layout.

## 3.4 Mixed Signal Simulation

A P-SPICE netlist is generated from the combined analog and digital schematics. P-SPICE digital primitives are used for the digital cells. Extracted parametric from analog cells are used for the analog devices.

## 3.5 Auto Place and Route

The Place-and-Route tool run off on a Tanner "tpr" netlist, translated from OrCAD wirelist. The Place-and-Route is a two step operation. In the first step, the interior core of the chip is routed using the standard cells from the cell library. In the second step, the pads are routed. The tool provides annealing algorithm also in order to optimize the chip area. The core placement and routing took about 2 hours an a 486/PC clone with 32 Mb of RAM.

### 3.6 Design Rule Check

DRC is built into the L-Edit. The MOSIS library from which the chip is built from contains the design rule for the process. This tool is run because the analog and wiring portions are added.

### 3.7 Layout vs Schematic Capture

As a verification of layout, LVS was used and compared SPICE files.

### 3.8 Fault Grading

GateSim contains a fault-grading utility. Fault detection is based on user-provided non-faulted simulation results.

## 4 Summary

The I.C. comprises a seven-bit successive approximation register, seven-bit digital-to-analog converter (R2R) ladder, an analog comparator and digital logic for display decoding and driving. The successive approximation register is clocked by an on-chip oscillator at a reasonably slow speed.

The chip is intended to be operated at 3 Vdc. The Ph reading is made by depressing a momentary "sample" button. This causes a reset pulse to the chip, which in turn will start the on-chip clock oscillator until the next sampling, the chip will shut off its clock oscillator until the next sampling is initiated by the user.

The I.C. design methodology includes the use of schematic capture, logic simulation, auto-placement-and-routing and layout-vs-schematic verification. Both the high-level and low-level simulations were performed. The fault grading and built-in self-test circuitry are included. Tanner Research's GateSim is used for the logic simulation and OrCAD is used for schematic capture. Tanner netlister and OrCAD library link the two different tools. The additional manual creations of the insufficient device library parts to the Tanner's cell library was added. The P-SPICE program was also merged with other software tools. The layout verification was performed using Tanners LVS tool.

## References

[1] Phillip Allen and Douglas Holberg, "CMOS Analog Circuit Design," Holt, Reinhart and Winston, Inc.

[2] Private communication.

[3] Phillip Allen and Douglas Holberg, "CMOS Analog Circuit Design," Holt, Reinhart and Winston, Inc., "Two-Stage Comparator," pp 333-349, 1987.

[4] HCMOS data book.

- Synopsis/general description of design and methodology
- Circuit description, block diagram, hierarchy partitioning
- Simulation
- Custom design
- Layout, parasitic extraction, back annotation

Figure 1: Outline of Presentation

- 1.25 um N-Well Cmos
- 7-bit Successive Approximation Register
- D/A Converter
- Analog Comparator
- Input Voltage from Sensor (0.5v to 1v)
- 3V Battery Powered
- Digital Decoding - Display of pH from 1.1 to 13.8
- Built-in Self Test

Figure 2: Design Features

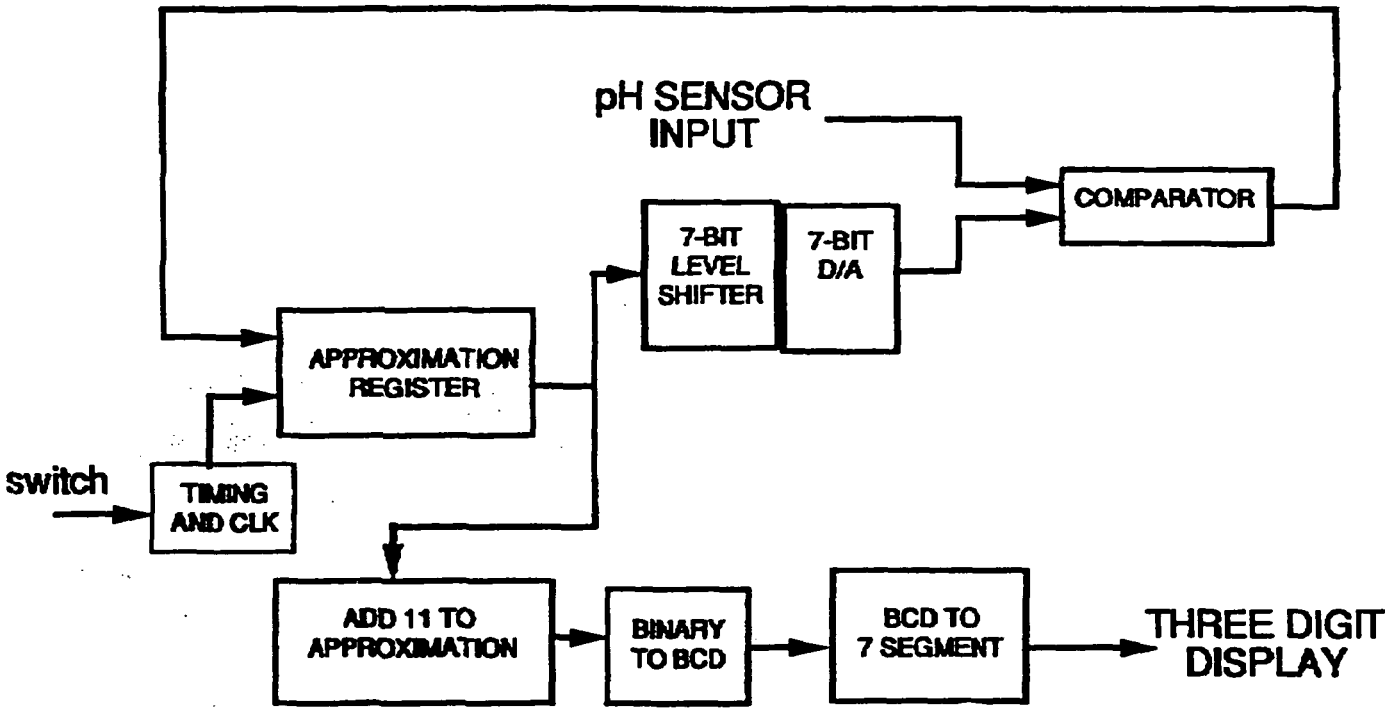


Figure 3: Block Diagram

```
approximation := 0;
approximation_temp := 0;

for n in 6 downto 0 loop
 approximation_temp := (approximation +2^n);
 if          (approximation_temp < analog_voltage)
             then approximation := approximation_temp;
end loop;
```

Figure 4: Successive Approximation

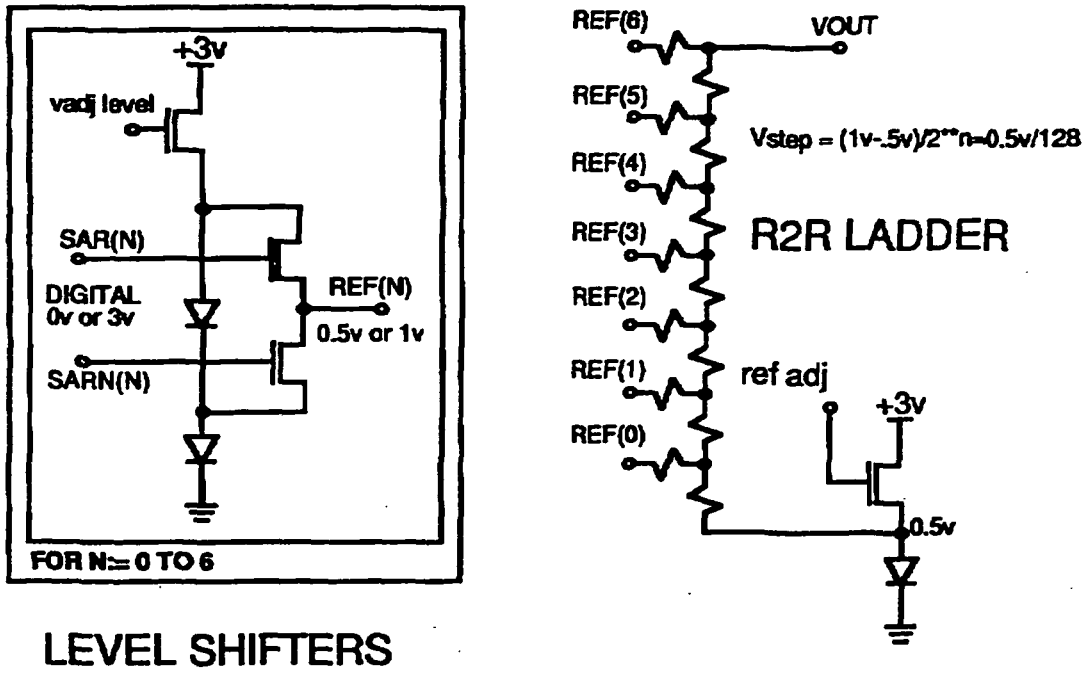


Figure 5: A/D Converter

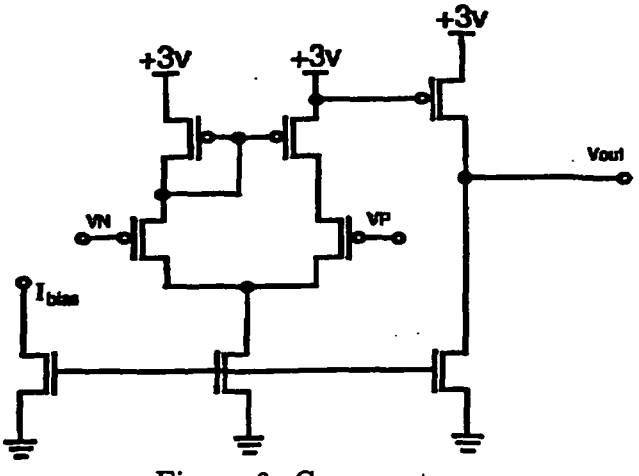


Figure 6: Comparator

schematic capture → logic simulation / analog simulation → place and route → layout vs schematic → mask data generation

Figure 7: CAE Flow

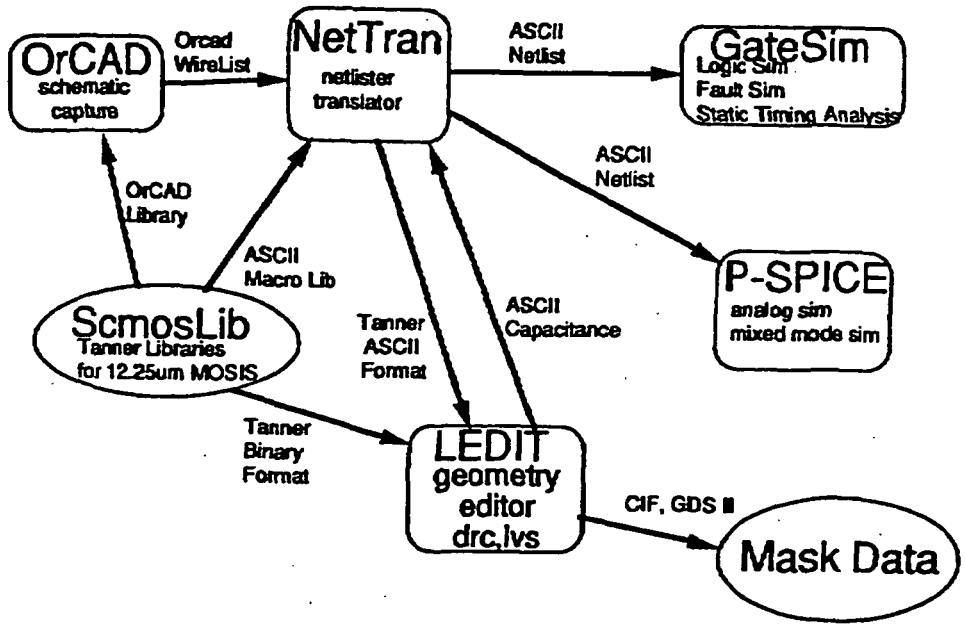


Figure 8: CAE Data Generation

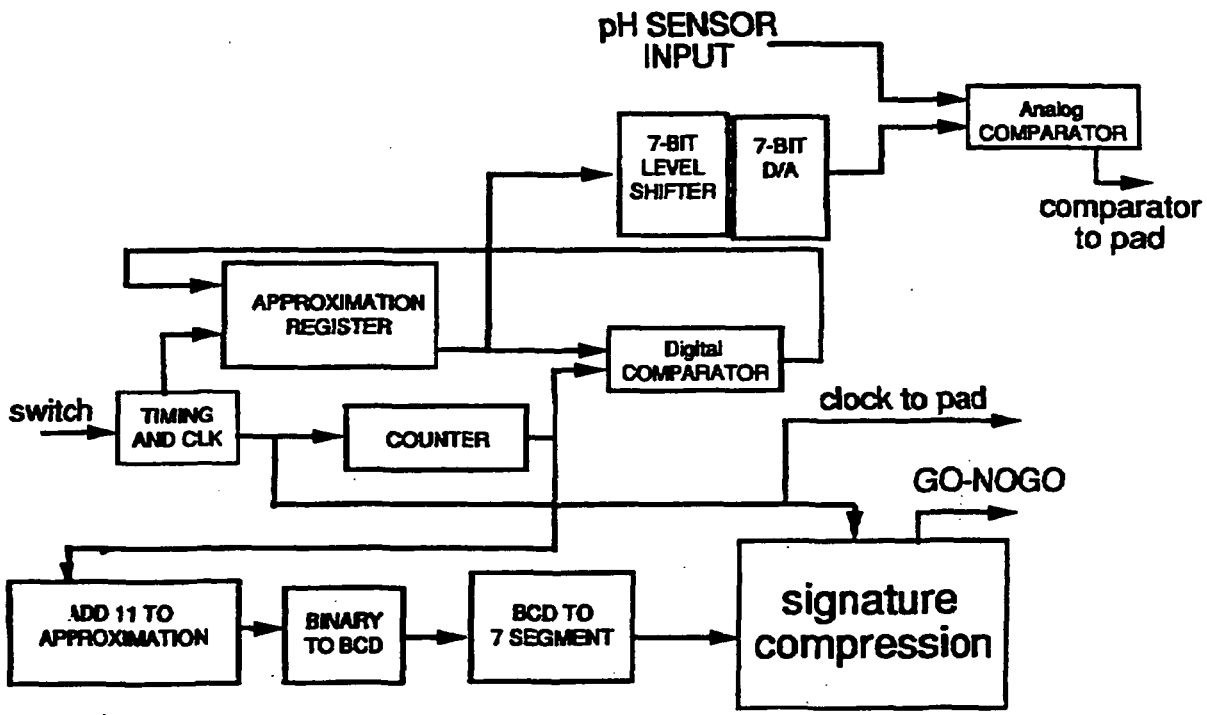


Figure 9: Built-In Self Test

- Analog symbols hand-made for OrCAD (LIBEDIT)
- "macro" definition (Tanner ascii format) for NetTran
- L-Edit cell created to match i/o port definition
- Capacitance information added to macro definition

Figure 10: Gluing the Analog Parts into NetTran/L-Edit

- OrCAD annotation two passes
  - 1st pass updates schematic references
  - 2nd pass generates annotation file
- OrCAD cleanup graphical rule checking
- OrCAD erc - electrical rule checking
- OrCAD Annotator (run twice ... explain details) – question - is this step superfluous?
- Tanner NetTran (run twice ... 2nd time to prune macros)

Figure 11: Net List Generation