An 18 Bit 50 kHz ADC for Low Earth Orbit

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Abstract - **A fourth order incremental analog to digital converter (ADC) is proposed which performs 18 bit conversions at a 50 kHz rate on sampled and held data. A new self calibration scheme is presented which eases the matching requirements of capacitors, and the performance of the operational amplifiers in the ADC by changing coefficients in the digital postprocessing.**

1 Introduction

Dynamic range in charge coupled device (CCD) image sensors is measured by the maximum number of electrons in a well divided by the minimum number of usable electrons in the well. This dynamic range can be as high as 18 bits for today's CCD detectors, where each increment corresponds to two electrons. The analog outputs of the CCD detector must be converted to digital words before they can be manipulated by a microprocessor, or stored in memory. With a readout rate of 50,000 pixels per second, CCD sensors are pushing the limits of analog to digital converter (ADC) performance.

Using voltage division techniques such as R-2R ladders or charge redistribution capacitor arrays to build an 18 bit ADC would require component matching on the order of 4ppm to get good linearity. The best matching achievable on a silicon chip without expensive trimming is about 1000ppm. Sophisticated techniques are clearly needed to fabricate an 18 bit ADC on a silicon chip, without increasing the complexity of the semiconductor processing.

Satellite applications impose the additional requirement that an ADC perform properly when exposed to the radiation in space. Proton radiation found in low earth orbits may cause an ADC chip to latch up or loose data due to single event upsets. Radiation can also generate noise [1, 2] in analog circuits which must be filtered out, or compensated for. This paper proposes an architecture for a 18 bit, 50kHz (ADC) for low earth orbit.

2 Architecture

Self calibrating, oversampling, and integrating techniques are effective ways to overcome basic process limitations to get high resolution. These techniques are reviewed here to determine which one will most likely meet the speed requirements, and reject noise caused by proton radiation.

Charge redistribution successive approximation ADC's can achieve 18 bit resolution at 50kHz when self calibration techniques are used to overcome the matching problems of on chip capacitors [3, 4]. The combination of resolution and speed is achieved by performing one comparison per bit (for an 18 bit conversion, the comparator must settle 18 times). While this leads to good conversion speed, there is no inherent rejection of noise in the ADC. A

noise spike caused by the arrival of an energetic proton could lead to an erroneous value for one of the more significant bits, which would lead to a large error in the final answer. The remaining conversion cycles can not change a bit which has been corrupted by noise. Algorithmic [5], and pipelined [6] ADC's are also one comparison per bit architectures, and will be plagued by the same noise rejection problem. A redundant ADC [7] could overcome this problem, but the self calibration routine becomes more complex. The redundancy adds to the conversion time, while decreasing the importance of each individual comparison in the final answer.

Integrating ADC's such as dual slope ADC's exhibit excellent linearity and rejection of noise added to the input signal, and can have very high resolution [8, 9]. Noise on the input is integrated along with the desired signal, so only the average value of the noise, which is usually zero, corrupts the accuracy. The main disadvantage of integrating ADC's is the notoriously slow conversion rate. One analog to digital conversion consumes 2^n comparison cycles, so to perform an 18 bit analog to digital conversion at a 50kHz rate would require a 13GHz comparator clock rate. This fast comparator would be required to compare signals whose difference is only about $20\mu V$. This is clearly beyond the capability of inexpensive integrated circuit technologies.

The most popular oversampled data conversion technique in use today is the delta sigma ADC [10]. Delta sigma ADC's convert an analog input into a pulse density modulated signal at a frequency well above the Nyquist rate, then smooth the modulated signal with a digital low pass filter. The pulse density modulated signal is viewed as the original signal plus quantization noise. The digital filter gets rid of the quantization noise, and any other noise on the input which is outside the bandwidth of the ADC. Delta sigma ADC's work well on continuous signals such as voice or music, but are not intended for multiplexed sampled and held data [11]. A charge coupled device (CCD) image detector is one example where an ADC is multiplexed between a large number of pixels.

The incremental ADC [11, 12] is also an oversampled ADC, but it is intended for sampled and held data, which makes it better suited for multiplexed inputs. Like the delta sigma ADC, the incremental ADC also uses a large number of input samples to get high resolution, but the signal processing is done on a sample by sample basis instead of on a continuous data stream. Noise on the input is averaged, and noise which causes a bad comparison can be corrected by later cycles. A fourth order incremental ADC with an internal sample rate of 4.25 MHz, and an external data rate of 50 kHz was chosen for its high accuracy, moderate speed, and rejection of noise.

3 First Order Incremental ADC

The incremental ADC is really a switched capacitor version of the charge balance ADC [13, 14]. The operation of a first order and second order incremental ADC are described in detail in [11, 12]. The operation of the first order incremental ADC, shown in Figure 1 is summarized here. The timing of the switch control signals, shown in Figure 2, is slightly different than that used in [11, 12] to help speed up the conversion rate. The ADC starts in the reset mode, where the integrating capacitor $C2$ is discharged, and the digital counter on the output of the comparator is set to zero. The phase 1 switches are then closed,

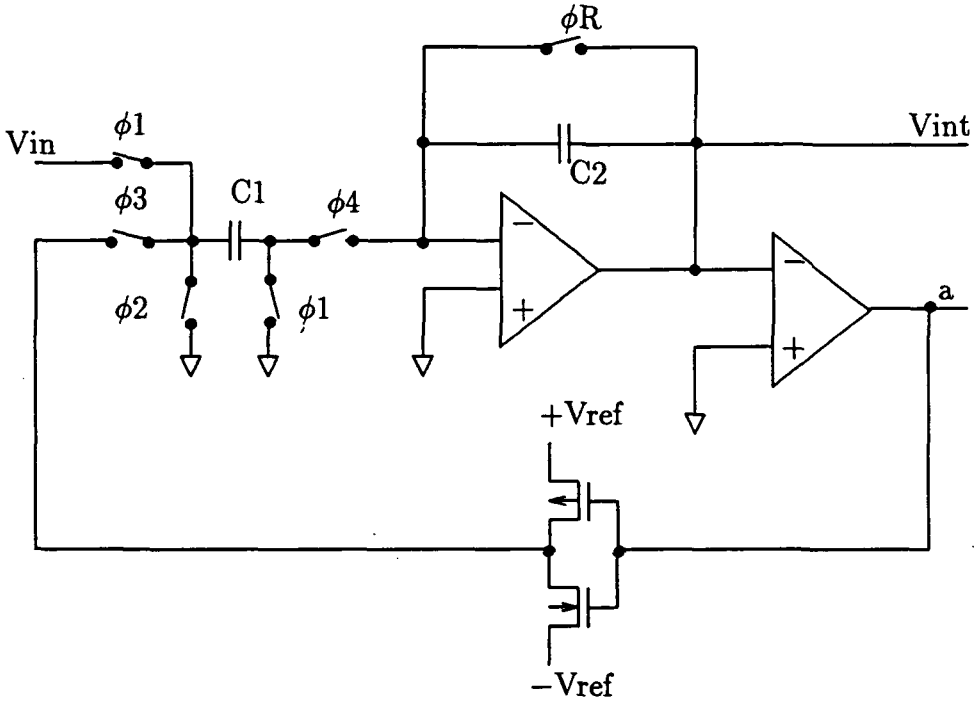

Figure 1: First Order Modulator

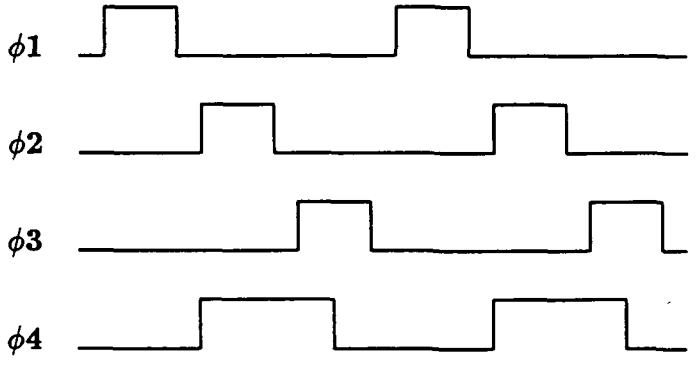

Figure 2: Switch Control Signal Timing

and V_{in} is sampled on $C1$. The phase 1 switches open, then the phase 2 and phase 4 switches close, transferring the charge $-V_{in}C1$ to the $C2$. The output of the integrator is now $V_{int} = V_{in}C1/C2$. Next the phase 2 switch opens, and the comparator is strobed. If $V_{in} > 0$, then the output of the comparator is a logic 0, and $+V_{ref}$ is applied to the input of the phase 3 switch. The phase 3 switch then closes (the phase 4 switch is also still closed) which transfers either $+V_{ref}C1$ or $-V_{ref}C1$ on $C2$, depending on the output of the comparator. If $V_{in} > 0$, the new integrator output is $V_{int} = (V_{in} - V_{ref})C1/C2$, while if $V_{in} < 0$, $V_{int} = (V_{in} + V_{ref})C1/C2$. A gated counter increments if the output of the comparator is a zero. This cycle repeats n times with the same input voltage, until the output of the integrator is given by equation 1 [12].

$$V_{int} = \alpha(nV_{in} - V_{ref}\sum_{i=1}^{n} a_i) \tag{1}$$

where α is the integrator gain ($C1/C2$), and a_i are the individual comparator outputs which have the values $+1$, or -1. Solving for the ratio of the input voltage to the reference voltage yields:

$$\frac{V_{in}}{V_{ref}} = \frac{V_{int}}{n\alpha V_{ref}} + \frac{1}{n}\sum_{i=1}^{n} a_i \tag{2}$$

We can interpret equation 2 to be the average of the comparator outputs, plus a residue. Setting $\alpha = \frac{1}{2}$ allows $V_{in}max = V_{ref} = V_{sw}$ where V_{sw} is the maximum signal swing allowed by the opamp. With $\alpha = \frac{1}{2}$, the maximum possible value of V_{int} is $V_{ref}/2$, so the maximum residue is $1/n$. Therefore, to get n bits of resolution, 2^n integration/comparison cycles are required, which means this technique is as slow as an integrating ADC.

Noise added to the input will be integrated along with the signal, so like the integrating ADC, only the average value of the noise will affect the ADC output. Unlike the integrating ADC, noise at the input of the comparator will not significantly affect the incremental ADC accuracy. If a noise spike causes the comparator in an incremental ADC to output an erroneous value, both the integrator (through the feedback path) and the digital counter will record this bad value. The output of the integrator is now very large, so on the next cycle, the comparator will output a value which compensates for the previous error.

4 Fourth Order Incremental ADC

A higher order integration of the input signal and feedback data can be achieved by cascading the first order modulators as shown in Figure 3 [11].

After n cycles, the voltage on the output of the fourth integrator is:

$$\begin{aligned} V_{int4} = \alpha_4(\alpha_3(\alpha_2(\alpha_1(&\frac{V_{in}(n-3)(n-2)(n-1)n}{6} - V_{ref}\sum_{i=1}^{n-3} a_i\frac{(n-i)(n-i-1)(n-i-2)}{6}) \\ &- V_{ref}\sum_{i=2}^{n-2} b_i\frac{(n-i)(n-i-1)}{2}) - V_{ref}\sum_{i=3}^{n-1} c_i(n-i)) - V_{ref}\sum_{i=4}^{n} d_i) \end{aligned} \tag{3}$$

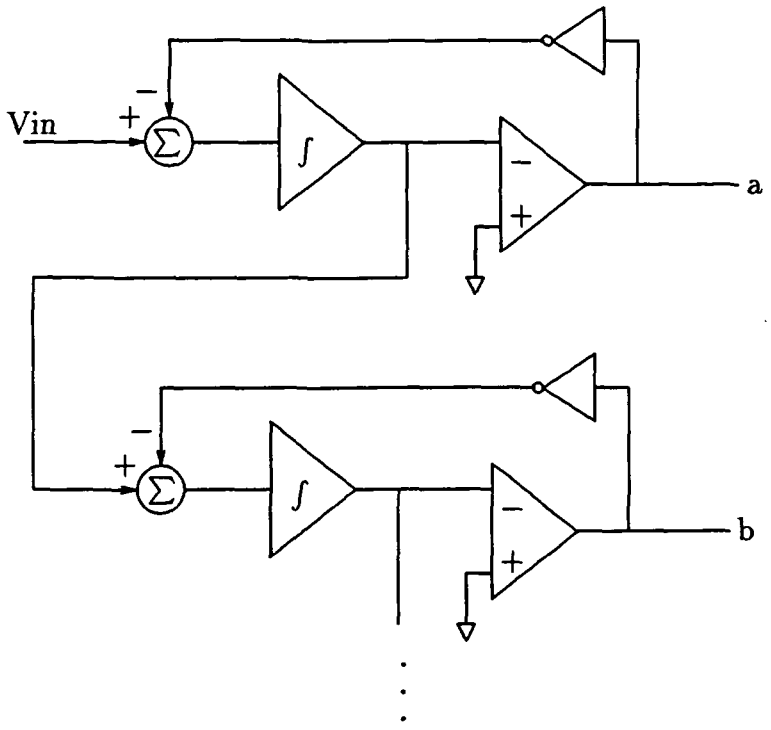

Figure 3: Cascade of First Order Modulators

The indices on the summations in equation 3 are skewed because there is a delay of one clock period in each of the integrators. The gain of the m^{th} integrator is α_m, a_i are the outputs of the first comparator, b_i the outputs of the second comparator, and so on. This equation can be solved for V_{in}/V_{ref}:

$$\begin{aligned}\frac{V_{in}}{V_{ref}} = & \frac{24}{(n-3)(n-2)(n-1)n}\sum_{i=4}^{n}(a_{i-3}\frac{(n-i+3)(n-i+2)(n-i+1)}{6} \\ & +\frac{b_{i-2}}{\alpha_1}\frac{(n-i+2)(n-i+1)}{2}+\frac{c_{i-1}}{\alpha_1\alpha_2}(n-i+1)+\frac{d_i}{\alpha_1\alpha_2\alpha_3}) \\ & +\frac{24V_{int}}{\alpha_1\alpha_2\alpha_3\alpha_4(n-3)(n-2)(n-1)nV_{ref}}\end{aligned} \quad (4)$$

The last term of equation 4 can again be considered to be a residue, which is not accounted for by the digital outputs, the smaller the residue, the higher the resolution. The decrease of the residue as n increases is now on the order of n^{-4}, which explains why the fourth order ADC is so much faster than the first order ADC. The decoder however, is more complex for the fourth order modulator than for the first order circuit. The outputs of the comparators now must be multiplied by a polynomial $f(i)$, where i increments with each clock cycle. We can interpret this to mean that the first digital outputs are to be weighted more heavily in the answer than the later ones. We can also see that the outputs of the first modulator are weighted more heavily than the outputs of the later modulators. If we have noise in the system, errors at the first part of the conversion cycle will affect the accuracy more than errors in the later part of the conversion cycle. Errors which are caused by single event

upsets of the data stored from the outputs of the comparators, and errors in the charge in the integrating capacitors can not be corrected.

5 Digital Processing and Self Calibration

The fourth order incremental ADC offers good trade offs between speed, accuracy, and noise rejection, but unfortunately gain errors in the integrators will cause nonlinearities in the ADC transfer function. The gain errors are caused by capacitor mismatch, and finite gain and bandwidth of the opamps. There are circuit techniques which correct the nonideal behavior of opamps and capacitor arrays, but in this case, the integrator gains do not need to be any particular value for the ADC to function properly, as long as the output processor knows exactly what the gain of each integrator is. It is usually preferable to increase the complexity of digital circuitry instead of analog circuitry, so I have chosen to calibrate this ADC by changing coefficients in the digital decoding logic to match the analog gain, instead of trying to set the gain of the analog integrators to exactly $\frac{1}{2}$. The digital decoding logic is shown in Figure 4.

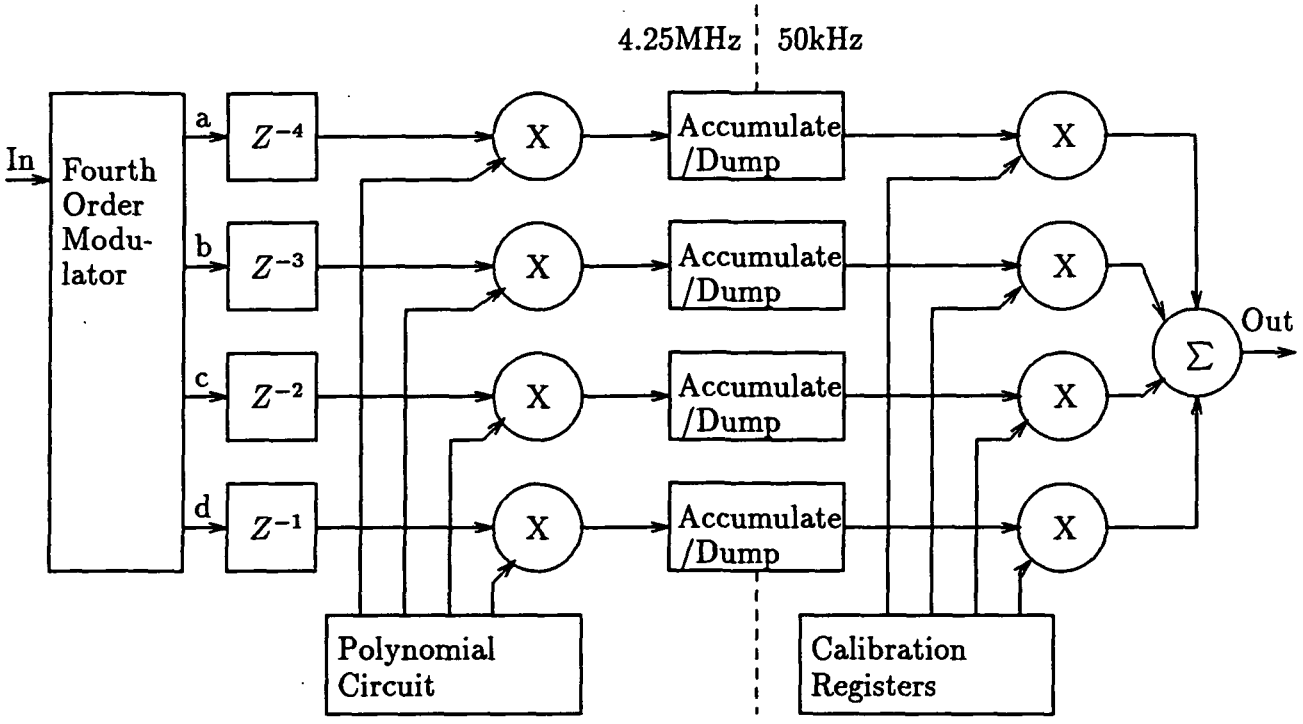

Figure 4: Decode and Calibration Logic

The z^{-x} blocks are delay lines which resynchronize the time shifted comparator outputs in equation 4. The polynomial circuit generates the terms $(n-i+3)(n-i+2)(n-i+1)$, $(n-i+2)(n-i+1)$, and $(n-i+1)$ where i is incremented each clock cycle. The finite differences technique is used to generate these terms, so no multiplications are necessary, which greatly simplifies the hardware. The multipliers of the delayed comparator data are

simply AND gates since the comparator outputs are only one bit wide. The accumulate and dump circuitry is reset when the integrators are reset and a new input sample is acquired. The sample rate of the signals coming into the accumulate and dump circuits is $n \times f_{reset}$ where f_{reset} is the input and output data rate of the overall ADC, and n is the number of comparison/integration cycles per input sample. The calibration registers store the exact values of integrator gains (α_m). The calibration registers are set during a self calibration routine, where inputs are applied which switch from $-V_{ref}$ to $+V_{ref}$ or from $-V_{ref}$ to $+V_{ref}$ part way through the conversion. These inputs precisely emulate input voltages without actually generating calibration voltages which must be accurate to 18 or more bits. An optimization routine then searches for the gains which make the combined errors of all the inputs a minimum, and stores these values in the calibration registers. Self calibration should be performed periodically to compensate for gain temperature coefficients, and component drift. The area of the self calibration circuitry can be made small by multiplexing the multipliers, since the circuitry after the accumulate and dump circuits runs at 50kHz.

6 Modulator Circuit

The modulator circuit in Figure 1 will be fabricated as a fully differential circuit to improve power supply rejection, cancel odd order capacitor nonlinearities, and increase signal to noise ratios. The phase 4 switch is turned off after the phase 3 switch to make the charge injection independent of which reference voltage is selected. The charge injection is then a common mode voltage which is rejected by the differential opamp [15]. Likewise, the phase 1 switch connected to ground is turned off before the phase 1 switch to V_{in}. Class A-B opamps [16], shown in Figure 5, are used to avoid nonlinear settling caused by slew rate limiting, and to reduce power consumption. The common mode feedback circuit for the opamp, Figure 6, provides continuous feedback through capacitors which are periodically zeroed to compensate for leakage.

The comparator, Figure 7, relies on positive feedback [18] to make a quick decision. The differential pair and input current mirrors isolate the integrator outputs from the switching noise in the later stages of the comparator. All circuits were simulated on Hspice [17], using the optimizer to help fine tune the transistor sizes.

7 Results

The number of integration/comparison cycles was chosen to be 85, which makes the sample rate 4.25MHz when the data rate is 50kHz. Simulations show that the fourth order incremental ADC is able to reject noise on it's input of $200\mu V_{rms}$, and noise at the comparator input of $20mV_{rms}$. A test chip will be fabricated to evaluate the feasibility of the self calibration scheme, as well as ADC performance in proton radiation. Test chip layout is in progress.

2.5.8

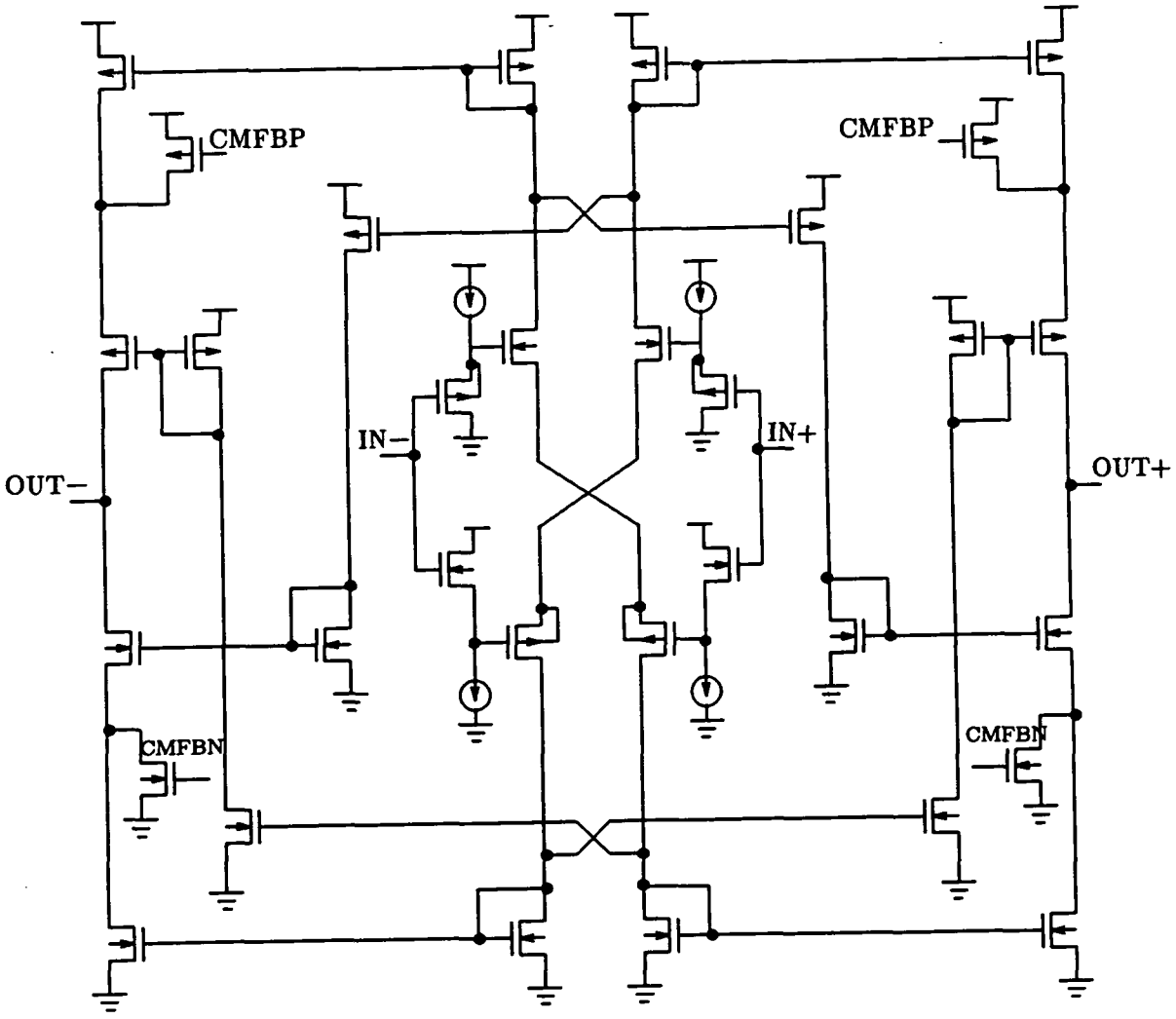

Figure 5: Class A-B Opamp

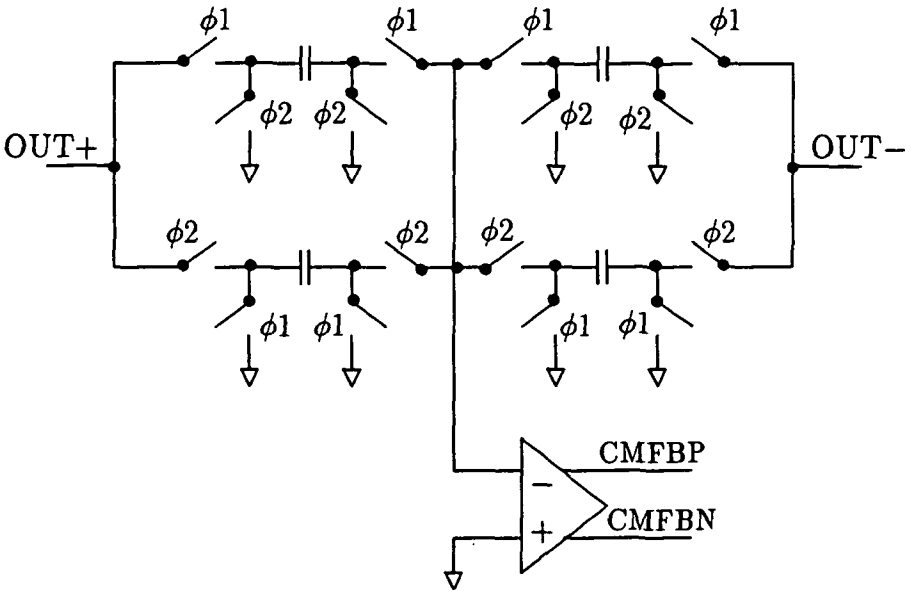

Figure 6: Common Mode Feedback Circuit

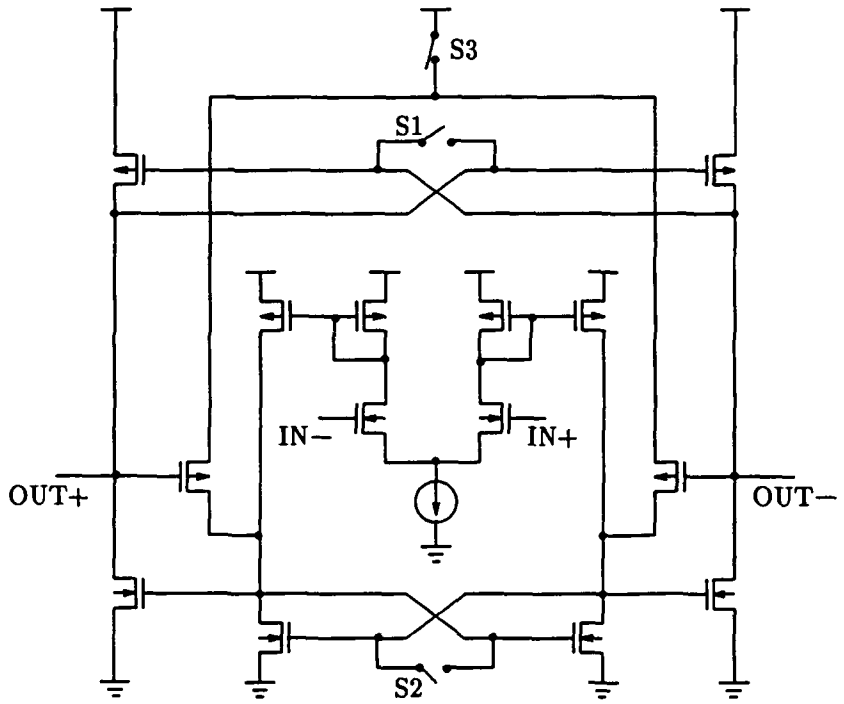

Figure 7: Positive Feedback Comparator

8 Future Work

A three level quantizer [19] can be used instead of the present two level quantizer to raise the resolution, or lower the sample rate. This change should not result in a loss of linearity for a differential circuit realization. MASH type Delta Sigma ADC's [10] are also sensitive to gain matching between integrators. This self calibration scheme could be extended to MASH Delta Sigma ADC's.

9 Acknowledgements

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