NASA SERC Digital Correlator Projects

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Abstract - **Interest in custom digital correlator processors is growing, in both the radio astronomy and earth sensing communities, as scientists realize that VLSI technology is available to them. This paper presents three digital correlator projects currently underway at the NASA SERC for VLSI Systems Design. The projects are a 60MHz chip for the ESTAR satellite, a 100MHz, 1024 channel autocorrelator and a 64 MHz, VLSI system consisting of 8 32 channel complex crosscorrelators, including phase rotators.**

1 Introduction

This paper presents three digital correlator projects currently underway at the NASA SERC for VLSI Systems Design. The projects are a 60MHz chip for the ESTAR satellite, a 100MHz, 1024 channel autocorrelator and a 64 MHz, VLSI system consisting of 8 32 channel complex crosscorrelators, including phase rotators.

2 ESTAR Correlator

This correlator chip is intended for use in synthetic aperture radiometer systems which require the non-time lag cross-correlation of multiple data streams. The large number of correlators (1600) makes the chip especially useful for applications requiring many antennas. The study phase for this chip has been completed. The design and fabrication of this IC is awaiting funding.

The correlator chip accepts 80 input streams, clocked at a maximum rate of 60 MHz. The 80 inputs are divided into two 40 input sections, one horizontal (**HBUS**), the other vertical (**VBUS**). Each horizontal input is multiplied by all vertical inputs with the products being accumulated in separate registers. This process continues for one integration period, as defined by the user. At the end of the integration period, data is made available for reading from an asynchronous interface. This interface is capable of operating at a maximum rate of 20 MHz. Correlated data is read out in 32-bit words. A new integration period can begin when all data has been read out. Input data can be either 2-bit, 3 level or 1-bit, 2 level, under user control. An 8 pin external test port is provided to simplify system testing. The key features of this correlator IC are listed below:

- 1600 correlators
- 60 Megasamples/second maximum input rate
- 20 MHz maximum data output rate
- Low Power ($\approx 500\mu W$/correlator)
- 2-bit/3-Level or 1-bit/2-level correlation supported

- Up to 1.11 second integration time at 60 MHz
- External Test Port
- Maskable Interrupt/Polling Supported
- Data output is independent of system clock
- 32-bit Data Bus
- Control circuitry uses SEU immune memory cells
- TTL compatible inputs, can be driven with CMOS

3 High Performance Correlator

Currently in design, this chip is targeted for radio astronomy applications and digital spectrometers, where large numbers of lags are needed. The chip is designed to be easily used in configurable systems.

This correlator chip accepts two data streams (Stream A and Stream B) at a maximum sample rate of 100 MHz. Samples from Stream A are successively delayed (in a 1024-stage internal shift register) and multiplied by the (undelayed) data from Stream B. Arithmetic is performed in 1024 individual multiplier/accumulators, operating in parallel. At the end of an integration period the data in the accumulators is parallel-loaded into 1024 output registers. New integration can begin immediately. The contents of the output registers can be shifted out at rates up to 20 MHz, via a 32-bit tri-stating output port. The chip supports data multiplexing and all control signals are passed through the chip, to simplify cascading. The key features of this correlator IC are listed below:

- Autocorrelation or Crosscorrelation
- 1024 lags
- 100 Megasamples/second
- Double Nyquist sampling supported
- 32-bit accumulator stages (no prescaler)
- 3-level or 2-level arithmetic supported
- Low Power
- Data and Control signals completely cascadable
- Selectable auxiliary ports on the data inputs
- Data input blanking supported
- Integration can continue while data is output
- TTL compatible inputs, can be driven with CMOS

4 Cross Correlator

This digital correlator is intended for use in interferometry applications in radio astronomy. This chip will integrate, in addition to the correlator itself, many of the functions needed by a multiple antenna interferometry system. The die will contain the equivalent of 512 real correlator channels, organized into 8 sections of 64 channels each. Each section can be configured into a 32 channel complex correlator. There will also be a phase generator circuit associated with each of the 8 sections. Internal muxing circuits will allow flexibility in

interconnecting the correlator sections. The correlator will be contain a control register and a 16 bit asynchronous I/O port. This crosscorrelator chip is currently in the study phase and is awaiting development funding. The key features of this correlator IC are listed below:

- Real or Complex Crosscorrelation
- 512 equivalent lags
- Flexible internal data path configurations
- 64 Megasamples/second
- 16-bit accumulator stages (plus 7 bit prescaler)
- 4-level arithmetic
- Low Power
- Asynchronous I/O port
- Selectable auxiliary ports on the data inputs
- Data input blanking supported
- Integration can continue while data is output
- TTL compatible inputs, can be driven with CMOS

5 Conclusion

The several correlator chip development projects at the NASA SERC are intended to provide the scientific community with levels of integration and correlator system complexity which have not previously been available.

6 Acknowledgements

This research was supported in part by NASA, under the NASA Space Engineering Research Center grant NAGW-1406 and contract G5-NAG-5-1635. The author would also like to thank Jon Hagen, at the NAIC Lab, and Will Aldrich, at the MIT-Haystack Observatory.