Fully-Depleted Silicon-on-Sapphire and Its Application to Advanced VLSI Design

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Abstract - **In addition to the widely recognized advantages of full dielectric isolation, e.g., reduced parasitic capacitance, transient radiation hardness and processing simplicity, fully-depleted silicon-on-sapphire offers reduced floating body effects and improved thermal characteristics when compared to other silicon-on-insulator technologies. The properties of this technology and its potential impact on advanced VLSI circuitry will be discussed.**

1 Introduction

Compared to the junction isolation of VLSI technologies based on bulk silicon, the full dielectric isolation afforded by silicon-on-insulator (SOI) offers many well known advantages. Of primary importance is the significant reduction in parasitic junction capacitance resulting from the replacement of the silicon under the source/drain regions with an insulator. This reduction in capacitance yields higher device switching speed and decreased dynamic power consumption. Additional benefits of SOI include reduced interconnect capacitance, unconditional latch-up immunity, insensitivity to transient radiation and single-event phenomena and the process simplicity inherent to the natural device isolation.

A further refinement of the SOI concept has led recently to the use of ever thinner silicon layers. MOS devices fabricated on very thin Si films operate in a fully depleted (FD) mode in which the gate-controlled depletion region extends to the back interface as the top interface inverts. Under these conditions SOI devices display some improved characteristics when compared to conventional, partially depleted SOI devices. Some of the advantages of full depletion include; reduction of the kink effect due to the absence of the neutral layer in the channel region [1]; better control of the channel region by the gate leading to reduced punch-through current [2]; higher carrier mobility due to reduced transverse electric field [3]; and reduced short-channel effects [4].

Of the leading SOI candidate materials silicon-on-sapphire (SOS) has the longest history of reliable service in harsh environments. We describe here the properties of a fully depleted VLSI technology based on ultra-thin (< 100 nm) SOS films and show some of the advantages of this technology to the designer of digital and analog CMOS circuitry. As with other fully depleted SOI approaches this technology can be scaled laterally with relative ease because the vertical scaling has already been accommodated by the thin active region. Because of the full dielectric isolation, source, drain, p-well and n-well design rules become limited only by the alignment capability of the lithographic tool and the ability to transfer patterns by dry etching. These advantages lead to processing simplicity and very high density circuitry.

2 Material

Until recently, SOS technologies were based on silicon layers of at least 300 nm in thickness because of the high density of grown-in defects occupying the region near the Si/sapphire interface. This high density of twinning defects had two effects which precluded CMOS operation in the fully depleted regime. First, these defects significantly reduced carrier mobilities in the near-interfacial region to levels which significantly limited transistor performance. Second, the presence of intra-gap states associated with these defects pinned the potential of the Si/sapphire interface thus inhibiting the control of back interface potential by the gate.

To deal with these two related problems we refined a defect reduction technique based on solid-phase epitaxial regrowth [5] to improve the SOS films in the region near the Si/sapphire interface. This method uses Si ions implanted at 185 keV at a dose of $6 \times 10^{14}/cm^2$ to amorphize the film near the interface. Regrowth through the amorphous region at 900 deg C results in dramatically improved films with significant reduction in twinning defect concentrations as shown by RBS [6] and TEM [7]. CMOS devices fabricated from 100 nm thick improved SOS show low field channel mobilities of $500cm^2$/V-sec and $200cm^2$/V-sec for NMOS and PMOS devices, respectively and back interface state densities of $1 - 2 \times 1011/cm^2$ [8].

3 Design Advantages

Figures 1 and 2 are cross sectional views of a CMOS/SOS device and a CMOS bulk device, respectively. The full dielectric isolation offered by SOS eliminates the need for field oxides, channel stop implants, and isolation techniques which can limit density and which make CMOS latchup a design issue. The natural isolation together with the fully depleted nature of the thin films lend a freedom to design novel structures and analog circuitry with different power supply voltages. For example, an analog multiplier that is an important part of a neural network design has been made in SOS at NRaD[9]. Design rules in SOS are made simple and planarization schemes can be relaxed because of the absence of a thick field oxide. Latchup is not an issue and radiation sensitivity is minimized. Decreased subthreshold slope factor due to the fully depleted nature of the films allows for lowered threshold voltages and hence faster switching times. The use of FD films also eliminates the need for body ties which results in more compact layouts. Parasitic capacitances are reduced to their absolute minimum in a FD SOS process, and if a silicide process is used, resistance of silicon and polysilicon areas can also be very low. These advantages can result in fast, dense, and low power designs.

4 Device Characteristics

Figures 2 and 3 show some typical drain current characteristics for a fully depleted n-channel device and a non-fully depleted device with an L_{eff} of $1.0 - \mu m$. Both devices have a nominal silicon film thickness of 100-nm but the channel of the non-fully depleted device has been doped such that the depletion width is less than 100-nm. Elimination of the kink effect in the FD device is clearly shown. It is also interesting to note that no negative slope is

observed in the output characteristics for the fully-depleted device. This is in contrast to other SOI technologies where a negative slope in the output characteristics of an n-channel device for a gate length of $1.0 - \mu m$ has been observed [10]. The poor thermal conductivity of the buried oxide in other SOI technologies as opposed to the higher thermal conductivity of sapphire is the reason attributed to this effect. The drain breakdown voltage (V_{bds}) of the FD $1.0 - \mu m$ device has been measured at 6.8 volts which is sufficient for use with a 5.0 volt power supply. This drain breakdown voltage is in sharp contrast to other $1.0 - \mu m$ n-channel SOI devices which have shown a breakdown less than 5.0 volts [11]. This reduction in Vbds for n-channel SOI devices without body ties has been shown to be due to parasitic bipolar conduction [12]. This effect is particularly troublesome for devices with gate lengths below about 1 micrometer fabricated in long lifetime materials such as SIMOX, ZMR, and bonded wafer SOI. Bipolar effects are enhanced in these materials because of relatively long minority carrier lifetimes which may exceed 100 ns in some of the more recently developed material. In comparison, drain breakdown voltages measured on fully-depleted SOS nMOS devices are shown in Fig. 5 as a function of effective channel length. From these data we conclude that a similar reduction in Vbds exists in down-scaled, fully-depleted nMOS/SOS devices but with a significant mitigation of this effect when compared to devices fabricated in other SOI materials.

5 Circuit Applications

SOS has been used for years for radiation hard, medium scale integration circuits. With the film improvement techniques available, SOS can be used for VLSI designs with all of the benefits and advantages of an ultra-thin, fully depleted technology. Analog-to-Digital converters, neural networks, and any space based application where low power, high speed, high functionality, and radiation insensitivity are needed, can all benefit from the advantages offered by SOS.

The microelectronics research facility at NRaD has fabricated a few technology demonstration chips using the process described in Table II. A 16×16 bit parallel multiplier with $0.75 - \mu m$ gate lengths and a 1K SRAM with effective gate lengths of $1.25 - \mu m$ have been fabricated in thin film fully depleted SOS. The 16×16 bit multiplier has shown CMOS loaded gate delays of 243 ps at 5.0 volts VDD. Although the design of the 1K SRAM was conservative, access times of 20ns were obtained. These designs at least demonstrate the viability of FD SOS for VLSI applications.

6 Challenges

Floating body effects, while mitigated by fully depleted films, are not eliminated entirely. This effect leads to early drain breakdown although for deep submicron devices it is predicted that SOI will have a higher breakdown voltage than a bulk device[13]. Body ties, although successful at eliminating the floating body (albeit at the expense of less dense circuitry) for thicker, non-fully depleted films are not effective for a FD film due to the lack of free carriers in the FD film. Lightly doped source and drains will increase drain breakdown voltage while

creating a trade-off of saturation current.

7 Summary

High quality thin films of SOS have made the use of fully depleted, sub-micron transistors possible. Due to the low minority carrier lifetimes in SOS, drain breakdowns over 5.0 volts for a gate length of 1.0-m have been observed. The potential for very high speed, low power and dense layout design has been demonstrated. The natural isolation offered by SOS and the very thin films described here offer advantages to the designer and make SOS a viable VLSI technology.

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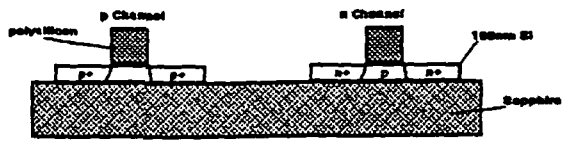

Figure 1: Cross section of CMOS/SOS device.

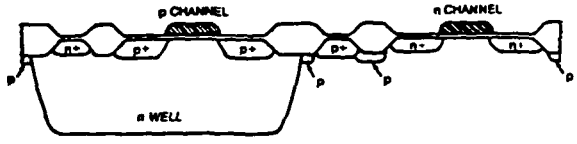

Figure 2: Cross section of CMOS/bulk device.

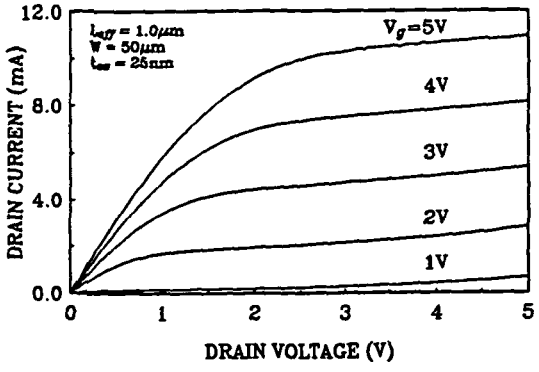

Figure 3: Drain characteristics of a fully-depleted NMOSFET.

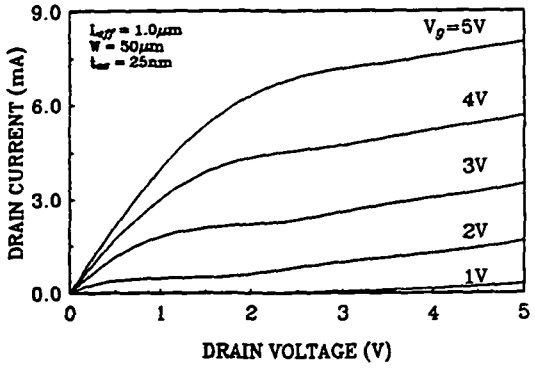

Figure 4: Drain characteristics of a non-fully depleted NMOSFET.

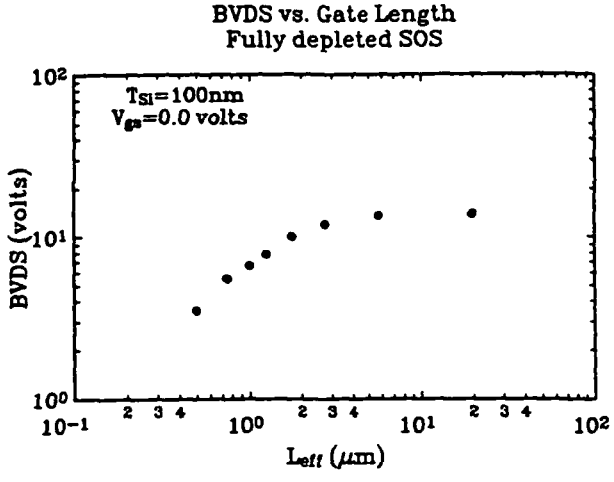

Figure 5: Drain breakdown vs. effective gate length at VGS=0.0 volts for fully-depleted SOS.

TABLE I

Advantages of a SOS/Fully Depleted Technology

Advantages	Primary Reason	Application
Reduced capacitance	Reduced junction capacitances due to very thin film and smaller area junctions	High-speed electronics
Immunity to transient upset	Very small active volume for electron-hole generation	Soft-error free memories; defense electronics
Elimination of "kink" effect	No neutral floating substrate (due to substrate fully depleted)	Analog VLSI
Increased drain breakdown voltage	Higher recombination rate due to short lifetime cause a reduction in gain of parasitic npn bipolar	Deep submicron VLSI

Table II
Silicide CMOS/SOS Process Steps

Description	Details
• Silicon thinned to 1000-Å	oxide grown in wet O_2 then stripped
• Island isolation	plasma etch
• NMOS threshold implant	boron: 2.5 x 10^{12} cm^{-2} at 35 keV
• Gate oxidation	11 min at 875°C in wet O_2
• Polysilicon deposition,doping, etch	T_{dep} = 580°C
• NMOS source/drain implant	arsenic: 2.0 x 10^{15} cm^{-2} at 55 keV
• PMOS source/drain implant	BF_2: 2.0 x 10^{15} cm^{-2} at 50 keV
• Sidewall oxide deposition	3000-Å undoped LTO
• Source/drain anneal	550°C 30min, 850°C,30min in N_2
• Sidewall oxide etch	plasma etch
• Titanium deposition	T_{Ti} = 500-Å
• Silicon implant	silicon: 1.0 x 10^{15} cm^{-2} at 100 keV
• RTA	675°C, 60sec, N_2
• Ti etch	1:1:5NH_4OH:H_2O_2:H_2O,60°C,3 min
• RTA	850°C, 60sec, N_2
• Contact oxide, etch contacts	6000-Å undoped LTO
• Metal deposition, etch	10,000-Å Al/1%Si
• Sinter	450°C for 30 min in N_2+H_2