Dimension Scaling Effects on the Yield Sensitivity of HEMT Digital Circuits

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Abstract - **In our previous works, using a graphical tool, yield factor histograms, we studied the yield sensitivity of High Electron Mobility Transistors (HEMT) and HEMT circuit performance with the variation of process parameters. This work studies the scaling effects of process parameters on yield sensitivity of HEMT digital circuits. The results applied to two HEMT circuits are presented.**

1 Introduction

The GaAs High Electron Mobility Transistor (HEMT) is being considered for VLSI circuit design for space applications because of its high speed and its tolerance to many forms of radiation. The digital HEMT circuit performances are strongly dependent on the process parameter variations and on the device dimensions. So, the study of circuit performances and their sensitivities to process parameter variations and to device dimension scalings is very important to avoid failure of costly and time-consuming circuit designs.

In our previous work [1], we studied the statistical sensitivities of the HEMTs to process parameter variations. Then in our second phase of the work [2], we designed two digital circuits with these HEMTs and studied the yield sensitivity to process parameter variations. For the HEMT yield sensitivity study, we statistically varied three parameters, gate length, L, gate width, Z and the carrier mobility, μ. It is important to study the yield and the yield sensitivity with more parameter variations like parasitic resistances and the threshold voltage and also observe the effect of HEMT sizing on yield and the yield sensitivity. So, the purpose of this work is to study the circuit yield sensitivity as a function of more parameter variations and also to study the HEMT sizing effect on the circuit yield sensitivity.

2 The HEMT Model and the Dimension Scaling

The basic structure of a uniformly doped AlGaAs/GaAs HEMT is shown in Figure 1. The dc model used in this work is taken from reference [3]. This model uses the Trofimenkoff type carrier velocity-field relationship to model the dc I-V characteristics for both normal and compressed transconductance regions. In the model, three parameters which are directly related to the physical parameters are needed to describe the I-V characteristics in the normal transconductance region. These are shown below:

$$A = \frac{Zq\beta\mu}{L} \tag{1}$$

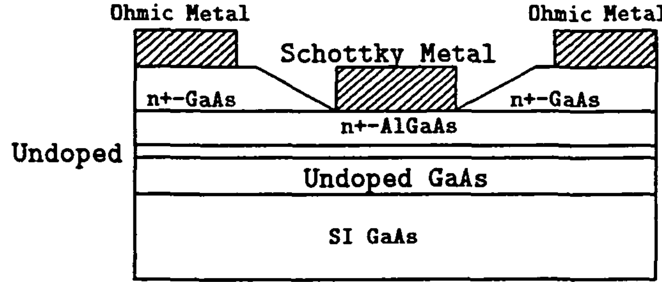


Figure 1: Structure of a Uniformly Doped AlGaAs/GaAs HEMT.

$$B = LE_c \tag{2}$$

$$C = \frac{L^2}{2\epsilon Z v_s \delta} \tag{3}$$

where β, E_c, ϵ, v_s and δ are the charge control coefficient, saturation electric field, permittivity of AlGaAs, saturation velocity and effective width of the conduction channel respectively. This dc model was validated in reference [4].

¿From the dc model, we have analytically derived the expressions for the small-signal parameters such as transconductance, g_m, gate to source capacitance, C_{gs} and the current gain cutoff frequency, f_T in the normal linear region. The expressions are given below:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{AV_D}{1 + V_D/B} \tag{4}$$

$$C_{gs} = \frac{\partial Q_T}{\partial V_G} = \frac{AL^2(2 + V_D/B)}{\mu} \tag{5}$$

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{\mu V_D}{2\pi L^2(1 + V_D/B)(2 + V_D/B)} \tag{6}$$

In the normal saturation region, we have applied numerical techniques to compute these circuit parameters. See reference [4] for details.

Another parameter "BETA" which is used in the JFET SPICE circuit model is calculated from the relation

$$BETA = \frac{g_m}{2(1 + \lambda V_D)(V_G - V_{th})} \tag{7}$$

where λ is the channel length modulation parameter.

In the dc or the small-signal model, the parasitic effects are not included explicitly. This effect was taken into account in the model by solving the nonlinear equations which are given below:

$$V_{GS} = V_G + I_D(V_G, V_D)R_S \tag{8}$$

$$V_{DS} = V_D + I_D(V_G, V_D)(R_S + R_D) \tag{9}$$

where V_{GS} and V_{DS} are the externally applied bias voltages and R_S and R_D are the parasitic source and the drain resistances.

Parameter	Normal Size Value	Scaled Size Value
L(μm)	0.35	0.35
Z(μm)	65	10
$\mu(m^2/Vs)$	0.44	0.44
$V_{tho}(V)$	-0.017	-0.017
$A(mA/V^2)$	49.517	7.618
B(V)	5.285	5.285
$C(K\Omega)$	8.341	54.216
D	0.015	0.015
$R_S(\Omega)$	5.9	38.35
$R_D(\Omega)$	6.0	39.0

Table 1: Physical and Model Parameters of the TRW #2078 HEMT.

In the subthreshold region of operation of the HEMT, a model parameter, D is used to model the threshold voltage shift of the two dimensional electron gas caused by the drain voltage. This threshold voltage correction is shown by the equation

$$V_{th} = V_{tho} - D \times V_D \tag{10}$$

The physical and the model parameters used for the TRW #2078 HEMT are given in Table 1 [3].

2.1 Scaling Rules for the HEMT

As we mentioned earlier, we did not consider the dimension sizing of the HEMT in the statistical sensitivity study of our previous works. Scaling rules for the HEMT can be arrived at from the analytical expressions for the parameters or from the measurements of different size HEMTs from the same foundry. Most of the HEMT small-signal parameter values are scaled up or down based on the gate width [5].

The drain source current, I_D and the depletion charge are proportional to the gate width, Z; so the partial derivative of these quantities, such as $g_m = \frac{\partial I_D}{\partial V_G}$, $g_{ds} = \frac{\partial I_D}{\partial V_D}$, $C_{gs} = \frac{\partial Q}{\partial V_G}$ and $C_{gd} = \frac{\partial Q}{\partial V_D}$ are also expected to be proportional to gate width. In addition, because C_{ds} is a geometric capacitance from source to drain, it is also proportional to gate width.

The circuit parameters of a HEMT with gate width Z can be related to a scaled HEMT with gate width Z_1 by using a scale factor $S_1 = \frac{Z}{Z_1}$. Then the circuit parameters are scaled to some arbitrary gate width, Z_1 as follows:

$$I_D^{\prime} = \frac{I_D}{S_1} \tag{11}$$

$$g_m^{\prime} = \frac{g_m}{S_1} \tag{12}$$

$$g'_{ds} = \frac{g_{ds}}{S_1} \tag{13}$$

$$C'_{gs} = \frac{C_{gs}}{S_1} \tag{14}$$

$$C'_{gd} = \frac{C_{gd}}{S_1} \tag{15}$$

$$C'_{ds} = \frac{C_{ds}}{S_1} \tag{16}$$

Scaling rules for the parasitic resistances R_S and R_D are different from the above parameters. These rules can be derived from simple Ohm's law: $R = \frac{V}{I}$. For either resistor

$$R_{S,D} = \frac{V}{I_D} \tag{17}$$

where V is the voltage drop across the resistor and I_D is the drain current that is proportional to gate width. Using the scale factor defined above, R_S and R_D can be scaled as

$$R'_S = R_S S_1 \tag{18}$$

$$R'_D = R_D S_1 \tag{19}$$

As we see from the above equations, the parasitic resistances are inversely proportional to the gate width. It can be shown from the definition of f_T, it is independent of gate width.

In this work, we have used the $65\mu m$ normal gate width HEMTs in the example circuits. We have used a scale factor of 6.5 to reduce the gate width to $10\mu m$ so that the HEMTs could be used for the VLSI design. The last column of Table 1 shows the scaled parameters.

A computer simulation program was developed to calculate circuit parameters such as drain current, transconductance, "BETA", gate-to-source capacitance and the current gain cutoff frequency for both the normal and scaled HEMT. In Table 2, we present the simulation results for the linear and the saturation regions. The bias conditions were chosen arbitrarily. As we see from the table, the results agree excellently. For all cases, the scaling factor is close to 6.5 as we expected.

3 Statistical Analysis

In our statistical analysis, we used the Monte Carlo technique and a computer program called SPICENTER developed at the University of Idaho. Mathematical development of the yield factor histograms and the yield sensitivity to process parameter variations can be found elsewhere [1,2,6]. Here we briefly describe the method we used in our work.

3.1 Monte Carlo Simulator

In this work, the scaled TRW #2078 HEMT was used to implement the example circuits. This HEMT shows only the normal transconductance effect. To describe this effect, six

Circuit Parameter	Bias Condition	Normal Size	Scaled Size
$I_D(\mu A)$	$V_{GS} = 0.5V, V_{DS} = 0.4V$	5091	783
$g_m(mS)$	$V_{GS} = 0.5V, V_{DS} = 0.4V$	15.79	2.43
$BETA(mA/V^2)$	$V_{GS} = 0.5V, V_{DS} = 0.4V$	16.05	2.47
$C_{gs}(fF)$	$V_{GS} = 0.5V, V_{DS} = 0.4V$	28.46	4.38
$f_T(GHz)$	$V_{GS} = 0.5V, V_{DS} = 0.4V$	88.32	88.34
$I_D(\mu A)$	$V_{GS} = 0.2V, V_{DS} = 1.0V$	1376	212
$g_m(mS)$	$V_{GS} = 0.2V, V_{DS} = 1.0V$	10.87	1.67
$BETA(mA/V^2)$	$V_{GS} = 0.2V, V_{DS} = 1.0V$	24.20	3.72
$C_{gs}(fF)$	$V_{GS} = 0.2V, V_{DS} = 1.0V$	6.51	1.00
$f_T(GHz)$	$V_{GS} = 0.2V, V_{DS} = 1.0V$	265.58	265.58

Table 2: Circuit Parameters of the TRW #2078 HEMT Calculated in this Work.

process related parameters such as L, Z, μ, V_{tho}, R_S and R_D are needed. In our Monte Carlo simulation, we have chosen a $\pm 5\%$ uniform and uncorrelated variation of these parameters about their nominal values listed in Table 1. In the simulation, we varied these parameters randomly at the same time. The random parameter values are used in the model program to calculate the circuit parameters g_m, C_{gs} and "BETA" for a particular bias condition. To create 1000 statistical HEMTs for normal size or for scaled size HEMT, 1000 simulations are performed. These 1000 HEMT circuit parameter values form a "TRUTH MODEL" [6] input to the JFET SPICE circuit model. Gate-to-drain capacitance C_{gd} is very small compared to the C_{gs}, so in the SPICE model we keep this capacitance constant.

For the Monte Carlo analysis, the program SPICENTER takes each set of parameter values created from the model program and computes the circuit performances like delay time, rise time, fall time etc. The circuit performance calculated from each simulation are compared with the nominal performance specification. If the circuit meets the specification then the circuit is accepted otherwise it is rejected. From the accepted circuits, the program creates the yield factor histograms for each of the independent parameters, L, Z, μ, R_D, R_S and V_{tho}. Our analysis technique is summarized in Figure 2. Details are to be found elsewhere [1,7].

The yield sensitivity was determined by linear fitting the yield factor histograms. The slope of each fit determines the yield sensitivity with respect to a particular parameter. These yield sensitivities are presented as yield%/parameter% and also as yield% per each unit dimension.

4 Results

In this work, we have chosen two example HEMT circuits to study the dimension scaling effects on the circuit performances and their yield sensitivities.

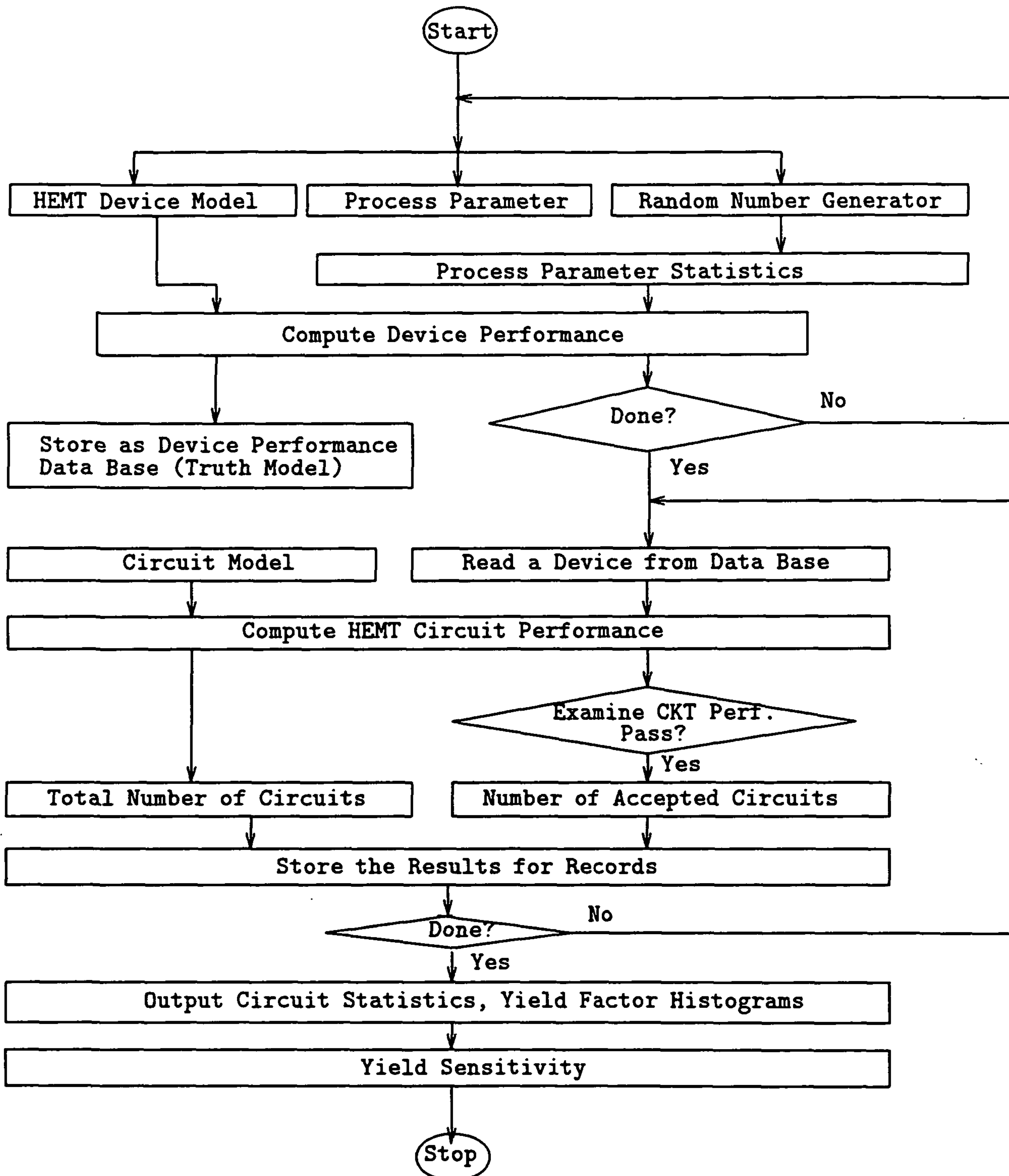


Figure 2: Algorithm of the Monte Carlo Simulator.

Parameter	Normal Size Yield Sensitivity (yield%/parameter%)	Normal Size Yield Sensitivity	Reduced Size Yield Sensitivity (yield%/parameter%)	Reduced Size Yield Sensitivity
Param. 1: L	-9.14 ± 0.49	$-2602.56 \pm 137.14\%/\mu m$	-9.81 ± 0.42	$-2794.87 \pm 120.92\%/\mu m$
Param. 2: Z	$+6.33 \pm 0.44$	$+9.74 \pm 0.67\%/\mu m$	$+5.29 \pm 0.49$	$52.95 \pm 4.87\%/\mu m$
Param. 3: μ	$+7.77 \pm 0.45$	$+1761.91 \pm 102.60\%/m^2/Vs$	$+7.79 \pm 0.59$	$+1765.31 \pm 132.94\%/m^2/Vs$
Param. 4: R_D	-0.90 ± 0.83	$-15.00 \pm 13.74\%/\Omega$	-1.05 ± 0.84	$-2.69 \pm 2.16\%/\Omega$
Param. 5: R_S	-2.19 ± 0.50	$-37.13 \pm 8.56\%/\Omega$	-1.47 ± 0.44	$-3.83 \pm 1.15\%/\Omega$
Param. 6: V_{tho}	-0.07 ± 0.50	$+0.44 \pm 2.90\%/mV$	$+0.36 \pm 0.45$	$+2.11 \pm 2.64\%/mV$

Table 3: Yield Sensitivity of the FFL NOR Gate.

4.1 Example I: 2-Input NOR Gate with Feedback FET Logic

Our first example circuit is a 2-input NOR gate with feedback FET Logic (FFL). This high-speed and low power feedback FET logic is based upon a push-pull output stage with a feedback inverter that shuts off the output current after the logic high state is reached. It is two to four times faster than the comparable GaAs direct-coupled FET logic. Figure 3 shows the circuit diagram of this FFL NOR gate [8]. All of the transistors in the circuit are n-channel type transistors. Using one type of transistors raises yield and reduces process complexity.

We have chosen delay time as the performance criterion for this NOR gate. In our analysis, the delay time is defined as the time taken at the output to reach 90% of its final steady state value from the instant the input is triggered with a step voltage. The nominal delay times for both the normal and the scaled size HEMT circuits were calculated by simulating the circuit with the nominal parameter values. The delay time was found to be 35.88 ps for normal size circuit and 34.06 ps for scaled size circuit. The output load capacitance was scaled down by the same factor to calculate the delay time of the scaled size circuit.

The Monte Carlo simulations were performed first with the normal size HEMT circuit parameters. The yield was only 12.2% which is very low. To increase the yield, we relax the delay time by 5% and resimulate. With this 5% increased delay time specification we achieve a 48.1% yield. The yield factor histograms for 1000 simulations of this circuit are shown in Figure 4. As we see from the figure, the yield is very sensitive to the gate length, width and the mobility. But it is almost insensitive to the parasitic resistances and the threshold voltage. However, we found a small decrement of yield with source resistance increment.

1000 simulations were also performed for the scaled size circuit and the yield was 13.2%. So, we increase the delay time by 5% in the specification to increase the yield to 56.2%. We observe similar results as the normal size HEMT circuit.

The yield sensitivity to each parameter variation was calculated for both the circuits and are shown in Table 3. These are presented as yield%/parameter% and also as yield% per unit dimension of the parameter.

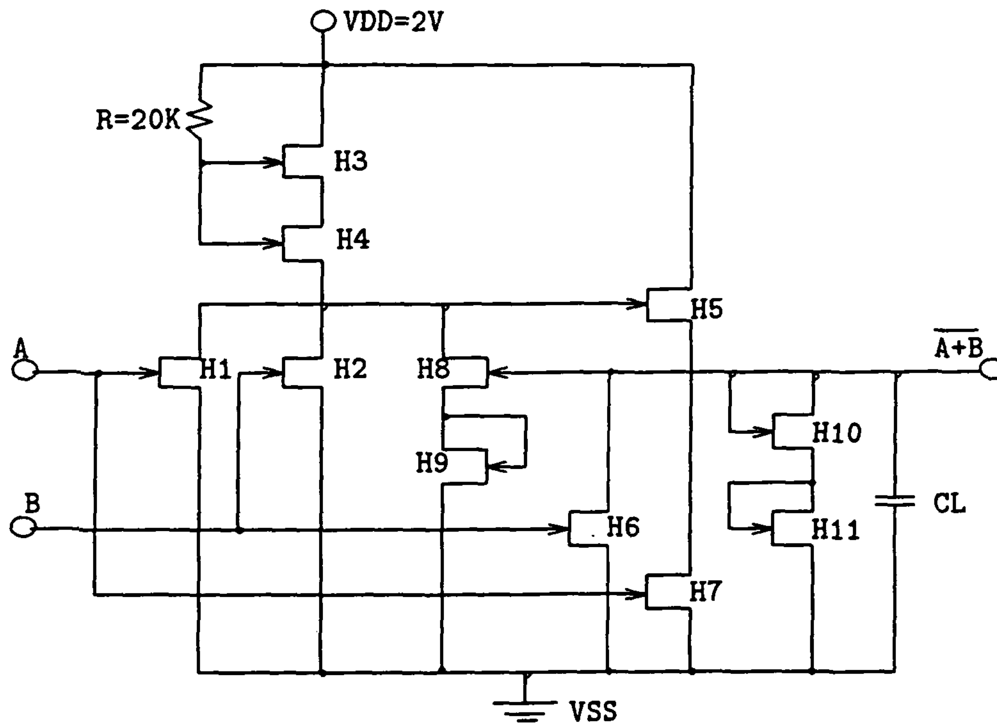


Figure 3: Circuit Diagram of an FFL HEMT NOR Gate.

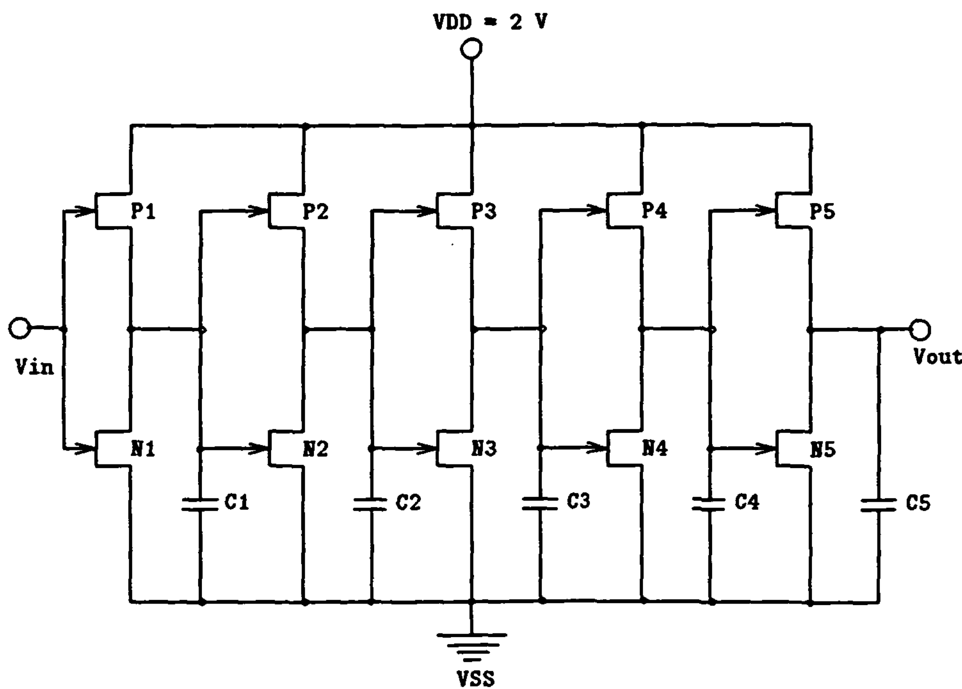


Figure 4: Yield Factor Histograms, Yield % vs. Parameter %, of an FFL NOR Gate.

Parameter	Normal Size Yield Sensitivity (yield%/parameter%)	Normal Size Yield Sensitivity	Reduced Size Yield Sensitivity (yield%/parameter%)	Reduced Size Yield Sensitivity
Param. 1: L	-7.80 ± 0.65	$-2222.22 \pm 183.60\%/\mu m$	-5.69 ± 0.59	$-1619.66 \pm 168.78\%/\mu m$
Param. 2: Z	$+2.21 \pm 0.49$	$+3.39 \pm 0.74\%/\mu m$	$+1.96 \pm 0.49$	$+19.65 \pm 4.82\%/\mu m$
Param. 3: μ	$+3.92 \pm 0.41$	$+887.76 \pm 91.74\%/m^2/Vs$	$+3.84 \pm 0.67$	$+870.75 \pm 149.91\%/m^2/Vs$
Param. 4: R_D	-1.64 ± 1.03	$-27.23 \pm 17.10\%/\Omega$	-5.29 ± 0.94	$-13.58 \pm 2.39\%/\Omega$
Param. 5: R_S	$+0.15 \pm 0.60$	$+2.53 \pm 10.26\%/\Omega$	$+3.67 \pm 0.70$	$+9.58 \pm 1.82\%/\Omega$
Param. 6: V_{tho}	$+0.52 \pm 0.58$	$+3.07 \pm 3.34\%/mV$	$+0.99 \pm 0.71$	$+5.79 \pm 4.14\%/mV$

Table 4: Yield Sensitivity of the HEMT Inverter Chain.

4.2 Example II: HEMT Inverter Chain with Complementary Logic

A chain of inverters mostly used in memory circuits is chosen as our second example circuit. We propose a chain of five inverters implemented with complementary logic [9] and the circuit is shown in Figure 5. In the circuit, P1-P5 are the p-channel and N1-N5 are the n-channel depletion mode HEMTs. The capacitances C1 through C5 are the output capacitances for each stage which are arbitrarily chosen to 0.1pF for the normal size circuit. A step input is applied and output is observed at the capacitor C5.

For this circuit, we have chosen rise time of the output at C5 as the performance criterion. The rise time calculated from the nominal values of the parameters were 20.44 ps for normal size and 23.77 ps for the scaled size circuit. Here also, we scale all capacitors down by the same factor.

1000 Monte Carlo simulations were performed first for the normal size HEMT and then for the scaled size HEMT inverters. The yields were not high enough, so we relax the specification by increasing the rise time of 5% and simulate again. With the new specification the yield went up to 52.1% and 56.8% for normal and scaled size circuit respectively. In Figure 6, we present the yield factor histograms of the Scaled size HEMT circuit with 5% relaxed rise time specification. For this circuit both in normal and scaled size, the yield and the yield sensitivity as a function of L, Z, μ and V_{tho} variation is similar as we observed for circuit I. The yield is not very sensitive to the parasitic resistances R_S and R_D for the normal size circuit but it is sensitive for the scaled size circuit. Yield increases with R_S and decreases as R_D increases. As a verification of our result, we choose fall time as performance specification in the Monte Carlo simulation and perform 1000 runs and we observed a consistent result as we expected. That is, the yield is higher for higher R_D value and lower for lower R_S value. The yield sensitivity of both normal and scaled HEMT inverters are shown in Table 4.

5 Conclusion

In this work, we first studied the dimension scaling rules of the HEMT circuit parameters. Results of our study are given in Table 2. Then we used the yield factor histograms graphical tools to study the dimension scaling of the HEMTs on the yield and the yield sensitivity of two circuits. From our study, we found, for the NOR gate, that the scaling of the gate width

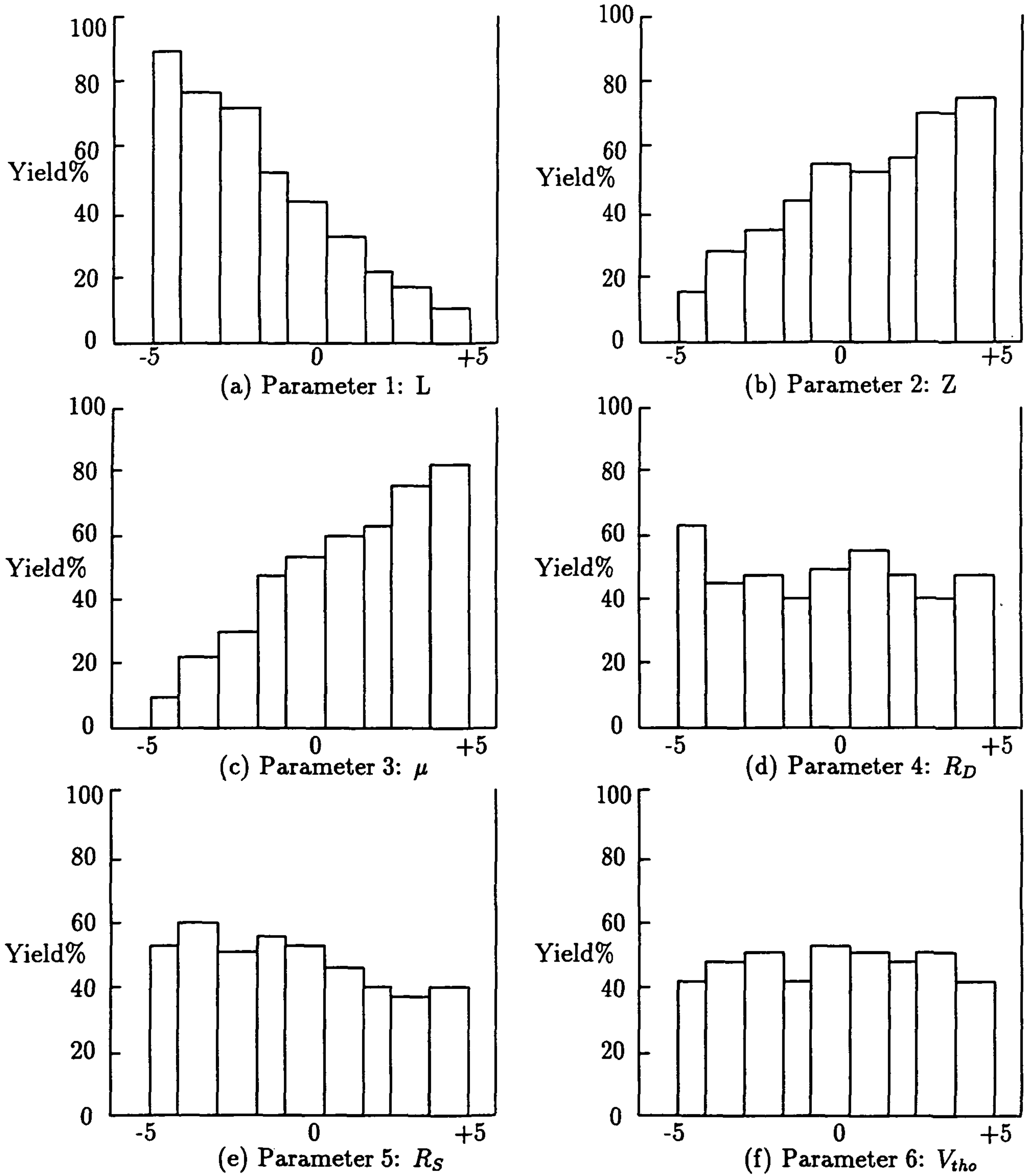
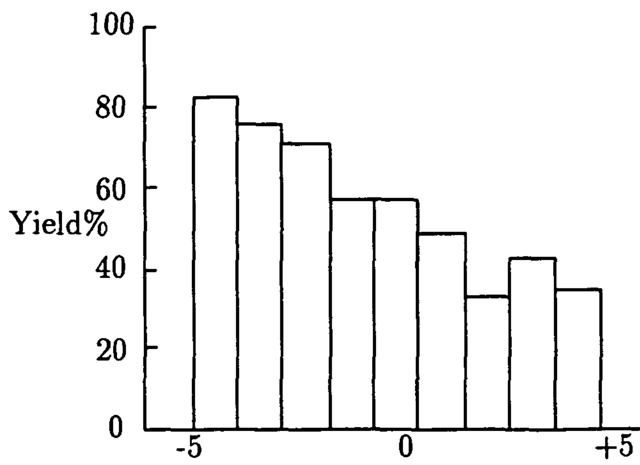
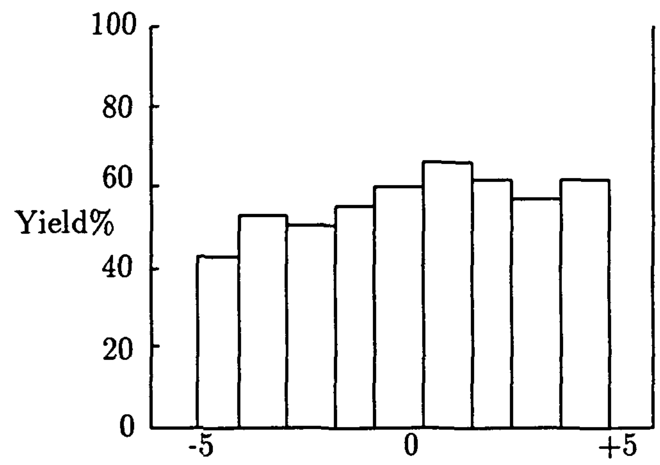


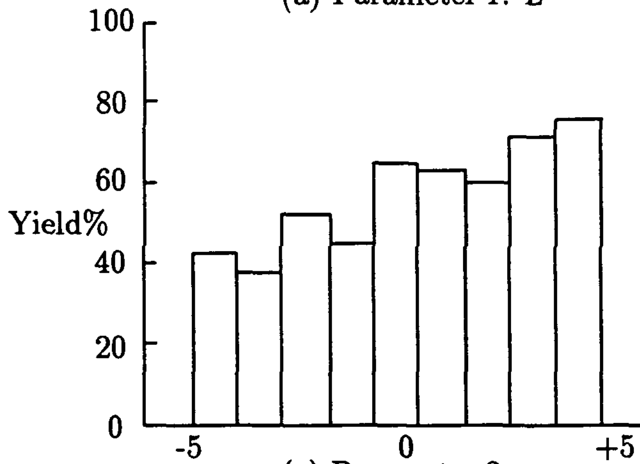
Figure 5: HEMT Inverter Chain with complementary Logic.



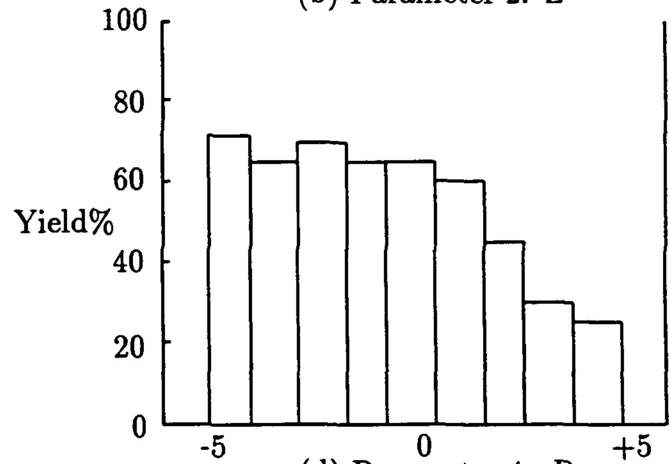
(a) Parameter 1: L



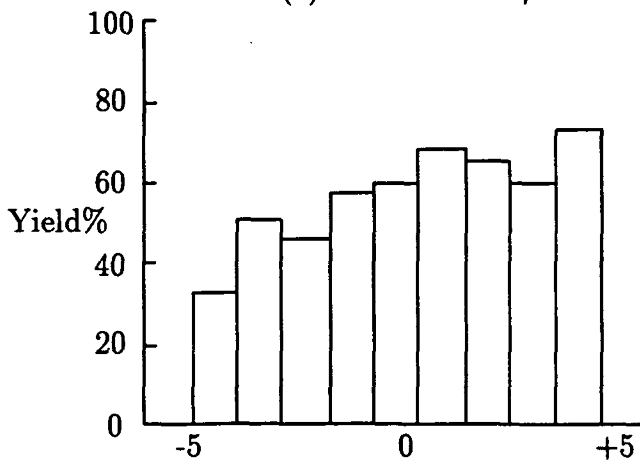
(b) Parameter 2: Z



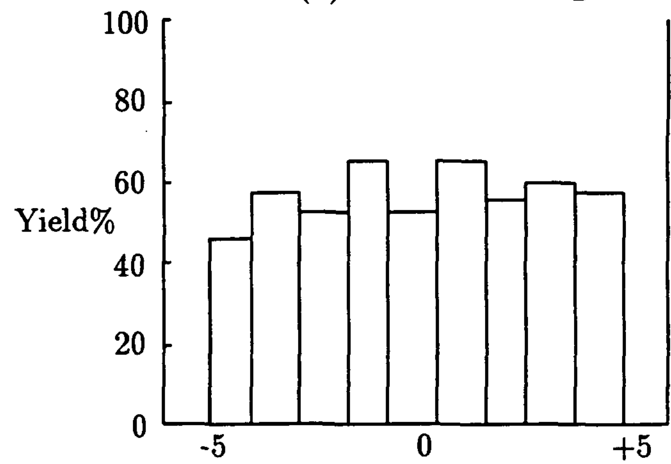
(c) Parameter 3: μ



(d) Parameter 4: R_D



(e) Parameter 5: R_S



(f) Parameter 6: V_{tho}

Figure 6: Yield Factor Histograms, Yield % vs. Parameter %, of HEMT Inverter Chain.

and the parasitic resistances do not change the yield and the yield sensitivity significantly. The yield and the yield sensitivity of the inverter chain do not change much with the scaling of the HEMT width. But yield is more sensitive to R_S and R_D for the scaled HEMT inverter.

6 Acknowledgement

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