A High Speed CMOS A/D Converter[1]

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Abstract – This paper presents a high speed A/D converter. The converter is a 7 bit flash converter with one half LSB accuracy. Typical parts will function at approximately 200 MHz. The converter uses a novel comparator circuit that is shown to out perform more traditional comparators, and thus increases the speed of the converter. The comparator is a clocked, precharged circuit that offers very fast operation with a minimal offset voltage (2 mv). The converter was designed using a standard 1 micron digital CMOS process and is 2,244 microns by 3,972 microns.

1   Introduction

Today, large integrated circuits (ICs) are involved in solving complex signal processing problems. A mixture of digital and analog signals often must be integrated into a single system [1]. Modern digital-to-analog (D/A) and analog-to-digital (A/D) converters have become common components for integrated signal processing. Of the many styles of A/D converters available [1]-[2], only three [3, 4], the flash, half flash, and successive approximation, take full advantage of the speed that CMOS technologies can provide.

Of the three types of converters, the flash converters are clearly the fastest, but they are also the largest. For high performance systems, the flash converter is, however, the choice. To minimize the area required this coverter was designed for 7 bits of resolution, thus limiting the comparator chain to the length of 128 comparator cells. Secondly, the comparator cell itself is highly optimized for both performance and size [5]. Finally, the state of the art process used to manufacture this converter will allow 1 micron gate lengths, thus helping to keep the size of the individual transistors to a minimum.

The basic configuration of a *flash* A/D converter is shown in Figure 1. This type of A/D converter is fully parallel, since it processes each of the n output bits simultaneously thus accounting for the speed of operation [6]. However, the price for this speed is the requirement for 2^n comparators. Thus, for large values of n this can make flash A/D converters prohibitively large.

This style of converter works by first taking a reference voltage (Vref) and dividing it down a chain of resistors. The voltage at each resistor is fed to a comparator, and is compared with the input voltage (Vin). Thus the output down the chain of comparators will be a logic zero until the divided reference voltage is less than the input voltage. At that point, and further down the comparator string, the outputs will be a logic one. The outputs of the
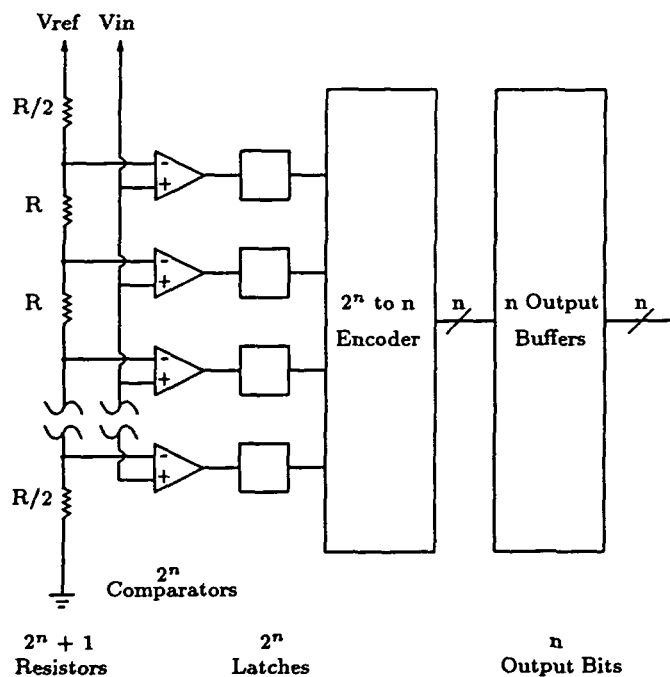
Figure 1: Flash A/D converter

comparators are then latched into flip-flops so that comparison of the next input sample may begin, without destroying the results of the previous conversion. The outputs of the flip-flops are fed into a 2^n to n encoder. This encoder is essentially a set of XOR (Exclusive Or) gates and a small ROM (Read Only Memory) that determines the n binary output bits given the sequence of m zeros and $2^n - m$ ones. Finally, the output from the encoder is sent to a set of output buffers, and the digital representation of the input sample is output from the converter [3, 7].

2   Circuit Design

MOSIS will be used to fabricate this part using Hewlett-Packard's CMOS-34 process. CMOS-34 is a single poly, double metal layer process with 1 micron minimum gate lengths. Using CMOS-34 design rules, this A/D converter was designed to perform at a worst case of 100 MHz. To make the digital logic sections of the converter function as fast as possible, precharged logic was used in the memory section of the converter. Additionally, a pipelined architecture was implemented throughout the part to assist in increasing circuit speed. A diagram of the basic structure a flash A/D converter can be seen in Figure 1.

This A/D converter was designed for a 6 volt analog voltage supply and a 5 volt digital supply. This results in a maximum analog input voltage swing of 5 volts. With a 5 volt swing possible at the analog input, each successive count of digital output represents approximately 40 mV of change on the input voltage.

Digital

Output

111
110
101
100
011
010
001
000
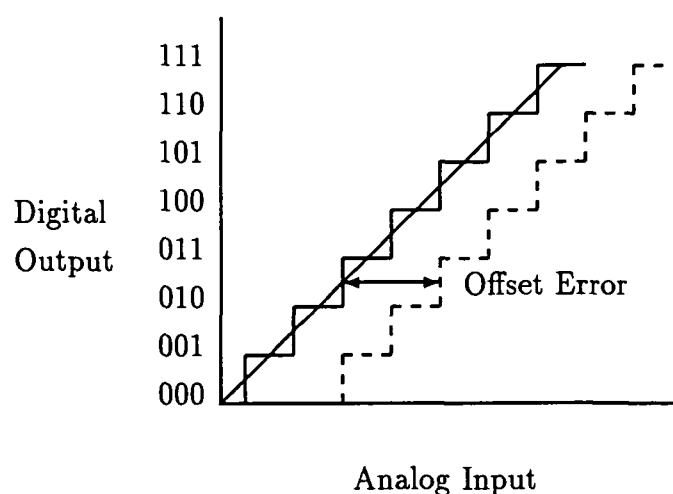
Offset Error

Analog Input

Figure 2: Offset Error Example

2.1 Accuracy Considerations

Before designing an analog integrated circuit, it is necessary to have an understanding of the types and sources of possible inaccuracies in the analog to digital conversion. In the worst case, a sum of all these errors should not result in either circuit failure, or skewed output of more than one half of a least significant bit (LSB), 20 mV.

The first type of error that can occur is called *offset error*. Offset error occurs when the analog input voltage for each digital step output is in error by a fixed amount. Pictured in Figure 2, offset error is most commonly caused by a uniform offset voltage being present on the inputs of all of the comparators. The comparators used in this design have a simulated offset voltage of less than 2 mV. Therefore, offset voltage problems should be reasonable. To determine the offset voltage of the comparators simulations were created that decreased the differential input voltage until the comparator failed.

The analog input voltage difference between two digital output steps is ideally one LSB. The difference from this ideal is called *differential linearity error*. This type of error, pictured in Figure 3, can be caused by systematic or random offsets in the comparators, or by resistance mismatches in the resistor chain. If differential errors are large enough, the A/D converter can lose its *monotonicity*. Monotonicity is the characteristic that there is a unique input voltage for each and every digital output word, and that the digital output always increases for increasing analog input voltages [3].

Another error that can occur in flash A/D converters is *integral linearity error*. Also picture in Figure 3, this error represents a summation of the differential errors up to any point in the digital output. Because of this, integral linearity errors generally have the same sources as differential linearity errors [3]. The measures taken to reduce these errors are discussed throughout the remainder of this paper.
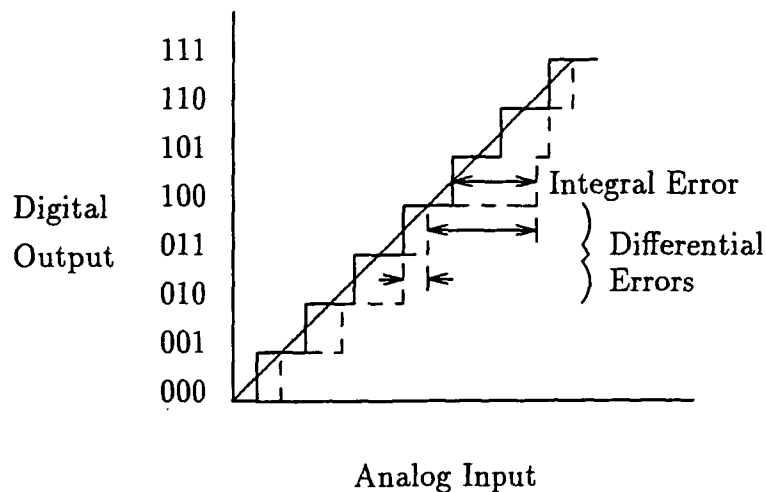
Figure 3: Integral and Differential Errors

2.2 Resistor Ladder

The chain of resistors shown at the left of Figure 1 was constructed from a long strip of polysilicon. The actual resistance of the the line, and thus each individual resistor value, is not critical. What is critical is that each resistor have the same value, such that the ratios of resistance at any point is fixed [8].

Additionally, in order to maintain a regular current density down the line of polysilicon, contacts (equipotential surfaces) are not placed in the current flow. Rather the voltage is tapped on "dog-leg" type structures that come from the polysilicon at regular intervals. Also, in order to keep the reference voltages as stable and noise free as possible, decoupling capacitors were integrated at each reference node. These capacitors help to greatly reduce noise that is coupled through the differential input on the comparator during the pre-charge phase of comparison.

2.3 Comparators

Three viable comparators with typical styles were selected and compared. After the analysis, the best comparator style for this project was selected, and then optimized using HP Spice. The analysis was performed by attempting to size the comparators so that they were of approximately equal speed and accuracy. The comparators were then simulated and their characteristics were compared. These characteristics included size, power, noise, offset, clocking, and input and output voltage levels.

The first comparator analyzed was a clocked, precharged CMOS comparator. This comparator is shown in Figure 4. The circuit functions as follows. First, while the clock, ($\phi 1$), is low, nodes one and two (N1 and N2) are precharged to VDD. Then when the clock goes high the input and reference voltages will turn on transistors Q5 and Q6. If there is a voltage difference between Vin and Vref, Q5 and Q6 will conduct different currents. This causes a potential difference between N3 and N4. This in turn provides positive feedback such that the current difference through Q3 and Q4 increases, and very rapidly, either N1 or N2 will
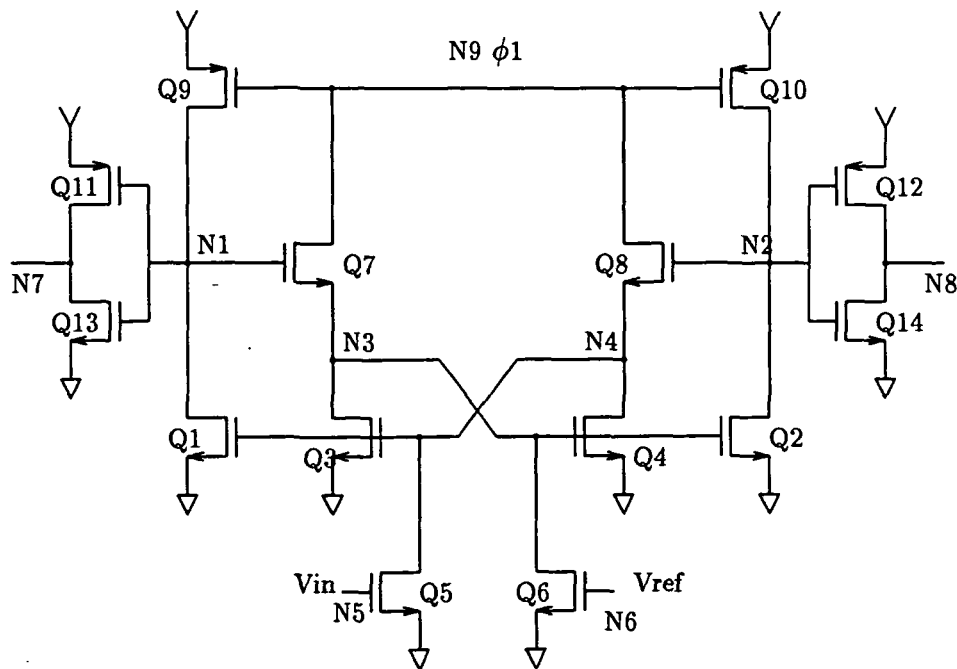
Figure 4: Clocked, Precharged, CMOS Comparator

be discharged to VSS. The output voltage may be read at either N7 or N8 depending on the logic level that is desired. Whichever of the two nodes is used for the output, the other inverter stage is left in place to create a balanced circuit.

The next comparator is slightly simplier than the previous comparator. It uses capacitively stored logic levels to increase its speed, and it requires two synchronized clocks. As seen in Figure 5, during $\phi1$ the input and reference voltages are stored on C1 and C2. Then, during $\phi2$, the comparator turns on and the two voltages on the capacitors are compared. The output of the comparator may be taken at either N1 or N2, or from both locations if a differential output is desired [9].

The final comparator was a three stage, autozeroing comparator. This comparator has the advantage of allowing the input voltage to swing from rail to rail. It also uses a clocked scheme to increase its speed. Figure 6 shows this comparator circuit. During $\phi1$, the reference voltage is placed on N1 and the first two stages are autozeroed. Then during $\overline{\phi1}$ the input voltage is placed on N1. The difference between the reference voltage and the input voltage is coupled into the three stages of inversion and gain with the output appearing at N6.

The three comparators were simulated and compared. Tables 1 through 3 represent a synopsis of the comparisons that were performed and the results. A simple ranking scheme was used to determine which comparator performed the best. Each attribute for each comparator is marked with either a 1, 2, or 3, depending on how the comparator performed. A 1 was given to the best, a 3 to the worst.

As can be seen from Tables 1 to 3, clearly the clocked, precharged, comparator of Figure 4 out performs the other two. Therefore, this comparator was used in the design of this A/D converter.
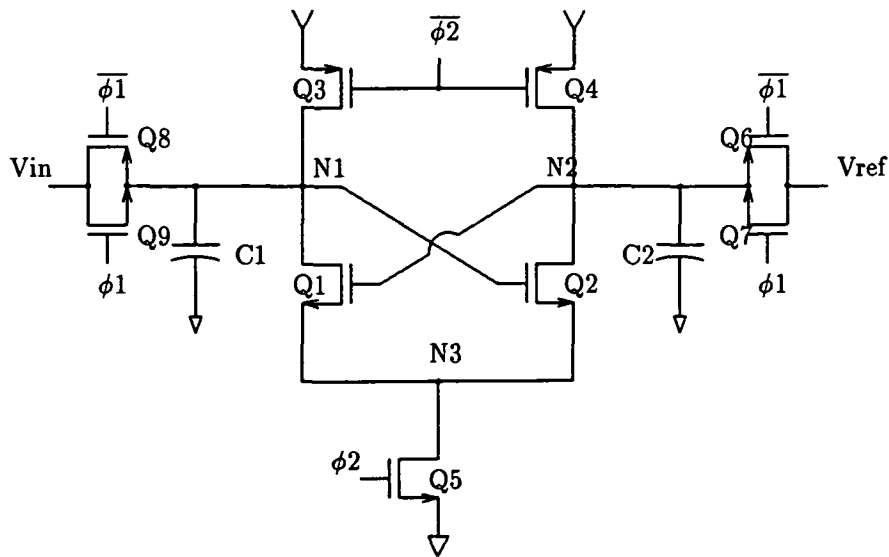
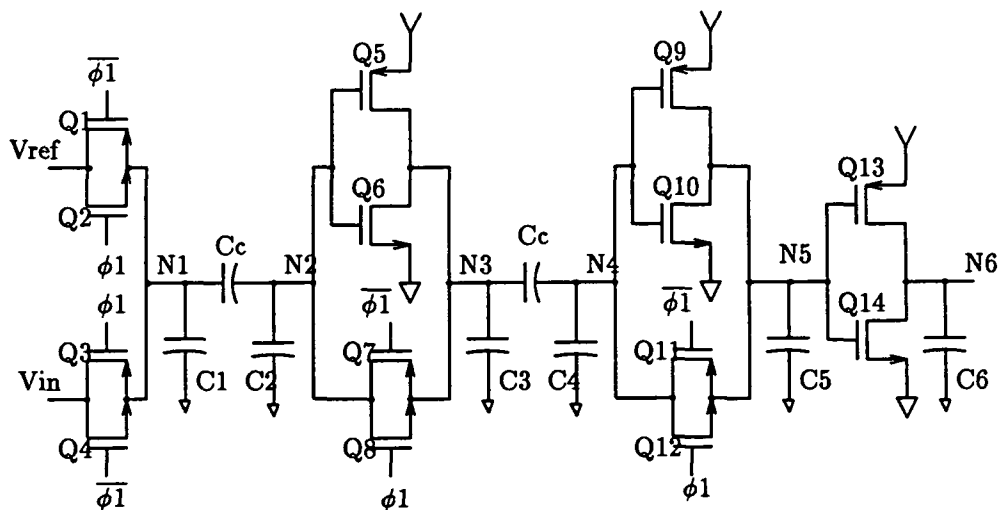Figure 5: Dual Clocked, Stored Level, CMOS Comparator

Figure 6: Three Stage, Autozeroed, CMOS Comparator

Attribute	Ranking	Comments
Size	2	14 somewhat large transistors.
Power	1	No DC paths to VSS or bias currents.
Noise Generation	1	Input signals have only minimal coupled noise.
Offset Errors	2	Offset reduced to 10mv fairly easily.
Clocking	1	Requires only one, single phase clock.
Input Levels	2	Input levels from VDD to VSS plus a threshold.
Output Levels	1	Outputs from VDD to VSS.

Table 1: Summary of Evaluations for Clocked, Precharged, Comparator

Attribute	Ranking	Comments
Size	1	Small number of transistors keeps this cell small.
Power	2	Draws power from inputs and bias current during $\phi2$.
Noise Generation	2	Some noise is transferred to input signals by C1 and C2.
Offset Errors	3	Offset harder to control.
Clocking	3	Requires two, double phase clocks.
Input Levels	3	Smallest valid input voltage range.
Output Levels	3	Reduced output voltage range.

Table 2: Summary of Evaluations for Dual Clocked, Stored Level, Comparator

Attribute	Ranking	Comments
Size	3	14 somewhat large transistors plus 5 capacitors.
Power	3	High power; large current while zeroing first two gain stages.
Noise Generation	3	Large noise transferred to inputs and to the power supplies.
Offset Errors	1	Because of autozeroing, no offset problems.
Clocking	2	Requires one, double phase clock.
Input Levels	1	Valid inputs from VDD to VSS.
Output Levels	1	Outputs from VDD to VSS.

Table 3: Summary of Evaluations for Three Stage, Autozeroed, Comparator

2.4 Other Cells

There are two other cells of some interest in the digital section of the A/D converter. First is an exclusive-or (XOR) gate. There are many XOR styles available, but a 6 transistor one was chosen primarily for its speed and low transistor count [10]. The only XOR gates with fewer transistors, require both complemented and uncomplemented input signals. This can reduce the transistor count by two in the XOR gate, but it actually increases the number of transistors in the flip-flop cell that feeds the XOR by two fairly large transistors since they are drivers. These not only add to the size of the cells, but also to the capacitance in the cell. Therefore, for overall size and speed of the converter, this XOR gate was chosen.

The other cell of interest is the encoding ROM. This ROM takes the 128 signals from the XOR gates and encodes them into to proper seven bit representation. In order to make this ROM as fast as possible, precharged logic is used. Basically, the cell functions by precharging all of the seven bit lines while the clock is low. During this time, all of the discharge transistors are turned off. Then during the high phase of the clock, the appropriate bit lines are discharged, and the correct digital representation is sent on to a bank of output drivers.

3 Layout Considerations

Because, of the speed and analog nature of this chip, the layout of the circuitry is just as critical as the circuit design. Any small oversight could introduce an error term that would make the part much less usable at higher speeds. In particular, the comparator cell was

drawn several times before a balance of all the important design criteria was reached. With the high speed digital side of the chip, there were several timing and noise challenges, as well.

The final layout of the chip core is shown in Figure 7. On the left side of the chip is the comparator chain and resistor ladder. A guard ring surrounds this section to isolate it from the digital side of the chip. The analog side is also fed from a power supply separated from the digital side, again to keep the sensitive analog circuitry as isolated as possible.

The dimensions of the core are $2,244$ microns by $3,972$ microns. The core was intentionally left in this rectangular fashion for several reasons. First, to square up the chip would either require several turns in the resistor ladder or running several critical signal lines over susceptible circuitry. Both of these options are very undesirable because of the potential error terms that would be introduced. Additionally, since the long term purpose of this converter is to be used as a macrocell on a larger chip, there is really no need for the converter to be square. Therefore, it was decided to leave the core slightly rectangular.

3.1   Comparator Layout

The comparator cell layout was the most critical layout on the chip. This is because the accuracy of the A/D converter is primarily set by performance of the comparator. Also, the speed of the converter is limited by the speed of the comparator. The layout for the cell is shown in Figure 8. (Refer back to Figure 4 for a schematic of this comparator.)

Because there is a stack of 128 of these cells, it was necessary to layout the comparator horizontally. Also, to minimize the comparator's offset, it was necessary to draw the cell symmetrically. This symmetry keeps the transistors as balanced as possible. The final size of the comparator cell is 317.2 microns by 24.8 microns.

It is difficult to simulate or calculate the exact amount of noise, offsets, and other error factors that may occur in this comparator, because they are so dependent on manufacturing tolerances. This fact is complicated by the lack of analog process modeling done for the CMOS-34 process. This process is primarily intended to be a digital, not analog, process. Therefore, every attempt was made in layout to optimize the comparator cell so that the most accurate cell possible in CMOS-34 would be created while retaining the desired speed characteristics.

Offset and noise effects were modeled into the comparator cell simulations in an attempt to ensure the accuracy of the circuit. As shown earlier, the offset voltage for the comparator is less than 2 mV. One half LSB accuracy is desired for the converter, so 17.5 mV of noise could appear on the inputs of the comparators and the circuit would still be within acceptable limits. Simulations that include noise sources like power supply noise, substrate noise, clocking noise, etc. show that the total error voltage that could be present on the inputs to the comparators is less than 13 mV. Therefore, this A/D converter will have better than 1/2 LSB accuracy.

On the right side of the cell is the poly-silicon strip that creates the resistor ladder. The nominal resistance of the poly-silicon strip is 670 ohms per cell. Next to the resistor is a gate capacitor structure which yields a nominal capacitance of 0.8 pF per cell. This capacitor, along with the resistor, form an RC time constant that helps to keep the reference input of
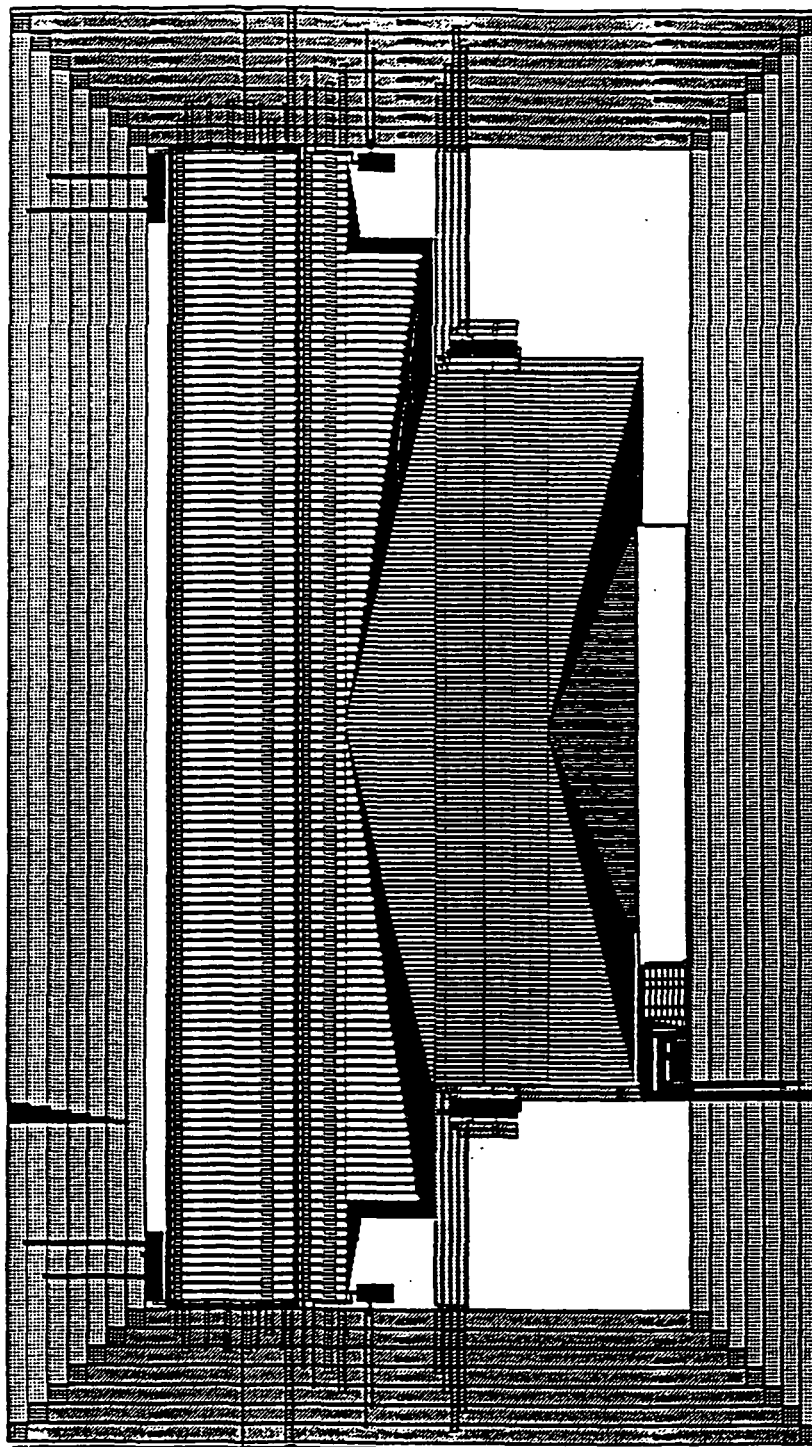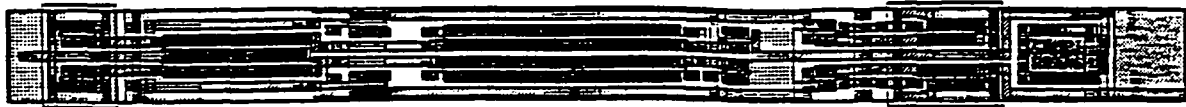
Figure 7: Layout Core of the A/D Converter

Figure 8: Comparator Cell Layout

the comparator (Vref) noise free. This in turn helps to minimize the differential errors that could occur during the conversion process from reference node noise.

Many other enhancements to the layout have been made to keep the cell as accurate as possible. First, the gates of large transistors are driven at both ends. This helps to minimize the resistance of the gate poly-silicon along the length of the transistor. Next, the source and drain diffusions of all the transistors are tied to metal down the entire length of the diffusion. This keeps source and drain resistance to a minimum, and thus increases the speed of the devices. Thirdly, the power supply lines that run throughout the cell are sized such that the noise on them (and thus the noise they couple into the cells) is kept to under 0.25 volts. If the lines were sized too small, large voltage spikes would appear on them and potentially couple into the comparator circuitry. Additionally, the cell was drawn so that signal lines do not cross over any sensitive nodes in the comparator. In certain instances, signals crossing over certain nodes could capacitively couple enough charge onto the node to corrupt or distort the comparator's operation. Also, the differential input pair of the comparator was sized minimally so that the noise that is coupled into the comparator through the parasitic capacitors of the transistor pair would be small.

3.2 Digital Cells

The stack of comparator cells feed directly into a stack of flip-flops. Recall that the comparator uses half of the clock phase for pre-charge, and the other half to evaluate the current analog input. Because of this, the output of the comparator is only valid during half the clock. This flip-flop will take the output of the comparator, amplify it to full digital levels, and turn it into a signal that is stable for an entire clock. The layout for the cell is shown in Figure 9.

In addition to accepting an analog input, these flip-flops must be able to function with worst case parameters at 100 MHz. This is extremely fast for current CMOS technologies, but simulations show that these cells work at that speed. The flip-flop has a setup time of less than 0.5 ns and a hold time of 0 ns. With these timings the flip-flop will accept 3.0 V for an input high voltage and 1.5 V for an input low voltage. It then drives the 0.6 pF of capacitance that the next cells (the exclusive or cells) presents to it in 3.0 ns.

The next stack of cells in the path of the data flow are the exclusive or (XOR) cells. The
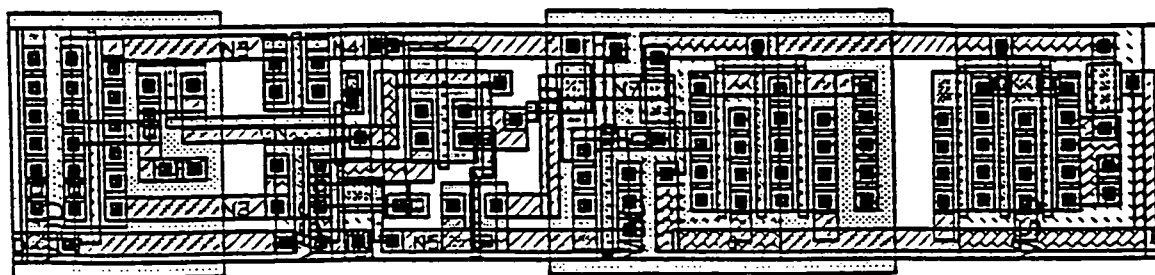
Figure 9: Layout of First Flip-Flop

output of each flip-flop, and thus each comparator, is XOR'd with its neighbor to find the point in the comparator stack where the reference voltage becomes smaller than the analog input voltage. Once this point is known, the digital output can be found through a simple memory lookup. The layout for the XOR cell is shown in Figure 10.

The remaining digital cells consist of a pulse type flip-flop, a precharged ROM, and an output flip-flop are not shown. Each cell has enlarged clock and power supply distribution networks to handle the high frequencies for which this circuit is designed. Additionally, the precharged ROM makes use of an unusual transistor configuration. The transistors in the ROM are constructed in a square or "waffle" type fashion. By doing this, the node at the center of the "waffle" has an absolutely minimal parasitic diffusion capacitance. This keeps the capacitance on the data lines as small as possible, and thus allows the ROM to function as quickly as possible. In fact, the capacitance on the data lines in the ROM cell is about 1.2 pF. This is quite small considering there are more than 64 transistor diffusions on each line. A single transistor drawn in this "waffle" fashion is shown in Figure 11.

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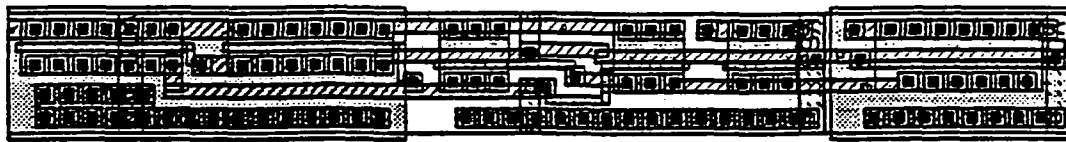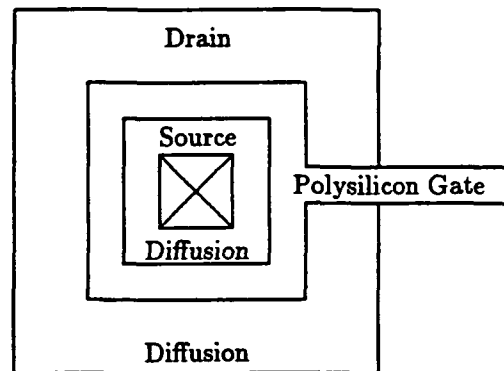
Figure 10: Layout of XOR Cell

Figure 11: Waffle Type Transistor Configuration

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