

A 1 GHz Sample Rate, 256-Channel, 1-Bit Quantization, CMOS, Digital Correlator Chip

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Abstract - This paper describes the development of a digital correlator chip with the following features:

- 1 Giga-sample/second
- 256 channels
- 1-bit quantization
- 32-bit counters providing up to 4 seconds integration time at 1GHz
- very low power dissipation per channel

The improvements in the performance-to-cost ratio of the digital correlator chip are achieved with a combination of systolic architecture, novel pipelined differential logic circuits, and standard 1.0 um CMOS process.

1 Introduction

Digital correlation spectrometers have been in use in radio astronomy since Weinreb introduced a 100-channel 1-bit autocorrelator built with transistors to measure the spectrum of radiation collected by a single antenna [8]. The power spectrum of radio astronomy signals is obtained after a Fourier transform, performed with a general purpose computer, of the correlation function.

A number of digital correlation spectrometers have been built over the past few years with either CMOS or bipolar ECL (Emitter Coupled Logic) technologies. However, existing correlators are either limited in bandwidth or in the number of channels (lags) per chip.

At Caltech, B. Von Herzen has developed a CMOS digital correlator for the Submillimeter Observatory at Hilo, Hawaii. The correlator comprising 320 channels is fabricated with a 1.0 um CMOS process and operates at a maximum clock frequency of 400 MHz with a power dissipation of 13W per chip [7]. Also at Caltech, S. Padin and S. L. Scott have developed an ECL digital correlator chip which operates with a sample rate of 250 MHz. This correlator has been installed at the Owens Valley Radio Observatory [5].

Another group of researchers from the University of Idaho led by J. Canaris and S. Whitaker have developed for NASA/JPL a 32-channel, CMOS correlator which operates with a maximum clock frequency of 25 MHz when it will be fabricated with a 0.8 um CMOS process [3]. Also at NASA/JPL a group of researchers lead by K. Chandra and W. Wilson have developed a 26-channel, ECL correlator chip capable of operating at a maximum clock frequency of 300 MHz [4].

Yet another group of researchers very active in the development of digital correlators is lead by Alexander Bos from the Netherlands Foundation for Radio Astronomy. They have constructed several digital correlators [1], [2].

At the NRAO (National Radio Astronomy Observatory) R. P. Escoffier and others have been developing different types of digital correlator spectrometers for the past two decades. Many of these correlators are installed in the VLBA Array Operation Center in Socorro, NM.

Traditionally, the CMOS technology has dominated high-density integrated circuits and bipolar ECL has been used to fabricate high-performance products. However, theoretical studies of computation in VLSI show that CMOS offers excellent opportunities for fabricating, not only moderate performance VLSI circuits, but also high performance products. Retiming can be used to transform combinational networks into systolic (maximum pipelined) structures with order-of-magnitude improvement in performance and throughout. Compared to other competing technologies (e.g., silicon bipolar, GaAs), CMOS is a technology in which transistors and wires (chip area) are extremely plentiful and inexpensive. Therefore, significant improvements in the performance-to-cost ratio could be obtained by using systolic systems fabricated with a CMOS technology.

In a prior research and development effort, we developed a novel CMOS circuit, called PDL (Pipelined Differential Logic), which is capable of operating with short propagation delays, low power dissipation and low switching noise. A total of 18 different designs using PDL circuits were fabricated for the past 6 years through the MOSIS service. A 256-bit shift register was designed with PDL circuits and it was fabricated with a 1.0 μm CMOS process. The shift register operated at a maximum clock frequency of 1 GHz [6].

2 Digital Correlator Spectrometer

The architectural organization of the correlator is illustrated in Fig. 1. The correlator calculates the correlation function of input signals A and B. To perform an auto correlation function inputs A and B are connected together. The A signal is delayed while the B signal is broadcast undelayed to all channel. Each correlator channel comprises a multiplier and an accumulator. One input of a channel receives one of the delayed signals while the other input receives one of the delayed the undelayed signal. The correlation products for each delay stage (channel) are accumulated in counters. The contents of all counters are read from the correlator by a computer for calculating the power spectrum by a Fourier transform.

A cell library using novel PDL (Pipelined Differential Logic) circuits has been developed for each logic function required by the correlator. This involved the sizing of transistors, by circuit simulation (SPICE), in order to achieve 1 GHz operation with minimum power dissipation. Since no layout was available when the first transistor sizing was performed, the loading capacitance of each interconnecting wire was estimated based on previous experience with a 1.0 μm CMOS process. In addition to the design of logic circuits, input and output circuits have also been designed to operate with 1 GHz clock signals, with standard ECL logic levels, on 50 ohm (characteristic impedance) transmission lines.

An example of PDL circuit [6], performing a 2-way exclusive-OR function, is illustrated in Fig. 2. A set of differential inputs (A, -A, B, -B) are connected to a cascade switch (tran-

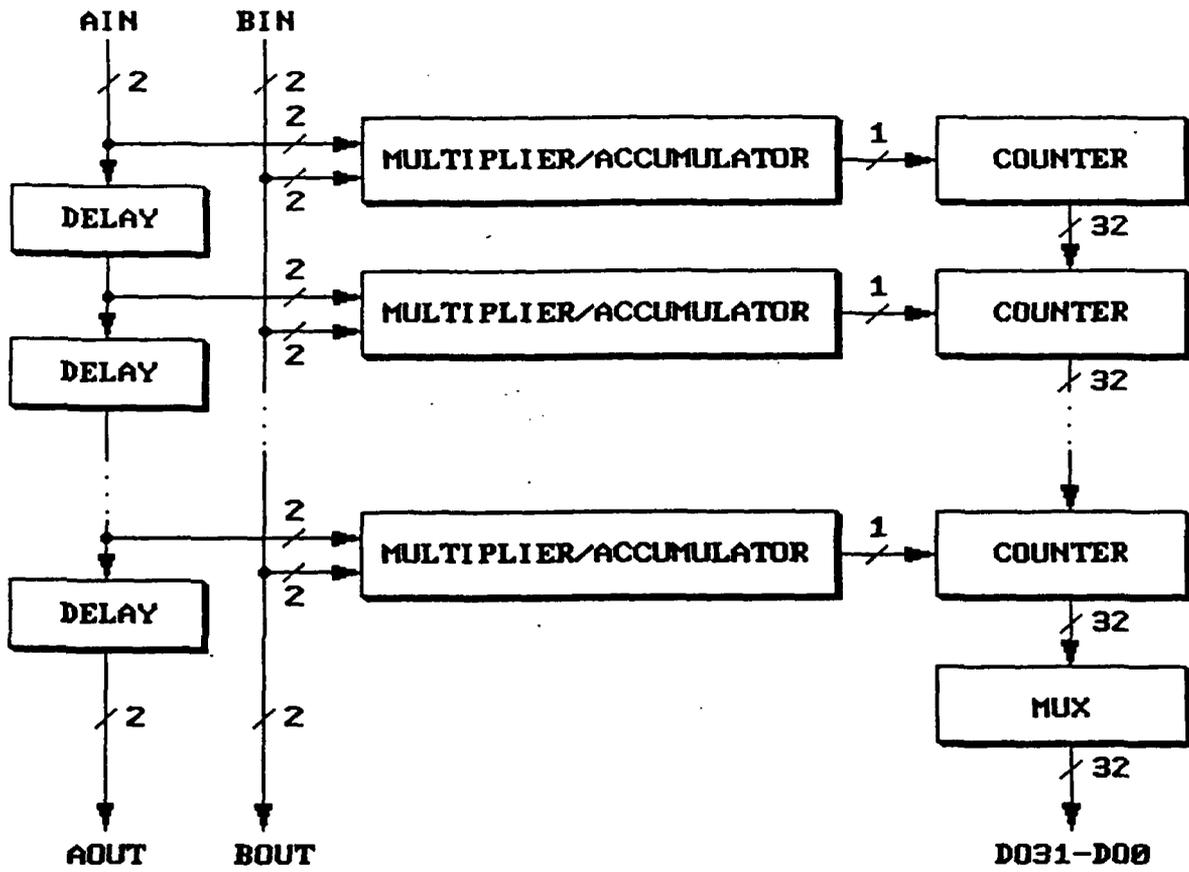


Figure 1: A block diagram of the proposed digital correlator showing the major functional elements

sistors N3-N8). A sense amplifier comprising transistors N1, N2, P1, P2 and equalization transistor N9 is connected on top of the cascade switch.

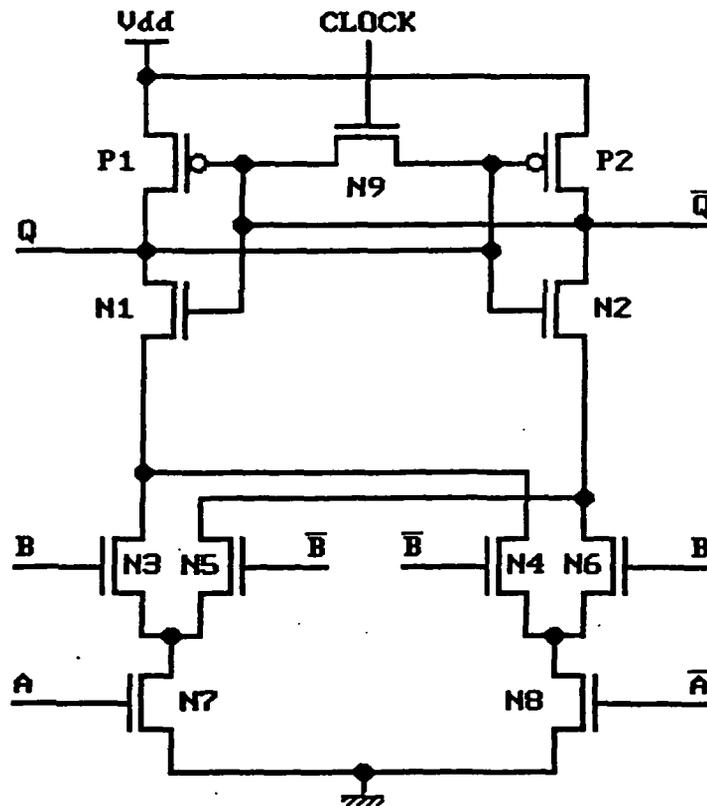


Figure 2: An example of a pipelined differential logic (PDL) circuit performing the exclusive-OR function

The PDL circuit operates in two phases. In one phase of the clock, the two output signals (Q, \bar{Q}) of the logic gate are forced by the equalization transistor to a voltage equal to one half of the power supply voltage. On a second phase of the clock, the outputs of the logic gate are partially released by the equalization transistor and the sense amplifier produces a differential output which is a function of the differential logic inputs applied to the cascade signal which has an amplitude substantially smaller than that of the power supply voltage.

The PDL circuits achieve extremely short switching time by:

1. reducing the voltage swing of the clock and logic signals
2. using a very fast current controlled sense amplifier
3. forcing the terminals of the sense amplifier to the most sensitive operating point, which is one half of the power supply voltage, before the circuit switches to valid logic levels

The performance of a very high speed PDL circuit is illustrated (Fig. 3) by an oscillogram showing the clock (top) and data out (bottom) of a 256 bit shift register fabricated with a 1.0 μm process. The voltage swings inside the chip was reduced from 5V swing, which is commonly used in conventional CMOS circuits, to only 1V. A PDL off-chip receiver amplifies an input ECL signal, with voltage swings as low as 350 mV, to PDL signals of 1V. An off-chip driver has the capability to deliver ECL levels (up to 800 mv) on 50 ohm transmission lines at a clock frequency is 1 GHz while the data out is shown at half the clock frequency. However, it is worth noting that in a pipelined system, in general, and in the 256 bit shift register, in particular, the data rate is equal to the clock rate.

After the development of a cell library in which the transistors of each logic cell had been sized with estimated loads, we perform the layout of a 16-channel 1-bit quantization correlator. We started with the placement of the power distribution buses and the clock distribution network arranged such as to accommodate a standard-cell layout style. Next, the layout of each logic cell was performed so that all logic cell had the same height but different width. The requirement for equal height was necessary so that each cell fits into the layout of power and clock structure. The logic cells have been placed and wired as indicated by the gate-level logic diagram. After the completion of all interconnections, actual loading capacitances for each logic cell were extracted and transistor sizing, with the newly available loads, was repeated. The final layout was then verified to assure that the schematic diagram had been translated correctly into mask specifications.

The fabrication of the 16-channel correlator is being done at Hewlett Packard through the MOSIS Service. The chip will be packaged in high frequency leaded chip carriers available from Triquint Corp.

3 Conclusions

The anticipated results of this project are expected to demonstrate experimentally that a 16-channel correlator will operate with a clock frequency of 1 GHz and that it will dissipate less than 1 W. The objective of a future project is to increase the number of channels per chip to 256 while maintaining the 1 GHz clock frequency and 40 mW power dissipation per channel. The 256-channel correlator will be fabricated in a 0.65 μm (L_{eff}) CMOS process (i.e., Hewlett Packard CMOS34) through the MOSIS service.

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