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Low Power, CMOS Digital Autocorrelator Spectrometer for Spaceborne Applications

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Abstract - **A 128-channel digital autocorrelator spectrometer using four 32 channel low power CMOS correlator chips has been built and tested. The CMOS correlator chip uses a 2-bit multiplication algorithm and a full-custom CMOS VLSI design to achieve low DC power consumption. The digital autocorrelator spectrometer has a 20 MHz band width, and the total DC power requirement is 6 Watts.**

1 Introduction

In the future, multi-channel spectrometers using digital correlation techniques will replace analog filterbank spectrometers in airborne, balloon and space-borne millimeter wave radiometers. The digital technique for spectrum analysis has advantages over analog filterbanks due to the inherent stability of the digital circuits, flexibility in reconfiguring the bandwidth and resolution between observations, reliability, small size, low mass and low cost of digital correlator chips for spectrometers with more than 50 channels. The digital autocorrelation technique is a proven method and has been in use in many ground-based astronomy observatories. With continuing developments in both materials, processing technologies and using novel logic circuit design, it will be possible to custom-design high speed digital correlator integrated circuits for wideband (1 GHz) and high resolution (1 MHz) spectrometers with very low DC power consumption. The Microwave Limb Sounder for the Earth Observing System (Eos/MLS) and the astrophysics missions such as the Submillimeter Intermediate Mission (SMIM), and the submillimeter lunar array are some of the flight projects that will require low power and stable spectrometers.

The Jet Propulsion Laboratory has been involved in developing low power, wideband digital autocorrelator spectrometers for the flight projects for many years. In 1990, a prototype 52-channel spectrometer using specially designed ECL correlator chip was completed and tested as proof of concept project (Chandra et al, 1990). This spectrometer was used for analyzing signals with a 125 MHz bandwidth and consumed 35 Watts of DC power. Due to the large DC power requirement, it is not suitable for spaceborne spectrometer applications; however, the ECL correlator chips will be used in balloon-borne spectrometers where the DC power consumption is not as critical.

To reduce the DC power requirements, a narrowband VLSI CMOS correlator chip was designed at the Microelectronic Research Center (MRC) at the University of Idaho in collaboration with JPL. The chip was fabricated at the Hewlett-Packard foundry at Corvallis, Oregon with a 1.2 micron CMOS process. A prototype 128-channel spectrometer was built using four of the correlator chips and it consumed only 6 Watts with a 20 MHz bandwidth.

This low power CMOS spectrometer may be used by the Eos/MLS project for its narrow-band, high resolution applications. Two spectrometers using the CMOS correlator chips will also be flown in the JPL/UCSB (University of California, Santa Barbara) balloon for astrophysics observation in 1993. The chips are also under investigation for possible use in the NOAA's (National Oceanographic and Atmospheric Administration) Microwave Temperature Sounder (MTS).

In this paper, the background information on autocorrelator spectrometers is provided followed by the design of the CMOS correlator chip and the 128-channel CMOS autocorrelator spectrometer.

2 Digital Autocorrelator

2.1 Background

The autocorrelation function of a signal is expressed as follows:

$$R(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_0^T f(t)f(t+\tau)dt \tag{1}$$

where $f(t)$ is the input signal,
τ is the delay time and
T is the integration time.

A theorem due to Wiener and Khintchine (Robinson, 1974) relates the autocorrelation function measured in the time domain to power spectrum in the frequency domain by the Fourier transform using the following equation:

$$S(f) = \sum_0^\infty R(\tau) cos\ 2\pi\ f\tau d\tau \tag{2}$$

where $S(f)$ is the power spectrum of the input signal.

Because the autocorrelation function is an even function, only the cosine transform is required. In the digital autocorrelator, shown in Figure 1, the input signal is band limited, sampled at the Nyquist rate and digitized to a few bits. The sampled signal is delayed using shift registers and multiplied with the undelayed sample using simple logic circuits. The multiplier output from each delay stage is accumulated in a binary counter. Each delay stage is called a channel or lag. The autocorrelation function for the sampled data can be expressed as:

$$R(n\delta t) = \frac{1}{K} \sum_{m=0}^{K-1} [X(t_(0)x(t_0 + (n+m)\delta t)] \tag{3}$$

where $n = 0, 1, ...N-1$ represent the delay in one of the signal paths,
K is the number of products in the integration time T,
$\pm$ is the delay, usually made equal to to the sampling interval.

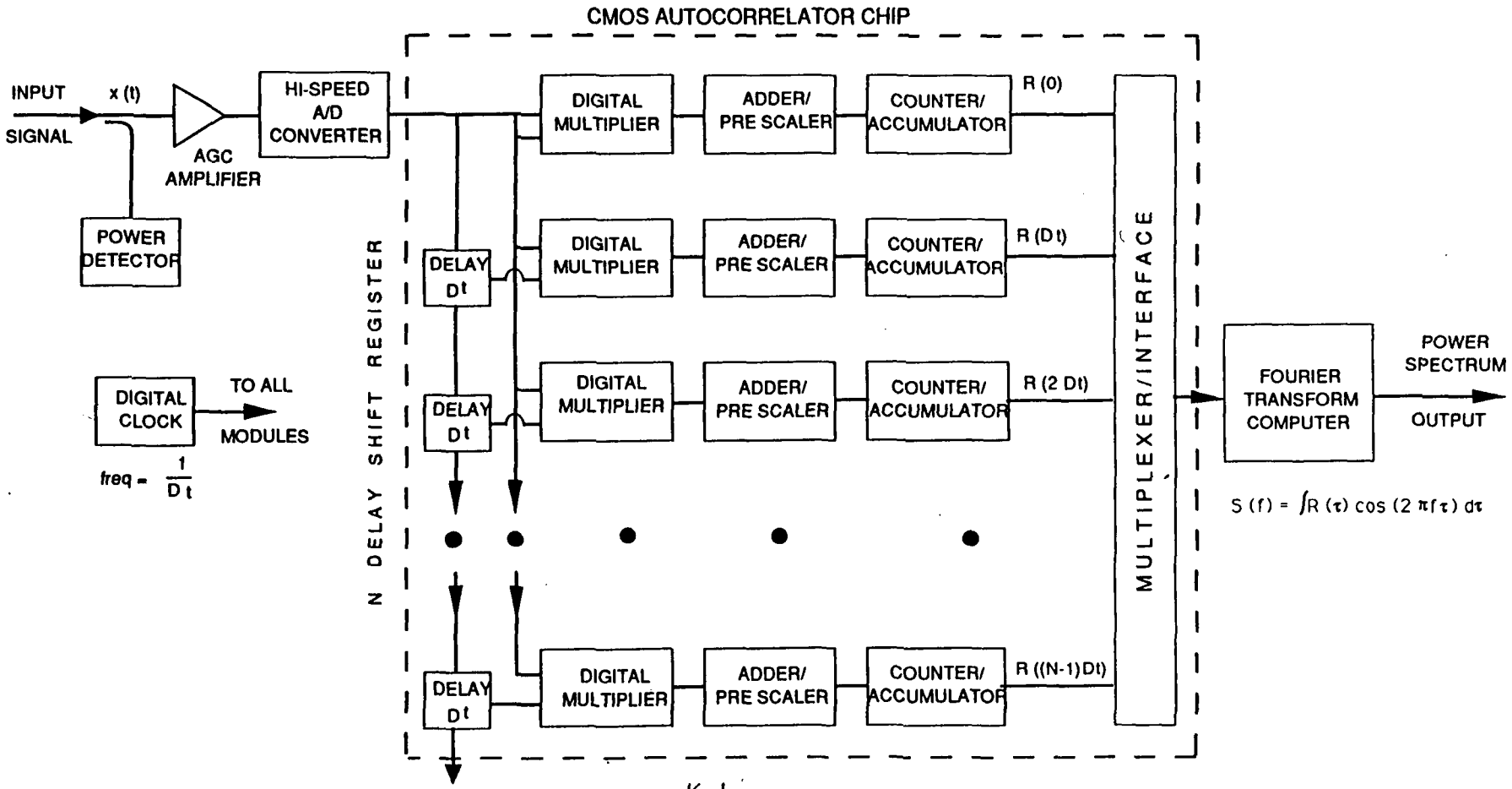

Fig. 1. DIGITAL AUTOCORRELATOR SPECTROMETER

The digital spectrometer uses the relationship between the autocorrelation function of the signal and its power spectrum by performing a Fourier transform on the autocorrelation data. The N channels or lags (corresponding to the N delay values) in the autocorrelation function, measured in the time domain, are transformed into N points on the frequency domain by using the Discrete Fourier transform (DFT) relationship,

$$P\frac{j}{2N\delta t} = \frac{1}{N}[R(n\delta t)cos(\pi nj/N)], j = 0, 1, ..., N-1 \quad (4)$$

where $P(j/2N \pm t)$ represents the power on the jth point on the output spectrum,
$R(0)$ is the correlation coefficient for the zero delay channel (=1 after normalization)
and $R(n \pm t)$ is the normalized autocorrelation coefficient for delay $n \pm t$.

Generally the input signal is digitized to only a few bits. Limiting the number of bits speeds up the multiplication and addition process because only a few digital operations are required. This permits the use of higher sampling frequency which increases the input bandwidth. However, the Signal to Noise Ratio (SNR) of the correlator is degraded by using only a few bits. The loss in SNR is 13% when two bit digitization is used with the correlator (Cooper, 1970). When more than two bits are used to digitize the input signal, the SNR increases rapidly to that of a continuous correlator. Quantizing schemes where the input signal is represented by more than two levels have also been considered by others (Cooper, 1976). However, the size and the complexity of the digital logic grows as the number of bits to represent the input signal increases. This will be of particular concern for space applications because the DC power requirement increases as the gate count is increased. The two-bit correlator scheme offers a reasonable trade-off between sensitivity and the size of the hardware which determines the DC power requirement for the logic circuit.

2.2 Digitizer

The first element in the digital correlator is the analog to digital converter is called the digitizer. The sensitivity and the stability of the spectrometer is determined by the digitizer characteristics such as threshold stability, gain variation, sampling aperture width and the uncertainties in the sample timings due to slow clock edges or jitter. The correlator sensitivity is decreased due to increase in the digitization noise by adverse effects in the above parameters.

The digitizer outputs a two-bit word for every sample of the input analog signal. One of the bits represents the sign (zero-crossing detector output) and the second bit represents the magnitude. The four states of the two-bit digitizer and the assigned weighting factors to these states are shown in Table 1. The sign bit is assigned a value "one" if the input voltage to the zero-crossing detector is negative and is assigned a value "zero" if the input voltage is positive. Similarly, the magnitude bit is assigned a value "one" if the input voltage to a window comparator is outside the pre-determined limits, $\pm Vref$, or assigned a value "zero"

SIGN	MAGNITUDE	WEIGHT
1	1	$-n$
1	0	-1
0	0	$+1$
0	1	$+n$

Table 1:

if the input voltage is between the limits.

For $n = 3$, setting the decision levels for the magnitude comparators at a level equal to the RMS voltage of the input signal gives an optimum SNR of 88% relative to the continuous correlator (Cooper, 1970).

2.3 Correlator Multiplier

Since the correlation is a multiplication and averaging process, the digitized signals represented as in Table 1 are multiplied after one of the signals is delayed in time using shift registers. A special multiplication algorithm (Cooper, 1970) is used to generate the products as shown in Table 2.

	Undelayed Signal				
Delayed Signal	SM	11	10	00	01
	11	+3	1	−1	−3
	10	1	0	0	−1
	00	−1	0	0	1
	01	−3	−1	1	3

Table 2:

The inner products are deleted which results in 1% loss to the correlator sensitivity (Cooper, 1976). A bias of +3 is added to the normalized multiplication Table 2 so that only positive numbers need to be added using full adders during each successive multiplication. Table 3 shows the final multiplication algorithm used in the hardware realization.

	Undelayed Signal				
Delayed Signal	SM	11	10	00	01
	11	6	4	2	0
	10	4	3	3	2
	00	2	3	3	4
	01	0	2	4	6

Table 3:

The binary coded output from the multiplier is added using a four bit adder and the carry output from the adder is accumulated using ripple counters.

2.4 Accumulators

The product from the 2-bit multiplier logic is counted using binary ripple counters. The length of the binary counters is determined by the rate at which a computer will be allowed to read the counter values. Typically the computer readout will occur a few times a second to once a second. The counter length is determined by the number of product terms that can be accumulated during each integration time. However not all the bits of the counter chain are readout to the computer and this reduces the size of the readout logic. In practice $(M/2)-3$ bits are discarded where M is the total number of bits in the binary counter chain (Cooper, 1976). A simple interface circuit is used to read the counter values from each delay channel in a short time compared to the integration period to minimize the "dead time" between each integration.

3 128-channel CMOS Autocorrelator Spectrometer

The prototype 128-channel autocorrelator spectrometer used four CMOS correlator chips. The chip was custom-designed at the Microelectronic Research Center (MRC) at the University of Idaho (Canaris, Whitaker, 1990) and fabricated at the Hewlett-Packard foundry at Corvallis, Oregon using 1.2 micron CMOS process. It measures 5.24 X 4.32 millimeters and is packaged in a 48-pin quad flat pack for surface mounting on a printed wiring board. The chip has 32 channels, consumes 400 milliWatts of DC power at 40 MHz clock speed. It also has 24-bit binary ripple counter in each channel and interface circuits for the computer to readout the correlated data. The block diagram of the 128-channel autocorrelator spectrometer is shown in Figure 2.

The CMOS autocorrelator spectrometer consists of two hardware modules. They are: amplifier and 2-bit analog to digital converter module and the 128-channel autocorrelator module. In addition, a personal computer (PC) and a digital I/O board are used for the autocorrelator data acquisition and spectrum calculations. The hardware modules are fabricated in multilayer printed wiring boards with controlled line impedance for handling the high frequency digital signals. Surface mount devices (SMD) are used for most of the logic gates. The power consumption for the two modules is about 6 Watts at a 40 MHz clock speed.

3.1 Low Power 2-bit Digitizer

The first circuit in the 128-channel autocorrelator spectrometer is a 2-bit digitizer. The amplifier is a part of the digitizer module and it consists of an AGC amplifier, and an op-amp which drives three ultrafast TTL comparators. The op-amp provides gain to the analog signal and impedance matching at the comparator inputs. The analog input to the comparators is set at 3 volts peak-to-peak across an equivalent resistance of 150 Ohms.

The three comparators are ultrafast TTL comparators, 9698KR and 9696KR, made by Analog Devices, Inc. The 9698KR is a dual comparator chip and it is used as the magnitude comparator. The 9696KR is a single comparator chip used as the sign or zero-crossing detector. The threshold voltages - two for the magnitude comparators, $+VTH$ and $-VTH$,

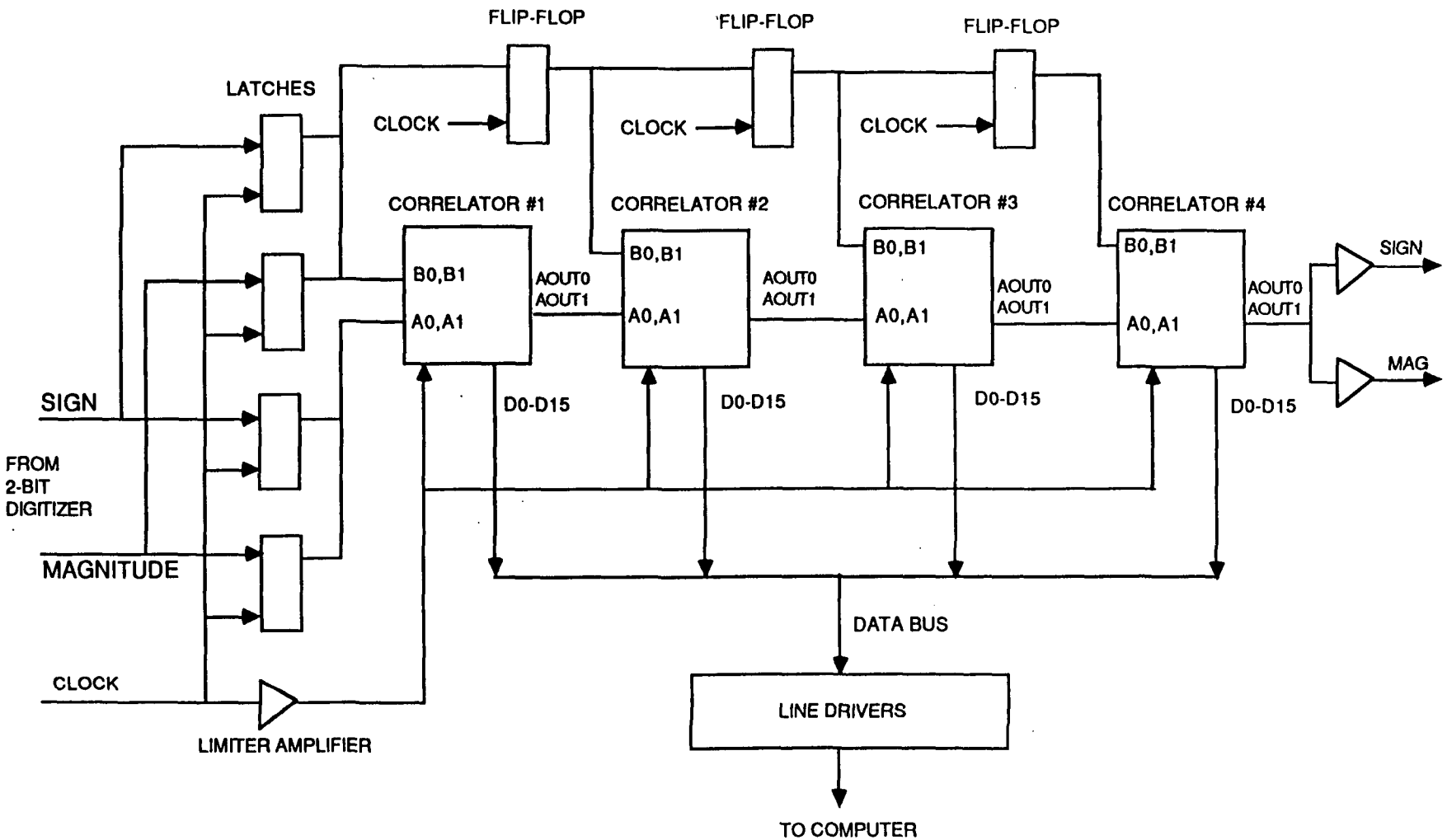

Fig. 2. 128-CHANNEL AUTOCORRELATOR BLOCK DIAGRAM

and one for the sign or the zero-crossing detector, VT0 - for the comparators are derived from a high stability voltage reference amplifier. The three threshold voltages can be set by low noise potentiometers. The three comparators digitize the input analog signal into a two-bit word shown in Table 1. The 2-bit data from the digitizer module is the input to the correlator module.

3.2 CMOS Correlator Integrated Chip

The CMOS correlator chip is an Application Specific Integrated Circuit (ASIC) implemented in VLSI technology. The chip performs 2-bit multiplication of digitized signal as given in Table 3. The main features of the correlator chip are listed below.

1. Autocorrelation or cross-correlation
2. 32 channels and integral binary ripple counter in each channel
3. Low power ($\leq$ 12 milliWatts per channel at 40 MHz clock rate)
4. Can be cascaded to increase the number of channels
5. Selectable auxiliary data input ports
6. Integration can continue while data is being sent to the computer
7. CMOS and TTL compatible input and outputs

3.3 128-channel Autocorrelator

The 128-channel autocorrelator spectrometer uses a four layer printed wiring board. The four correlator chips are mounted on a special carrier printed circuit board. The correlator board, shown in Figure 3, has circuits to drive the correlator clock input, to readout the channel data and a timer circuit to signal the end of an integration period. A programmable 32-bit timer IC counts the correlator clock and generates a pulse every 0.8 second. This pulse interrupts the correlation and the chip transfers the correlated counts in the 24-bit binary ripple counter into a shift register within the correlator chip. The chip also sets a data ready flag. The computer polls the data ready flag and resets the timer for a new integration cycle. The computer then reads the counter values in the shift register by generating a series of readout clocks until all the counter data is read. The correlator board has a hardware jumper connection to select the data output in either 8-bit byte or 16-bit word mode. The computer can also do post integration of the counter values.

The input clock and the output data lines of the four correlator chips are connected in a bus structure. The input clock to the correlator chips is also the sampling clock used in the digitizer. The prototype correlator chips require that the clock "high" input should not be more than 2.8 Volts. A limiter amplifier is used to limit the clock amplitude to the correlator chips. Also, to reduce the current transients due to simultaneous switching, the computer generated readout clock is skewed with respect to the correlator clock edges.

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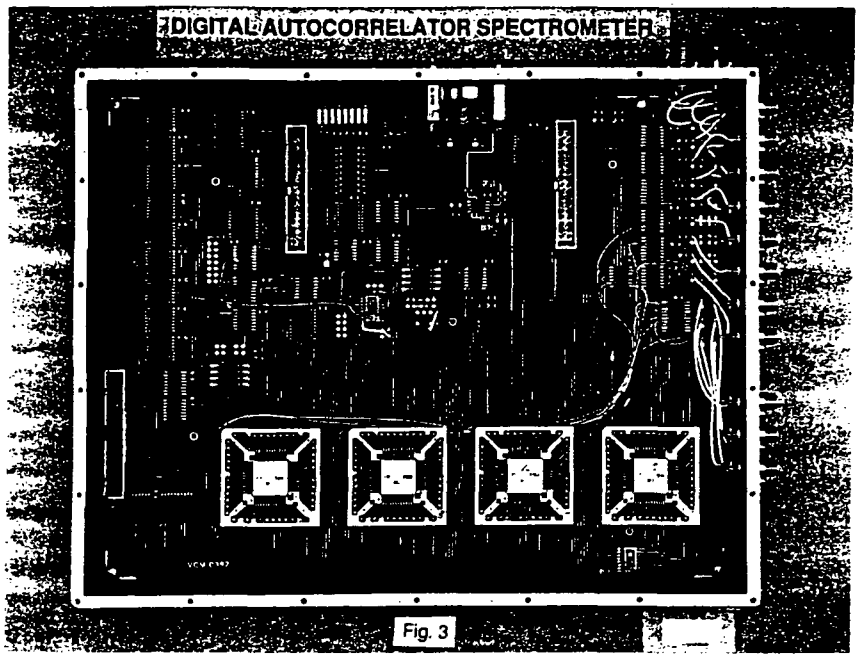

3.4 Computer Interface

The output data from the correlator module is CMOS/TTL compatible. A Burr-Brown, digital I/O board (PCI-20087W-1) is used with the computer to read the data from 128 channels in byte mode. The digital I/O board, under program control, reads each correlator chip's counter values from the output shift register by generating 96 readout clock pulses. Under program option, post integration and the averaging of the channel data can be performed in the computer before the Fourier transform is done on the autocorrelator data. Also, before the Fourier transformation, a continuous correlation function is obtained by applying a correction formula to the 2-bit correlation values.

$$R_{cont} = 1.146R_2 - 0.049R_2^2 \; for \; 0 \leq R_2 \leq 0.9 \tag{5}$$

$$R_{cont} = 1.34R_2 - 0.034R_2^2 \; for \; 0.9 \leq R_2 \leq 1.0 \tag{6}$$

where *Rcont* is the correlation coefficient for the continuous correlator and R_2 is the correlation coefficient using 2-bit digitization.

The above formulas are derived from the conversion table given by Cooper (1970). The computer uses separate programs to acquire the autocorrelation data, display the autocorrelation function, perform a 128-point cosine Fourier transform and display the power spectrum.

4 Power Spectrum Measurements

Tests on the correlator module were done with both static and dynamic inputs. The test setup is shown in Figure 4. A frequency synthesizer was used for generating the sample clock and a second synthesizer was used as the analog signal source for measuring the frequency and spacing of the channels. A stable, wideband noise source was also used as the input signal for the power spectrum measurements. The synthesizer frequency for the sampling clock was set at 25 MHz. The amplitude from the second synthesizer was set to give a 3 volts peak to peak signal at the three comparator inputs. The frequency of the second synthesizer was varied and the output spectrum from the autocorrelator spectrometer was displayed for each frequency setting. This test verified that the input frequencies appeared at the right channels after the autocorrelation and its Fourier transform. For the test with a noise source, a 19.8 MHz low pass filter was used at the digitizer input to eliminate alising of frequencies above 40 MHz which was used as the (Nyquist) sampling frequency. The results from the spectrum measurements made with a CW signal and a band limited noise signal are shown in Figure 5(a) and 5(b).

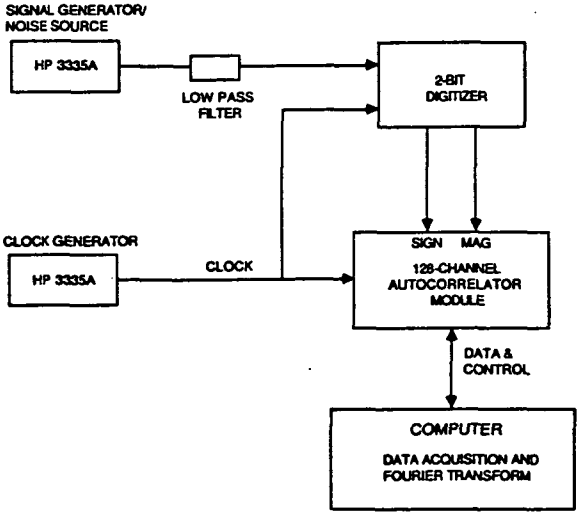

Fig. 4. 128-CHANNEL CMOS AUTOCORRELATOR TEST SETUP

One important test is to measure the stability of the spectrometer. According to the radiometer formula, the standard deviation of the power spectrum decreases with the increase in integration time as given by the equation:

$$\frac{\delta T}{T_{sys}} = \frac{2\beta}{\sqrt{B_N T}} \tag{7}$$

where $\pm T$ is the expected RMS value,
T_{sys} is the system noise temperature,
$B_N = 0.5/\tau_{max}$ is the noise bandwidth
β is the quantization loss factor (= 1.13 for two-bit correlator),
T is the integration time.

The factor 2 in the above equation is due to spending equal time on the signal and reference measurements and then subtracting two noisy signals for the RMS calculations. For the RMS calculations, two sets of spectra were measured, each set of two spectra for 0.8 and 80 seconds, with no difference in the input power level. One of the spectra is subtracted from the second and is gain normalized by the second spectrum. This is generally referred to as Y-factor measurement and expressed as where $\pm T$ is the expected RMS of input spectrum. Normally the Signal has the spectral feature of interest and the Reference is a comparison spectrum having uniform power over the bandwidth. The stability test showed that the spectrum RMS decreased with the increase in integration time and agreed closely with the calculated value.

5 Conclusion

Though the CMOS correlator chips were initially specified for 25 MHz clock speed, the tests revealed that the chips can be clocked at 40 MHz. Due to its low DC power consumption, and stability of at least 80 seconds the spectrometer is well suited for signals with bandwidth up to 20 MHz and high spectral resolution.

Acknowledgement

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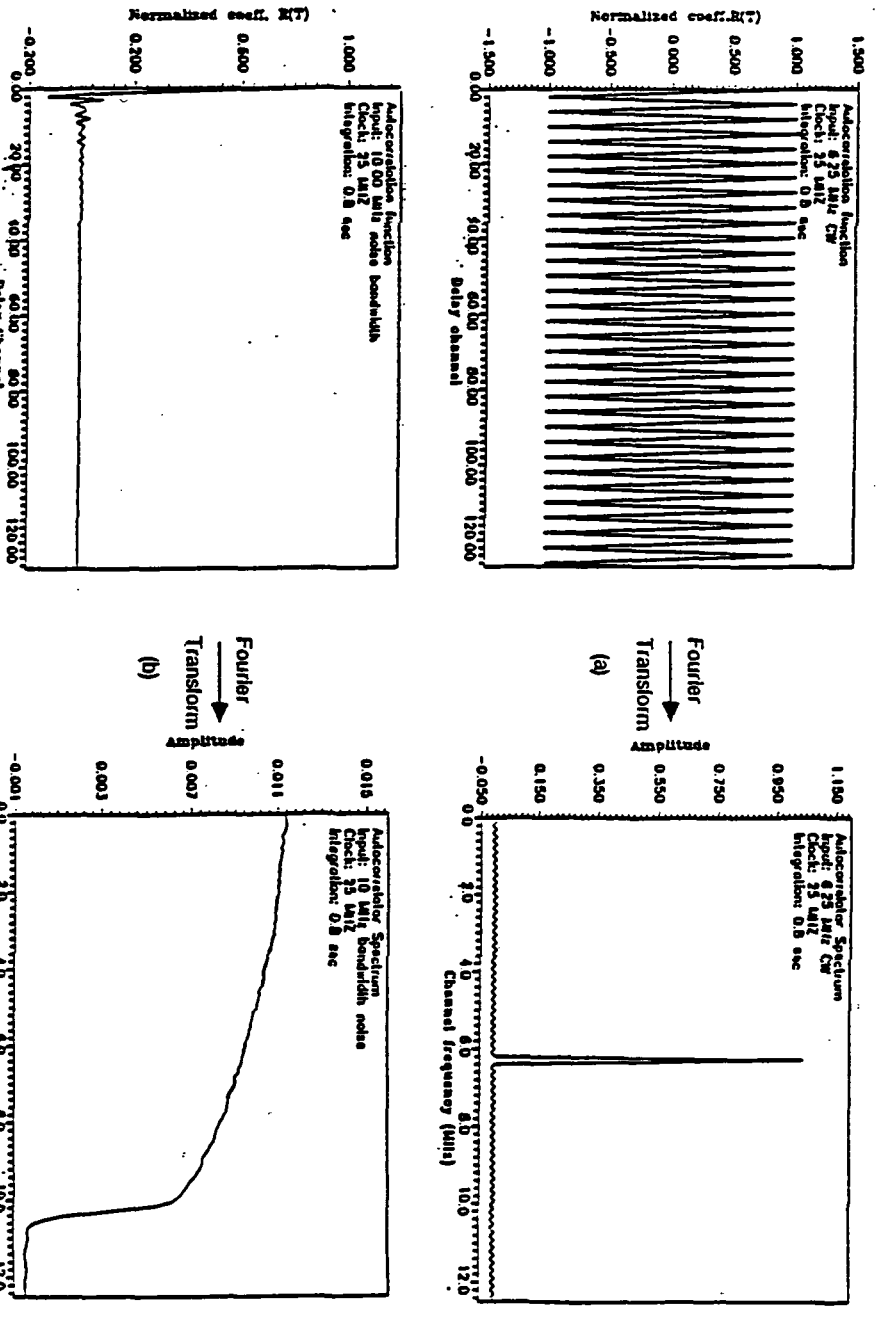

Fig. 5. AUTOCORRELATOR SPECTRUM MEASUREMENTS