A NEW HIGH-SPEED IR CAMERA SYSTEM

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ABSTRACT

A multi-organizational team at the Goddard Space Flight Center is developing a new far infrared (FIR) camera system which furthers the state of the art for this type of instrument by incorporating recent advances in several technological disciplines. All aspects of the camera system are optimized for operation at the high data rates required for astronomical observations in the far infrared. The instrument is built around a Blocked Impurity Band (BIB) detector array which exhibits responsivity over a broad wavelength band and which is capable of operating at 1000 frames/sec, and consists of a focal plane dewar, a compact camera head electronics package, and a Digital Signal Processor (DSP)-based data system residing in a standard 486 personal computer. In this paper we discuss the overall system architecture, the focal plane dewar, and advanced features and design considerations for the electronics. This system, or one derived from it, may prove useful for many commercial and/or industrial infrared imaging or spectroscopic applications, including thermal machine vision for robotic manufacturing, photographic observation of short-duration thermal events such as combustion or chemical reactions, and high-resolution surveillance imaging.

INTRODUCTION

For astronomical imaging applications, large two-dimensional detector arrays can cover proportionally more sky in less time than single elements or linear arrays. Using a small telescope with a wide field of view and a suitably designed camera, astronomers can use such arrays to study the structure of star-forming regions in our own galaxy or distant galactic clusters. At visual and near-infrared wavelengths, the technology of silicon charge-coupled device (CCD) imagers is well understood, highly developed, and widely used, from astronomical instruments at the world's leading observatories to the hand-held video recorders found in many homes; arrays have been produced in formats as large as 4096x4096 pixels. Only recently, however, have two-dimensional arrays been developed for observations at far-infrared wavelengths. For example, the Rockwell Science Center has developed hybrid focal plane arrays (HFPAs) based on Blocked Impurity Band (BIB) technology. These HFPAs exhibit excellent responsivity over a broad wavelength band (see Fig. 1) and are capable of operating at 1000 frames/sec. [1, 2]

Ground-based and airborne observations at far-infrared wavelengths differ in two important aspects from comparable observations at visual wavelengths: i) the level of random background radiation from the telescope, as seen at the focal plane, is considerably higher than the level of radiation from distant astronomical targets; and ii) the relative level of atmospheric transmission can vary on the time scale of hours due to variations in line-of-sight water vapor. We have designed a high-speed camera system optimized for operation within these two constraints. To accomodate the high radiative background, we exploit the high-speed readout capability of the BIB array. A compact camera head electronics package continuously reads out and acquires data from the array at top speed, preventing it from saturating, while a digital signal processor (DSP) - based data system performs co-addition of frames in real time to improve the contrast. To monitor changes in atmospheric transmission, we have incorporated in our optical design a simple diffraction grating. This allows the instrument to operate as a spectrometer, and can be inserted into or removed from the optical path by means of a mechanical actuator.

Infrared detectors have been produced from a variety of materials and in a variety of formats to sense radiation from the near infrared (1.0μm) to the far infrared (longer than 20μm). The choice of detector technology is driven by the specific requirements for the imaging task that needs to be accomplished. Although our instrument is designed around the BIB array, all of the electronics in the system have sufficient flexibility and modularity of architecture to accommodate other detector technologies for other applications.

SYSTEM OVERVIEW

A block diagram of the camera system is shown in Fig. 2. The BIB detector array and system optics are housed in a bench-top vacuum dewar. Infrared radiation from the telescope enters the dewar though a window in the outer case and is filtered by optical elements prior to focusing. The array is driven by a compact electronics package consisting of 6 boards: a timing generator, a clock driver/bias board, and 4 correlated double sampler (CDS) boards. This complement of boards provides all clocks and DC bias voltages required to operate the BIB array and digitizes its

analog output signals. Mounted on the outside of the dewar is a compact four-channel preamplifier module -- one channel for each output of the array. The preamplifier outputs are capable of driving 50Ω coaxial cable with very fast settling times, allowing the rest of the camera head electronics to be located several feet from the dewar. Digitized data from the camera head electronics is sent to the data system over four optical fibers, allowing the data system to be located arbitrarily far away and isolating the camera head from electrical noise generated by the data system.

The data system consists of four custom DSP circuit boards residing in the backplane of an IBM-compatible personal computer (PC). Each DSP board processes digitized detector data from one output port of the BIB array. The data is accumulated in local memory on the DSP board and is collected, post-processed, displayed, and stored by the host central processing unit (CPU) following a complete observation.

FOCAL PLANE DEWAR

The camera/spectrometer optics and the BIB array are housed in a LHe reservoir dewar produced by Infrared Laboratories, lowering their temperature to approximately 4°K to reduce background radiation produced by the optics and thermally-generated signal produced by the BIB array. The cold plate of the reservoir is 8 inches in diameter. The optical path in the dewar is a folded, two-level design which attaches to the cold plate as a module and can be easily removed for alignment and test; we illustrate the design in Figure 3. The module is built up on a deck, also 8 inches in diameter, which divides the optical path into upper and lower sections for re-imaging and spectroscopy, respectively. The deck is elevated above the cold plate by means of precision machined, thermally conductive standoffs. The BIB array looks into the exit pupil of the optics module. Both sections of the optical path use pair-wise off-axis parabolic mirror segments. The segments are matched in a complementary fashion so as to cancel the aberrations normally incurred by a single off-axis mirror. The mirrors are fabricated from copper for high thermal conductivity, diamond-turned for an accurate figure, and gold-plated for high reflectivity.

The re-imaging portion of the optics module combines two off-axis paraboloids with differing focal lengths for a resultant focal plane magnification of 1.5. A single rectangular flat mirror folds the beam to accommodate the 8" diameter of the deck. The imaging section also includes a pupil stop and an adjustable filter slide. The pupil stop restricts the camera's field of view to the secondary and primary mirrors. Band-pass optical filters mounted on the filter slide restrict the spectral pass band of the camera for both imaging and spectroscopic observations. The parabolic mirror segments and a second beam-folding mirror form a second focal plane image at the deck's midplane. A bistable slide actuator positions a long-slit field stop in an opening at this location during spectroscopic observations.

The spectroscopic portion of the optics module contains two identical off-axis parabolic mirror segments and a second bistable actuator for a two-sided mirror/grating mount. The mirror/grating mount actuator is operated in conjunction with the field stop actuator. In the imaging configuration, the mirror re-images the midplane field stop onto the infrared active portion of the BIB array. In the spectroscopic configuration, an echelette grating is used to disperse light along the dimension of the restricted midplane field stop. Spot diagrams computed for the system suggest that the distortion of point sources at the outer edges of the focal plane's field of view are expected to lie within the area of a single pixel of the array. Our initial grating selection provides a dispersion of 20-40μm with a spectral resolution of $\lambda/\Delta\lambda \approx 30$.

The BIB array is located beneath the exit pupil of the optics module. Thermal coupling to the cold plate is made via a "cold finger", onto which the array package is gently clamped, while electrical connections are made by means of a printed circuit board with a socket which fits the array package. Individual coaxial cables are soldered directly to the printed circuit board to bring clock and bias signals to the board from the dewar electrical feedthrough and to return analog outputs to the preamplifiers. Simple transistor follower circuits on the printed circuit board protect the array outputs against external short circuits and reduce the output impedance of the array, allowing the transmission of high-speed analog signals over short lengths of coaxial cable to get to the external preamplifiers.

CAMERA HEAD ELECTRONICS

In the main camera head electronics package, the timing generator produces all of the digital signals required to operate the array and control the operation of the CDS boards. The circuit is based around the Am29CPL154 field programmable controller (FPC), produced by Advanced Micro Devices. This approach to timing generation is compact, flexible, and reprogrammable, and has a long heritage at GSFC. [3] The timing generator circuitry is completely isolated from all other camera head circuitry via optocouplers and an isolated power supply. Four clock signals are required to operate the BIB array; ten others are required to control the operation of the CDS boards. Four input lines are provided for interfacing to the data system or other external components.

The clock driver/bias board accepts logic level (0 to +5V) timing signals from the timing generator and shifts their voltage levels to meet the requirements of the BIB array multiplexer (+3 to +7V). It also generates the DC bias voltages required by the array. These voltages are referenced to a "virtual ground" which is at 0V with respect to the ground of the clock driver circuitry, but which is isolated from it. Both grounds are carried to the array fanout board in the dewar and kept separate, so that sensitive analog signals originating in circuits biased by the DC voltages are not corrupted by transient voltage noise on the clock lines.

The circuit design of the preamplifiers, and the way in which they are packaged and connected to the array, are critical to the preservation of the integrity of the analog output signals; the settling time (to 12-bit accuracy) of the analog signals, as measured at the input pins of the analog to digital converters (ADCs) must be in the 20-40ns range in order to fully realize the capability of the array. Low capacitance coaxial cables inside the dewar bring the buffered analog signals to the dewar electrical feedthrough, where they are mated with controlled-impedance connectors to get to the outside. The close proximity of the preamplifier package to the feedthrough assures a minimum cable run. The preamplifier package is carefully shielded against both radiated and conducted interference.

The CDS boards incorporate several significant new technologies to achieve a high degree of functionality in a compact form factor. The boards are designed around the ADS-119 ADC, produced by Datel. This part is a complete sampling 12-bit converter which employs a two-pass subranging scheme to achieve a maximum sample rate of 10MHz. The CDS board has sockets for two ADCs, and is capable of operating both at the maximum data rate that the BIB array will allow; however, in order to provide a "clean" interface -- from preamplifier to CDS board to DSP board, thereby simplifying integration and test -- we have chosen instead to populate only one of the two sockets. All analog circuitry on the CDS board, including the ADCs, is isolated from the digital side via optocouplers and isolated power supplies. The analog circuit ground is connected to the "virtual ground" generated on the clock driver/bias board via the preamplifier return lines from the dewar.

The analog signals from the preamplifiers are sampled twice per pixel period -- once for the reference level and once for the video level -- hence the term "correlated double sampling". The two conversion results are written into separate registers. The reference is then subtracted from the video via addition in ones complement form. The resulting 12-bit-plus-sign number is written out in two 10-bit words, along with synchronization bits from the timing generator. All of the registers and subtraction logic are implemented in a single field programmable gate array (FPGA) IC produced by Xilinx; all control signals for the CDS board (convert commands, register writes, multiplexer select lines, etc.) come from the timing generator. The use of the FPGA allows the CDS board a large measure of flexibility in its application. The FPGA can be configured for operation with one or both ADCs and single or double sampling. In addition, the FPGA can provide digital data to a digital to analog converter (DAC), located on the analog side of the board, for control of the DC level of the analog signal.

The 10-bit data words from the FPGA are written to a "Transparent Asynchronous Xceiver Interface" (TAXI) transmitter IC, produced by Advanced Micro Devices. The TAXI is mated with a fiber optic transmitter (available from several vendors), which incorporates interface circuitry, the optical transmitter element, and an "ST"-style fiber optic connector in a 16-pin dual in-line package (DIP). Sockets for differential TTL drivers are also provided for application in systems that do not employ fiber optics.

DATA SYSTEM ELECTRONICS

To handle the high data rate of our application, we have designed a custom circuit board around the ADSP21020 floating-point digital signal processor, produced by Analog Devices. The ADSP21020 utilizes a pipelined Harvard architecture (two identical independent buses, nominally for Program and Data) to achieve an instruction cycle time of 40ns at 25MHz. Its design includes a full complement of specialized circuitry, including an on-chip instruction cache, to optimize the processor for DSP applications, and it performs 40-bit floating-point operations according to the standard published by the Institute of Electrical and Electronic Engineers (IEEE).

The program memory data (PMD) bus has over 1.5 megabytes of 12ns static random-access memory (SRAM), organized as 256K words by 48 bits, for the storage of programs and co-added (accumulated) detector data. The word width is necessary to accomodate the 48-bit instruction format of the ADSP21020. The amount of memory on the PMD bus is sufficient to contain not only the DSP operating program, but also a number of independent frame accumulator areas, depending on the detector array being used and the nature of the DSP software (for example, each output of the BIB array requires only 4K words per frame accumulator); in addition, the PMD memory is expandable by mounting a "daughter board" containing the extra memory onto headers provided for that purpose. The data memory data (DMD) bus has 320 kilobytes of high speed SRAM, organized as 64K words x 40 bits, so that any floating-point computation may take place in the DMD space without interfering with real time accumulation in the PMD space.

Each DSP board receives detector data from a CDS board over a fiber optic cable using an integrated fiber-optic receiver interfaced to a TAXI receiver. The TAXI receiver is configured to receive 10-bit words at an effective rate of 8 million words/second. When the TAXI transmitter on the CDS board is not transmitting meaningful data, it continually transmits a synchronization pattern so that the transmitter and receiver remain in lock even when not in use.

Data from the TAXI receiver are stored into a 16K word x 18-bit first-in/first-out (FIFO) memory, two words at a time. The two spare bits are ignored. The Frame Sync, Chopper, and Sign bits are stored into the FIFO along with their accompanying data word; these bits are used by the DSP software to assign incoming data to the proper frame accumulator area. Reading a word of data with the Frame Sync bit set causes the highest priority interrupt to the ADSP21020. Reading a word of data with a Chopper bit that is different from the previous pixel causes a next lower priority interrupt.

The DSP board communicates with the host CPU via a set of registers mapped into the CPU's input/output (I/O) space. These registers appear in the I/O map in a space referred to in most documentation as "prototype board" at addresses 300H - 377H. Jumpers on the DSP board configure exactly where in this space the DSP board will reside to allow the four boards to be mapped into the prototype space without conflict.

HOST CPU & SOFTWARE

The PC platform we have assembled for the data system is a rack-mounting unit with a passive Extended Industry Standard Architecture (EISA) backplane. The CPU, like the four DSPs, is on a circuit board which plugs into the backplane. The CPU card incorporates an Intel 80486DX/50 microprocessor and 16 megabytes of RAM. Other system features include: a 1 gigabyte hard disk; a 128 megabyte magneto-optical cartridge drive; 5.25", 1.2 megabyte and 3.5", 2.88 megabyte floppy disk drives, and a Super VGA video adapter.

The data system software is a custom application which provides user interface and controls real-time data processing on the DSP boards. The software handles the details of data acquisition and processing, the transfer of accumulated data from the DSP boards to the host CPU, the user interface, and display, storage, and post-processing of the data. The DSPs are running a separate program from that running on the host CPU (a conventional microprocessor) and require their own unique development environment and programming language. However, the interaction between the two pieces of software is transparent to the user -- the appearance is only that the PC platform is collecting the data, processing and storing it.

Upon initiation of the application, identical executable machine code is loaded into the PMD space of each DSP board and execution initiated. This code processes operating commands from the host CPU, controls the fiber optic interface, retrieves the detector data, co-adds the data in the frame accumulators in real time, and communicates the results to the host CPU via registers which are mapped into the CPU's I/O space. The host CPU software allows the user to specify parameters for the acquisition (i.e., number of frames to be averaged, number of on target and off target frames, trigger conditions etc.) to the DSPs, waits for acquisition to be completed, and transfers the acquired data into the main system memory for image display, storage, and post processing.

CONCLUSIONS: INDUSTRIAL/COMMERCIAL APPLICATIONS

Infrared radiation is essentially a thermal phenomenon -- the hotter a body is, the shorter the wavelength of radiation it emits. Temperature differentials which are invisible to the eye can be converted into visible images on a computer screen if the scene is imaged onto an IR detector array and then digitized. Hence, IR detectors, from the very short wavelength IR (1.0μm) to the far IR (longer than 20μm) find application anywhere where it is desired to sense thermal structure in a scene. IR detectors are commonly used in medical electronics, weather satellites, industrial process monitoring, food analysis, air traffic collision avoidance, air pollution analysis, monitoring thermal pollution from industrial effluents, and agricultural and oceanic biological content analysis, as well as a wide range of military and space applications. Generally, low-cost, rugged systems can be operated at ambient temperatures, whereas high performance, high sensitivity detection systems such as the one described in the present paper must be cooled to anywhere from 4 to 273°K, the exact temperature depending on the specific detector material and performance required. Although originally designed as an astronomical instrument, our camera system could be reconfigured for a variety of commercial and/or industrial IR imaging or spectroscopic applications, including thermal machine vision for robotic manufacturing, photographic observation of short-duration thermal events such as combustion or chemical reactions, and high-resolution surveillance imaging.

The application for which our system is designed is a very demanding one, hence the cost of the individual components required to meet the demands of the application, as well as the overall system cost, is high. However, the same basic system architecture could be implemented in less costly versions for other applications. Each of the major components -- detector array, optics, camera head electronics, data system hardware, and data system software -- could be selected, modified slightly, or redesigned to accomodate the requirements of the intended application.

The wavelength range of the BIB array may not be suitable for observing high-temperature phenomena; another IR technology, such as a platinum silicide (PtSi) photodiode array (roughly 1-5μm), for example, might be more desirable. If another detector array were chosen, it might be possible to cool it only to liquid nitrogen (LN_2) temperatures (about 77°K), which would reduce operating costs considerably, or even to use a thermoelectric cooler (TEC) if the operating temperature were higher. Clearly, our modular approach to the optical design allows a great deal of flexibility in this area. Depending on the application, cold optics might not even be required at all.

In the camera head electronics, we have already discussed the reprogrammability of the timing generator and the reconfigurability of the CDS boards. If the application does not require the high speed at which we are operating, the preamplifier module and CDS boards are two areas where cost could be reduced by using lower speed parts. Likewise, for the DSP boards, we are using the highest speed parts available in order to meet our system throughput requirements; significant cost savings could be realized by using slightly slower parts if the application would allow for it. The expandability of the DSP memory is intended to provide a simple upgrade path for use with larger format arrays. Lastly, our data system software is completely flexible with regard to detector array format and measurement scenario, limited only by the amount of memory on the DSP board and in the host system.

REFERENCES

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3. Hostetter, M., McCloskey, J., and Reed, K., "Microcontrollers Generate Timing Signals for CCD Arrays", NASA Tech Briefs, June, 1992, pp. 41-42.

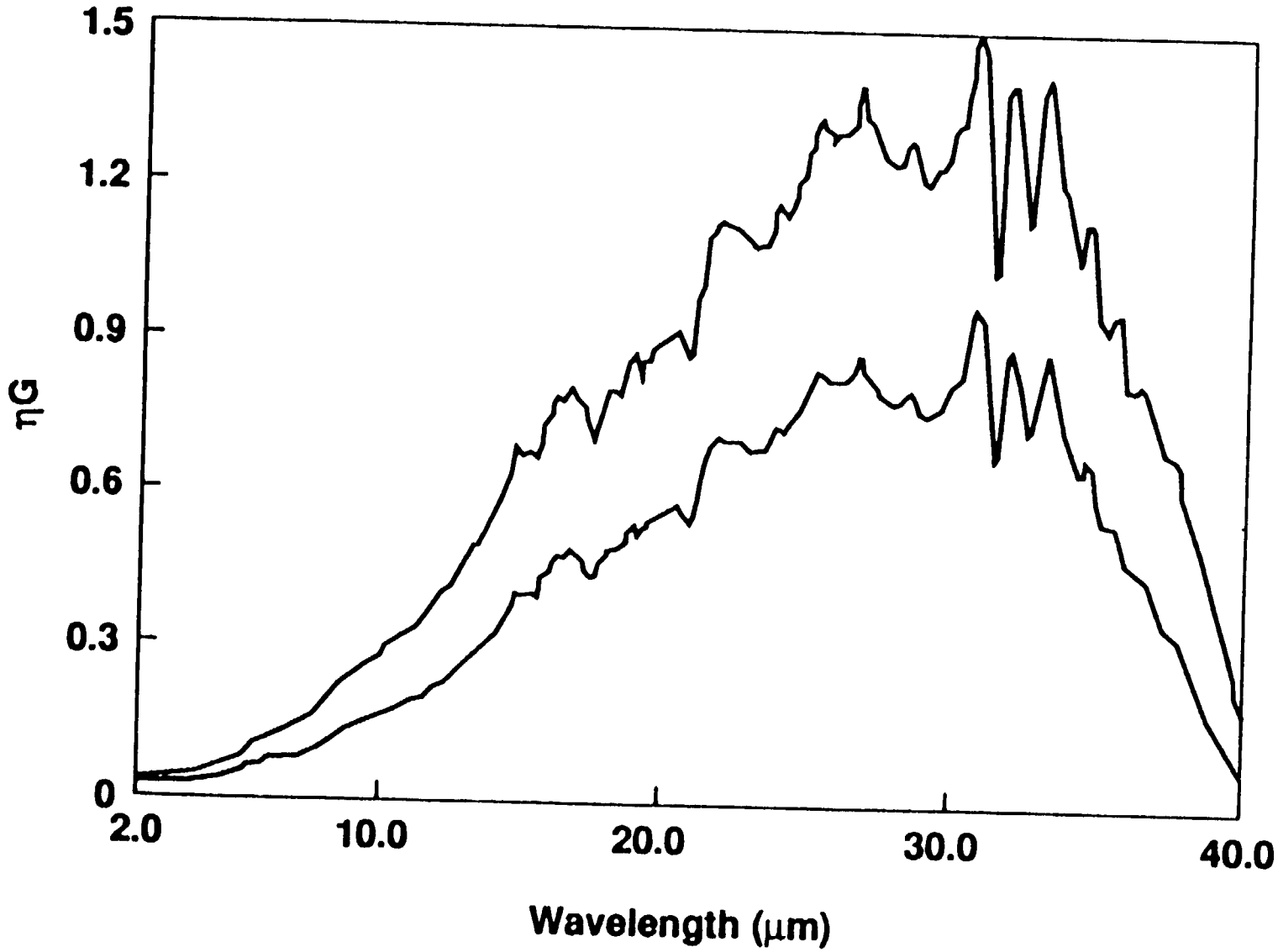

Figure 1. A figure taken from Huffman et al. (1991) on the spectral response of an earlier BIB detector design operating at two different bias voltages. The vertical axis notation, ηG (dimensionless), represents the relative responsivity of the device.

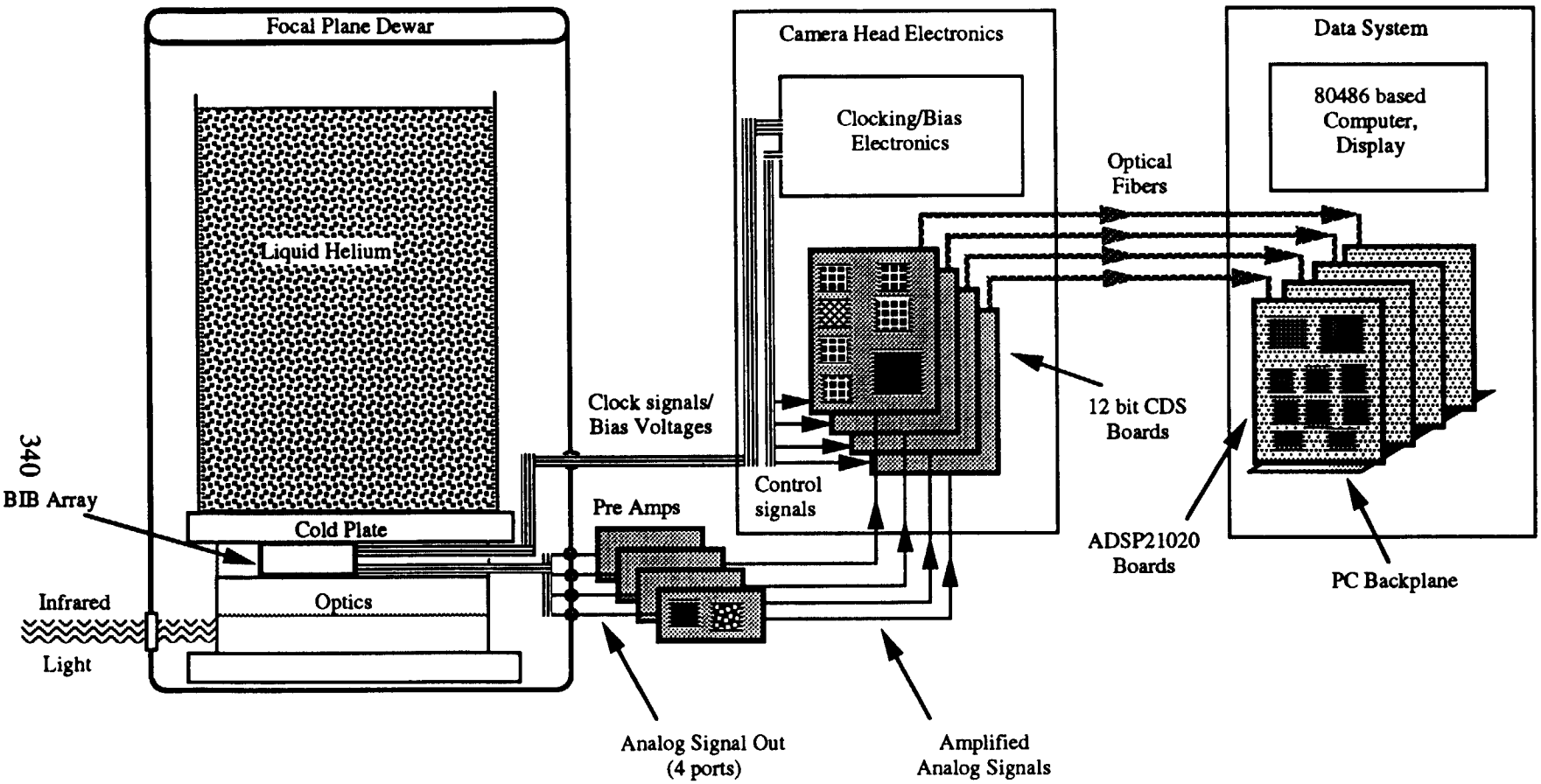

Figure 2. A block diagram of the BIB camera system. Note that the dewar is in the "operating" orientation; directional references in the text are with the dewar in the "assembly" orientation, i.e., top and bottom reversed.

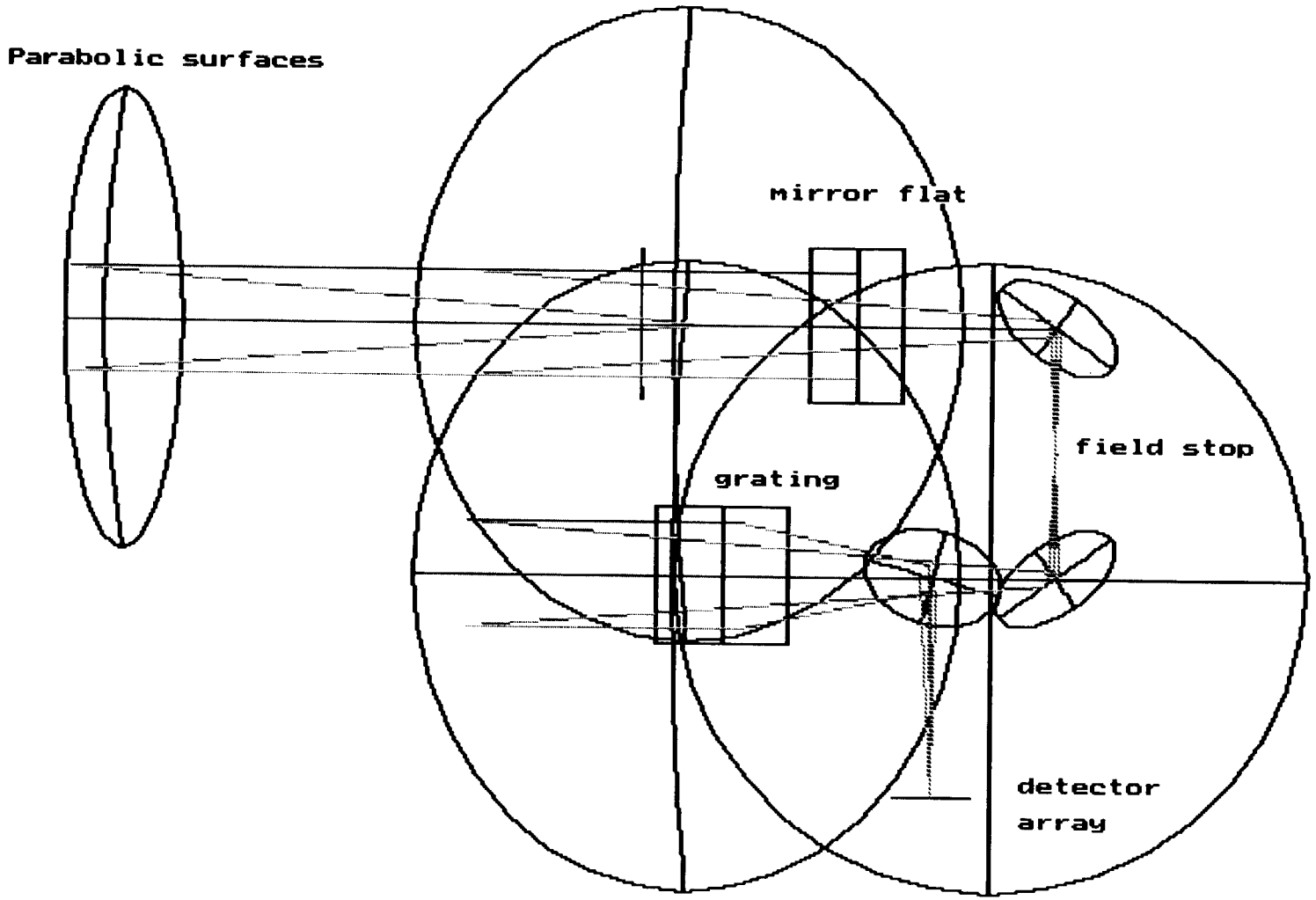

Figure 3. A schematic of the optical ray trace for our imaging/spectrometer camera design. The mirrors as depicted are the complete parabolic surfaces used by the ray tracing program BEAM4; only off-axis segments are used in the actual design.