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Jeff I. Cleveland II
Project Engineer

National Aeronautics and Space Administration
Langley Research Center
Hampton, Virginia 23681-0001

ABSTRACT

In order to meet the stringent time-critical requirements for real-time man-in-the-loop flight simulation, computer processing operations must be deterministic and be completed in as short a time as possible. This includes simulation mathematical model computation and data input/output to the simulators. In 1986, in response to increased demands for flight simulation performance, personnel at NASA's Langley Research Center (LaRC), working with the contractor, developed extensions to a standard input/output system to provide for high bandwidth, low latency data acquisition and distribution. The Computer Automated Measurement and Control technology (IEEE standard 595) was extended to meet the performance requirements for real-time simulation. This technology extension increased the effective bandwidth by a factor of ten and increased the performance of modules necessary for simulator communication. This technology is being used by more than 80 leading technological developers in the United States, Canada, and Europe. Included among the commercial applications of this technology are nuclear process control, power grid analysis, process monitoring, real-time simulation, and radar data acquisition. Personnel at LaRC have completed the development of the use of supercomputers for simulation mathematical model computation to support real-time flight simulation. This includes the development of a real-time operating system and the development of specialized software and hardware for the CAMAC simulator network. This work, coupled with the use of an open systems software architecture, has advanced the state-of-the-art in real-time flight simulation. This paper describes the data acquisition technology innovation and experience with recent developments in this technology.

INTRODUCTION

NASA's Langley Research Center (LaRC) has used real-time flight simulation to support aerodynamic, space, and hardware research for over forty years. In the mid-1960s LaRC pioneered the first practical, real-time, digital, flight simulation system with Control Data Corporation (CDC) 6600 computers. In 1976, the 6600 computers were replaced with CDC CYBER 175 computers. In 1987, the analog-based simulation input/output system was replaced with a high performance, fiber-optic-based, digital network. The installation of supercomputers for simulation model computation was completed in 1992.

The digital data distribution and signal conversion system, referred to as the Advanced Real-Time Simulation System (ARTSS) is a state-of-the-art, high-speed, fiber-optic-based, ring network system. This system, using the Computer Automated Measurement and Control (CAMAC) technology, replaced two twenty year old analog-based systems. The ARTSS is described in detail in references [1] through [6].

An unpublished survey of flight simulation users at LaRC conducted in 1987 projected that computing power requirements would increase by a factor of eight in the coming decade. Although general growth was indicated, the pacing discipline was the design testing of high performance fighter aircraft. Factors influencing growth included: 1) active control of increased flexibility, 2) less static stability requiring more complex automatic attitude control and augmentation, 3) more complex avionics, 4) more sophisticated weapons systems, and 5) multiple aircraft interaction, the so called "n on m" problems.

Finding no alternatives to using large-scale general-purpose digital computers, LaRC issued a Request for Proposals in May, 1989 and subsequently awarded a contract to Convex Computer Corporation in December of that year. As a result of this action, two Convex supercomputers are used to support flight simulation. The
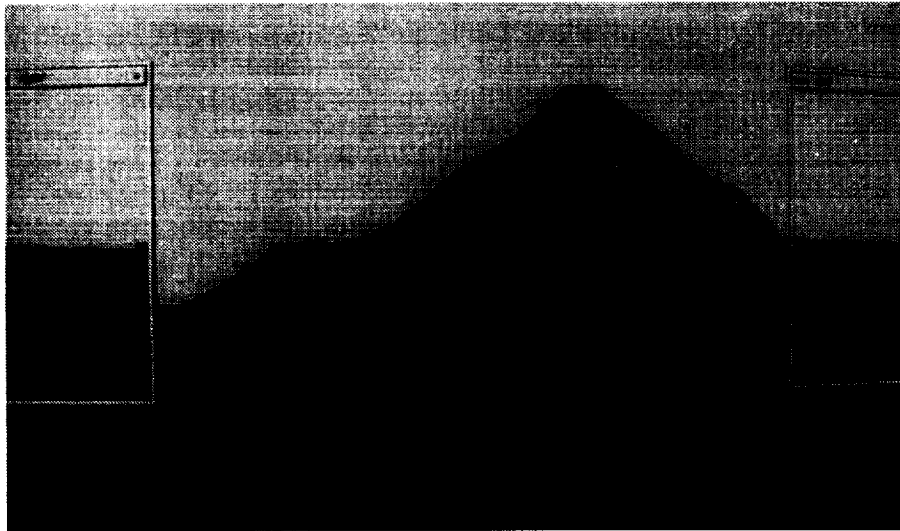
Figure 9: The operator's view displayed with two side mirrors' view

resulting computational facility provided by this contract is the Flight Simulation Computing System (FSCS). This system is described in references [8] through [11].

ADVANCED REAL-TIME SIMULATION SYSTEM

Through design efforts by both LaRC design engineers and design engineers at KineticSystems Corporation, Lockport, Illinois, three components of the ARTSS were developed to meet LaRC requirements. These were the serial highway network, the network configuration switch, and the signal conversion equipment.

Serial Highway Network

The LaRC ARTSS employs high-speed digital ring networks called CAMAC highways. At any given time, four totally independent simulations can be accommodated simultaneously. The equations of motion for an aircraft are solved on one of the mainframe computers and the simulation is normally assigned one highway. The purpose of the network is to transfer data between the central computers and simulation sites (control console, cockpit, display generator, etc.). The elements of a CAMAC highway are: the Block Transfer Serial Highway Driver (BTSHD); the fiber-optic U-port adaptor, the Block Transfer Serial Crate Controller (BTSCC); the List Sequencer Module (LSM); and the CAMAC crate. Three features of the networks were developed to meet the LaRC requirement. First, the mainframe computer interface to the BTSHD was developed. Second, the block transfer capability was developed to meet LaRC performance requirements. This capability resides in the BTSHD, BTSCC, and LSM. Third, the fiber optic capability was developed to satisfy a site distance problem. The simulator sites are from 350 to 6,000 feet from the computer center.

Prior to the development of the block transfer capability, a CAMAC message was approximately 19 bytes long which included addressing, 24 bits of data, parity information, and response information. The addition of the block transfer capability allowed for the inclusion of many CAMAC data words in a single message. During block transfers, data reads or writes proceed synchronously at one 24-bit CAMAC data word per microsecond. This is several times faster than the normal single word message rate. Besides the CAMAC standard message, there are two modes of block transfer. In the first, the entire block of data goes to a single module within a crate. It is implemented by the BTSCC repeating the module-select and function bits on the crate dataway for each CAMAC word. In the second block transfer mode, the block, either on read or write, is divided among several modules within a crate. This mode employs the LSM module which is loaded by the mainframe computer at set-up time with up to four lists of module-select and function bits. When this type of block transfer is in progress, the BTSCC acquires module number, function, and subaddress for each sequential CAMAC word in the block from the indicated list in the LSM.

To support the high performance requirements for flight simulation at LaRC and Convex supercomputers, a new generation serial highway driver was developed. This driver provides direct connection to VMEbus and allows data to be streamed onto the network. Previous equipment transmitted 24 bits out of the 32 available on the host computer interface; however, the new hardware transmits the full 32 bits from the host computer. Packing/unpacking operations are no longer required to provide the 24 bits in 32 which results in lower input/output latency and increased computer time available for model computation. The new serial highway driver has met the high performance requirements and provides a higher level of programmability.

Network Configuration Switch

The purpose of the network configuration switch system is to provide complete connectability between the simulation applications on the mainframe computer and the various simulation sites. Upon request, any sensible combination of available sites can be combined into a local CAMAC ring network in support of a single simulation. This network configuration for a given simulation is done during the initialization phase, after a highway has been assigned by the scheduling software. The application job requests sites by resource request statements and if the sites are available, the network configuration switch system will electrically and logically configure the network without disturbing other running simulations. The switch is built for a maximum of 12 highways and 36 sites. Each highway may be connected to a different host computer. During the transition

period, four computers were routinely used simultaneously doing flight simulation. Two of these computers were CDC CYBER 175 computers and two Convex supercomputers. In the final configuration, two Convex supercomputers with a total of six configuration switch ports are used.

Signal Conversion Equipment

Three types of output converter modules and two types of input modules were designed and built to LaRC specifications. The converters are high quality and have been added to the KineticSystems Corporation catalog. The digital-to-analog converters (DAC), analog-to-digital converters (ADC), and digital-to-synchro converters (DSC) are 16-bit devices with 14 bits of accuracy. The data transmitted uses 16 bits although only 14 are meaningful. This implementation allows LaRC to change converter precision without major changes in software or protocol. To decrease transmission time, data words are packed such that three converter words (16 bits each) are contained in two CAMAC words (24 bits each). The discrete input converters contain 48 bits per module and the discrete output modules contain 24 bits per module.

Clocking System

Flight simulation at LaRC is implemented as a sampled data system. The equations of motion are solved on a frame-by-frame basis using a fixed time interval. To provide the frame interval timing signals and a clocking system for synchronization of independent programs, LaRC designed and built the real-time clock system. This system is patented and is described in reference [7]. The clock system is composed of a central unit and multiple CAMAC modules called Site Clock Interface Units (SCIUs) which are connected by means of a separate fiber optic star network. Two distinct time intervals are broadcast by the central unit on a single fiber. The first time interval has a constant 125-microsecond period. The tic count necessary for a real-time frame is set in the SCIU by initialization software. This count is decremented by one for each occurrence of the interval timer. When the count reaches zero, each SCIU issues a signal that indicates beginning of frame. The frame time is determined independently for each simulation but must be a multiple of 125 microseconds. The second clock signal, called the job sync tic, has a longer period called the clock common multiple which is set manually, typically in the 1 to 6 second range. This longer period is used for synchronization. Each frame time must divide evenly into the clock common multiple, ensuring that all simulations will be synchronized on the occurrence of the job sync tic.

HIGH PERFORMANCE COMPUTING SYSTEM

The computers that LaRC has put in place to fulfill the requirements are Convex Computer Corporation C3200 and C3800 series computers. These computers are classified as supercomputers and support both 64- and 32-bit scalar, vector, and parallel processing. The first delivery consisted of a Convex C3230 (3 CPUs expandable to 4) with two CAMAC interfaces. The system was delivered with two peripheral buses (PBUS): one PBUS that is used for input/output to standard peripherals such as tape, disk, and line printer and one PBUS that is used exclusively for real-time input/output to the ARTSS CAMAC network. Each VME Input/Output Processor (VIOP) is a Motorola 68020 microcomputer that provides programmable input/output control. Each VIOP is connected to a standard 9U VMEbus and to the corresponding PBUS. The CAMAC interface consists of a KineticSystems Model 2140 Enhanced Serial Highway Driver for VMEbus. The second delivery consisted of one Convex C3850 (5 CPUs expandable to 8) computer configured similar to the C3230 with 3 PBUSs and two CAMAC interfaces. The computer contains 512 megabytes of main memory and sufficient disk and other peripherals to support flight simulation. The C3230 is installed in a secure room and is used for secure simulation and software development.

There are four critical aspects of a computing system to support real-time simulation. These are: CPU performance, memory capacity, time-critical system response, and deterministic system performance.

The first computer installed (C3230) performs a simulation of an X-29 aircraft in 245 seconds per CPU which is 2.7 times faster than the computers being replaced. With two CPUs available for real-time, this results in over 5 times the CPU performance. The second computer (C3840) performs the X-29 in 117 seconds per CPU which is

5.6 times faster than the computers being replaced. With four CPUs available for real-time, this results in over 18 times the CPU performance. The X-29 benchmark has been used to measure performance of other computer systems. Preliminary results of a recent study are shown in Table 1. The reader is cautioned to note that the benchmark measures only scalar CPU performance. The performance index does not necessarily imply any suitability for any application. These results are planned to be reported in a formal NASA publication.

Memory capacity is more than adequate to meet the requirements. The expanded memory capacity, compared with the old system, has allowed LaRC researchers to greatly increase the complexity of the simulations. The increase in memory capacity, coupled with the increase in CPU performance, has led to much higher fidelity simulations. Memory capacity is high enough to permit its use for real-time data storage and retrieval. If the data requirements of the real-time simulations exceed the memory capacity, a disk spooler program will be developed.

Time-critical system response is a measure of how fast the computing system can respond to real-time events from outside the computing system. Time-critical system response on both the computing systems has been measured at 31 microseconds, which exceeds the LaRC requirement.

Deterministic system performance is a measure of how consistently on a frame-by-frame basis the computing system calculates the simulation model without any loss in synchronization with real-time. To use a computing system for real-time simulation, the system must be able to solve the model in a very nearly fixed amount of time, no matter what the demands on the system are for other computing. The C3850 performs simulation models with less than one percent variation in model computing speed. Modifications to the C3230 software are being done to improve its model computing behavior.

Operating System

Convex Computer Corporation offers two real-time operating systems. The operating system currently in use at LaRC requires one CPU for all non-real-time activity: editing, program compilation, and other UNIX activities. The other CPUs may be dedicated to real-time simulation. At the request of a real-time program, the program is locked down in memory to prevent page faults and the CPU or CPUs are dedicated exclusively to the real-time program.

The second real-time operating system incorporates a specially developed real-time kernel that the entire operating system is built upon. With this version of the real-time operating system, the UNIX operating system portion will be pre-empted by real-time requests and the response to real-time interrupts will be deterministic and very short. This version supports, on a single CPU, all activities of a normal UNIX operating system and also simultaneously supports real-time applications.

ADDITIONAL HARDWARE

Processor Communication

LaRC has developed two processor communication CAMAC modules. The Q-bus Microcomputer Interface Module (QMIM) provides an interface between the CAMAC Dataway and a DEC Q-bus on an in-crate microcomputer. The Universal Minicomputer Interface Module (UMIM) provides an interface between the CAMAC Dataway and a DEC DR11-W interface to a compatible computer system. These modules are constructed with two FIFOs, one for input and one for output. They take full advantage of the Look-At-Me CAMAC capability of providing interrupt capability. Input can be done independently of output.

These modules are widely used at LaRC. They provide interfacing to Evans and Sutherland CT-6 image generators, Silicon Graphics devices, Symbolics computers, a variety of DEC computers, and Terabit Eagle 1000 graphics generators.

The contact person for these modules is Don Bennington of LaRC at (804) 864-7353.

Color Target Projector Controller

McDonnell Douglas Corporation has recently developed a color target projection (CTP) system for displaying one target aircraft or other high resolution inset image in a flight simulator projection dome. The system consists of a five axis servo, optical system, and a controller. Two axes, azimuth and elevation, position the projected image on the flight simulator dome surface. Two other axes, zoom A and zoom B, control the image size and focus. A fifth axis, for a neutral density filter wheel, controls the image brightness. The system also has a discrete position solenoid-actuated optical fader disk which may be placed in or out of the projector's optical path to help blend the projected image into the dome's background imagery.

The CAMAC CTP controller module is a circuit card assembly for controlling one CTP from a CAMAC crate. The module occupies one slot in a CAMAC crate and cables directly to the servo amplifier chassis of a CTP system. The module has the following input/output capabilities:

- CAMAC Dataway interface
- two channels of incremental encoder input for CTP azimuth and elevation position servo feedback
- eight channels of 12-bit DAC output for servo amplifier command voltages and test signals
- one discrete output for controlling the CTP fader disk
- one RS-232 serial input/output port

The simulation system host computer communicates CTP servo commands to the module over the CAMAC serial highway and through the CAMAC Dataway. The module inputs CTP azimuth and elevation servo position feedback information from encoders on the CTP body through cabling to the servo amplifier chassis and outputs analog servo command voltages and fader disk position command to the servo amplifier chassis.

The module performs digital position servo control for the CTP azimuth and elevation axes at an iteration rate of 2 KHz. The velocity loops for these two axes are controlled at the analog level through circuitry in the servo amplifier chassis. The position and velocity servo loops for the two CTP zoom axes and the density wheel axis are controlled at the analog level through circuitry in the servo amplifier chassis. The host computer sends position commands to the CAMAC controller module for these three axes and the module relays them to the servo chassis as DAC analog output voltages with no other control action of its own. The host computer also commands the discrete state of the CTP fader disk and the module relays this command to fader disk solenoid driver circuitry in the servo amplifier chassis.

Five of the module's eight DAC channels are required for position servo axis control. The remaining three DAC channels are used by the module to output test signals to aid in system maintenance.

The RS-232 serial input/output port is programmed to communicate with a VT100 compatible terminal. This port is used to display host computer command and status information, monitor CAMAC Dataway transfers, perform programming functions to change capabilities, and perform system configuration and maintenance functions.

Host computer commands for the CTP are sent to the module as blocks of eight CAMAC data words. Each eight word block contains position command values for the five CTP servo axes and fader disk. The blocks also tell the module the rate at which the host computer will send commands to the module. The module is able to receive and process CAMAC command blocks at a rate of up to 500 Hz.

The module is a microcomputer system built using the Intel 8OC186EB microprocessor. The software executed by the module is written primarily in Borland Turbo C++ with some assembly language routines. Software development for the module can be done with an IBM compatible PC hosting Borland C+ + compilers and assemblers and using Datalight Corporation's C-thru-ROM development tools. The controller can be customized for other applications through programming of the microprocessor. Reference [12] contains additional information. The contact person is Dave Beaman at (314) 234-0386.

CONCLUSION

NASA Langley Research Center has recently completed the development of a system to simulate in real-time increasingly complex and high performance modern aircraft. Utilizing centralized supercomputers coupled with a proven real-time network technology, scientists and engineers are performing advanced research using flight simulation. Hardware and software developed and concepts used are applicable to a wide range of commercial applications that require time-critical computer processing including process control, power grid analysis, process monitoring, radar data acquisition, and real-time simulation of a wide variety of systems.

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Computer	Time Seconds	Performance Index*
Hewlett-Packard 9000-735	49	13.5
Cray Y-MP	68	9.7
DEC 3000 Model 500X	76	8.7
HP 9000-720	90	7.3
DEC 3000 Model 500	101	6.5
Cray-2	109	6.1
Convex C3850	117	5.6
IBM RS/6000 970	120	5.5
IBM RS/6000 560	140	4.7
SGI Onyx	176	3.7
SGI Crimson	185	3.6
Convex C3230	240	2.7
CDC Cyber 175	660	1.0

*Note that Performance Index is CPU speed relative to CDC Cyber 175

Table 1
CPU Performance Using NASA Langley X-29 Simulation Benchmark