1995

NASA/ASEE Summer Faculty Fellowship Program

Marshall Space Flight Center

The University of Alabama in Huntsville

Development of the SEASIS Instrument for SEDSAT

Prepared By:	Mark W. Maier, Ph.D.
Academic Rank:	Assistant Professor
Institution and Department:	University of Alabama in Huntsville Department of Electrical and Computer Engineering
NASA/MSFC:	
Office:	Program Development
Division:	
Branch:	
MSFC Colleague:	Charles C. Rupp

Project Goals and Summary

July 1997 is the target date for the combined SEDS tether and SEDSAT mission. In this mission a small satellite (the SEDSAT) will be deployed on a 20 kilometer tether from the Space Shuttle. The tether will deploy in an unreel and braking profile that will be used to "slingshot" the SEDSAT at the end of the tether into a higher orbit with a three year expected lifetime. The SEDSAT will carry out a variety of experiments during and after tether deployment.

1. Measure and record accelerations experienced at the end of the tether.
2. Record panoramic imagery through the SEASIS instrument that will allow reconstruction of the three axis orientation history of the SEDSAT during portions of tether deployment.
3. Record imagery during tether cut and recoil to reveal tether recoil dynamics.

After the tether has been cut at both the shuttle and SEDSAT end the SEDSAT will enter a post tether mission phase. During the post tether mission the objectives are:

1. Downlink all recorded tether data.
2. Measure SEDSAT attitude in real-time and attitude stabilize the satellite with the SEASIS telephoto lens pointing earthward.
3. Record imagery of the Earth and atmosphere across the visible spectrum in response to ground command.
4. Serve as an amateur radio relay satellite.

As the list makes clear, the SEASIS instrument plays a central role in many of the SEDSAT objectives. When this faculty fellowship began in May, 1995, the SEASIS instrument had been worked on for several years under the leadership of its student principal investigator, Ms. Cheryl Bankston. However, since Ms. Bankston graduation a year previously very little progress had been made on the instrument. At that time a considerable body of design work had been completed and much of the hardware had been procured, but very little had been assembled or tested. The optical design was largely complete, but very little fabrication had been done. A considerable

camera can determine three axis attitude anytime the earth and one other recognizable celestial object (for example, the sun) is in the field of view. This well be essentially all the time during tether deployment.

2. A second camera system using telephoto lens and filter wheel. The camera is a black and white standard video camera. The filters are chosen to cover the visible spectral bands of remote sensing interest.
3. A processor and mass memory arrangement linked to the cameras. Video signals from the cameras are digitized, compressed in the processor, and stored in a large static RAM bank. The processor is a multi-chip module consisting of a T800 Transputer and three Zoran floating point Digital Signal Processors. This processor module was supplied under ARPA contract by the Space Computer Corporation to demonstrate its use in space.

SEASIS System Design

When the faculty fellowship began many aspects of the SEASIS design were effectively frozen. The basic two camera structure with PAL and telephoto lenses was fixed. Among the most important frozen elements was the selection of the SCC-100 processor. The processor had been selected in conjunction with ARPA support for the program. In retrospect, there could have been happy choices. Replacement of the processor was actively considered, but interface design and lack of funding for an alternative were dominant factors.

The principal goal during the fellowship has been to complete the design requirements and supervise the assigned students to the point that NASA can be given a reasonable assurance of flight readiness for July, 1997. To that end we have produced a complete set of requirements, design, interface, and development plan documents. Those documents are included with this report as appendices. A key element of the development plan is demonstration of an end-to-end prototype by September 1, 1995. At the time of this writing (August 4, 1995) that prototype is still in development.

Hardware Architecture

The SEASIS hardware architecture is shown in figure 1. Figure 1 shows the division of the SEASIS into its principal modules and their physical interfaces. The SEASIS processor board contains an SCC-100 processor module, boot hardware, and some of the digitizer interface hardware. Transputer links from the SCC-100 are used for most of the I/O. Video data is digitized in the Weber digitizer and passes into the SCC-100 through its shared memory interface. Images are stored in the mass memory, which is accessed through the second SCC-100 memory port . A full companion architecture flow diagram is provided in the referenced appendices.

SEASIS Hardware Development

Three major hardware development efforts have been carried out by the student investigators for SEASIS during the fellowship period.

1. Mr. Robert Hillman has designed and fabricated the camera control electronics. The interface implemented by this unit is documented (principally from the software point of view) in the SEASIS interface document included as an appendix. This design uses an Altera erasable programmable logic device (EPLD) reduce the projected four camera control boards to one. A secondary advantage to this design is that it is "self-documenting" in the sense that the Altera schematic capture files are used to directly program the chip leaving no latitude for on board hardware changes that don't get updated on the schematic.

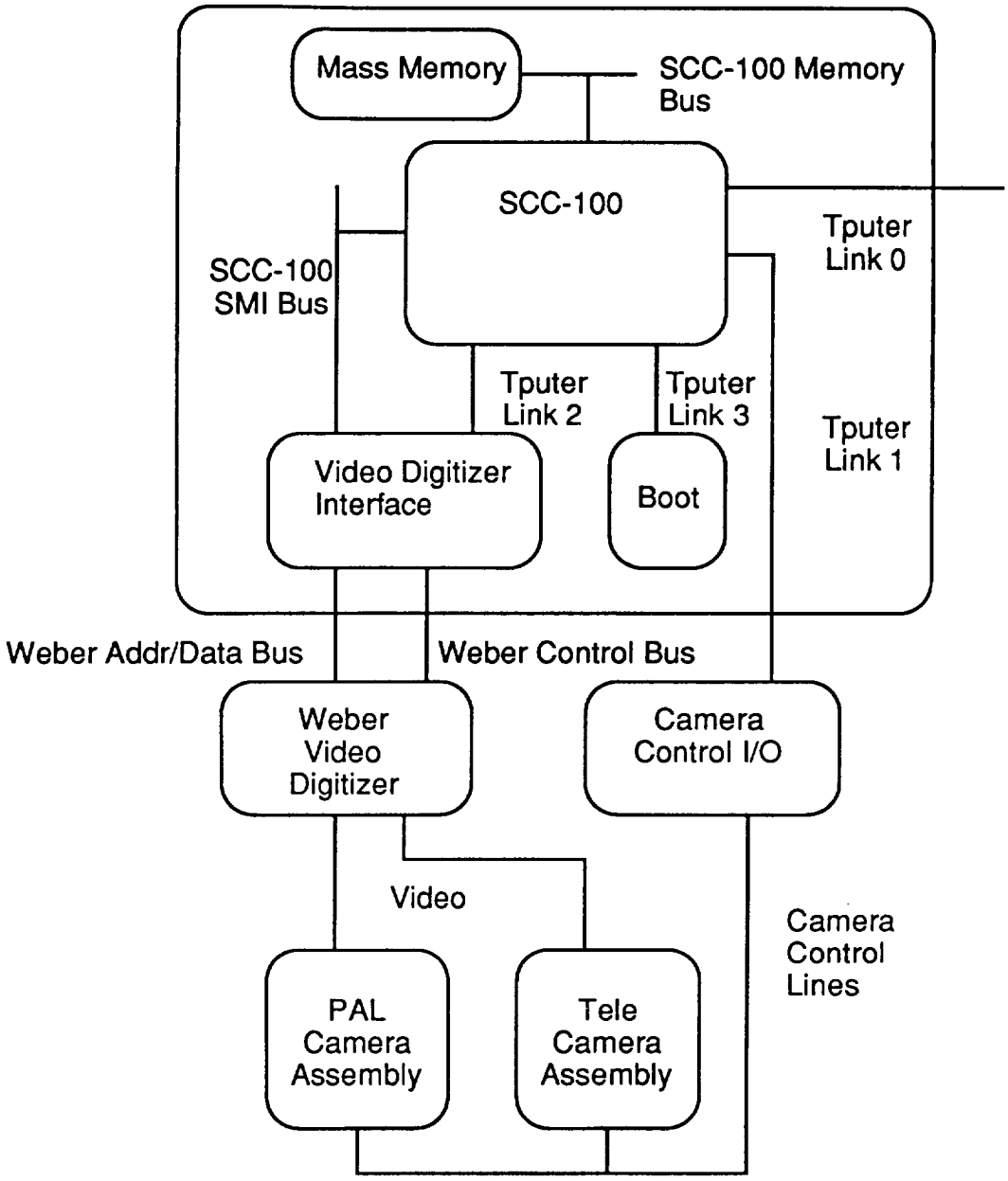

Figure 1: SEASIS architecture interconnect diagram. Processor I/O is predominantly done through Transputer links. Several specialized interfaces are necessary for experiment control and data acquisition.

2. Mr. Hillman has also fabricated a video interface board transfer control codes and digitized video to and from the Weber video digitizer.
3. Ms. Amy Houts has fabricated a breadboard version of the PAL lens camera for use in the prototype and for integrity testing. This unit includes the filters and transfer lenses.

One issue we believe has been effectively resolved is the radiation resistance of the Altera EPLD's. An Altera application note states that resistance above 10krads is achieved when input voltages are maintained below 5 volts. This would be adequate, at least for the tether portion of the mission. The lifetime dose is expected to be 14krads.

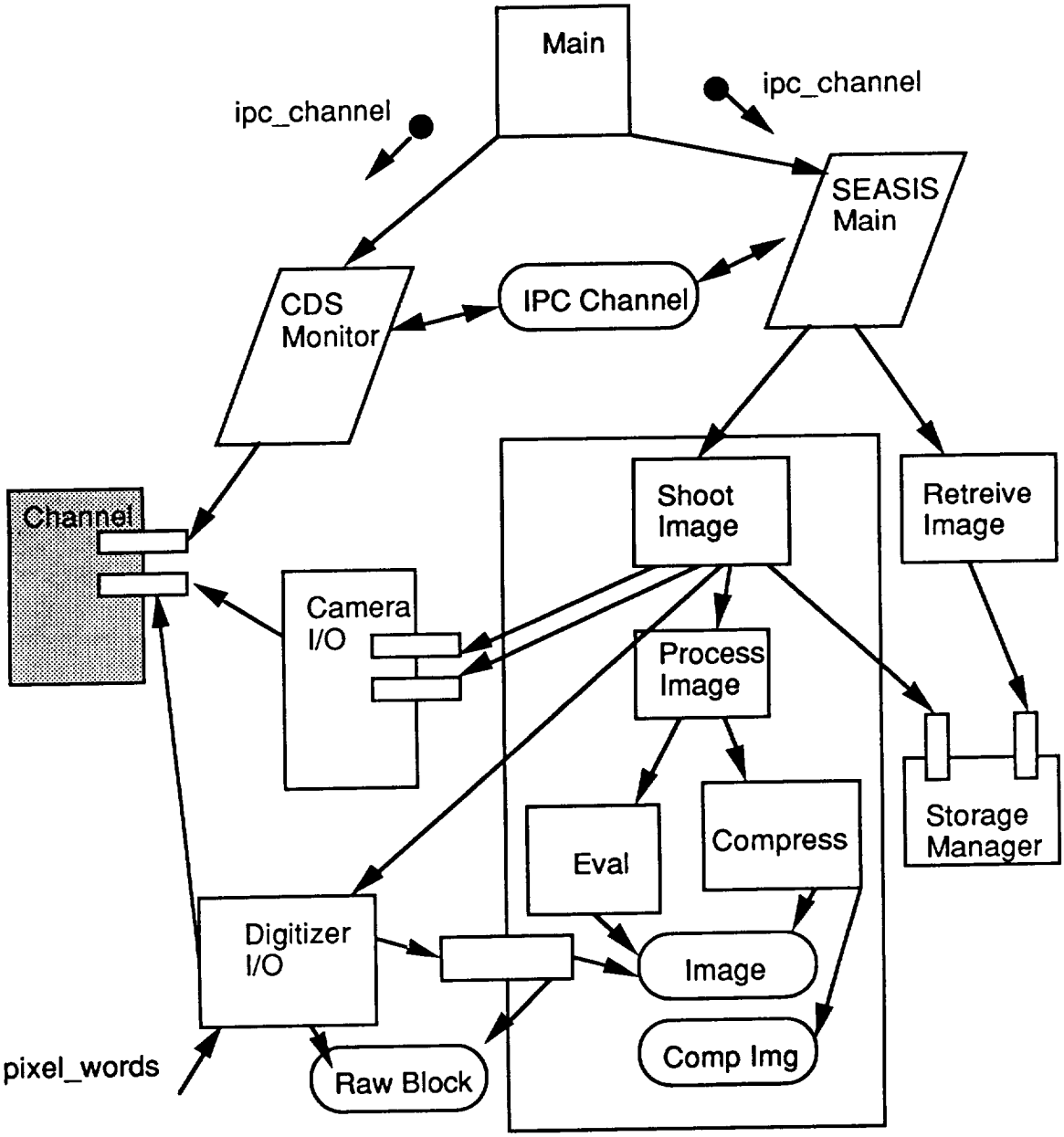

Figure 2: SEASIS software architecture diagram.

Appendices

Appendix A: SEASIS System Requirements Document

Appendix B: SEASIS System Development Plan

Appendix C: SEASIS Software Design Document

Appendix D: SEASIS Interface Document