RESONANT TUNNELING ANALOG-TO-DIGITAL CONVERTER

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Abstract

As sampling rates continue to increase, current analog-to-digital converter (ADC) device technologies will soon reach a practical resolution limit. This limit will most profoundly effect satellite and military systems used for e.g. electronic countermeasure, electronic and signal intelligence, and phased-array radar. New device and circuit concepts will be essential for continued progress. We will describe a novel, folded architecture ADC which could enable a technological discontinuity in ADC performance. The converter technology is based on the integration of multiple resonant tunneling diodes (RTD) and heterojunction transistors on an indium phosphide substrate. The RTD consists of a layered semiconductor heterostructure AlAs/InGaAs/AlAs (2/4/2 nm) clad on either side by heavily-doped InGaAs contact layers. Compact quantizers based around the RTD offer a reduction in the number of components and a reduction in the input capacitance. Because the component count and capacitance scale with the number of bits N, rather than by 2^N as in the flash ADC, speed can be significantly increased. A 4-bit, 2-GSps quantizer circuit is now under development to evaluate the performance potential. Circuit designs for ADC conversion with a resolution of 6-bits at 25 GSps may be enabled by the resonant tunneling approach.

Introduction

Since the initial investigations of resonant tunneling by Chang, Esaki, and Tsu [1] and the measurements of terahertz response in resonant-tunneling diodes (RTDs) by Sollner et al. [2], the physics and applications of resonant tunneling devices have received increasing attention [3,4]. Today, a wide range of applications are being explored including high speed and multistate memory [5-7], shift registers/correlators [8], and logic [9-13], where the number of interconnects and transistor delays are reduced by the use of the multi-state tunneling device. Other applications for tunneling devices include analog-to-digital convertors [14-16], optical receivers [17], samplers [18], and triggering circuits [19], all with microwave to millimeter wave bandwidths. In addition tunneling device architectures based on universal logic gates [20,21] could provide solutions to the interconnect bottleneck of post ULSI ICs.
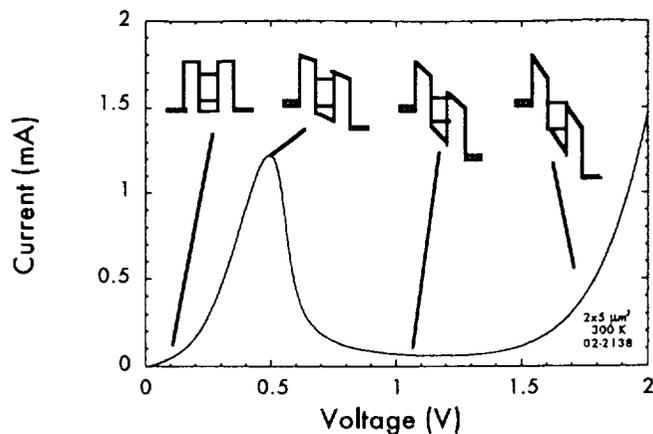
Figure 1. Current-voltage characteristic of an AlAs / In₀.₅₃Ga₀.₄₇As / InAs resonant-tunneling diode. The curve shown is the result of a *SPICE* simulation with close agreement to measured data at room temperature. In the insets, energy band diagrams indicate the relative alignments of electrons and quantum well states at selected bias conditions.

The RTD, in its simplest form, is a trilayer heterojunction device consisting of two wide bandgap electronic barriers cladding an interior quantum well region as depicted in the inset of Fig. 1. The total thickness of the structure is typically 10 nm or less. A peak in the current-voltage characteristic occurs when electrons in the emitter are energetically aligned with the lowest quasi-bound well state, while the valley (minimum) occurs when the lowest quantum-well state is energetically below the conduction band minimum (see again Fig. 1).

Multiple-Peak Resonant-Tunneling Diodes and Transistor Integration

Beyond the single peak I-V characteristic of Fig. 1, the RTD can be combined epitaxially in series to create multiple current peaks. Shown in Fig. 2 is a *SPICE* simulation illustrating the I-V characteristics of a 4-diode stack. In combination with a transistor, the multiple current peaks of the series RTD combination
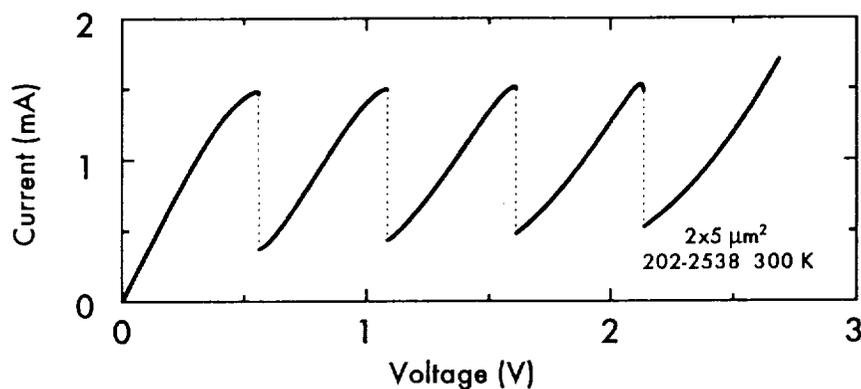

Figure 2. Formation of multi-peak current-voltage characteristics by series combination of resonant tunneling diodes; *SPICE* simulation based on a fit to experimental data.

can be translated into a multi-state transfer characteristic as illustrated in Fig. 3. In this configuration using a 3-RTD stack in the source of a heterojunction field-effect transistor (HFET), a binary output characteristic can be obtained for a multi-valued input characteristic. As we will show this characteristic is naturally suited to analog-to-digital convertor applications. The combination of RTD and transistor occupies less space than the two devices fabricated separately since the epitaxy for the two devices, one above the other, allows vertical integration with only a single additional metallization.
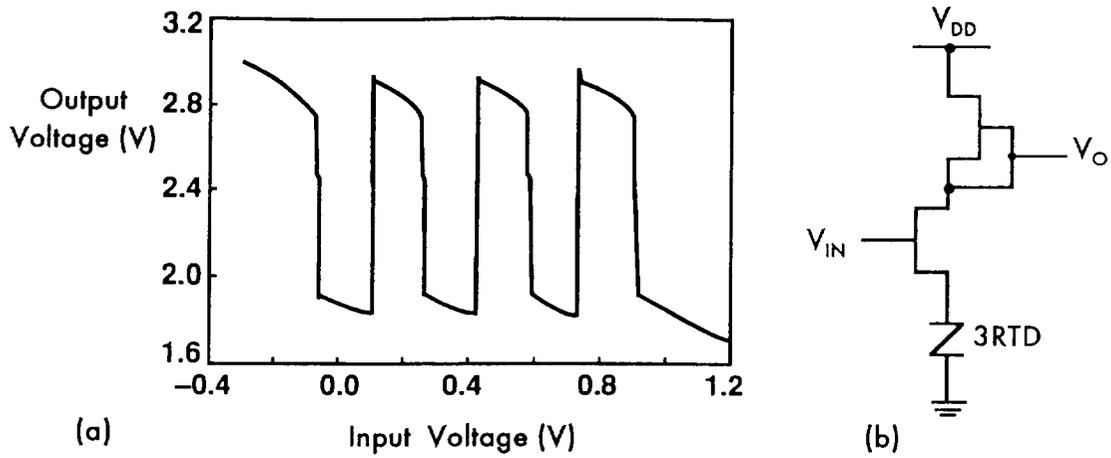
Figure 3. *SPICE* simulated transfer characteristic of a 3-peak AlAs/InGaAs resonant tunneling diode and an InAlAs/InGaAs heterostructure field-effect transistor circuit to yield multistate output.

Resonant Tunneling Quantizer

A simplified schematic diagram of a novel 4-bit quantizer that uses RTDs, HFETs, and resistors is shown in Fig. 4. Four identical multilevel folding amplifiers, each consisting of an HFET with a four-peak RTD
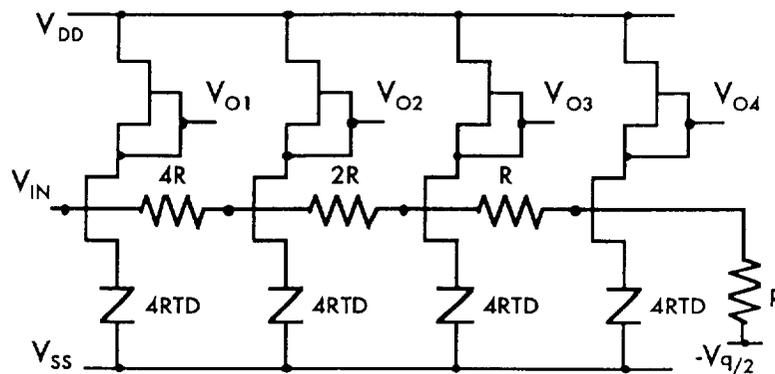

Figure 4. Four bit folding quantizer using 4-peak resonant-tunneling diodes (4RTD) and field effect transistors.

in series with the source and a load resistor, are connected by a binary-weighted resistor ladder. The gate current to the HFETs is at all times much less than the current through the resistor chain; the sum of the resistances, 8R, can be 50 Ω. Four-peak RTDs are used here for a four-bit quantizer (however, only two-peak RTDs are needed for a 3-bit quantizer). The first multilevel folding amplifier generates the LSB as follows. As the gate voltage of the HFETs, V_{IN}, is swept upward from the off-state, the output voltage, V_{o1}, starts high and goes low as V_{IN} exceeds the threshold voltage of the HFET, V_t. As the gate voltage continues to increase, the RTD switches from its peak current to its first valley current thereby restricting the HFET current and forcing V_{o1} high again. For further increases in V_{IN}, this cycle repeats and the input/output relation is as shown in the top trace of Fig. 5.
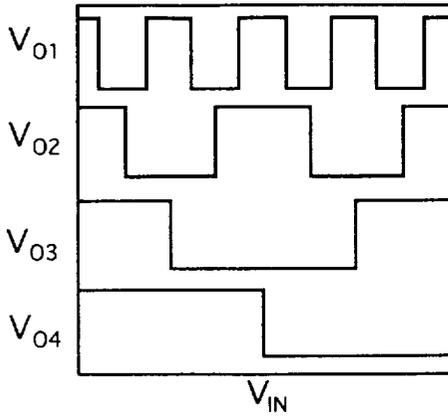
Figure 5. Output voltages of a folded four-bit resonant-tunneling quantizer for the circuit shown in Figure 4.

The more significant bits, V_{o2}, V_{o3}, and V_{o4}, are generated in a similar fashion; however, the binary-weighted resistor ladder divides V_{IN} so that 2, 4, and 8 times the LSB are required to generate the first switching transition, respectively. The four outputs in Fig. 5 are an inverted Gray code representation of the analog input. This novel circuit topology fully folds the analog input directly to a digital output. Since both the number of components and the input capacitance scale as the number of bits N, rather than as 2^N for the conventional 4-bit quantizer, the speed and component count can be significantly reduced. We estimate that the full 4-bit ADC operating at 2 GHz can be constructed with fewer than 100 components and with power dissipation less than 500 mW. Both number of components and power are reduced by an order of magnitude over conventional approaches.

Resonant Tunneling Memory

In addition this resonant tunneling technology can also be used for memory [4-8]. Shown in Fig. 6 are two cells which can be used to latch and store data at speeds as high as 25 GHz. In combination with the necessary drive circuitry these enable the direct storage of digitized data at the full sampling rate of the ADC. The cell shown in Fig. 6 (a) is used for latch/registers and shift-registers whereas the cell shown in Fig. 6 (b) is typically used in SRAM type arrays.
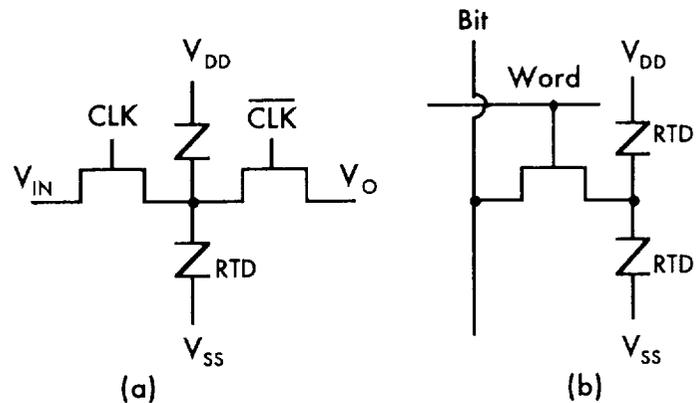

Figure 6. Resonant tunneling diode memory cells: (a) latch and (b) SRAM.

Conclusions

We have outlined the critical elements of a resonant tunneling analog-to-digital converter technology which can provide 4 bits resolution at 2 GHz with potential for 6 bits resolution at 25 GHz. In addition, memory based on RTDs can also provide data storage at frequencies as high as 25 GHz.

Acknowledgments

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