Advanced packaging for Integrated Micro-Instruments

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Abstract

The relationship between packaging, microelectronics, and microelectromechanical systems (MEMS) is an important one, particularly when the edges of performance boundaries are pressed, as in the case of miniaturized systems. Packaging is a sort of physical backbone that enables the maximum performance of these systems to be realized, and the penalties imposed by conventional packaging approaches is particularly limiting for MEMS devices. As such, advanced packaging approaches, such as multi-chip modules (MCMs) have been touted as a true means of electronic "enablement" for a variety of application domains.

Realizing an optimum system application of packaging, however, is not as simple as replacing a set of single chip packages with a substrate of interconnections. Research at Phillips Laboratory have turned up a number of interesting options in the two- and three-dimensional rendering of miniature systems with physical interconnection structures with intrinsically high performance. Not only do these structures motivate the redesign of integrated circuits (ICs) for lower power, but they possess interesting features that provide a framework for the direct integration of MEMS devices. Cost remains a barrier to the application of MEMS devices, even in space systems. As such, several innovations are suggested that will result in lower cost and more rapid cycle time. First, the novelty of a "constant floor plan" multichip module (MCM) which encapsulates a variety of commonly used components into a stockable, easily customized assembly is discussed. Next, the use of low-cost substrates is examined. The anticipated advent of ultra-high density interconnect (UHDI) is suggested as the limit argument of advanced packaging. Finally, the concept of a heterogeneous 3-D MCM system is outlined, which allows the combination of different compatible packaging approaches into a uniformly dense structure that could also include MEMS-based sensors.

Introduction

Electronics comprise 30 - 40 % of space systems, and their presence clearly has significant logistics implications and overhead. New approaches and processes have been developed for the packaging and design of electronic systems. The combination of these technologies imply tremendous reductions in size, weight, and power and improvements in performance, which will allow and enable the systematic reductions in spacecraft weight for a given function, or greatly improved functionality for a given weight. New technologies are furthermore under research and development that may reach the theoretical limit for density in a planar packaging approach, where even the semiconductor layers are thinned to a pliable regime. The possibilities of creating conformable electronic building blocks suggests that there is a new paradigm in the missile and satellite construction. Clearly, these payoffs can expand past space applications, which will clearly realize the most significant and immediate advantage.

In the whole of microelectronics and packaging research, two trends are clear: (1) increased functionality per unit volume, and (2) increased mixtures of functionality. The first trend is accelerated through advances in IC processes and the advent of two- and three-dimensional packaging. The second trend refers to the increased tendency to consider the mixture of disparate types of electronics functions (e.g., analog instrument, digital processing, communications, and power) within the same electronic module, also known as "mixed signal technology". The implications of these trends, extended in time, are that eventually most electronic systems of a given capability can be hosted in increasingly smaller volumes. The

degree to which this will be possible in general, depends as much upon packaging as it currently depends on IC feature size reduction, simply because no single monolithic IC process could be made to address disparate functional realms profitably at the feature sizes of interest.

Packaging technologies deal with the problem of physically supporting and interconnecting system components. In the specific case of an all-electronic system, one is concerned with at least four functions: (1) structural support and environmental protection of thin semiconductor slivers or "chips"; (2) thermal management; (3) information-bearing signal distribution; and (4) electrical power and grounding distribution. But a generalization of packaging requires that components which convert information-bearing electrical signals into another form of energy (or vice versa) be dealt with, and that class of components include conventional and MEMS-based sensors and actuators. Such a generalization would also deal with various non-electrical permutations of interfaces between components, such as the capability to deal with aggregations of actuator forces from individual components or routing complex fluidic manifolds throughout a system.

Conventional packaging schemes fall along the package-board-box-system (PBBS) paradigm. The paradigm implies a hierarchy in electronics packaging, as suggested in Figure 1. Chips are placed into packages, which are placed onto printed wiring boards (PWBs), that are in turn grouped into a "card cage" or chassis, an ensemble of which, when combined with the associated harnesses and connectors, constitute an electrical system. Most system designers are enslaved by (as opposed to enabled by) the convenience of conventional packaging, in stressing cases, however. One example of a stressing case is when order-of-magnitude size and weight reductions are clearly indicated, as they are in, for example, micro-spacecraft. If the PBBS cycle could be modified or broken, then tremendous opportunities exist for further optimization. If the normal traversing distances of feet between boxes can be reduced to centimeters or millimeters, it is conceivable that the associated functions could be further re-engineered to exploit the reduced drive required, saving power consumption and reducing latency.

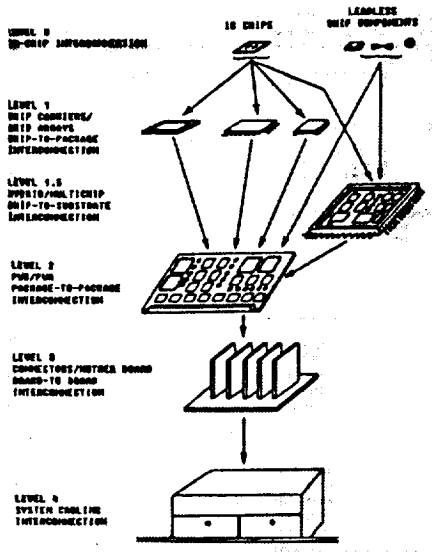

Figure 1. The hierarchical nature of packaging.[1]

It would seem that this hierarchical approach would also apply to electronics systems that contain MEMS components, while the paradigm for many non-electronic systems is more diverse and modular, reflecting a unified integration of structure and functionality, such as the case of a bicycle, combustion engine, or jet fighter aircraft. An integrated microsystems may combine the best features of both hierarchical and modular approaches.

Advanced packaging is very much about optimizing the way that components are contained and interconnected within an electronics system. For space-constrained systems, conventional packaging is particularly poor in efficiency -- typically less than one percent[2]. Through advanced packaging, the volume packing efficiency can be improved upon considerably, perhaps as much as 40 times better than conventional approaches. For performance-intensive systems, conventional packaging systems become increasingly problemmatic, due to the continuous demands for increased throughput and bandwidth. The conventional approaches introduce significant series loss and capacitive parasitic components, and, as frequencies are increased, the time-of-flight delays in packaging become so significant as to warrant treating interconnections as transmission lines.

Planar (2D) Advanced Packaging Approaches

Advanced packaging concepts can be applied at each level at the packaging hierarchy. The most well-known concept in advanced packaging is the multi-chip module (MCM), which combines a number of ICs and discrete components that would normally be individually packaged in a much denser form within a common package, as suggested in Figure 2. MCMs offer advantages similar to monolithic wafer scale integration (WSI), but without many of the intrinsic problems. MCMs are realized in one of two configurations, patterned substrate and patterned overlay, and are categorized by the industry using three types: MCM-C, MCM-D, and MCM-L.

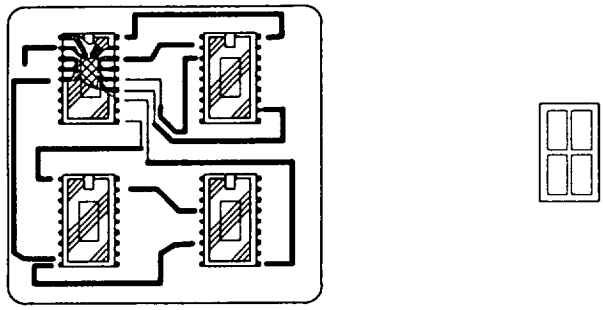

Figure 2. Impact of advanced packaging on size reduction.

Defining the configuration of MCMs requires an understanding of the construction of a typical MCM substrate (Figure 3a). The mechanical substrate provides the essential physical support for components on an MCM. The interconnecting substrate provides the wiring media for signal and power distribution. In the patterned substrate configuration (Figure 3b), the components are placed onto both substrates. In the patterned overlay process (Figure 3c), however, components are contained in the mechanical substrate, but signal distribution is accomplished with an interconnecting substrate which is applied over the components and mechanical substrate.

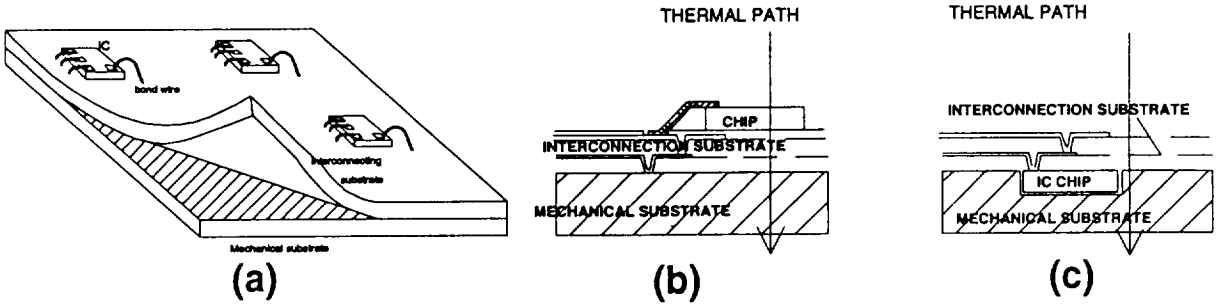

Figure 3. MCM configurations. (a) General construction. (b) Patterned substrate. (c) Patterned overlay.

MCM types are often designated as MCM-C, MCM-D, and MCM-L, which represent ceramic, thin-film, and laminate MCM technologies, respectively. These designations refer to the type of interconnecting substrate material, and in the MCM-C and MCM-L cases, the mechanical and interconnecting substrates coincide. MCM-C approaches are contemporary versions of the "chip and wire" hybrid. MCM-C modules have and continue to be the most prevalent form of advanced packaging in use in military and space systems, due to maturity and lack of organic materials, or, in other words, due to tradition. The thin-film MCM-D approaches are among the most recent developments in MCM technology, often boasting higher connection density and electrical performance (and unfortunately cost). The forms of MCM-D in research vary widely, ranging from nChip's silicon/SiO_2 patterned substrate approach to Lockheed Martin's High Density Interconnect Cu/polyimide/ceramic patterned overlay approach. MCM-L technology is sometimes referred to as "chip-on-board", and is usually thought of as the least capable and expensive of the MCM types, although modules of increasing sophistication have been achieved with this approach. Acceptance of MCM-L in military and space applications has been controversial due to concerns over the high content of organic materials. The significant research interest in these technologies have led to continued advancemeents in each MCM type, making it increasingly difficult to make any absolute assertions about which type is better for a given metric. It is also possible to mix the types, leading to sometimes confusing nomenclature. Another distinguishing characteristic of MCMs is the method by which components are

attached to the substrates. Prevalent forms of chip to substrate attach include wirebonding, tape automated bonding, and flip-chip attachment, with wirebonding remaining by far the most prevalent attachment method.

MCM Technology Benefits and Challenges. The most compelling case for MCMs, particularly for complex and mixed-signal applications, is the ability to greatly compress the size and weight of an otherwise conventionally packaged assembly. For these assemblies, it is not uncommon to observe ten-fold improvements in packaged configurations. For highly regular structures, such as memory components, the benefit is considerably reduced, usually 20-50%, in packaged configurations. MCM packaging enables designers to enhance electrical perfomance. In early ARPA/Phillips Laboratory research, it was not uncommon to operate complex digital systems at twice their normal operating frequency.[3] MCMs heuristically afford a higher reliability, as the number of interfaces are greatly reduced, lowering the actual number of failure modes.

While the benefits are great, MCMs are not without issues. The most significant problem facing theacceptance of MCMs is the so-called "known-good-die" problem. Conventionally, single chip assemblies are usually tested in-line in their final package, and non-functional components are discarded. In MCM assemblies, however, the die are included in substrates prior to packaging, and are usually not fully tested to the confidence levels of single chip packages. Hence, yield loss in MCMs are magnified tremendously as a function of the number of components and the yield of each component. The MCM developer can at this point only choose to develop more complex test fixturing to actually perform at-speed tests on bare die or to simply test a finished MCM assembly and "repair-to-yield" or discard the assembly. Each of these options add cost to the MCM, which is already high. The second most significant problem with MCM technology is cost of the packaging medium itself. The reason most often attributed to the high cost of MCM packaging aside from component issues is the relatively low production volume, particularly for MCM-D processes. In the aerospace communicty, another barrier to MCM use is the lack of adequate acceptance criteria for MCMs, and the general reluctance to use new technologies. The most advanced MCM approaches employ polymeric materials in their construction, which has historically been problemmatic. The most cost effective MCM assemblies feature non-hermetic encapsulation, which is furthermore considered taboo to many systems development programs. As such, plastic encapsulated microcircuits, whether single or multi-chip packages, have faced an uphill battle for use in aerospace systems.

Despite the challenges, considerable progress is being made in the development and insertion of advanced packaging for use in space systems. Most significant and representative forms of MCM technology are in-orbit slated for spaceflight in the near future. Increased awareness and understanding will be key to continuuing the trend.

Three-dimensional (3D) packaging

While MCMs provide significant improvements in planar packaging density, it is not always enough. First, MCMs are not always applied in an intelligent manner. If board designs, for example, are not carefully planned, MCMs may be used in a space inefficient manner, mitigating much of the benefit that an MCM approach could have provided. As such, some designs have realized little if any real improvement, due to lack of balance in considering advanced packaging at all levels in the Figure 1 hierarchy. Still, after all considerations have been effectively dealt with, 2-D is fundamentally limited, and the highest efficiency, which occurs when the sidewalls of ICs contact one another, is still not the best achievable. The situation begs the question that: if one would go to such lengths in planar packaging, then why ignore the third dimension?

Three-dimensional packaging refers to the consideration of non-planar techniques to improve overall system packaging efficiency on a volumetric basis. It is a natural consequencce and extension of planar MCM and board packaging methodologies. Far less mature than MCM approaches, a great diversity of 3-D approaches exist, range from 3-D integrated circuits (monolithic ICs that are "grown" one atop another) to stacked IC and MCM approaches. Examples of representative 3-D approaches are shown in FigureXXX.

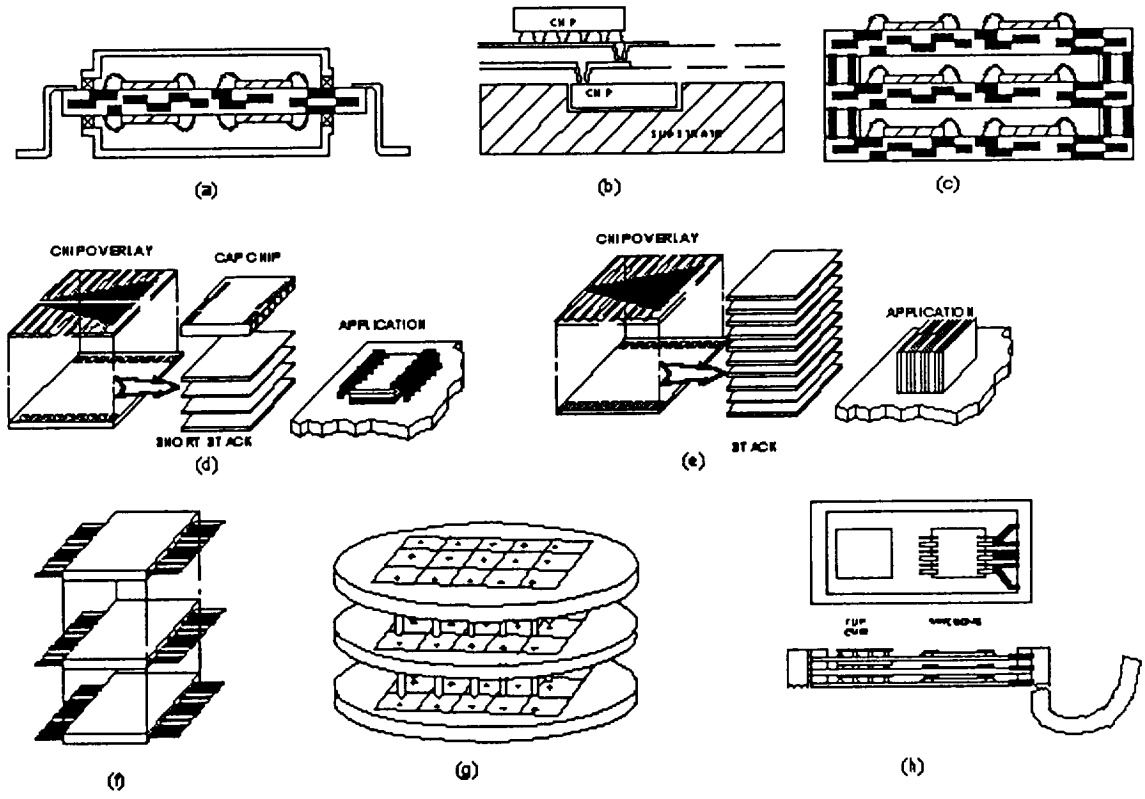

Figure 4. Representative 3-D Packaging Approaches.[3] (a) Double-sided cofired ceramic substrate. (b) Patterned overlay with surface-mounted components. (c) Cofired ceramic or thin-film, patterned substrates, stacked with interposer/spacers. (e) Thin-film patterned chip stack, short form. (f) Thin-film patterned chip stack, cube form. (g) 3-D monolithic wafer scale integration with areal connection technique. (h) Sensor electronics packaging of very thin (0.004") layers with ortogonal mounted imaging sensor detector array.

The benefits and challenges of 3-D packaging are similar to 2-D packaging, and differ largely only by degree. With 3-D packaging, greater reductions in size and weight are possible, and the potential to accelerate performance is improved. On the other hand, the pre-test and cost issues are also enhanced. One must now consider "known good assemblies", in addition to the "known good die" problem of MCMs. Cost for achieving the connections between layers is also high, for much the same reasons that 2-D MCM substrates are presently expensive. If MCMs have a problem in terms of economy of scale, it is only that much worse for 3-D MCMs and packages. It should be noted that sometimes, however, that a simpler form of 3-D packaging can sometimes be employed in an application with greater effectiveness than even the most sophisticated 2-D approach, especially for regular, simple electronic structures, such as mass memory. On the other hand, 3-D packaging is subject to the same abuses of misinterpretation in application as 2-D MCM approaches.

In fact, 3-D packaging promotes new thinking in design to some degree. For space-constrained systems, an increasingly larger fraction of an entire electronics system could be contained within the boundary of a single 3-D assembly. While much of the research in 2-D MCMs today is focussed on digital-only applications, it is the case, particularly for submunitions, missiles, and space systems that the 3-D MCM will have to deal with the packaging of analog instrumentation, microwave, power electronics, and even sensors and actuators. The high performance system, another driver for 3-D packaging, requires shorter electrical paths and many more of them. Thermal management, important in both cases, is a particularly acute concern for high-performance systems. Also of increasing importance is the notion that integrated circuits could and should be re-engineered in 3-D packaging to most advantageously support the

tremendously lower capacitance and series loss potential of that packaging environment. Doing this effectively suggests that it is highly desirable to establish a standard physical packaging architecture for heterogeneous systems. This architecture would include features such as:

- highly compact form factor, as a small monolithic block of functional electronics, with a density one to two orders of magnitude for digital and mixed-signal systems, even those that currently employ hybrid and MCM technology;
- open standards to accommodate a great number of existing and emergent hybrid/MCM technologies;
- flexible interface provisions and serviceable (demountable) layer and computer-aided-design (CAD) protocols;
- high signal integrity potential (based on adherence to specified design rules), allowing the merger of digital, analog instrument, microwave, and power circuitry within a single, functional block;
- adequate thermal management facilitation and comprehensive thermal characterization, allowing cookbook design methodologies (vs PhD-operated sophisticated numerical analyses)

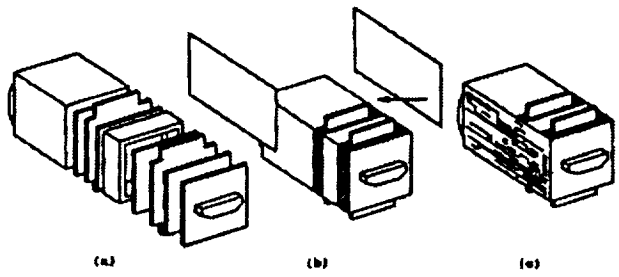

Figure 5. Three-dimensional packaging system developed for the Monolithic Interceptor Processor (MiP) project. Removes several levels of packaging hierarchy, integrates many forms of functionality, includes mechanical components, in a coffee cup size (1.6x1.6x3.5 inches).

These were essentially the conclusions reached in a recent Phillips Laboratory research program that studied methods of re-packaging the entire electronics functionality of a next-generation interceptor platform in the most efficient way possible. The program, referred to as the Monolithic Interceptor Processor (MiP), evaluated the integration of imaging sensors and inertial guidance systems within the same coffee cup form factor that housed 500 megaflops of digital processor, analog interfacing, and high-speed communications linkages. As shown in Figure 5, an integrated packaging system can eliminate entire levels of the packaging hierarchy. The advantages of the boardless, even box-less system packaging approach are clear for miniature systems, but improved performance and physical robustness are other potential benefits of interest to a great number of other systems. PL research concluded that the 3-D approaches required the flexibility to accommodate a great variety if not all possible electronics components of interest to a system designer, even mechanical components, such as MEMS devices.

Given the possibility of creating a three-dimensional compact packaging system, if sufficiently flexible, it is possible to integrate modules from a variety of industry and laboratory processes. Functions may be implemented by different vendors and integrated at one location. This packaging framework is extensible to the most aggressive technologies, as well as the most primitive.

Towards an Ultra-High Density Interconnect (UHDI)

Another area of exciting research is the drive toward the outer edges of packaging density. The working definition of UHDI processes may be provided as follows:

advanced packaging approaches and related infrastructure to achieve reliable and affordable assemblies with densities substantially beyond and properties atypical to the practiced state-of-the-art in practical multi-chip module (MCM) technologies. The delineation of layer thickness, volume efficiency, and price per cubic inch, as well as better metrics, are yet to be defined. UHDI processes are expected to achieve

greatest volume efficiencies through their ability to be stacked directly, and they are thought to be most versatile by virtue of an expected conformable abilities.

One representation of a UHDI process is shown in Figure 6. The conformable properties and associated metrics for UHDI assemblies are among its most intriguing and speculative features. Other potential benefits to UHDI process include:

- Tremendous volume densities for solid-state storage systems (e.g., > 10^9 bits/in^3)
- Enhanced potential for exploiting monolithic wafer scale integration
- Complex, heterogeneous subsystem construction for embedding into sensors, structures
- Greater reliability and operating potential due to improved thermal transport
- Increased radiation tolerance, similar to that provide by dielectrically isolated technologies.

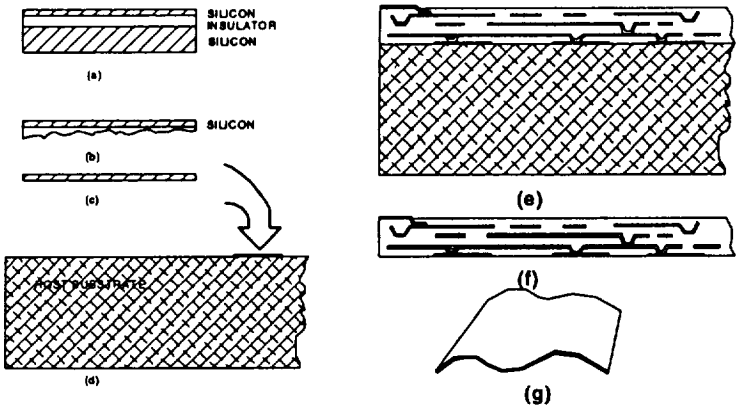

Figure 6 A potential UHDI process sequence. (a) Starting material, in this case an SOI wafer/component. (b)-(c) Epitaxial removal. (d) Attachment to temporary host substrate. (e) Patterned overlay formation. (f) Removal of host substrate. (g) Resultant UHDI membrane[4].

UHDI may well represent the limit argument in advanced packaging. It is predicated on the combination of patterned overlay multichip modules (MCMs) and integrated circuit (IC) thinning approaches to form electronic decal-like membranes. This intriguing next-step in packaging research has far-reaching consequences for almost any form of electronics system, particularly those with intense miniaturization goals.

The weight reduction potential of UHDI and an integrated 3-D packaging are tremendous: in combination, 1000x reductions of system functions are possible for certain classes of system functions. It is conceivable with this approach to re-engineer satellites that are collapsible to an extremely small form for launch and are expanded during deployment to provide the surface area needed for solar panels and communications equipment. Launch payloads could field ten times the number of satellites in a given mission, enabling a dramatic increase in the number of scientific objectives serviced by a single launch opportunity.

Integrated 3-D packaging and UHDI represent limit arguments in advanced packaging. The former establishes a 3-D packaging framework, allowing the commodization of component layers, predictability of physical characteristics, and a true leap ahead of most other 3-D packaging concepts, which typically focus on one level of packaging instead of the entire hierarchy. UHDI can operate inside or outside of this framework. Inside the framework, UHDI represents a preferred layer construction method. A typical UHDI layer would represent a slice less than 0.005" in thickness, compared to 0.040" - 0.200" for normal hybrid/MCM layers. This would represent an eightfold worst case density improvement. A 3-D implementation of UHDI would result in highly dense "pucks", which could be inserted as thicker layers, each of which might consist of several or many component layers, but less in aggregate thickness than a single 2-D MCM layer. Hence, a UHDI re-implementation of a non-UHDI system could be reduced to a credit card sized system in some cases. Outside the 3-D framework, UHDI could conceivably be conformed to structures of opportunity within the satellite, and directly integrated in multi-functional structures under research at Phillips Laboratory (PL/VTS) to eliminate cables and harnesses throughout a satellite.

Breaking Barriers for Rapid Development of Application Specific Integrated Microinstruments: Constant-Floor Plan Multichip Module Design Concept

For reasons that should be evident by now, MCM implementations of integrated MEMS systems represent an intelligent approach for extracting and preserving this performance and density benefits. Of course, the aforementioned barriers to routine MCM implementations, most notably those associated with cost, hinder progress towards establishing prototypes. A common complaint of engineers who would like to experiment with MCMs is the difficulty of justifying or raising the capital necessary to build even a simple design. Even design tools alone can exceed the capability of small companies, not to mention the problems associated with component selection, procurement, pre-test, MCM interconnect design, layout, fabrication, test, and assembly. Little standardization exists in the industry, but even if it did, only part of these issues are ameliorated. Let's examine these issues in a little more detail:

Computer Equipment for MCM Design. Buying a CAD system capable of doing MCM layouts is commonly perceived as a significant hardware/software expense. While it is of some comfort that an EDA infrastructure is emerging, such that it is possible for one to develop MCM designs in a structured and supported framework, the price for this capability is often well over $50,000. Beyond the ability to perform "mere" electrical layout, would-be MCM designers must confront decisions about investing even more money to perform linked thermal, mechanical, electrical, and reliability analyses through additional electronic design automation (EDA) packages sold by OEM and third-party suppliers. MCM designers who must also perform IC designs for a project is in double jeopardy, as he must also acquire IC EDA equipment as well. As such, the price tag to achieve entry design capability can be exorbitant, which is especially trying for "fence straddlers" who are as apt to find "better" uses for the money. It must be remembered that not every one is inexorably convinced of the necessity or even the viability of MCMs.

Component selection. Assuming that one is even in the position to begin an MCM design from an EDA standpoint, floorplanning requires that the components be nominally identified and enough information be secured to permit preliminary assessments of physical footprints. Little guidance exists for this process. Even companies such as Motorola who have supported the KGD Task Force specification activity are not monolithic, giving novice MCM designers mixed signals about die availability. He quickly learns that only a subset of the ICs in his databooks may be procured in die form. Moreover, he finds that even when there is a hint of availability, he will most likely have to construct die bond maps from third generation faxes or will have constructed a physical representation only to learn that the vendor has performed what is commonly referred to as a "die shrink". Passive components are sometimes as bad as integrated circuits on these bases. An added dimension of complexity is the practice of "thinking MCM" when making passive component selections, as not every type of capacitor or transformer, etc.

The situation has been improved considerably by the advent of MCM foundry services (resulting from ARPA sponsorship of the MOSIS "brokerage" of nChip and IBM substrate fabrication services, combined with third party assembly). Even with this service, however, die procurement, rapid design changes, and MEMS component integration are not easily accommodated. Another possibility exists that involves the use of patterned overlays to create rapidly customizable designs that amortize the cost of ubiquitous commodity components across multiple designs and lends itself to ready integration of MEMS devices. This concept is referred to as a *constant floor plan* MCM.

Constant floor plan (CFP) MCMs provide an MCM analog to gate array ICs with fixed underlayers. Simply put, a CFP MCM is based on a custom interconnection of standard, commonly required components, embedded within the substrate of a patterned overlay MCM. It is based on the premise that a judiciously chosen set of ICs and discrete components can satisfy a large percentage of designs (say 65-80%) of a particular class. For example, most microinstruments require analog conditioning circuitry, such as operation amplifiers, switches, multiplexers, and analog-to-digital converters (ADCs). A more complete, stand-alone instrument may require the addition of a microcontroller, miscellaneous logic functions (which could be accommodated using a field programmable gate array), and memory. Chances are that no tow designs, however, will connect these components together in the same manner. By fixing an ensemble of commodity components into a substrate in a pre-determined (i.e., a

constant floor plan), patterned overlay designs can be designer-specified to complete an almost arbitrary interconnection pattern of these components long after the substrate is formed. A production lot could contain many substrates with identical floor plans, but each with a completely different, user-specified interconnection scheme. It is also likely that by allowing a few components t be added that are unique to a particular design, that an even larger number of designs could be accommodated.

Since patterned overlays form interconnections after substrate assembly, it is possible to inventory a large number of identical substrates in unpatterned form for various customers, reducing the expense of many separate component purchases (each die within a design -- up to several dozen -- may be subject to $5,000-$100,000 minimum purchase) by amortizing them across a group of individual customers. The effective turn-around time for a CFP MCM would clearly be less than a full-custom MCM, since many of the die preparation steps as well as component assembly step would have already been performed. For commodity CFPs, it would in principle be possible to pre-test components in known-good-die style test fixtures. Furthermore, it is conceivable that a custom probe apparatus could be fashioned to test the entire substrate prior to locking in its personalization.

Rather than creating a single, "mega"-floorplan in a large substrate containing many components (a clear impracticality), it would be logical to establish a family of constant floor plan designs. A speculative set of constant floor plan MCMs would include: a memory CFP (for creating various parity and block organizations); an all-digital CFP; an mixed-signal, medium quality instrument CFP, a precision instrument CFP; and a digitally controlled microwave CFP. With this range of CFP options, a large number of general purpose instrumentation, memory module, digital logic, and radio-frequency designs could be readily accommodated. While even this range of options will not address every possibility, a great many possibilities for prototype MCMs can realized at the fraction of the cost of a normal MCM prototype.

The constant floor plan MCM concept has several novel features. A symbolic example of the process is shown in Figure 7.

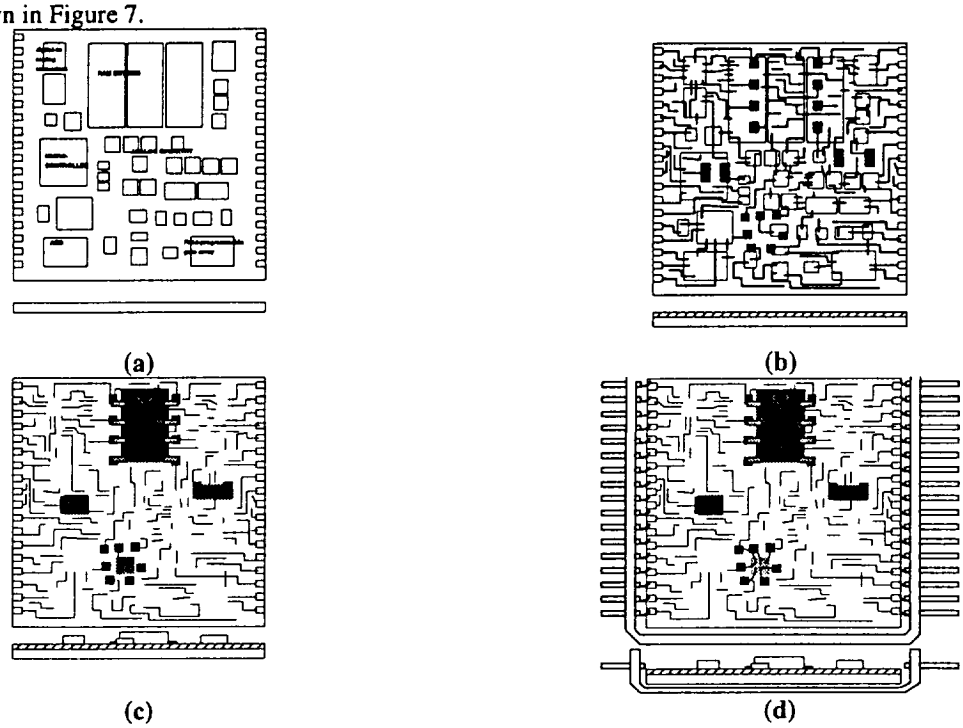

Figure 7. Constant floor plan (CFP) MCM concept. (a) Substrate, containing constant floor plan arrangement of components. (b) Formation of user-programmed interconnections, yielding "smart substrate". (c) Addition of surface-mount components, including MEMS devices. (d) Final bonding and assembly, showing optional kovar package, delidded.

First, design is simplified. Since the initial component placement is optimized at the factory, the user is not forced to assume this task. Pre-defined CAD representations of the CFP MCM would greatly simplify the routing of interconnection patterns, a task which may be automated with a variety of CAD systems, ranging from a PWB design tool on a PC to a full-featured design system on a UNIX-based workstation. Only the final routing patterns need be transmitted electronically to a foundry for processing.

A second feature of CPF is that it establishes a richer infrastructure for a class of a designs than previously possible. The instrument designer is freed from the burden of locating components, securing purchases, capturing die-specific parameters, verifying process compatibility, and of course, floor-planning and die attachment. It is possible to bundle CFP CAD files with more complete and standard information on its specific ensemble of components and applications than would be possible for many quick-turn designs. Driver models and data sheets for each IC could be included in a designer's kit. As more applications are constructed, the experience base would result in a richer accumulation of proven examples in both paper and electronic form. Even as macro cells are defined for gate array ICs, it is also possible to establish libraries of interconnect patterns corresponding to frequently used sub-circuits, such as an instrument amplifier. These macro patterns could be "cut and pasted", greatly reducing design latency. Alternately, a complete pre-worked design could be loaded into a CAD program and edited as necessary to adjust functionality for a related application. The designer's kit could also include pre-worked signal integrity and canned thermal analyses based on the floor plan itself. New thermal analyses could be re-accomplished in a small fraction of the time normally required, simply by adjusting component activity duty factors and re-executing a canned but validated thermal model.

The greatest single novelty of the constant floor plan approach for MEMS-based designers in particular is the fact that the entire top surface of the module is uncommited and could be used for mounting additional components. These components range from additional ICs to augment functionality; passive components to tailor analog functions; programmable memory devices to configure field programmable devices and computers, controllers, and micro-sequencers; and MEMS devices. In this manner, the "real estate" of the MCM can be "double-booked". Alternately, the CFP MCM can be viewed as a "smart substrate", similar to a bare, unassembled hybrid which has a completely unobstructed surface area to work with. As such, the CFP could be configured as an instrument with amplifiers, signal conditioners, digitizers, a computer, and serial interface built inside of the substrate, and completed by surface mounting a few MEMS-based sensors on the top surface. It is possible that the interconnect system, if based on certain polyimides, could serve as a process shield used to release the MEMS devices in final processing.

Next Steps Towards a Viable Heterogeneous 3-D Packaging

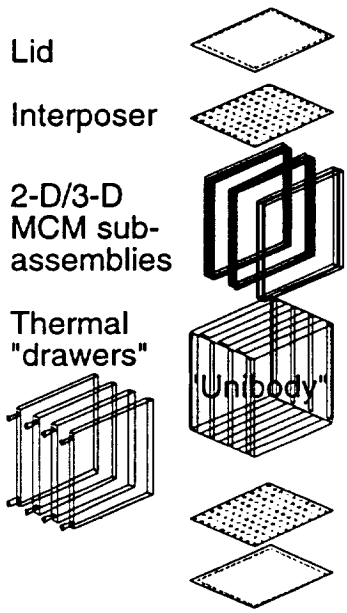

Figure 8. A prospective integrated 3-D packaging system.

Based on the precedents explored in the Monolithic Interceptor Processor (MiP) program, a new effort, termed the Highly Integrated Packaging and Processing (HIPP) program, has been established to promote the development of a heterogeneous packaging framework for 3-D systems, as previously suggested. Two visions for this framework, presented in **Figure 8**, illustrate the principle of an integrated 3-D architecture.. In one case, packaging systems are not only made more efficient, but they are demystified. A systems designer could specify the overall structure and compete the construction of the constituent layers. In this case, a unibody package provides structural reinforcement for the overall assembly (other approaches use a sliding frame to expand or contract accordion-style as layers are added or removed). MCM substrates of many forms may be inserted into the assembly. Thermal management is facilitated by access plenums in one plane, while electrical interface is achieved on the other. Thermal design is a cookbook exercise in this vision of packaging: if a designer exceeds the standard heat-handling capacity, he chooses an improved thermal material or method and slides it into a "thermal drawer".

Conclusions

The increasing sophistication of packaging technologies makes it possible to consider not only the inclusion of MEMS within what has been referred to as "physical packaging frameworks", but also a great variety of other functions, including analog instrumentation, power control, and microwave, in addition to the normal application base on complex digital functions. The trend of megafunctionality is suggested as a future paradigm, which favors in part the trend of micro-spacecraft, even though it is not currently considered an important trend in USAF space systems.

The virtues of reduction in size, weight, power, and cost, regardless of the size of the spacecraft, however, are important. USAF will increasingly rely on these technologies to prevent "growing" satellites to next, more expensive classes of launch vehicles. When DoD space is ready for micro-spacecraft, the technologies described here will enable their advent. To achieve the greatest benefit, optimization at all levels of the packaging hierarchy will be required. As long as MCMs are treated as fancy single-chip packages and merely mounted onto circuit boards, the realization of the paradigm is incomplete. On the other hand, heterogeneous 3-D MCM technologies, MEMS devices, and multifunctional structures will provide the technology infrastructure necessary to enable the construction of true micro-spacecraft without compromise.

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