DEVELOPMENT OF A 3-PHASE CCD TIMING GENERATOR

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ABSTRACT:

Charge-Coupled Devices (CCDs) are used in a wide range of commercial, scientific, and defense applications. They are primarily utilized for imaging and spectroscopic functions. Compact, cost-effective technology to miniaturize the auxiliary electronics required to operate the CCD is highly desirable. Because of the importance of reducing size and weight in defense and space applications, emphasis must be placed on the reduction in size.

The purpose of this project is to minimize the CCD timing generator electronics for 3-phase CCDs by replacing conventional ICs with a single programmable IC. This timing generator will give the user the ability to vary the number of horizontal and vertical pixels and to chose between integration and readout modes. This, in turn, will reduce the size and weight of CCD focal plane assemblies as a whole.

Charge coupled devices are semiconductor devices which employ storage elements (pixels) capable of transferring electric charge. For a 2 dimensional array, the charges stored in the pixel elements are usually read out row by row. Once a row is transferred into the horizontal or serial register, each pixel of that row is read out before another row is transferred. Ultimately, these packets of electrical charge are converted to voltage levels, digitized, and stored in memory. However, because there are various manufacturers of 3-phase CCDs, different types of auxiliary electronics, ranging in size, are necessary to support the CCDs. The size of the supporting electronics can pose a problem when limited space is available. My project is one proposed solution to this problem.

The first step, which is still underway, in my approach was to survey commercially available 3-phase CCDs, determine how they function, and become familiar with the various engineering software design tools on the CAEDE system. The design tools which will be needed for this project are;

1. VHDL (hardware descriptive language) is an alternative to physically drawing numerous logic gates in order to create a logic diagram. The types & functions of logic gates can be represented linguistically rather than graphically. VHDL saves time and makes it easier to understand the operability/function of the design being described.

2. LEAPFROG is a design tool that detects errors in the VHDL program, simulates the VHDL program, synthesizes, and converts the VHDL description into a diagram of logic gates in simplest form.

3. XILINX is a type of programmable logic device which consists of Field Programmable Gate Arrays. The VHDL program can be synthesized through the Leapfrog simulator
into the final XILINX product (chip).

In order for the timing generator to successfully operate 3-phase CCDs, a study of timing diagrams from the leading manufacturers had to be conducted in order to note any similarities or differences in the phase relationships, pulse widths, delay times, and other timing parameters. The review of timing diagrams for 1024 x 1024 CCDs manufactured by Loral, EG&G Reticon, and Scientific Imaging Technologies is still in progress and the results of the review are not final at this time.

The second step in my approach will be to incorporate the results of the study of various timing diagrams into a final timing generator recipe for either a XILINX product or an ASIC fabricated at a foundry yet to be determined. The design will be produced through the use of the design tools mentioned above using various logical elements such as shift registers and state machines. The work on this design will be continued at North Carolina Agricultural & Technical State University with access to NASA's CAEDE system enabling more efficient design work.

Through discussion with my mentor and responsible engineers, this project was determined to be too involved for a summer project. Therefore, it was concluded, in agreement with my academic advisor Dr. Busaba, that the topic would be an excellent topic for a master's thesis. Provisions for the use of NASA's facilities, especially interaction with the CAEDE system, will be made prior to the end of this summer's LARSS program. The thesis will be completed prior to graduation (Summer of 1996).

In conclusion, the development of a single programmable IC (timing generator) which miniaturizes CCD auxiliary electronics will result in a reduction of the size and weight of focal planes based on CCDs. This will be very beneficial to a wide range of commercial, scientific, and defense applications.